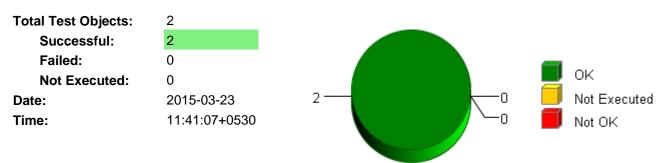


#### **Summary**

#### **Overall Test Object Results (including Coverage)**



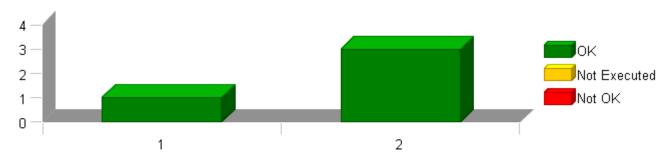
#### **Selected Project Items**

Test Object "CBD\_UnitTest/AssistFireWall/AssistFirewall\_Init1" Test Object "CBD\_UnitTest/AssistFireWall/AssistFirewall\_Per1"

#### **Used Test Environments**

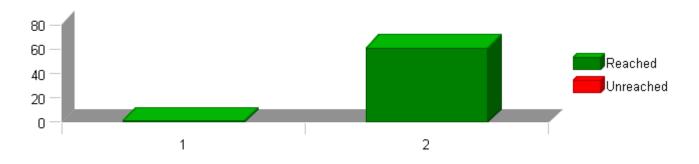
TI TMS 570 PLS UDE (Default)

#### **Test Case Results for Each Test Object (without Coverage)**



The table above shows each test object on the x axis and the number of test cases of the respective test object on the y axis. Each bar is divided into passed, not executed and failed test cases. The test case results do not take into account any coverage result (i.e. if all test cases of a test object are passed in this table but the coverage is failed, the overall test object result will be failed).

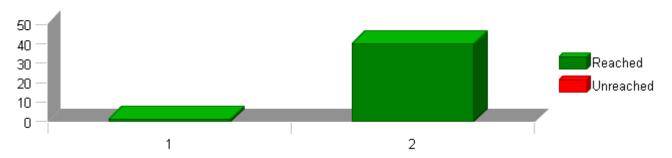
#### Statement (C0) Coverage: Total Statements for Each Test Object





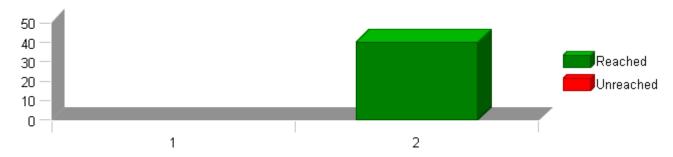
The table above shows each test object on the x axis and the number of statements of the respective test object on the y axis. Each bar is divided into reached statements (i.e. statements that have been executed during the test) and unreached statements.

#### Branch (C1) Coverage: Total Branches for Each Test Object



The table above shows each test object on the x axis and the number of branches of the respective test object on the y axis. Each bar is divided into reached branches (i.e. branches that have been executed during the test) and unreached branches.

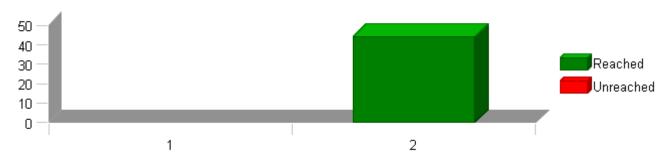
#### **Decision Coverage: Total Decision Outcomes for Each Test Object**



The table above shows test objects on the x axis and the number of possible outcomes of all decisions of the respective test object on the y axis. To achieve full DC coverage, each decision must evaluate to both true and false.

Each bar is divided into reached and unreached decision outcomes.

#### MC/DC Coverage: Total Condition Combinations for Each Test Object

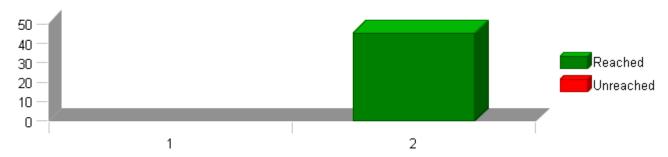


The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MC/DC coverage, each decision requires all contained atomic conditions to evaluate to both true and false independently of all other conditions. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.



#### MCC Coverage: Total Condition Combinations for Each Test Object



The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MCC coverage, each decision requires all contained atomic conditions to evaluate to all possible combinations of true and false values. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.



#### **Test Object List**

The following table lists all test objects with their test case and coverage results. The cumulated results for modules, folders and test collections are also displayed, the indentation within the name column indicates the parent relationship of the elements.

Please note that only test objects are numbered within the first column. This number is referenced on the x axis within the overview charts for test case and coverage results available on previous pages (if included into the report).

No.	Name	C0	C1	DC	MC/DC	MCC	Test Cases Res	sult
	AssistFirewall	100 %	100 %	100 %	100 %	100 %	4 of 4 passed	•
	CBD_UnitTest	100 %	100 %	100 %	100 %	100 %	4 of 4 passed	•
	AssistFireWall	100 %	100 %	100 %	100 %	100 %	4 of 4 passed	•
1	AssistFirewall_Init1	100 %	100 %	-	-	-	1 of 1 passed	•
2	AssistFirewall Per1	100 %	100 %	100 %	100 %	100 %	3 of 3 passed	~

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Project AssistFirewall

Module AssistFireWall

Test Object AssistFirewall\_Per1

#### Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
<b>Decision Coverage</b>	100 %
Branch (C1) Coverage	100 %
MCC Coverage	100 %
MC/DC Coverage	100 %

#### **Statistics**

Total Testcases	3	
Successful	3	~
Failed	0	
Not Executed	0	

#### **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\AssistFirewall
Configuration File	D:\Synergy_Work_Area\AssistFirewall\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\src\Ap_AssistFirewall.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -DBC_ASSISTFIREWALL_FAULTINJECTIONPOINT=STD_OFF -I\$(PROJECTROOT)\utp\contract \Ap_AssistFirewall -I\$(PROJECTROOT)\utp\contract -I\$(PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include -I\$ (Compiler Install Path)\include
File	\$(PROJECTROOT)\NxtrLib\src\interpolation.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -DBC_ASSISTFIREWALL_FAULTINJECTIONPOINT=STD_OFF -I\$(PROJECTROOT)\utp\contract \Ap_AssistFirewall -I\$(PROJECTROOT)\utp\contract -I\$(PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include -I\$ (Compiler Install Path)\include

Name	Text
Module 'AssistFireWall'	Name of Tester:Ankita Bhardwaj Code File(s) Under Test:Ap_AssistFirewall.c Code File(s) Version:14 Module Design Document:Assist_Firewall_MDD.docx Module Design Document:Version:14 Data Dictionary Version:16 Unit Test Plan Version:11 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.31 Total FLASH Used (Bytes):1568 Total RAM Used (Bytes):79 Total CALS Used (Bytes):79 Total CALS Used (Bytes):480 Special Test Requirements: Test Date:03-23-2015 Comments:"NOTE:1) Inline functions defined in GlobalMacro.h are not Unit Tested. 2)""CBD_Sandbox_dbg.map" map file is embedded for reference. 3) In ""AssistFirewall_Per1"" function, ""Defeat_AsstTbl_Service_Cnt_Jgc" always kept FALSE to make ""if((DefeatAsstTblSvc_Cnt_T_lgc <> D_FALSE_CNT_LGC) And (MECCounter_Cnt_T_enum <> ProductionMode))"" condition FALSE except Boundray Test for variables used in Condition and Path coverage.  "
	***************************************

Attributes	
Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9



Attributes			
Name	Value		
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj		
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src		
Linker File	\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd		
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl		
Target Install Path	\$(ProgramFiles)\pls\UDE 3.2		
Time Unit	Cycles		
Timer Enabled	false		
Timer Prescale	0		
Timer Resolution			
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg		
Workspace File	D:\Synergy_Work_Area\AssistFirewall\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP		



#### **Test Case 1: Metrics Test**

Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)
CPU Cycles:

TC1.1 6628.00 Cycles TC1.2 6630.00 Cycles

#### Description Vector description

TS1.1Shortest Execution Path:((HysteresisComp\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitHysComp\_MtrNm\_f32))=True && ((HighFreqAssist\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitHFA\_MtrNm\_f32))=True && ((BaseAssistCmd\_MtrNm\_T\_f32)<=(-k\_AsstFWInpLimitBaseAsst\_MtrNm\_f32))=True && ((DefeatAsstTblSvc\_Cnt\_T\_lgc != D\_FALSE\_CNT\_LGC) && (MECCounter\_Cnt\_T\_enum != ProductionMode))=True TS1.2"Longest Execution Path:""((HysteresisComp\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitHysComp\_MtrNm\_f32))=False && 1S1.2\*Longest Execution Path: "(InysteresisComp\_withini\_i\_i3z)>=(k\_AsstrWinpLimithyScomp\_MtrNm\_T\_f32)<=(-k\_AsstrWinpLimitHyScomp\_MtrNm\_T\_f32))=False && ((HighFreqAssist\_MtrNm\_T\_f32)>=(k\_AsstrWinpLimitHFA\_MtrNm\_f32))=False && ((HighFreqAssist\_MtrNm\_T\_f32)>=(k\_AsstrWinpLimitHFA\_MtrNm\_f32))=False && ((BaseAssistCmd\_MtrNm\_T\_f32)>=(k\_AsstrWinpLimitBaseAsst\_MtrNm\_f32))=False && ((BaseAssistCmd\_MtrNm\_T\_f32)>=(k\_AsstrWinpLimitBaseAsst\_MtrNm\_f32))=True && ((DefeatAsstTblSvc\_Cnt\_T\_lgc!= ((BaseAssistCind\_Mithini\_\_\_i\_\_iz\_)<= (-K\_Assir WinipLinitibaseAssi\_Mithini\_\_iz\_)= inter && ((DeleatAssi bisvc\_Chi\_\_i\_\_igc != D\_FALSE\_CNT\_LGC) && (MECCounter\_Cnt\_T\_enum != ProductionMode)) = False && ((LowFreqInput\_MtrNm\_T\_f32)>= (-UprBoundFilt\_MtrNm\_T\_f32))=False && ((LowFreqInput\_MtrNm\_T\_f32)<= (-UprBoundFilt\_MtrNm\_T\_f32))=False && DelftAsst\_MtrNm\_T\_f32 = DelftAsstLookup\_MtrNm\_T\_f32 \*
((float32)Sign\_f32\_m(HwTorque\_HwNm\_T\_f32))=True && ((LowFreqInput\_MtrNm\_T\_f32 < LwrBoundFilt\_MtrNm\_T\_f32) ||
((LowFreqInput\_MtrNm\_T\_f32 > UprBoundFilt\_MtrNm\_T\_f32) )=False
&& ((AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16) > ((AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16) > (Cot\_M\_u16) > (Cot\_M\_u16

axi(AssistFireWall\_ActiveRawAcc\_Cnt\_M\_u16 >= t\_AsstFWPstepNstepThresh\_Cnt\_u16[1])=False && (AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16 >= t\_AsstFWPstepNstepThresh\_Cnt\_u16[1])=False && (AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16 >= t\_AsstFWPstepNstepThresh\_Cnt\_u16[0])=True && (((Abs\_132\_m(SumInput\_MtrNm\_T\_f32 - AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32) > k\_RestoreThresh\_MtrNm\_f32) && (AssistFirewall\_AsstReducedPerfSV\_Cnt\_M\_lgc == TRUE)) || (TRUE == AssistFirewall\_PNCountStatus\_Cnt\_M\_lgc))=False && (AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32>8.8)=False && (AsstFWActive\_Uls\_T\_f32>1)=False && (AsstFWActive\_Uls\_T\_f32<0)=True ""

lame	Input Value
	· ·
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.30000019
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.40000006
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11199999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.119999997
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.219999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
_AsstFWInpLimitBaseAsst_MtrNm_f32	4.80000019
_AsstFWInpLimitHFA_MtrNm_f32	6.40999985
_AsstFWInpLimitHysComp_MtrNm_f32	6.71000004
_AsstFWNstep_Cnt_u16	4052
_AsstFWPstep_Cnt_u16	2460
_RestoreThresh_MtrNm_f32	4.42999983
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
z_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	-18432
12_AsstFWUprBoundX_HwNm_s4p11[3][0]	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_Asst WopiBoundX_HwNm_s4p11[5][2] t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
:2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144
z_AsstFWUprBoundX_HWNm_s4p11[7][5] 2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	14336



	( -4 10-10
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2 AsstFWUprBoundY MtrNm s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-6144
t2_Asst WoprBoundY_MtrNm_s4p11[3][9]	-4096
t2_Asst WopiBoundY_MtrNm_s4p11[3][10]	-2048
	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
t2_Asst WopiBoundY_MtrNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
	-8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
10. A = 4F\A(I   I = D = + I)/ A(+b) = - 4 = 44[0][4.0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	
	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384 -14336
t2_Asstr-Wuprisoundmitrim_s4p11[0][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefitAssistX_HwNm_u8p8[0]	947
	973
t_AsstFWDeftAssistX_HwNm_u8p8[1]	
t_AsstFWDefltAssistX_HwNm_u8p8[2]	998
t_AsstFWDefltAssistX_HwNm_u8p8[3]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1382
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1408
t_AsstFWDefitAssistX_HwNm_u8p8[19]	1434
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-205
t_AsstFWDefitAssistY_MtrNm_s4p11[1]	0
,	
t_AsstFWDeftAssistY_MtrNm_s4p11[2]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
t AsstFWDefltAssistY MtrNm s4p11[16]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720
t_AsstFWPstepNstepThresh_Cnt_u16[0]	234
t_AsstFWPstepNstepThresh_Cnt_u16[1]	655
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
t_AsstFWVehSpd_Kph_u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7.30000019
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	1
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.19999981
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.4000001
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
•	1
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_li	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.30000019	-5.30000019 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487	8487 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	17.9200001	17.9200001 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-3.35039997	-3.35039997 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019	-5.30000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999	5.0999999 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	17.9200001	17.9200001 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x00	0x00	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	<b>✓</b>

Test Step 1.2 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	-3.4000001
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.10000001
AssistFirewall ActiveRawAcc Cnt M u16	4797
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.5999999
AssistFirewall HiFreqKSV M str.LPF Str.SV Uls f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.019999996
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.5
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.60000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00899999961
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	1.79999995
k_AsstFWInpLimitHFA_MtrNm_f32	3.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	3.29999995
k_AsstFWNstep_Cnt_u16	4551
k_AsstFWPstep_Cnt_u16	2337
k_RestoreThresh_MtrNm_f32	6.9000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2 AsstFWUprBoundX HwNm s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2 AsstFWUprBoundX HwNm s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
LZ_MOSIL WOPIDOUNGT_WILLIAMS_S4PTT[O][S]	12200



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	14336
t2 AsstFWUprBoundY MtrNm s4p11[5][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-12288 -10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-12288 -10240 -8192 -6144



	Input Value
	0
	2048
	4096 6144
	8192
	282
t_AsstFWDefltAssistX_HwNm_u8p8[1]	307
t_AsstFWDefltAssistX_HwNm_u8p8[2]	333
t_AsstFWDefltAssistX_HwNm_u8p8[3]	358
	384
,	410
	435 461
,	486
	512
	538
t_AsstFWDefltAssistX_HwNm_u8p8[11]	563
t_AsstFWDefltAssistX_HwNm_u8p8[12]	589
t_AsstFWDefltAssistX_HwNm_u8p8[13]	614
	640
,	666
	691 717
	717
	768
	4096
	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	8192
	8192
	8192
	8192
	8192 8192
	10240
	12288
	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	16384
	18432
, ,	20480
	22528
	24576 26624
	28672
, , ;	30720
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720
t_AsstFWPstepNstepThresh_Cnt_u16[0]	170
t_AsstFWPstepNstepThresh_Cnt_u16[1]	399
	19072
	19200
	19328
1 1 1 1 1	19456 19584
	19712
	19840
	19968
-	-8.5
	0
<u> </u>	1.10000002
	-9
	1.10000002 0
•	77
	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_l_triggram = 0.0000000000000000000000000000000000$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32  Actual Value Expected Value Result



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveRawAcc_Cnt_M_u16	246	246 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	0.400000095	0.400000095 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.08599997	1.08600008 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-6.19999981	-6.19999981 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.90100002	7.90100002 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	0.400000095	0.400000095 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	<b>✓</b>

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~



Test Case 2: Boundary Test



#### Specification

```
Performance Metrics (With "None" Instrumentation and WithPS Environment)
        CPU Cycles:
CPU Cycles:

TC2.1 6628.00 Cycles
TC2.2 6628.00 Cycles
TC2.3 6629.00 Cycles
TC2.3 6629.00 Cycles
TC2.4 6629.00 Cycles
TC2.5 6629.00 Cycles
TC2.6 6629.00 Cycles
TC2.7 6629.00 Cycles
TC2.8 6629.00 Cycles
TC2.10 6629.00 Cycles
TC2.11 6629.00 Cycles
TC2.11 6629.00 Cycles
TC2.12 6629.00 Cycles
TC2.13 6629.00 Cycles
TC2.14 6629.00 Cycles
TC2.15 6629.00 Cycles
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TC2.11 6629.00 Cycles
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TC2.108 6629.00 Cycles
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TC2.108 6629.00 Cycles TC2.109 6629.00 Cycles TC2.110 6629.00 Cycles



TC2.111 6629.00 Cycles
TC2.112 6629.00 Cycles
TC2.113 6629.00 Cycles
TC2.114 6629.00 Cycles
TC2.115 6629.00 Cycles
TC2.116 6629.00 Cycles
TC2.117 6629.00 Cycles
TC2.118 6629.00 Cycles
TC2.118 6629.00 Cycles
TC2.119 6629.00 Cycles



#### **Description** Vector Description

```
TS2.1BaseAssistCmd MtrNm f32 = min
  TS2.2BaseAssistCmd_MtrNm_f32 = max
  TS2.3BaseAssistCmd_MtrNm_f32 = zero
TS2.4BaseAssistCmd_MtrNm_f32 = pos
TS2.5BaseAssistCmd_MtrNm_f32= neg
  TS2.6HighFreqAssist_MtrNm_f32 = min
TS2.7HighFreqAssist_MtrNm_f32 = max
TS2.8HighFreqAssist_MtrNm_f32 = zero
  TS2.9HighFreqAssist_MtrNm_f32 = pos
 TS2.10HighFreqAssist_MtrNm_f32 = neg
TS2.11HwTorque_HwNm_f32 = min
   TS2.12HwTorque_HwNm_f32 = max
  TS2.13HwTorque_HwNm_f32 = zero
TS2.14HwTorque_HwNm_f32 = pos
TS2.15HwTorque_HwNm_f32 = neg
  TS2.16HysteresisComp_MtrNm_f32 = min
TS2.17HysteresisComp_MtrNm_f32 = max
   TS2.18HysteresisComp_MtrNm_f32 = zero
  TS2.19HysteresisComp_MtrNm_f32 = pos
TS2.20HysteresisComp_MtrNm_f32 = neg
TS2.21VehicleSpeed_Kph_f32 = min
  TS2.22VehicleSpeed_Kph_f32 = max
TS2.23VehicleSpeed_Kph_f32 = mid
TS2.24t_AsstFWVehSpd_Kph_u9p7[8] = min
  TS2.25t_AsstFWVehSpd_Kph_u9p7[8] = max
TS2.26t_AsstFWVehSpd_Kph_u9p7[8] = mid
TS2.27t2_AsstFWUprBoundX_HwNm_s4p11[11] = min
TS2.27t2_AsstFWUprBoundX_HwNm_s4p11[11] = min TS2.28t2_AsstFWUprBoundX_HwNm_s4p11[11] = max TS2.29t2_AsstFWUprBoundX_HwNm_s4p11[11] = zero TS2.30t2_AsstFWUprBoundX_HwNm_s4p11[11] = pos TS2.31t2_AsstFWUprBoundX_HwNm_s4p11[11] = neg TS2.32t2_AsstFWUprBoundY_MtrNm_s4p11[11] = min TS2.33t2_AsstFWUprBoundY_MtrNm_s4p11[11] = max TS2.34t2_AsstFWUprBoundY_MtrNm_s4p11[11] = zero TS2.35t2_AsstFWUprBoundY_MtrNm_s4p11[11] = pos TS2.36t2_AsstFWUprBoundY_MtrNm_s4p11[11] = neg TS2.37AssistFirewall_UprBoundKSV_M_str_SV = min TS2.38AssistFirewall_UprBoundKSV_M_str_SV = max
  TS2.38AssistFirewall_UprBoundKSV_M_str.SV = max
TS2.39AssistFirewall_UprBoundKSV_M_str.SV= zero
TS2.40AssistFirewall_UprBoundKSV_M_str.SV.SV = pos
  TS2.41AssistFirewall_UprBoundKSV_M_str.SV.SV = neg TS2.42AssistFirewall_UprBoundKSV_M_str.K= min TS2.43AssistFirewall_UprBoundKSV_M_str.K= max
  TS2.44AssistFirewall_UprBoundKSV_M_str.K.K = mid TS2.45AssistFirewall_LwrBoundKSV_M_str.SV= min TS2.46AssistFirewall_LwrBoundKSV_M_str.SV= max
   TS2.47AssistFirewall_LwrBoundKSV_M_str.SV= zero
 TS2.48AssistFirewall_LwrBoundKSV_M_str.SV= pos
TS2.49AssistFirewall_LwrBoundKSV_M_str.SV = neg
   TS2.50AssistFirewall_LwrBoundKSV_M_str.K= min
  TS2.51AssistFirewall_LwrBoundKSV_M_str.K= max TS2.52AssistFirewall_LwrBoundKSV_M_str.K= mid
TS2.52AssistFirewall_ActiveKSV_M_str.K= mir TS2.53AssistFirewall_ActiveKSV_M_str.SV = min TS2.54AssistFirewall_ActiveKSV_M_str.SV = zero TS2.56AssistFirewall_ActiveKSV_M_str.SV = zero TS2.56AssistFirewall_ActiveKSV_M_str.SV = pos TS2.57AssistFirewall_ActiveKSV_M_str.SV = neg TS2.57AssistFirewall_ActiveKSV_M_str.K= min TS2.59AssistFirewall_ActiveKSV_M_str.K= max TS2.60AssistFirewall_ActiveKSV_M_str.K= max TS2.60AssistFirewall_ActiveKSV_M_str.K= min TS2.50AssistFirewall_ActiveKSV_M_str.K= min TS2.60AssistFirewall_ActiveKSV_M_str.K= min TS2.60Assi
  TS2.60AssistFirewall_ActiveKSV_M_str.K= mid
TS2.61AssistFirewall_HiFreqKSV_M_str.LPF.SV = min
TS2.62AssistFirewall_HiFreqKSV_M_str.LPF.SV = max
  TS2.63AssistFirewall_HiFreqKSV_M_str.LPF.SV= zero
  TS2.64AssistFirewall_HiFreqKSV_M_str.LPF.SV= pos
TS2.65AssistFirewall_HiFreqKSV_M_str.LPF.SV= neg
  TS2.66AssistFirewall_HiFreqKSV_M_str.LPF.K= min
  TS2.67AssistFirewall_HiFreqKSV_M_str.LPF.K= max TS2.68AssistFirewall_HiFreqKSV_M_str.LPF.K= mid TS2.69AssistFirewall_HiFreqKSV_M_str.CF = min
  TS2.70AssistFirewall_HiFreqKSV_M_str.CF = max
TS2.71AssistFirewall_HiFreqKSV_M_str.CF=mid
TS2.72k_AsstFWInpLimitHysComp_MtrNm_f32 = min
   TS2.73k_AsstFWInpLimitHysComp_MtrNm_f32 = max
 TS2.74k_AsstFWInpLimitHysComp_MtrNm_f32 = mid
TS2.75k_AsstFWInpLimitHFA_MtrNm_f32 = mid
TS2.75k_AsstFWInpLimitHFA_MtrNm_f32 = max
TS2.77k_AsstFWInpLimitHFA_MtrNm_f32 = mid
TS2.78k_AsstFWInpLimitBaseAsst_MtrNm_f32 = min
   TS2.79k_AsstFWInpLimitBaseAsst_MtrNm_f32 =max
IS2.79k_AsstF-WInpLimitBaseAsst_MtrNm_f32 = max TS2.80k_AsstF-WInpLimitBaseAsst_MtrNm_f32 = mid TS2.81AssistF-irewall_ActiveRawAcc_Cnt_M_u16 = min TS2.82AssistF-irewall_ActiveRawAcc_Cnt_M_u16 = max TS2.83AssistF-irewall_ActiveRawAcc_Cnt_M_u16 = mid TS2.84t_AsstF-WPstepNstepThresh_Cnt_u16[2] = min TS2.85t_AsstF-WPstepNstepThresh_Cnt_u16[2] = min TS2.86t_AsstF-WPstepNstepThresh_Cnt_u16[2] = mid TS2.87k_AsstF-WPstep_Cnt_u16 = min TS2.88k_AsstF-WPstep_Cnt_u16 = max TS2.88k_AsstF-WPstep_Cnt_u16 = max TS2.88k_AsstF-WPstep_Cnt_u16 = min TS2.89k_AsstF-WPstep_Cnt_u16 = min TS2.8
 TS2.88K_AsstFWPstep_Cnt_u16 = max
TS2.89k_AsstFWPstep_Cnt_u16 = mid
TS2.90k_AsstFWNstep_Cnt_u16 = min
TS2.91k_AsstFWNstep_Cnt_u16 = max
TS2.92k_AsstFWNstep_Cnt_u16 = mid
TS2.93AssistFirewall_PNCountStatus_Cnt_M_lgc = FASLE
TS2.94AssistFirewall_PNCountStatus_Cnt_M_lgc = TRUE
```



```
TS2.95AssistFirewall_CombAsstSV_MtrNm_M_f32 = min
TS2.96AssistFirewall_CombAsstSV_MtrNm_M_f32 = max
TS2.97AssistFirewall_CombAsstSV_MtrNm_M_f32 = pos
TS2.98AssistFirewall_CombAsstSV_MtrNm_M_f32 = pos
TS2.99AssistFirewall_CombAsstSV_MtrNm_M_f32 = neg
TS2.100AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc = FALSE
TS2.101AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc = TRUE
TS2.1031_AsstFWDefltAssistX_HwNm_u8p8[20] = min
TS2.1031_AsstFWDefltAssistX_HwNm_u8p8[20] = mia
TS2.1051_AsstFWDefltAssistX_HwNm_u8p8[20] = mia
TS2.1051_AsstFWDefltAssistY_MtrNm_s4p11[20] = min
TS2.1051_AsstFWDefltAssistY_MtrNm_s4p11[20] = max
TS2.1071_AsstFWDefltAssistY_MtrNm_s4p11[20] = pos
TS2.1091_AsstFWDefltAssistY_MtrNm_s4p11[20] = pos
TS2.1094_AsstFWDefltAssistY_MtrNm_s4p11[20] = neg
TS2.110k_RestoreThresh_MtrNm_f32 = min
TS2.111k_RestoreThresh_MtrNm_f32 = mid
TS2.113Defeat_AsstTbl_Service_Cnt_lgc==Max
TS2.113Defeat_AsstTbl_Service_Cnt_lgc==Min
TS2.115MEC_Counter_Cnt_enum==>Max
TS2.117MEC_Counter_Cnt_enum==>Max
TS2.117MEC_Counter_Cnt_enum==>Pos
TS2.118All_min
TS2.119All_Max
```

Test Step 2.1 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.090000036
AssistFirewall_ActiveRawAcc_Cnt_M_u16	109
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.8999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0700000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0099999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4
k_AsstFWInpLimitHFA_MtrNm_f32	2.5
k_AsstFWInpLimitHysComp_MtrNm_f32	3.78999996
k_AsstFWNstep_Cnt_u16	3928
k_AsstFWPstep_Cnt_u16	1107
k_RestoreThresh_MtrNm_f32	1.8999998
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2 AsstFWUprBoundX HwNm s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048



Name	Input Value	
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096	
	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]		
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384	
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432	
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480	
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288	
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144	
	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]		
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336	
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288	
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096	
, , , , , , , , , , , , , , , , , , , ,		
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432	
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384	
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288	
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192	
	-6144 -6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]		
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-30720	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-28672	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-26624	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-24576	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-20480	
	-18432	
12_AsstFWUprBoundY_MtrNm_s4p11[0][6]		
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192	
t2_Asst WopiBoundY_MtrNm_s4p11[1][4]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
t2 AsstFWUprBoundY MtrNm s4p11[3][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	26
t_AsstFWDefitAssistX_HwNm_u8p8[1]	51
C. 1991 AA Delityosisty T. IMIAIII Trobo[1]	01



Name	Input Value		
t_AsstFWDefltAssistX_HwNm_u8p8[2]	77		
t_AsstFWDefltAssistX_HwNm_u8p8[3]	102		
t_AsstFWDefltAssistX_HwNm_u8p8[4]	128		
t_AsstFWDefltAssistX_HwNm_u8p8[5]	154		
t_AsstFWDefltAssistX_HwNm_u8p8[6]	179 205		
t_AsstFWDefltAssistX_HwNm_u8p8[7] t_AsstFWDefltAssistX_HwNm_u8p8[8]	230		
t_AsstFWDefltAssistX_HwNm_u8p8[9]	256		
t_AsstFWDefltAssistX_HwNm_u8p8[10]	282		
t_AsstFWDefltAssistX_HwNm_u8p8[11]	307		
t_AsstFWDefltAssistX_HwNm_u8p8[12]	333		
t_AsstFWDefltAssistX_HwNm_u8p8[13]	358		
t_AsstFWDefltAssistX_HwNm_u8p8[14]	384		
t_AsstFWDefltAssistX_HwNm_u8p8[15]	410		
t_AsstFWDefltAssistX_HwNm_u8p8[16]	435		
t_AsstFWDefltAssistX_HwNm_u8p8[17]	461		
t_AsstFWDefltAssistX_HwNm_u8p8[18] t_AsstFWDefltAssistX_HwNm_u8p8[19]	486 512		
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-205		
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	-184		
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	-164		
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	-143		
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	-123		
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	-102		
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	-82		
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	-61		
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	-41		
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	-20 0		
t_AsstFWDefltAssistY_MtrNm_s4p11[10] t_AsstFWDefltAssistY_MtrNm_s4p11[11]	20		
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	41		
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	61		
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	82		
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	102		
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	123		
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	143		
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	164		
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	184		
t_AsstFWPstepNstepThresh_Cnt_u16[0]	0		
t_AsstFWPstepNstepThresh_Cnt_u16[1] t AsstFWVehSpd Kph u9p7[0]	1408		
t_AsstFWVehSpd_Kph_u9p7[1]	1536		
t_AsstFWVehSpd_Kph_u9p7[2]	1664		
t_AsstFWVehSpd_Kph_u9p7[3]	1792		
t_AsstFWVehSpd_Kph_u9p7[4]	1920		
t_AsstFWVehSpd_Kph_u9p7[5]	2048		
t_AsstFWVehSpd_Kph_u9p7[6]	2176		
t_AsstFWVehSpd_Kph_u9p7[7]	2304		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-8.80000019		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	9 1.10000002		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90.1999969		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	_Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_M	ltrNm_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall.Ass$			
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mt		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_N		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_MEC_Counter_Cnt		
tgt_kte_inst_Ap_Assistr-irewaii.Assistr-irewaii_Peri_venicleSpeed_kpn_r32  Name	tgt_AssistFirewall_Per1_VehicleSpeed_Kph  Actual Value	The second secon	Basul
Name AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	2.82099986	Expected Value 2.8210001 ± 4.88E-04	Resul
AssistFireWall_ActiveRov_M_str.5v_UIs_r32 AssistFireWall_ActiveRawAcc_Cnt_M_u16	0	2.8210001 ± 4.88E-04 0 ± 1	
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	
AssistFirewall_CombAsstSV_MtrNm_M_f32	0.08984375	0.08984375 ± 4.88E-04	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.9920001	1.99199998 ± 4.88E-04	
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.2329998	5.2329998 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
	1.11900008	1.11899996 ± 4.88E-04	



Name	Actual Value	Expected Value	Result
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	0.08984375	0.08984375 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	✓

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	•
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.2 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0199999996
AssistFirewall_ActiveRawAcc_Cnt_M_u16	200
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.13
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0099999978
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.20000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00899999961
ssistFirewall_PNCountStatus_Cnt_M_lgc	0
ssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2
ssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00300000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
_AsstFWInpLimitBaseAsst_MtrNm_f32	2.20000005
_AsstFWInpLimitHFA_MtrNm_f32	1.20000005
_AsstFWInpLimitHysComp_MtrNm_f32	3
_AsstFWNstep_Cnt_u16	4796
_AsstFWPstep_Cnt_u16	246
_RestoreThresh_MtrNm_f32	1.20000005
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
P_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
2 AsstFWUprBoundX HwNm s4p11[0][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288 14336
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][7] 2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0 2048



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
2 AsstFWUprBoundX HwNm s4p11[7][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
2 AsstFWUprBoundX HwNm s4p11[7][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
2 AsstFWUprBoundY MtrNm s4p11[0][0]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-24576
:2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-22528
:2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-14336
:2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-12288
:2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-10240
:z_AsstFWUprBoundY_MtrNm_s4p11[0][9] :2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	
	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	51



Name	Input Value		
t_AsstFWDefltAssistX_HwNm_u8p8[1]	77		
t_AsstFWDefltAssistX_HwNm_u8p8[2]	102		
t_AsstFWDefltAssistX_HwNm_u8p8[3]	128		
t_AsstFWDefltAssistX_HwNm_u8p8[4]	154 179		
t_AsstFWDefltAssistX_HwNm_u8p8[5] t_AsstFWDefltAssistX_HwNm_u8p8[6]	205		
t_AsstFWDefitAssistX_HwNm_u8p8[7]	230		
t_AsstFWDefltAssistX_HwNm_u8p8[8]	256		
t_AsstFWDefltAssistX_HwNm_u8p8[9]	282		
t_AsstFWDefltAssistX_HwNm_u8p8[10]	307		
t_AsstFWDefltAssistX_HwNm_u8p8[11]	333		
t_AsstFWDefltAssistX_HwNm_u8p8[12]	358		
t_AsstFWDefltAssistX_HwNm_u8p8[13]	384		
t_AsstFWDefltAssistX_HwNm_u8p8[14]	410		
t_AsstFWDefltAssistX_HwNm_u8p8[15]	435		
t_AsstFWDefltAssistX_HwNm_u8p8[16]	461		
t_AsstFWDefltAssistX_HwNm_u8p8[17]	486		
t_AsstFWDefltAssistX_HwNm_u8p8[18]	512		
t_AsstFWDefltAssistX_HwNm_u8p8[19]	538		
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-205		
t_AsstFWDefltAssistY_MtrNm_s4p11[1] t_AsstFWDefltAssistY_MtrNm_s4p11[2]	-143 -82		
t_AsstFwDefitAssistY_witrNm_s4p11[2] t_AsstFWDefitAssistY_MtrNm_s4p11[3]	-82 -20		
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	41		
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	102		
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	164		
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	225		
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	287		
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	348		
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	410		
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	471		
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	532		
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	594		
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	655		
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	717		
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	778 840		
t_AsstFWDefltAssistY_MtrNm_s4p11[17] t_AsstFWDefltAssistY_MtrNm_s4p11[18]	901		
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	963		
t_AsstFWPstepNstepThresh_Cnt_u16[0]	123		
t_AsstFWPstepNstepThresh_Cnt_u16[1]	211		
t_AsstFWVehSpd_Kph_u9p7[0]	4352		
t_AsstFWVehSpd_Kph_u9p7[1]	4480		
t_AsstFWVehSpd_Kph_u9p7[2]	4608		
t_AsstFWVehSpd_Kph_u9p7[3]	4736		
t_AsstFWVehSpd_Kph_u9p7[4]	4864		
t_AsstFWVehSpd_Kph_u9p7[5]	4992		
t_AsstFWVehSpd_Kph_u9p7[6]	5120		
t_AsstFWVehSpd_Kph_u9p7[7]	5248		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	8.80000019		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	2 20000005		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	2.20000005 2		
tgt_AssistFirewall_Per1_HwTorque_HwNm_r32.value tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2 2		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	20.1000004		
tgt_Assisti iiewaii_r eri_veriideopeed_rpri_isz.value tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 AsstFirewallActive UIs f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	Uls f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_M		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_M		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	•		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mt		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_	_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_N	1trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt	_enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph	_f32	
Name	Actual Value	Expected Value	Resu
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.92000008	3.92000008 ± 4.88E-04	•
AssistFirewall_ActiveRawAcc_Cnt_M_u16	211	211 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	•
AssistFirewall_CombAsstSV_MtrNm_M_f32	0.439941406	0.439941406 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.02399993	3.02399993 ± 4.88E-04 6.01800013 ± 4.88E-04	
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.01800013		



Name	Actual Value	Expected Value	Result
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.98199999	1.98199999 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	0.439941406	0.439941406 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	•
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	-
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Fest Step 2.3 (Repeat Count = 1)	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	5
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.029999993
AssistFirewall_ActiveR3v_ivi_str.K_Ois_i32	400
AssistFirewall_ActiveRawAcc_Cit_iw_u16 AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall_AssiReducedFeffSv_Cfft_ivi_igt	
	1.13999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0199999996
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.29999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0099999978
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00400000019
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
x_AsstFWInpLimitBaseAsst_MtrNm_f32	3.20000005
z_AsstFWInpLimitHFA_MtrNm_f32	1.39999998
_AsstFWInpLimitHysComp_MtrNm_f32	4
_AsstFWNstep_Cnt_u16	4672
_AsstFWPstep_Cnt_u16	369
_RestoreThresh_MtrNm_f32	1.29999995
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
2 AsstFWUprBoundX HwNm s4p11[1][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
2 AsstFWUprBoundX HwNm s4p11[1][9]	14336
2 AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
z_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
z_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
z_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
z_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
z_AsstFWUprBoundX_HWNm_s4p11[2][6] 2 AsstFWUprBoundX HwNm s4p11[2][7]	2048



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3] t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][3] t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-12288
t2 AsstFWUprBoundY MtrNm s4p11[5][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
12_10011110ppound1_minim_0-prin[r][r0]	102.10



Name	Input Value		
t_AsstFWDefltAssistX_HwNm_u8p8[0]	77		
t_AsstFWDefltAssistX_HwNm_u8p8[1]	102		
t_AsstFWDefltAssistX_HwNm_u8p8[2]	128		
t_AsstFWDefltAssistX_HwNm_u8p8[3]	154		
t_AsstFWDefltAssistX_HwNm_u8p8[4]	179		
t_AsstFWDefltAssistX_HwNm_u8p8[5]	205		
t_AsstFWDefltAssistX_HwNm_u8p8[6] t_AsstFWDefltAssistX_HwNm_u8p8[7]	230 256		
t_AsstFWDefltAssistX_HwNm_u8p8[8]	282		
t_AsstFWDefltAssistX_HwNm_u8p8[9]	307		
t_AsstFWDefltAssistX_HwNm_u8p8[10]	333		
t_AsstFWDefltAssistX_HwNm_u8p8[11]	358		
t_AsstFWDefltAssistX_HwNm_u8p8[12]	384		
t_AsstFWDefltAssistX_HwNm_u8p8[13]	410		
t_AsstFWDefltAssistX_HwNm_u8p8[14]	435		
t_AsstFWDefltAssistX_HwNm_u8p8[15]	461		
t_AsstFWDefltAssistX_HwNm_u8p8[16] t_AsstFWDefltAssistX_HwNm_u8p8[17]	486 512		
t_AsstFWDefitAssistX_HwNm_u8p8[18]	538		
t_AsstFWDefltAssistX_HwNm_u8p8[19]	563		
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2458		
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2662		
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2867		
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3072		
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3277		
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3482		
t_AsstFWDefltAssistY_MtrNm_s4p11[6] t_AsstFWDefltAssistY_MtrNm_s4p11[7]	3686 3891		
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	4096		
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4301		
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4506		
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	4710		
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	4915		
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5120		
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5325		
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5530		
t_AsstFWDefltAssistY_MtrNm_s4p11[16] t_AsstFWDefltAssistY_MtrNm_s4p11[17]	5734 5939		
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6144		
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6349		
t_AsstFWPstepNstepThresh_Cnt_u16[0]	124		
t_AsstFWPstepNstepThresh_Cnt_u16[1]	215		
t_AsstFWVehSpd_Kph_u9p7[0]	7296		
t_AsstFWVehSpd_Kph_u9p7[1]	7424		
t_AsstFWVehSpd_Kph_u9p7[2]	7552		
t_AsstFWVehSpd_Kph_u9p7[3]	7680		
t_AsstFWVehSpd_Kph_u9p7[4] t AsstFWVehSpd Kph u9p7[5]	7808 7936		
t_AsstFWVehSpd_Kph_u9p7[6]	8064		
t_AsstFWVehSpd_Kph_u9p7[7]	8192		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	0		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3.0999999		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2 20 200000		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	30.2000008	Ille f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_AsstFirewallActive tgt_AssistFirewall_Per1_BaseAssistCmd_N		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_N		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_			
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_M		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm	_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_t		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cn		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kpl		1_
Name	Actual Value	Expected Value	Resu
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4.8499999	4.8499999 ± 4.88E-04	•
AssistFirewall_ActiveRawAcc_Cnt_M_u16 AssistFirewall_AcetPodusedPodSV_Cnt_M_las	215	215 ± 1	
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall_CombAsstSV_MtrNm_M_f32	1 3.10009766	1 3.10009766 ± 4.88E-04	
Assisti ilewaii_CuliibAssis v_ivittiviii_ivi_isz	3.10003700	3.10003700 ± 4.00€-04	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0079999	4.0079999 ± 4.88E-04	



Name	Actual Value	Expected Value	Result
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.97600007	2.97600007 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.10009766	3.10009766 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

au				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.4 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	6
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0399999991
AssistFirewall_ActiveRawAcc_Cnt_M_u16	6500
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.14999998
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall HiFreqKSV M str.LPF Str.K Uls f32	0.029999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.3999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.019999996
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	4
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0049999989
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3
k_AsstFWInpLimitHFA_MtrNm_f32	1.5
k_AsstFWInpLimitHysComp_MtrNm_f32	1.10000002
k_AsstFWNstep_Cnt_u16	4548
k_AsstFWPstep_Cnt_u16	492
k_RestoreThresh_MtrNm_f32	1.3999998
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_Asst WopiBoundX_HwNm_s4p11[2][10] t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-4096
	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0] t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144 -4096



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6] t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	
	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-4096 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096 2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096 2048 4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096 2048 4096 6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096 2048 4096 6144 8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096 2048 4096 6144 8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096 2048 4096 6144 8192 10240 12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-4096 2048 4096 6144 8192 10240 12288 14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	-4096 2048 4096 6144 8192 10240 12288 14336 16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	-4096 2048 4096 6144 8192 10240 12288 14336 16384 18432 20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	-4096 2048 4096 6144 8192 10240 12288 14336 16384 18432 20480 22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	-4096 2048 4096 6144 8192 10240 12288 14336 16384 18432 20480 22528 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-4096 2048 4096 6144 8192 10240 12288 14336 16384 18432 20480 22528 -8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096 2048 4096 6144 8192 10240 12288 14336 16384 18432 20480 22528 -8192 -6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-4096 2048 4096 6144 8192 10240 12288 14336 16384 18432 20480 22528 -8192 -6144 -4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3] t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096 2048 4096 6144 8192 10240 12288 14336 16384 18432 20480 22528 -8192 -6144 -4096 -2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3] t2_AsstFWUprBoundY_MtrNm_s4p11[7][4] t2_AsstFWUprBoundY_MtrNm_s4p11[7][4] t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096 2048 4096 6144 8192 10240 12288 14336 16384 18432 20480 22528 -8192 -6144 -4096 -2048 0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3] t2_AsstFWUprBoundY_MtrNm_s4p11[7][4] t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096 2048 4096 6144 8192 10240 12288 14336 16384 18432 20480 22528 -8192 -6144 -4096 -2048 0 2048



Name	Input Value		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288		
t_AsstFWDefltAssistX_HwNm_u8p8[0]	102		
t_AsstFWDefltAssistX_HwNm_u8p8[1]	128		
t_AsstFWDefltAssistX_HwNm_u8p8[2]	154		
t_AsstFWDefltAssistX_HwNm_u8p8[3]	179		
t_AsstFWDefltAssistX_HwNm_u8p8[4]	205		
t_AsstFWDefltAssistX_HwNm_u8p8[5]	230		
t_AsstFWDefltAssistX_HwNm_u8p8[6]	256		
t_AsstFWDefltAssistX_HwNm_u8p8[7] t AsstFWDefltAssistX HwNm u8p8[8]	282 307		
t_AsstFWDefitAssistX_HwNm_u8p8[9]	333		
t_AsstFWDefltAssistX_HwNm_u8p8[10]	358		
t_AsstFWDefltAssistX_HwNm_u8p8[11]	384		
t_AsstFWDefltAssistX_HwNm_u8p8[12]	410		
t_AsstFWDefltAssistX_HwNm_u8p8[13]	435		
t_AsstFWDefltAssistX_HwNm_u8p8[14]	461		
t_AsstFWDefltAssistX_HwNm_u8p8[15]	486		
t_AsstFWDefltAssistX_HwNm_u8p8[16]	512		
t_AsstFWDefltAssistX_HwNm_u8p8[17]	538		
t_AsstFWDefltAssistX_HwNm_u8p8[18]	563		
t_AsstFWDefltAssistX_HwNm_u8p8[19]	589		
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2662		
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2867		
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3072		
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3277		
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3482		
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3686		
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	3891		
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4096		
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4301		
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4506		
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4710		
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	4915		
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5120		
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5325		
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5530		
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5734		
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	5939 6144		
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6349		
t_AsstFWDefltAssistY_MtrNm_s4p11[18] t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6554		
t_AsstFWPstepNstepThresh_Cnt_u16[0]	125		
t_AsstFWPstepNstepThresh_Cnt_u16[1]	219		
t_AsstFWVehSpd_Kph_u9p7[0]	10240		
t_AsstFWVehSpd_Kph_u9p7[1]	10368		
t_AsstFWVehSpd_Kph_u9p7[2]	10496		
t_AsstFWVehSpd_Kph_u9p7[3]	10624		
t_AsstFWVehSpd_Kph_u9p7[4]	10752		
t_AsstFWVehSpd_Kph_u9p7[5]	10880		
t_AsstFWVehSpd_Kph_u9p7[6]	11008		
t_AsstFWVehSpd_Kph_u9p7[7]	11136		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.5		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4.0999999		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	40.2999992		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive		
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32$	32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_N		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt	-		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mi		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32			
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cni		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph		
Name	Actual Value	Expected Value	Resul
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.76000023	5.76000023 ± 4.88E-04	•
	219	219 ± 1	
AssistFirewall_ActiveRawAcc_Cnt_M_u16			· ·
AssistFirewall_ActiveRawAcc_Cnt_M_u16 AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall_CombAsstSV_MtrNm_M_f32	1 3.20019531	1 3.20019531 ± 4.88E-04	•



Name	Actual Value	Expected Value	Result
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8.03999996	8.03999996 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.97000003	3.97000003 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.20019531	3.20019531 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T →				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.5 (Repeat Count = 1)	·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0500000007
AssistFirewall_ActiveRawAcc_Cnt_M_u16	800
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.15999997
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.039999991
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.5
AssistFirewall LwrBoundKSV M str.SV Uls f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.029999993
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00600000005
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2
k_AsstFWInpLimitHFA_MtrNm_f32	1.70000005
k_AsstFWInpLimitHysComp_MtrNm_f32	2.099999
k_AsstFWNstep_Cnt_u16	4424
k_AsstFWPstep_Cnt_u16	615
k_RestoreThresh_MtrNm_f32	1.5
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
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	• "	
Name	Input Value	
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240	
	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]		
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288	
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384	
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144	
	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]		
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432	
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384	
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336	
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288	
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-4096	
	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]		
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-30720	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-28672	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
t2_AsstrWUprBoundY_MtrNm_s4p11[4][6]	4096
	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144 8192



	Name	Input Value		
2. AsserVinchbasers   Tarkets   uplied    54   A Lear Foundbasers   Tarkets   uplied    55   A Lear Foundbasers   Tarkets   uplied    53   A Lear Foundbasers   Tarkets   uplied    53   A Lear Foundbasers   Tarkets   uplied    53   A Lear Foundbasers   Tarkets   uplied    54   A Lear Foundbasers		•		
Laces Victobioscent C. Herbinspirit				
**LaceFWORTAccount** Inwhit** updge[0]				
Aces PWORIAssack   Nehron .uspiks    200	t_AsstFWDefltAssistX_HwNm_u8p8[1]	154		
Application	t_AsstFWDefltAssistX_HwNm_u8p8[2]	179		
Lases Workshoeses L. Jahrhon	t_AsstFWDefltAssistX_HwNm_u8p8[3]			
Class Provinciasion   Chemistry   Chemis				
Laser TVOMEAssext, Namin				
LABERT VORTHASHERS, HARMIN, MIGHT				
Laser TV-cellhassist Namu uppell				
LaserWorkshaseN_Helm_upgil19  400	· · · ·			
LaseTW00HRasistX_Hwhm_u6g8[19]	, , ,			
LasaFW0/MRASexi   Hwhm   1995 19   496				
ChastPVDHIRAsestX_Nebm_ubS0149   512   538   ChastPVDHIRAsestX_Nebm_ubS0149   512   538   ChastPVDHIRAsestX_Nebm_ubS0149   539   539   ChastPVDHIRAsestX_Nebm_ubS0149   514   539   614   539   614	t_AsstFWDefltAssistX_HwNm_u8p8[12]	435		
LastPWDMPAcasist	t_AsstFWDefltAssistX_HwNm_u8p8[13]	461		
Laser WorkPack Nation   Laser Work   Sept	t_AsstFWDefltAssistX_HwNm_u8p8[14]	486		
Laser PMORThAssist X Hwhm   ubg8117    553     Laser PMORThAssist X Hwhm   ubg8119    614     Laser PMORTHASSIST X Hwhm   ubg112    3072     Laser PMORTHASSIST X Hwhm   ubg118    3689     Laser PMORTHASSIST X Hwhm   ubg118    3689     Laser PMORTHASSIST X Hwhm   ubg118    4086     Laser PMORTHASSIST X Hwhm   ubg118    5020     Laser PMORTHASSIST X Hwhm   ubg118    5020     Laser PMORTHASSIST X Hwhm   ubg118    5734     Laser PMORTHASSIST X Hwhm   ubg118    6084     Laser PMORTHASSIST X Hw				
LastPVDeffAcsistY, Mehm. usp01150   561   LastPVDeffAcsistY, Mehm. usp01170   2267   LastPVDeffAcsistY, Minhm. usp11170   2267   LastPVDeffAcsistY, Minhm. usp11170   3077   LastPVDeffAcsistY, Minhm. usp11170   3077   LastPVDeffAcsistY, Minhm. usp11170   3086   LastPVDeffAcsistY, Minhm. usp11170   3086   LastPVDeffAcsistY, Minhm. usp11170   3086   LastPVDeffAcsistY, Minhm. usp11170   3086   LastPVDeffAcsistY, Minhm. usp11170   4091   LastPVDeffAcsistY, Minhm. usp11170   4091   LastPVDeffAcsistY, Minhm. usp11170   4710   LastPVDeffAcsistY, Minhm. usp11170   5326   LastPVDeffAcsistY, Minhm. usp11170   5326   LastPVDeffAcsistY, Minhm. usp11170   5326   LastPVDeffAcsistY, Minhm. usp11170   5326   LastPVDeffAcsistY, Minhm. usp11170   5329   LastPVDeffAcsistY, Minh				
LassFWDeRhassinX_MnPm_sep119				
LassFWDefiaes/Mintrysp11(3)   3072   3277   2265FWDefiaes/Mintrysp11(3)   3072   3277   2265FWDefiaes/Mintrysp11(3)   3082   3277   2265FWDefiaes/Mintrysp11(4)   3086   3277				
LaseFWDelfAssisty_Minns_s4p115				
LassFWDefiassity Minkm scip11g  3892     LassFWDefiassity Minkm scip11g  3893     LassFWDefiassity Minkm scip11g  4096     LassFWDefiassity Minkm scip11g  5120     LassFWDefiassity Minkm scip11g  6144     LassFWDefiassity Minkm scip11g  6154     LassFWDefiassity Minkm scip11g  615				
LassFWDeltAssierY_Minhm_sdp113				
LassFWDeltAssisrY_Mnhm_sdp11[9]				
AssEPWORITASSIN' Minkm_s4p11 5		3686		
AssEPWOHBASSEY_MINTMsdp11[9]	t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3891		
LASSEFWOERIAGSSEY_MINTM_SEPTING  LASSEFWOERIAGSSET_MINTM_SEPTING  LASSEFTWOERIAGSSET_MINTM_SEPTING  LASSEFTWOERIAGSSET_MINTM_SEPTING  LASSEFTWOERIAGSSET_MINTM_SEPTING  LASSEFTWOERIAGSSET_MINTM_SEPTING  LASSEFTWOERIAGSSET_MINTM_SEPTING  LASSEFTWOERIAGSSET_MINTM_SEP	t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4096		
AssiFWDefiXasiSY_Mrhm_s4p11[9]	t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4301		
L'AssIFWDeffMasistY_Mirkm_s4p11[10]				
AssiFWDefitAssiSY_Minkm_sep11[13]   5120   5325     LassiFWDefitAssiSY_Minkm_sep11[13]   5535     LassiFWDefitAssiSY_Minkm_sep11[14]   5734     LassiFWDefitAssiSY_Minkm_sep11[15]   5539     LassiFWDefitAssiSY_Minkm_sep11[16]   6144     LassiFWDefitAssiSY_Minkm_sep11[17]   6349     LassiFWDefitAssiSY_Minkm_sep11[17]   6349     LassiFWDefitAssiSY_Minkm_sep11[18]   6554     LassiFWDefitAssiSY_Minkm_sep11[18]   6758     LassiFWDefitAssiSY_Minkm_sep11[19]   6758     LassiFWDefitAssiSY_Minkm_sep11[19]   6758     LassiFWDefitAssiSY_Minkm_sep11[19]   126     LassiFWDefitAssiSY_Minkm_sep11[19]   13184     LassiFWDefitAssiSY_Minkm_sep11				
LASSIFWOEITASSITY_MINTM_S4P11[12]   5325   5305				
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L'AssiFWDelftAssistY_MirNm_s4p11[15]				
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LAssIFWDefthAssistY_MtrNm_s4p11[19]	t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6349		
LAssIFWPstepNstepThresh_Cnt_u16[0] 126 LAssIFWPestpNstepThresh_Cnt_u16[1] 223 LAssIFWPestpOktph_LepDrtol	t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6554		
LAssIFWPstepNstepThresh_Cnt_u16[1] 223  LAssIFWVenSpd_Kph_u9p7(1) 13184  LAssIFWVenSpd_Kph_u9p7[2] 13440  LAssIFWVenSpd_Kph_u9p7[3] 13460  LAssIFWVenSpd_Kph_u9p7[3] 13668  LAssIFWVenSpd_Kph_u9p7[5] 13824  LAssIFWVenSpd_Kph_u9p7[6] 13892  LAssIFWVenSpd_Kph_u9p7[6] 13892  LAssIFWVenSpd_Kph_u9p7[7] 14080  LAssIFWVenSpd_Kph_u9p7[7] 14080  LAssIFWVenSpd_Kph_u9p7[7] 14080  LAssIFWVenSpd_Kph_u9p7[7] 14080  LAssIFIVVenSpd_Kph_u9p7[8] 13892  LAssIFIVVenSpd_Kph_u9p7[8] 13892  LAssIFIVVenSpd_Kph_u9p7[8] 14080  LAssIFIVVenSpd_Kph_u9p7[8] 1595  LASSIFIVENSIL_Per1_HysteresisComp_MtrNm_i32 1595  LASSISHIFWAIL_Per1_HysteresisComp_MtrNm_i32 1595  LASSISHIFWAIL_Per1_HysteresisComp_MtrNm_i32 1595  LASSISHIFWAIL_Per1_HysteresisCom	t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6758		
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t_AssitFWVehSpd_Kph_u9p7[6]				
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tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value  tgt_AssistFirewall_Per1_Mec_Counter_Cnt_enum.value  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_AsstFirewallActive_Uls_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_CombinedAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgt  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_Mec_Counter_Cnt_enum  tgt_Rte_Inst_Ap_AssistFirewall_Per1_VehicleSpeed_Kph_f32  Name  Actual Value  Expected Value  AssistFirewall_ActiveRawAcc_Cnt_M_u16  223				
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value  tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_AsstFirewallActive_Uls_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_AsstFirewallAssistMtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstThl_Service_Cnt_lgt  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_MEC_Counter_Cnt_enum  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_MEC_Counter_Cnt_enum  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_VehicleSpeed_Kph_f32  Name  Actual Value  Expected Value  AssistFirewall_ActiveRawAcc_Cnt_M_u16	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.5		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value  tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value  tgt_Rte_Inst_Ap_AssistFirewall_Per1_AsstFirewall_Per1_AsstFirewallActive_Uls_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Rel_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Rel_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_AssistFirewall_AssistFirewall_Per1_MEC_Counter_Cnt_enum  tgt_Rte_Inst_Ap_AssistFirewall_Per1_WEC_Counter_Cnt_enum  tgt_Rte_Inst_Ap_AssistFirewall_Per1_VehicleSpeed_Kph_f32  Name  Actual Value  AssistFirewall_ActiveKSV_M_str.SV_Uls_f32  Actual Value  AssistFirewall_ActiveRawAcc_Cnt_M_u16	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value  tgt_Rte_Inst_Ap_AssistFirewall_Per1_AsstFirewallActive_Uls_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_MEC_Counter_Cnt_enum  tgt_Rte_Inst_Ap_AssistFirewall_Per1_VehicleSpeed_Kph_f32  Name  Actual Value  Expected Value  AssistFirewall_ActiveRawAcc_Cnt_M_u16				
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value  tgt_Rte_Inst_Ap_AssistFirewall_Per1_AsstFirewallActive_Uls_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_CombinedAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Int_ tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Int_ tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_MEC_Counter_Cnt_enum  tgt_Rte_Inst_Ap_AssistFirewall_Per1_VehicleSpeed_Kph_f32  Name  Actual Value  Expected Value  AssistFirewall_ActiveRawAcc_Cnt_M_u16				
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value  tgt_Rte_Inst_Ap_AssistFirewall_Per1_AsstFirewallActive_Uls_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igt  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_Hyorque_HwNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_Hyorque_HwNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_Hyorque_HwNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_Hyorque_HwNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_Per1_Hyorque_Hyorq				
tgt_Rte_Inst_Ap_AssistFirewall_Per1_AsstFirewall_Per1_AsstFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgt tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall_Per1_VehicleSpeed_Kph_f32  Name  Actual Value  Expected Value  AssistFirewall_ActiveRawAcc_Cnt_M_u16	•			
tgt_Rte_Inst_Ap_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgt tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgt tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall_Per1_VehicleSpeed_Kph_f32  Name  Actual Value  Expected Value  6.6500001  6.6500001 ± 4.88E-04  AssistFirewall_ActiveRawAcc_Cnt_M_u16			Ille f32	
tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AssitD_Service_Cnt_lgt tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AssitD_Service_Cnt_lgt tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall_Per1_VehicleSpeed_Kph_f32  Name Actual Value  AssistFirewall_ActiveKSV_M_str.SV_Uls_f32 AssistFirewall_ActiveRawAcc_Cnt_M_u16  tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_UpsteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_		*		
tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgt tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall_Per1_VehicleSpeed_Kph_f32  Name  Actual Value  AssistFirewall_ActiveKSV_M_str.SV_Uls_f32 AssistFirewall_ActiveRawAcc_Cnt_M_u16  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32  Actual Value  6.6500001 6.6500001 ± 4.88E-04 AssistFirewall_ActiveRawAcc_Cnt_M_u16		-		
tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall_Per1_VehicleSpeed_Kph_f32  Name  Actual Value  AssistFirewall_ActiveKSV_M_str.SV_Uls_f32 AssistFirewall_ActiveRawAcc_Cnt_M_u16  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_Hys				
tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_VehicleSpeed_Kph_f32  Name  Actual Value  AssistFirewall_ActiveKSV_M_str.SV_Uls_f32 AssistFirewall_ActiveRawAcc_Cnt_M_u16  tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_Hyste		-		
tgt_Rte_Inst_Ap_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_VehicleSpeed_Kph_f32  Name Actual Value Expected Value AssistFirewall_ActiveKSV_M_str.SV_Uls_f32 AssistFirewall_ActiveRawAcc_Cnt_M_u16  223 223 ± 1				
tgt_Rte_Inst_Ap_AssistFirewall_Per1_VehicleSpeed_Kph_f32  Name  Actual Value  Expected Value  AssistFirewall_ActiveKSV_M_str.SV_Uls_f32  AssistFirewall_ActiveRawAcc_Cnt_M_u16  Expected Value  223 ± 1	$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_M	ltrNm_f32	
Name         Actual Value         Expected Value           AssistFirewall_ActiveKSV_M_str.SV_Uls_f32         6.6500001         6.6500001 ± 4.88E-04           AssistFirewall_ActiveRawAcc_Cnt_M_u16         223         223 ± 1	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt	_enum	
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32 6.6500001 6.6500001 ± 4.88E-04 AssistFirewall_ActiveRawAcc_Cnt_M_u16 223 223 ± 1	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph	_f32	
AssistFirewall_ActiveRawAcc_Cnt_M_u16         223         223 ± 1	Name	Actual Value	Expected Value	Resul
				•
Assisterewall AssisteducedPertSV Cnt M Inc. 11				•
AssistFirewall_AssitSV_MtrNm_M_f32 3.29980469 3.29980469 3.29980469 ± 4.88E-04	AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	•



Name	Actual Value	Expected Value	Result
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.83199978	5.83199978 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.39700007	1.39699996 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.96400023	4.96400023 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.29980469	3.29980469 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Τ				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	-

Test Step 2.6 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1000
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.16999996
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.60000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0399999991
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00700000022
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
<_AsstFWInpLimitBaseAsst_MtrNm_f32	1
<_AsstFWInpLimitHFA_MtrNm_f32	1.8999998
<pre>c_AsstFWInpLimitHysComp_MtrNm_f32</pre>	2.5
c_AsstFWNstep_Cnt_u16	4300
c_AsstFWPstep_Cnt_u16	738
c_RestoreThresh_MtrNm_f32	1.60000002
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
2 AsstFWUprBoundX HwNm s4p11[2][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
:2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
	0
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_Asst WopiBoundX_HwNm_s4p11[6][4]	-8192
	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	
12_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-10240
:2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-6144
LZ_N9911. AN Obliponina i "IAITIAIII" 24b i i[n][1]	-6144 -4096
2 ApptEW/UprPoundV Mt-Nim - 44440303	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	
:2_AsstFWUprBoundY_MtrNm_s4p11[0][8] :2_AsstFWUprBoundY_MtrNm_s4p11[0][9] :2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-2048 0



ame	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-24576
P_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-22528
P_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-18432
P_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-16384
P_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-14336
P_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-12288
P_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-10240
P_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-8192
P_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-30720
P_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-28672
P_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-26624
P_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-20480
	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	
P_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-16384
P_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-14336
P_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-10240
P_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336
P_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288
P_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240
P_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192
P_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144
	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	
?_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048
P_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0
P_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048
P_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096
P_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144
P_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
P_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
P_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
P_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
P_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
P_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
P_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
P_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
P_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-20480
P_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-18432
P_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-16384
P_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-14336
?_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-12288
?_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-10240
P_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-8192
P_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-6144
P_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-4096
P_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-2048
P_AsstFWUprBoundY_MtrNm_s4p11[5][10]	0
P_AsstFWUprBoundY_MtrNm_s4p11[6][0]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144 8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	8192
?_AsstFWUprBoundY_MtrNm_s4p11[6][1] !_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192 10240
?_AsstFWUprBoundY_MtrNm_s4p11[6][1] ?_AsstFWUprBoundY_MtrNm_s4p11[6][2] ?_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192 10240 12288
:_AsstFWUprBoundY_MtrNm_s4p11[6][1] :_AsstFWUprBoundY_MtrNm_s4p11[6][2] :_AsstFWUprBoundY_MtrNm_s4p11[6][3] :_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192 10240 12288 14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192 10240 12288 14336 16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 2_AsstFWUprBoundY_MtrNm_s4p11[6][5] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	8192 10240 12288 14336 16384 18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 2_AsstFWUprBoundY_MtrNm_s4p11[6][5] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192 10240 12288 14336 16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 2_AsstFWUprBoundY_MtrNm_s4p11[6][5] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	8192 10240 12288 14336 16384 18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 2_AsstFWUprBoundY_MtrNm_s4p11[6][5] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192 10240 12288 14336 16384 18432 20480
2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 2_AsstFWUprBoundY_MtrNm_s4p11[6][5] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192 10240 12288 14336 16384 18432 20480 22528
2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 2_AsstFWUprBoundY_MtrNm_s4p11[6][5] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192 10240 12288 14336 16384 18432 20480 22528 24576 26624
2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 2_AsstFWUprBoundY_MtrNm_s4p11[6][5] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192 10240 12288 14336 16384 18432 20480 22528 24576 26624 -2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 2_AsstFWUprBoundY_MtrNm_s4p11[6][5] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 2_AsstFWUprBoundY_MtrNm_s4p11[7][0] 2_AsstFWUprBoundY_MtrNm_s4p11[7][0] 2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	8192 10240 12288 14336 16384 18432 20480 22528 24576 26624 -2048 0
2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 2_AsstFWUprBoundY_MtrNm_s4p11[6][5] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 2_AsstFWUprBoundY_MtrNm_s4p11[7][0] 2_AsstFWUprBoundY_MtrNm_s4p11[7][0] 2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	8192 10240 12288 14336 16384 18432 20480 22528 24576 26624 -2048 0 2048
2.AsstFWUprBoundY_MtrNm_s4p11[6][1] 2.AsstFWUprBoundY_MtrNm_s4p11[6][2] 2.AsstFWUprBoundY_MtrNm_s4p11[6][3] 2.AsstFWUprBoundY_MtrNm_s4p11[6][4] 2.AsstFWUprBoundY_MtrNm_s4p11[6][5] 2.AsstFWUprBoundY_MtrNm_s4p11[6][6] 2.AsstFWUprBoundY_MtrNm_s4p11[6][7] 2.AsstFWUprBoundY_MtrNm_s4p11[6][8] 2.AsstFWUprBoundY_MtrNm_s4p11[6][9] 2.AsstFWUprBoundY_MtrNm_s4p11[6][0] 2.AsstFWUprBoundY_MtrNm_s4p11[7][0] 2.AsstFWUprBoundY_MtrNm_s4p11[7][0] 2.AsstFWUprBoundY_MtrNm_s4p11[7][1] 2.AsstFWUprBoundY_MtrNm_s4p11[7][1] 2.AsstFWUprBoundY_MtrNm_s4p11[7][2] 2.AsstFWUprBoundY_MtrNm_s4p11[7][3]	8192 10240 12288 14336 16384 18432 20480 22528 24576 26624 -2048 0 2048 4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 2_AsstFWUprBoundY_MtrNm_s4p11[6][5] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 2_AsstFWUprBoundY_MtrNm_s4p11[7][0] 2_AsstFWUprBoundY_MtrNm_s4p11[7][0] 2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	8192 10240 12288 14336 16384 18432 20480 22528 24576 26624 -2048 0 2048 4096 6144
2.AsstFWUprBoundY_MtrNm_s4p11[6][1] 2.AsstFWUprBoundY_MtrNm_s4p11[6][2] 2.AsstFWUprBoundY_MtrNm_s4p11[6][3] 2.AsstFWUprBoundY_MtrNm_s4p11[6][4] 2.AsstFWUprBoundY_MtrNm_s4p11[6][5] 2.AsstFWUprBoundY_MtrNm_s4p11[6][6] 2.AsstFWUprBoundY_MtrNm_s4p11[6][7] 2.AsstFWUprBoundY_MtrNm_s4p11[6][8] 2.AsstFWUprBoundY_MtrNm_s4p11[6][9] 2.AsstFWUprBoundY_MtrNm_s4p11[6][0] 2.AsstFWUprBoundY_MtrNm_s4p11[7][0] 2.AsstFWUprBoundY_MtrNm_s4p11[7][0] 2.AsstFWUprBoundY_MtrNm_s4p11[7][1] 2.AsstFWUprBoundY_MtrNm_s4p11[7][1] 2.AsstFWUprBoundY_MtrNm_s4p11[7][2] 2.AsstFWUprBoundY_MtrNm_s4p11[7][3]	8192 10240 12288 14336 16384 18432 20480 22528 24576 26624 -2048 0 2048 4096
2.AsstFWUprBoundY_MtrNm_s4p11[6][1] 2.AsstFWUprBoundY_MtrNm_s4p11[6][2] 2.AsstFWUprBoundY_MtrNm_s4p11[6][3] 2.AsstFWUprBoundY_MtrNm_s4p11[6][4] 2.AsstFWUprBoundY_MtrNm_s4p11[6][5] 2.AsstFWUprBoundY_MtrNm_s4p11[6][6] 2.AsstFWUprBoundY_MtrNm_s4p11[6][7] 2.AsstFWUprBoundY_MtrNm_s4p11[6][8] 2.AsstFWUprBoundY_MtrNm_s4p11[6][9] 2.AsstFWUprBoundY_MtrNm_s4p11[6][10] 2.AsstFWUprBoundY_MtrNm_s4p11[7][0] 2.AsstFWUprBoundY_MtrNm_s4p11[7][1] 2.AsstFWUprBoundY_MtrNm_s4p11[7][1] 2.AsstFWUprBoundY_MtrNm_s4p11[7][2] 2.AsstFWUprBoundY_MtrNm_s4p11[7][3] 2.AsstFWUprBoundY_MtrNm_s4p11[7][3] 2.AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192 10240 12288 14336 16384 18432 20480 22528 24576 26624 -2048 0 2048 4096 6144



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Name	Input Value			
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336			
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384			
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432			
t_AsstFWDefltAssistX_HwNm_u8p8[0]	154			
t_AsstFWDefltAssistX_HwNm_u8p8[1]	179			
t_AsstFWDefltAssistX_HwNm_u8p8[2]	205			
t_AsstFWDefltAssistX_HwNm_u8p8[3]	230			
t_AsstFWDefltAssistX_HwNm_u8p8[4]	256			
t_AsstFWDefltAssistX_HwNm_u8p8[5]	282			
t_AsstFWDefltAssistX_HwNm_u8p8[6]	307			
t_AsstFWDefltAssistX_HwNm_u8p8[7]	333			
t_AsstFWDefltAssistX_HwNm_u8p8[8]	358			
t_AsstFWDefltAssistX_HwNm_u8p8[9]	384			
t_AsstFWDefltAssistX_HwNm_u8p8[10]	410			
t_AsstFWDefltAssistX_HwNm_u8p8[11]	435 461			
t_AsstFWDefltAssistX_HwNm_u8p8[12] t_AsstFWDefltAssistX_HwNm_u8p8[13]	486			
t_AsstFWDefltAssistX_HwNm_u8p8[14]	512			
t_AsstFWDefitAssistX_HwNm_u8p8[15]	538			
t AsstFWDefitAssistX HwNm u8p8[16]	563			
t_AsstFWDefltAssistX_HwNm_u8p8[17]	589			
t_AsstFWDefitAssistX_HwNm_u8p8[18]	614			
t_AsstFWDefltAssistX_HwNm_u8p8[19]	640			
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3072			
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3277			
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3482			
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3686			
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3891			
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4096			
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4301			
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4506			
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t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4915			
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5120			
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5325			
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5530			
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5734			
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5939			
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6144			
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t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6554			
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6758			
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6963			
t_AsstFWPstepNstepThresh_Cnt_u16[0]	127			
t_AsstFWPstepNstepThresh_Cnt_u16[1]	227			
t_AsstFWVehSpd_Kph_u9p7[0]	16128			
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	16256 16384			
t_AsstFWVehSpd_Kph_u9p7[3]	16512			
t_AsstFWVehSpd_Kph_u9p7[4]	16640			
t_AsstFWVehSpd_Kph_u9p7[5]	16768			
t_AsstFWVehSpd_Kph_u9p7[6]	16896			
t_AsstFWVehSpd_Kph_u9p7[7]	17024			
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1			
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0			
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-8.80000019			
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	6			
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6			
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2			
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	60.2999992			
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	Uls_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_Mt	rNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_M	trNm_f32		
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AsstTbl\_Service\_Cnt\_$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Se	rvice_Cnt_lgc		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mti	·Nm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_			
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_M			
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt			
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph	The second secon		
Name	Actual Value	Expected Value		Resul
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7.51999998	7.51999998 ± 4.88E-04		
AssistFirewall_ActiveRawAcc_Cnt_M_u16	227	227 ± 1		•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1		•



Name	Actual Value	Expected Value	Result
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.39990234	3.39990234 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.73000002	6.73000002 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.51200008	2.51200008 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.95800018	5.95800018 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.39990234	3.39990234 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	•
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Τ				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	-

Test Step 2.7 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8
AssistFirewall ActiveKSV M str.K Uls f32	0.0599999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1000
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.17999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.050000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.60000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall LwrBoundKSV M str.K Uls f32	0.039999991
AssistFirewall PNCountStatus Cnt M lqc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	6
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00700000022
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	tgt_kte_inst_Ap_Assistriiewaii
k_AsstFWInpLimitHFA_MtrNm_f32	1.89999998
k_AsstFWInpLimitHysComp_MtrNm_f32	2.5
k_AsstFWNstep_Cnt_u16	4300
k_AsstFWPstep_Cnt_u16	738
·	1,70000005
k_RestoreThresh_MtrNm_f32	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	· · · · · · · · · · · · · · · · · · ·
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1] t2 AsstFWUprBoundX HwNm_s4p11[7][2]	-4090 -2048
	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	2048
L_, SSS TOPIDOGIGI_WILLTIN_STP11[O][10]	2010



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-30720
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-20480
ادر Asst WopiBoundY_MtrNm_s4p11[4][6]	-18432
ادر المحادث ا	-16384
	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
= -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1	12288



Name	Input Value		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480		
t_AsstFWDefltAssistX_HwNm_u8p8[0]	179		
t_AsstFWDefltAssistX_HwNm_u8p8[1]	205		
t_AsstFWDefltAssistX_HwNm_u8p8[2]	230		
t_AsstFWDefltAssistX_HwNm_u8p8[3]	256		
t_AsstFWDefltAssistX_HwNm_u8p8[4]	282		
t_AsstFWDefltAssistX_HwNm_u8p8[5]	307		
t AsstFWDefltAssistX HwNm u8p8[6]	333		
t AsstFWDefltAssistX HwNm u8p8[7]	358		
t_AsstFWDefltAssistX_HwNm_u8p8[8]	384		
t_AsstFWDefltAssistX_HwNm_u8p8[9]	410		
t_AsstFWDefltAssistX_HwNm_u8p8[10]	435		
t_AsstFWDefltAssistX_HwNm_u8p8[11]	461		
t_AsstFWDefltAssistX_HwNm_u8p8[12]	486		
t_AsstFWDefltAssistX_HwNm_u8p8[13]	512		
t AsstFWDefltAssistX HwNm u8p8[14]	538		
t_AsstFWDefltAssistX_HwNm_u8p8[15]	563		
	589		
t_AsstFWDefltAssistX_HwNm_u8p8[16]			
t_AsstFWDefltAssistX_HwNm_u8p8[17]	614		
t_AsstFWDefltAssistX_HwNm_u8p8[18]	640		
t_AsstFWDefltAssistX_HwNm_u8p8[19]	666		
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3277		
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3482		
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3686		
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3891		
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096		
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4301		
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4506		
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4710		
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4915		
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5120		
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5325		
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5530		
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5734		
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5939		
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6144		
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6349		
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6554		
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6758		
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6963		
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7168		
t_AsstFWPstepNstepThresh_Cnt_u16[0]	128		
t_AsstFWPstepNstepThresh_Cnt_u16[1]	231		
t_AsstFWVehSpd_Kph_u9p7[0]	19072		
t_AsstFWVehSpd_Kph_u9p7[1]	19200		
t_AsstFWVehSpd_Kph_u9p7[2]	19328		
t_AsstFWVehSpd_Kph_u9p7[3]	19456		
t_AsstFWVehSpd_Kph_u9p7[4]	19584		
t_AsstFWVehSpd_Kph_u9p7[5]	19712		
t_AsstFWVehSpd_Kph_u9p7[6]	19840		
t_AsstFWVehSpd_Kph_u9p7[7]	19968		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
-			
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	8.80000019		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	6		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	60.2000008		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_Mt		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_Mi		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lg	1 -		
	•	•	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mtr		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_	enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_	_f32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7.51999998	7.51999998 ± 4.88E-04	-
AssistFirewall_ActiveRawAcc_Cnt_M_u16	231	231 ± 1	¥



Name	Actual Value	Expected Value	Result
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.5	3.5 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.92000008	6.92000008 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.47200012	2.47199988 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.95800018	5.95800018 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.5	3.5 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	•
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Name		
AssistFrewall LeviceNSV_M_str. Vu_str.	Test Step 2.8 (Repeat Count = 1)	
AssistFirewall ActiveRsV_M_str.K_UIs_132		·
AssistFrewall ActivePawAcc_Cnt_M_ut6         1           AssistFrewall_AssiReducePerfsV_cnt_M_ut6         1           AssistFrewall_HiFreqKSV_MrMm_M_32         1.19000002           AssistFrewall_HiFreqKSV_M_str_LPF_Str_KU_lls_[32         0,0700000003           AssistFrewall_HiFreqKSV_M_str_LPF_Str_KU_lls_[32         0,0700000003           AssistFrewall_HiFreqKSV_M_str_LPF_Str_KU_lls_[32         1,79999995           AssistFrewall_HiFreqKSV_M_str_LV_lls_[32         4,099999           AssistFrewall_PNOuntStatus_Cnt_M_lgc         0           AssistFrewall_UprBoundKSV_M_str_LV_lls_[32         8           AssistFrewall_UprBoundKSV_M_str_LV_lls_[32         8           AssistFrewall_UprBoundKSV_M_str_LV_lls_[32         0,0089999961           Rte_Inst_Ap_AssistFrewall         1,2999995           Rte_Inst_Ap_AssistFrewall         1,2999995           Rte_Inst_Ap_AssistFrewall         3,29999995           Rte_Inst_Ap_AssistFrewall         4,052           R_assifWinpLimitHs_Almin_[32         1,2999995           R_assifWinpLimitHs_Almin_[32         1,79999995           R_assifWinpLimitHs_Almin_[32         1,79999995           R_assifWinpLimitHs_Almin_[32         1,79999995           R_assifWinpLimitHs_Almin_[32         0           R_assifWinpLimitHs_Almin_[41]10[10]         4096		
AssistFirewalL CombAssiSV_MtrNm_M_52 1.19000006 AssistFirewalLHFreqKSV_MtrNm_M_52 1.19000002 AssistFirewalLHFreqKSV_MtrLPF_StrK_Uls_f32 0.0700000003 AssistFirewalLHFreqKSV_MtrLPF_StrK_Uls_f32 1.79999995 AssistFirewalLLHFreqKSV_MtrLPF_StrK_Uls_f32 1.79999995 AssistFirewalLLWBoundKSV_M_str.CP_Uls_f32 4.0999999 AssistFirewalLLWBoundKSV_M_str.CV_Uls_f32 4.099999987 AssistFirewalLLWBoundKSV_M_str.CV_Uls_f32 0.0599999987 AssistFirewalLUPBoundKSV_M_str.CV_Uls_f32 0.05999999987 AssistFirewalLUPBoundKSV_M_str.CV_Uls_f32 0.00899999961 Rtl.plf_QuantStr.CV_M_str.CV_Uls_f32 0.00899999961 Rtl.plf_QuantStr.CV_M_str.CV_Uls_f32 0.00899999961 Rtl.plf_QuantStr.CV_M_str.CV_Uls_f32 0.00899999961 Rtl.plf_QuantStr.CV_M_str.CV_Uls_f32 0.00899999961 Rtl.plf_QuantStr.CV_M_str.CV_Uls_f32 0.00899999961 Rtl.plf_QuantStr.CV_M_str.CV_Uls_f32 0.00899999961 Rtl.plf_QuantStr.CV_Uls_f32 0.00899999961 Rtl.plf_QuantStr.CV_Uls_f32 0.0089999999999999999999999999999999999		
AssistFirewalLiFreqKSV M. str.LPF. Str.K. Uis.132 1.100000002 AssistFirewalLiFreqKSV M. str.LPF. Str.K. Uis.132 0.0700000003 AssistFirewalLiFreqKSV M. str.CPF. Uis.132 1.79999995 AssistFirewalLiFreqKSV M. str.CP Uis.132 1.79999999 AssistFirewalLiFreqKSV M. str.CP Uis.132 1.79999999 AssistFirewalLiFreqKSV M. str.CV Uis.132 0.05999999997 AssistFirewalLiPRDCountStatus_Cnt_M.lgc 0.05999999997 AssistFirewalLiPRDCountStatus_Cnt_M.lgc 0.0599999999999999999999999999999999999	AssistFirewall_ActiveRawAcc_Cnt_M_u16	· · · ·
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_HiFreqKSV_M_str.CF_UIs_f32         0.0700000003           AssistFirewall_HiFreqKSV_M_str.CF_UIs_f32         1.79999995           AssistFirewall_LwrBoundKSV_M_str.K_UIs_f32         0.0599999987           AssistFirewall_LwrBoundKSV_M_str.K_UIs_f32         0.0599999987           AssistFirewall_LyrBoundKSV_M_str.K_UIs_f32         8           AssistFirewall_UprBoundKSV_M_str.K_UIs_f32         0.00899999961           Rte_Inst_Ap_AssistFirewall         tg.Ret_Inst_Ap_AssistFirewall           K_asstFWInpLimitHFs_MtrNm_f32         3           K_AsstFWInpLimitHFs_MtrNm_f32         1.29999995           K_AsstFWInpLimitHFs_Ont_u16         4052           K_AsstFWInpLimitHFs_MtrNm_f32         1.799999995           K_AsstFWInpLimitHFs_MtrNm_s4p110[0]         4052           K_AsstFWInpLimitHFs_MtrNm_s4p110[0]         4062           K_AsstFWInpLimitHFs_MtrNm_s4p110[0]         4066           K_AsstFWInpLimitHFs_MtrNm_s4p110[0]         4096           L_AsstFWUprBoundX_HwNm_s4p110[0]         0           L_AsstFWUprBoundX_HwNm_s4p110[0]         4096           L_AsstFWUprBoundX_HwNm_s4p110[0]         4096           L_AsstFWUprBoundX_HwNm_s4p110[0]         4096           L_AsstFWUprBoundX_HwNm_s4p110[0]         4096           L_AsstFWUprBoundX_HwNm_s4p110[0]         1228	AssistFirewall_CombAsstSV_MtrNm_M_f32	
AssistFirewall_HiFreqKSV_M_str.Cy_Uls_f32         4.0999999           AssistFirewall_LwBoundKSV_M_str.K_Uls_f32         0.059999987           AssistFirewall_PNCountStatus_Cnt_M_lgc         0           AssistFirewall_UprBoundKSV_M_str.K_Uls_f32         8           AssistFirewall_UprBoundKSV_M_str.K_Uls_f32         0.00999999961           Rte_Inst_Ap_AssistFirewall         tgt.Rte_Inst_Ap_AssistFirewall           k_AsstFWInpLimitBaseAsst_MtrNm_f32         1           k_AsstFWInpLimitHFA_MtrNm_f32         3.29999995           k_AsstFWInpLimitHFA_MtrNm_f32         3.29999995           k_AsstFWInpLimitHFA_MtrNm_f32         3.29999995           k_AsstFWInpLimitHFA_MtrNm_f32         1.79999995           k_AsstFWInpLimitHFA_MtrNm_f32         1.79999995           k_AsstFWInpLimitHFA_MtrNm_f32         1.79999995           k_AsstFWInpLimitHFA_MtrNm_f32         1.79999995           k_AsstFWInpBoundX_HwNm_s4p11[0][0]         4096           t_AsstFWUpBoundX_HwNm_s4p11[0][0]         2048           t_AsstFWUpBoundX_HwNm_s4p11[0][0]         0           t_AsstFWUpBoundX_HwNm_s4p11[0][0]         6144           t_AsstFWUpBoundX_HwNm_s4p11[0][0]         6144           t_AsstFWUpBoundX_HwNm_s4p11[0][0]         14336           t_AsstFWUpBoundX_HwNm_s4p11[0][0]         14336           t_Asst		
AssistFirewall_LwrBoundKSV_M_str.K_Uls_[32         0.059999999           AssistFirewall_LwrBoundKSV_M_str.K_Uls_[32         0.05999999987           AssistFirewall_UprBoundKSV_M_str.SV_Uls_[32         8           AssistFirewall_UprBoundKSV_M_str.K_Uls_[32         0.00899999991           Ke_Inst.Ap_AssistFirewall         tg_Rte_Inst.Ap_AssistFirewall           k_AsstFWInpLimitBaseAss_MrNm_[32         1.29999995           k_AsstFWInpLimitHsA_MrNm_[32         1.29999995           k_AsstFWInpLimitHysComp_MtrNm_[32         3.29999995           k_AsstFWInpLore, _Cnt_u16         4052           k_AsstFWDeto_Cnt_u16         984           k_RestoreThresh_MtrNm_[32         1.79999995           2_AsstFWDpfBoundX_HwNm_s4p11[0][0]         4096           2_AsstFWUprBoundX_HwNm_s4p11[0][1]         2048           2_AsstFWUprBoundX_HwNm_s4p11[0][3]         2048           2_AsstFWUprBoundX_HwNm_s4p11[0][4]         4096           2_AsstFWUprBoundX_HwNm_s4p11[0][5]         6144           2_AsstFWUprBoundX_HwNm_s4p11[0][6]         8192           2_AsstFWUprBoundX_HwNm_s4p11[0][7]         10240           2_AsstFWUprBoundX_HwNm_s4p11[0][9]         14336           1_AsstFWUprBoundX_HwNm_s4p11[0][1]         12288           1_AsstFWUprBoundX_HwNm_s4p11[1][1]         1228           1_AsstFWUprBou	AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	
AssistFirewall_LyrBoundKSV_M.str.K_Uls_f32	AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	
AssistFirewall_DPCountStatus_Cnt_M_sic.XV_Uls_f32         8           AssistFirewall_UprBoundKSV_M_str.X-Uls_f32         0.0099999961           Rte_Inst_Ap_AssistFirewall         tg_Rte_Inst_Ap_AssistFirewall           k_AsstFWInpLimitBaseAsst_MtrNm_f32         1.29999995           k_AsstFWInpLimitHysComp_MtrNm_f32         1.29999995           k_AsstFWInpLimitHysComp_MtrNm_f32         3.29999995           k_AsstFWInpLimitHysComp_MtrNm_f32         4052           k_AsstFWInpLimitHysComp_MtrNm_f32         1.799999995           k_AsstFWInpBoundX_HwNm_s4p11[0]I0]         4096           k_AsstFWInpBoundX_HwNm_s4p11[0]I0]         4096           k_AsstFWUpBoundX_HwNm_s4p11[0]I1]         2048           k_AsstFWUpBoundX_HwNm_s4p11[0]I3         0           k_AsstFWUpBoundX_HwNm_s4p11[0]I3         4096           k_AsstFWUpBoundX_HwNm_s4p11[0]I6]         6144           k_AsstFWUpBoundX_HwNm_s4p11[0]I6]         6144           k_AsstFWUpBoundX_HwNm_s4p11[0]I6]         10240           k_AsstFWUpBoundX_HwNm_s4p11[0]I6]         12288           k_AsstFWUpBoundX_HwNm_s4p11[0]I0]         14336           k_AsstFWUpBoundX_HwNm_s4p11[0]I0]         14336           k_AsstFWUpBoundX_HwNm_s4p11[1]I0]         14336           k_AsstFWUpBoundX_HwNm_s4p11[1]I1]         12288           k_AsstFWUpBoun	AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_UprBoundKSV_M_str.KV_Uls_f32         8           AssistFirewall_UprBoundKSV_M_str.K_Uls_f32         0.00899999961           Ke_Inst_Ap_AssistFirewall         tgt_Rte_Inst_Ap_AssistFirewall           k_AsstFWInpLimitBaseAsst_MtrNm_f32         3           k_AsstFWInpLimitHysComp_MtrNm_f32         1.29999995           k_AsstFWsp_Cnt_u16         4052           k_AsstFWsp_Cnt_u16         984           k_RestoreThresh_MtrNm_f32         1.79999995           k_AsstFWUprBoundX_HwNm_s4p11[0][0]         4096           12_AsstFWUprBoundX_HwNm_s4p11[0][0]         2048           12_AsstFWUprBoundX_HwNm_s4p11[0][2]         0           12_AsstFWUprBoundX_HwNm_s4p11[0][3]         2048           12_AsstFWUprBoundX_HwNm_s4p11[0][5]         6144           12_AsstFWUprBoundX_HwNm_s4p11[0][6]         8192           12_AsstFWUprBoundX_HwNm_s4p11[0][7]         10240           12_AsstFWUprBoundX_HwNm_s4p11[0][8]         12288           12_AsstFWUprBoundX_HwNm_s4p11[0][9]         14336           12_AsstFWUprBoundX_HwNm_s4p11[0][9]         14336           12_AsstFWUprBoundX_HwNm_s4p11[0][1]         12288           12_AsstFWUprBoundX_HwNm_s4p11[0][1]         12288           12_AsstFWUprBoundX_HwNm_s4p11[0][1]         12288           12_AsstFWUprBoundX_HwNm_s4p11[1][1]	AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32 0.0089999961  Rte_Inst_Ap_AssistFirewall tg_Rte_Inst_Ap_AssistFirewall tk_AsstFWInpLimitBaseAss_MtrNm_f32 1.2999995  k_AsstFWInpLimitHFA_MtrNm_f32 3.2999995  k_AsstFWInpLimitHFA_CDU_t06 4052  k_AsstFWPstep_Cnt_u16 4052  k_AsstFWPstep_Cnt_u16 4096  k_AsstFWD_stop_Cnt_u16 4096  k_AsstFWUprBoundX_HwNm_s4p11[0][0] 4096  12_AsstFWUprBoundX_HwNm_s4p11[0][1] 4096  12_AsstFWUprBoundX_HwNm_s4p11[0][2] 0 4096  12_AsstFWUprBoundX_HwNm_s4p11[0][3] 2048  12_AsstFWUprBoundX_HwNm_s4p11[0][4] 4096  12_AsstFWUprBoundX_HwNm_s4p11[0][5] 6144  12_AsstFWUprBoundX_HwNm_s4p11[0][6] 8192  12_AsstFWUprBoundX_HwNm_s4p11[0][6] 10240  12_AsstFWUprBoundX_HwNm_s4p11[0][8] 12288  12_AsstFWUprBoundX_HwNm_s4p11[0][9] 14336  12_AsstFWUprBoundX_HwNm_s4p11[0][9] 14336  12_AsstFWUprBoundX_HwNm_s4p11[1][0] 16384  12_AsstFWUprBoundX_HwNm_s4p11[1][0] 14336  12_AsstFWUprBoundX_HwNm_s4p11[1][0] 16384  12_AsstFWUpr	AssistFirewall_PNCountStatus_Cnt_M_lgc	0
Rte_Inst_Ap_AssistFirewall         tgt_Rte_Inst_Ap_AssistFirewall           k_AsstFWInpLimitBaseAsst_MtrNm_f32         1.29999995           k_AsstFWInpLimitHs_MtrNm_f32         3.29999995           k_AsstFWNhpLimitHs_Comp_MtrNm_f32         3.29999995           k_AsstFWNstep_Cnt_u16         4052           k_AsstFWPstep_Cnt_u16         984           k_RestoreThresh_MtrNm_f32         1.79999995           2_AsstFWUprBoundX_HwNm_s4p11[0][0]         4096           1_AsstFWUprBoundX_HwNm_s4p11[0][1]         2048           1_2_AsstFWUprBoundX_HwNm_s4p11[0][2]         0           1_2_AsstFWUprBoundX_HwNm_s4p11[0][3]         2048           1_2_AsstFWUprBoundX_HwNm_s4p11[0][4]         4096           1_2_AsstFWUprBoundX_HwNm_s4p11[0][5]         6144           1_2_AsstFWUprBoundX_HwNm_s4p11[0][6]         8192           1_2_AsstFWUprBoundX_HwNm_s4p11[0][7]         10240           1_2_AsstFWUprBoundX_HwNm_s4p11[0][9]         14336           1_2_AsstFWUprBoundX_HwNm_s4p11[0][10]         14336           1_2_AsstFWUprBoundX_HwNm_s4p11[1][1]         12288           1_2_AsstFWUprBoundX_HwNm_s4p11[1][1]         10240           1_2_AsstFWUprBoundX_HwNm_s4p11[1][1]         12288           1_2_AsstFWUprBoundX_HwNm_s4p11[1][1]         12288           1_2_AsstFWUprBoundX_HwNm_s4p11[1][2]	AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
k. AsstFWInpLimitBaseAsst_MtrNm_f32         3           k. AsstFWInpLimitHps.Comp_MtrNm_f32         1.29999995           k. AsstFWInpLimitHpsComp_MtrNm_f32         3.29999995           k. AsstFWPstep_Cnt_u16         4052           k. AsstFWPstep_Cnt_u16         984           k. RestoreThresh_MtrNm_f32         1.79999995           12_AsstFWUprBoundX_HwNm_s4p11[0][0]         -4096           12_AsstFWUprBoundX_HwNm_s4p11[0][1]         -2048           12_AsstFWUprBoundX_HwNm_s4p11[0][2]         0           12_AsstFWUprBoundX_HwNm_s4p11[0][3]         2048           12_AsstFWUprBoundX_HwNm_s4p11[0][4]         4096           12_AsstFWUprBoundX_HwNm_s4p11[0][5]         6144           12_AsstFWUprBoundX_HwNm_s4p11[0][6]         8192           12_AsstFWUprBoundX_HwNm_s4p11[0][7]         10240           12_AsstFWUprBoundX_HwNm_s4p11[0][8]         12288           12_AsstFWUprBoundX_HwNm_s4p11[0][10]         16384           12_AsstFWUprBoundX_HwNm_s4p11[1][0]         -14336           12_AsstFWUprBoundX_HwNm_s4p11[1][0]         -1436           12_AsstFWUprBoundX_HwNm_s4p11[1][0]         -1436           12_AsstFWUprBoundX_HwNm_s4p11[1][0]         -1436           12_AsstFWUprBoundX_HwNm_s4p11[1][0]         -1436           12_AsstFWUprBoundX_HwNm_s4p11[1][3]         -8192 <td>AssistFirewall_UprBoundKSV_M_str.K_Uls_f32</td> <td>0.00899999961</td>	AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00899999961
k_AsstFWInpLimitHFA_MtrNm_f32       1.29999995         k_AsstFWInpLimitHysComp_MtrNm_f32       3.29999995         k_AsstFWPstep_Cnt_u16       4052         k_Restore Thresh_MtrNm_f32       1.79999995         12_AsstFWUprBoundX_HwNm_s4p11[0][0]       4096         12_AsstFWUprBoundX_HwNm_s4p11[0][1]       2048         12_AsstFWUprBoundX_HwNm_s4p11[0][2]       0         12_AsstFWUprBoundX_HwNm_s4p11[0][3]       2048         12_AsstFWUprBoundX_HwNm_s4p11[0][4]       4096         12_AsstFWUprBoundX_HwNm_s4p11[0][5]       6144         12_AsstFWUprBoundX_HwNm_s4p11[0][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[0][7]       10240         12_AsstFWUprBoundX_HwNm_s4p11[0][8]       12288         12_AsstFWUprBoundX_HwNm_s4p11[0][9]       14336         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       16384         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       14336         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       14336         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       14336         12_AsstFWUprBoundX_HwNm_s4p11[1][1]       12288         12_AsstFWUprBoundX_HwNm_s4p11[1][2]       10240         12_AsstFWUprBoundX_HwNm_s4p11[1][3]       8192         12_AsstFWUprBoundX_HwNm_s4p11[1][3]       8192         12_AsstFWUprBoundX_HwNm_s4p11[1][3]	Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitHysComp_MtrNm_f32       3.2999995         k_AsstFWStep_Cnt_u16       4052         k_AsstFWStep_Cnt_u16       984         k_RestoreThresh_MtrNm_f32       1.79999995         12_AsstFWUprBoundX_HwNm_s4p11[0][0]       4096         12_AsstFWUprBoundX_HwNm_s4p11[0][1]       2048         12_AsstFWUprBoundX_HwNm_s4p11[0][2]       0         12_AsstFWUprBoundX_HwNm_s4p11[0][4]       4096         12_AsstFWUprBoundX_HwNm_s4p11[0][5]       6144         12_AsstFWUprBoundX_HwNm_s4p11[0][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[0][7]       10240         12_AsstFWUprBoundX_HwNm_s4p11[0][8]       12288         12_AsstFWUprBoundX_HwNm_s4p11[0][9]       14336         12_AsstFWUprBoundX_HwNm_s4p11[0][10]       16384         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       14336         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       14336         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       12288         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       10240         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       10240         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       10240         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       10240         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       4040         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       4040 <td>k_AsstFWInpLimitBaseAsst_MtrNm_f32</td> <td>3</td>	k_AsstFWInpLimitBaseAsst_MtrNm_f32	3
k_AsstFWNstep_Cnt_u16         4052           k_AsstFWPstep_Cnt_u16         984           k_RestoreThresh_MtrNm_f32         1,79999995           t2_AsstFWUprBoundX_HwNm_s4p11[0][0]         4096           t2_AsstFWUprBoundX_HwNm_s4p11[0][1]         2048           t2_AsstFWUprBoundX_HwNm_s4p11[0][2]         0           t2_AsstFWUprBoundX_HwNm_s4p11[0][4]         4096           t2_AsstFWUprBoundX_HwNm_s4p11[0][5]         6144           t2_AsstFWUprBoundX_HwNm_s4p11[0][6]         8192           t2_AsstFWUprBoundX_HwNm_s4p11[0][7]         10240           t2_AsstFWUprBoundX_HwNm_s4p11[0][8]         12288           t2_AsstFWUprBoundX_HwNm_s4p11[0][9]         14336           t2_AsstFWUprBoundX_HwNm_s4p11[1][0]         16384           t2_AsstFWUprBoundX_HwNm_s4p11[1][0]         12288           t2_AsstFWUprBoundX_HwNm_s4p11[1][0]         12288           t2_AsstFWUprBoundX_HwNm_s4p11[1][0]         12288           t2_AsstFWUprBoundX_HwNm_s4p11[1][0]         12288           t2_AsstFWUprBoundX_HwNm_s4p11[1][0]         16364           t2_AsstFWUprBoundX_HwNm_s4p11[1][0]         6143           t2_AsstFWUprBoundX_HwNm_s4p11[1][0]         6140           t2_AsstFWUprBoundX_HwNm_s4p11[1][0]         6144           t2_AsstFWUprBoundX_HwNm_s4p11[1][0]         6144	k_AsstFWInpLimitHFA_MtrNm_f32	1.29999995
k_AsstFWPstep_Cnt_u16 k_RestoreThresh_MtrNm_f32 1.79999995 12_AsstFWUprBoundX_HwNm_s4p11[0][0] 4.096 12_AsstFWUprBoundX_HwNm_s4p11[0][1] 2.048 12_AsstFWUprBoundX_HwNm_s4p11[0][2] 0 12_AsstFWUprBoundX_HwNm_s4p11[0][3] 2.4sstFWUprBoundX_HwNm_s4p11[0][4] 4.096 12_AsstFWUprBoundX_HwNm_s4p11[0][5] 6144 12_AsstFWUprBoundX_HwNm_s4p11[0][6] 8192 12_AsstFWUprBoundX_HwNm_s4p11[0][7] 10240 12_AsstFWUprBoundX_HwNm_s4p11[0][8] 12_AsstFWUprBoundX_HwNm_s4p11[0][8] 12_AsstFWUprBoundX_HwNm_s4p11[0][9] 12_AsstFWUprBoundX_HwNm_s4p11[0][9] 12_AsstFWUprBoundX_HwNm_s4p11[0][9] 1336 12_AsstFWUprBoundX_HwNm_s4p11[0][1] 16384 12_AsstFWUprBoundX_HwNm_s4p11[1][0] 12_AsstFWUprBoundX_HwNm_s4p11[1][1] 12288 12_AsstFWUprBoundX_HwNm_s4p11[1][1] 12288 12_AsstFWUprBoundX_HwNm_s4p11[1][2] 10240 12_AsstFWUprBoundX_HwNm_s4p11[1][3] 2-AsstFWUprBoundX_HwNm_s4p11[1][3] 2-AsstFWUprBoundX_HwNm_s4p11[1][3] 2-AsstFWUprBoundX_HwNm_s4p11[1][4] 2-AsstFWUprBoundX_HwNm_s4p11[1][5] 4096	k_AsstFWInpLimitHysComp_MtrNm_f32	3.29999995
k_RestoreThresh_MtrNm_f32       1.79999995         t2_AsstFWUprBoundX_HwNm_s4p11[0][0]       -4096         t2_AsstFWUprBoundX_HwNm_s4p11[0][1]       -2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][2]       0         t2_AsstFWUprBoundX_HwNm_s4p11[0][3]       2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][4]       4096         t2_AsstFWUprBoundX_HwNm_s4p11[0][5]       6144         t2_AsstFWUprBoundX_HwNm_s4p11[0][6]       8192         t2_AsstFWUprBoundX_HwNm_s4p11[0][7]       10240         t2_AsstFWUprBoundX_HwNm_s4p11[0][8]       12288         t2_AsstFWUprBoundX_HwNm_s4p11[0][9]       14336         t2_AsstFWUprBoundX_HwNm_s4p11[0][0]       16384         t2_AsstFWUprBoundX_HwNm_s4p11[1][0]       -14336         t2_AsstFWUprBoundX_HwNm_s4p11[1][0]       -12288         t2_AsstFWUprBoundX_HwNm_s4p11[1][1]       -10240         t2_AsstFWUprBoundX_HwNm_s4p11[1][2]       -10240         t2_AsstFWUprBoundX_HwNm_s4p11[1][4]       -8192         t2_AsstFWUprBoundX_HwNm_s4p11[1][4]       -6144         t2_AsstFWUprBoundX_HwNm_s4p11[1][5]       -6144         t2_AsstFWUprBoundX_HwNm_s4p11[1][6]       -6144         t2_AsstFWUprBoundX_HwNm_s4p11[1][6]       -6144	k_AsstFWNstep_Cnt_u16	4052
12_AsstFWUprBoundX_HwNm_s4p11[0][0]       -4096         12_AsstFWUprBoundX_HwNm_s4p11[0][1]       -2048         12_AsstFWUprBoundX_HwNm_s4p11[0][2]       0         12_AsstFWUprBoundX_HwNm_s4p11[0][3]       2048         12_AsstFWUprBoundX_HwNm_s4p11[0][4]       4096         12_AsstFWUprBoundX_HwNm_s4p11[0][5]       6144         12_AsstFWUprBoundX_HwNm_s4p11[0][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[0][7]       10240         12_AsstFWUprBoundX_HwNm_s4p11[0][8]       12288         12_AsstFWUprBoundX_HwNm_s4p11[0][9]       14336         12_AsstFWUprBoundX_HwNm_s4p11[0][0]       16384         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       -14336         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       -14336         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       -12288         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       -12288         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       -12288         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       -8192         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       -6144         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       -6144         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       -6144         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       -6144         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       -6144         12_AsstFWUprBoun	k_AsstFWPstep_Cnt_u16	984
12_AsstFWUprBoundX_HwNm_s4p11[0][1]       -2048         12_AsstFWUprBoundX_HwNm_s4p11[0][2]       0         12_AsstFWUprBoundX_HwNm_s4p11[0][3]       2048         12_AsstFWUprBoundX_HwNm_s4p11[0][4]       4096         12_AsstFWUprBoundX_HwNm_s4p11[0][5]       6144         12_AsstFWUprBoundX_HwNm_s4p11[0][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[0][7]       10240         12_AsstFWUprBoundX_HwNm_s4p11[0][8]       12288         12_AsstFWUprBoundX_HwNm_s4p11[0][9]       14336         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       -14336         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       -14336         12_AsstFWUprBoundX_HwNm_s4p11[1][1]       -12288         12_AsstFWUprBoundX_HwNm_s4p11[1][2]       -10240         12_AsstFWUprBoundX_HwNm_s4p11[1][3]       -8192         12_AsstFWUprBoundX_HwNm_s4p11[1][4]       -6144         12_AsstFWUprBoundX_HwNm_s4p11[1][4]       -6144         12_AsstFWUprBoundX_HwNm_s4p11[1][5]       -6144	k_RestoreThresh_MtrNm_f32	1.79999995
12_AsstFWUprBoundX_HwNm_s4p11[0][2]       0         12_AsstFWUprBoundX_HwNm_s4p11[0][3]       2048         12_AsstFWUprBoundX_HwNm_s4p11[0][4]       4096         12_AsstFWUprBoundX_HwNm_s4p11[0][5]       6144         12_AsstFWUprBoundX_HwNm_s4p11[0][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[0][7]       10240         12_AsstFWUprBoundX_HwNm_s4p11[0][8]       12288         12_AsstFWUprBoundX_HwNm_s4p11[0][9]       14336         12_AsstFWUprBoundX_HwNm_s4p11[0][0]       16384         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       -14336         12_AsstFWUprBoundX_HwNm_s4p11[1][1]       -12288         12_AsstFWUprBoundX_HwNm_s4p11[1][2]       -10240         12_AsstFWUprBoundX_HwNm_s4p11[1][3]       -8192         12_AsstFWUprBoundX_HwNm_s4p11[1][4]       -6144         12_AsstFWUprBoundX_HwNm_s4p11[1][5]       -4096	t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
12_AsstFWUprBoundX_HwNm_s4p11[0][3]       2048         12_AsstFWUprBoundX_HwNm_s4p11[0][4]       4096         12_AsstFWUprBoundX_HwNm_s4p11[0][5]       6144         12_AsstFWUprBoundX_HwNm_s4p11[0][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[0][7]       10240         12_AsstFWUprBoundX_HwNm_s4p11[0][8]       12288         12_AsstFWUprBoundX_HwNm_s4p11[0][9]       14336         12_AsstFWUprBoundX_HwNm_s4p11[0][0]       16384         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       -14336         12_AsstFWUprBoundX_HwNm_s4p11[1][1]       -12288         12_AsstFWUprBoundX_HwNm_s4p11[1][2]       -10240         12_AsstFWUprBoundX_HwNm_s4p11[1][3]       -8192         12_AsstFWUprBoundX_HwNm_s4p11[1][4]       -6144         12_AsstFWUprBoundX_HwNm_s4p11[1][5]       -4096	t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
12_AsstFWUprBoundX_HwNm_s4p11[0][4]       4096         12_AsstFWUprBoundX_HwNm_s4p11[0][5]       6144         12_AsstFWUprBoundX_HwNm_s4p11[0][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[0][7]       10240         12_AsstFWUprBoundX_HwNm_s4p11[0][8]       12288         12_AsstFWUprBoundX_HwNm_s4p11[0][9]       14336         12_AsstFWUprBoundX_HwNm_s4p11[0][0]       16384         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       -14336         12_AsstFWUprBoundX_HwNm_s4p11[1][1]       -12288         12_AsstFWUprBoundX_HwNm_s4p11[1][2]       -10240         12_AsstFWUprBoundX_HwNm_s4p11[1][3]       -8192         12_AsstFWUprBoundX_HwNm_s4p11[1][4]       -6144         12_AsstFWUprBoundX_HwNm_s4p11[1][5]       -4096	t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
12_AsstFWUprBoundX_HwNm_s4p11[0][5]       6144         12_AsstFWUprBoundX_HwNm_s4p11[0][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[0][7]       10240         12_AsstFWUprBoundX_HwNm_s4p11[0][8]       12288         12_AsstFWUprBoundX_HwNm_s4p11[0][9]       14336         12_AsstFWUprBoundX_HwNm_s4p11[0][10]       16384         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       -14336         12_AsstFWUprBoundX_HwNm_s4p11[1][1]       -12288         12_AsstFWUprBoundX_HwNm_s4p11[1][2]       -10240         12_AsstFWUprBoundX_HwNm_s4p11[1][3]       -8192         12_AsstFWUprBoundX_HwNm_s4p11[1][4]       -6144         12_AsstFWUprBoundX_HwNm_s4p11[1][5]       -4096	t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
12_AsstFWUprBoundX_HwNm_s4p11[0][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[0][7]       10240         12_AsstFWUprBoundX_HwNm_s4p11[0][8]       12288         12_AsstFWUprBoundX_HwNm_s4p11[0][9]       14336         12_AsstFWUprBoundX_HwNm_s4p11[0][0]       16384         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       -14336         12_AsstFWUprBoundX_HwNm_s4p11[1][1]       -12288         12_AsstFWUprBoundX_HwNm_s4p11[1][2]       -10240         12_AsstFWUprBoundX_HwNm_s4p11[1][3]       -8192         12_AsstFWUprBoundX_HwNm_s4p11[1][4]       -6144         12_AsstFWUprBoundX_HwNm_s4p11[1][5]       -4096	t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
12_AsstFWUprBoundX_HwNm_s4p11[0][7]       10240         12_AsstFWUprBoundX_HwNm_s4p11[0][8]       12288         12_AsstFWUprBoundX_HwNm_s4p11[0][9]       14336         12_AsstFWUprBoundX_HwNm_s4p11[0][10]       16384         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       -14336         12_AsstFWUprBoundX_HwNm_s4p11[1][1]       -12288         12_AsstFWUprBoundX_HwNm_s4p11[1][2]       -10240         12_AsstFWUprBoundX_HwNm_s4p11[1][3]       -8192         12_AsstFWUprBoundX_HwNm_s4p11[1][4]       -6144         12_AsstFWUprBoundX_HwNm_s4p11[1][5]       -4096	t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
12_AsstFWUprBoundX_HwNm_s4p11[0][8]       12288         12_AsstFWUprBoundX_HwNm_s4p11[0][9]       14336         12_AsstFWUprBoundX_HwNm_s4p11[0][10]       16384         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       -14336         12_AsstFWUprBoundX_HwNm_s4p11[1][1]       -12288         12_AsstFWUprBoundX_HwNm_s4p11[1][2]       -10240         12_AsstFWUprBoundX_HwNm_s4p11[1][3]       -8192         12_AsstFWUprBoundX_HwNm_s4p11[1][4]       -6144         12_AsstFWUprBoundX_HwNm_s4p11[1][5]       -4096	t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
12_AsstFWUprBoundX_HwNm_s4p11[0][9]       14336         12_AsstFWUprBoundX_HwNm_s4p11[0][10]       16384         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       -14336         12_AsstFWUprBoundX_HwNm_s4p11[1][1]       -12288         12_AsstFWUprBoundX_HwNm_s4p11[1][2]       -10240         12_AsstFWUprBoundX_HwNm_s4p11[1][3]       -8192         12_AsstFWUprBoundX_HwNm_s4p11[1][4]       -6144         12_AsstFWUprBoundX_HwNm_s4p11[1][5]       -4096	t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]       16384         t2_AsstFWUprBoundX_HwNm_s4p11[1][0]       -14336         t2_AsstFWUprBoundX_HwNm_s4p11[1][1]       -12288         t2_AsstFWUprBoundX_HwNm_s4p11[1][2]       -10240         t2_AsstFWUprBoundX_HwNm_s4p11[1][3]       -8192         t2_AsstFWUprBoundX_HwNm_s4p11[1][4]       -6144         t2_AsstFWUprBoundX_HwNm_s4p11[1][5]       -4096	t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
12_AsstFWUprBoundX_HwNm_s4p11[1][0]       -14336         12_AsstFWUprBoundX_HwNm_s4p11[1][1]       -12288         12_AsstFWUprBoundX_HwNm_s4p11[1][2]       -10240         12_AsstFWUprBoundX_HwNm_s4p11[1][3]       -8192         12_AsstFWUprBoundX_HwNm_s4p11[1][4]       -6144         12_AsstFWUprBoundX_HwNm_s4p11[1][5]       -4096	t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
12_AsstFWUprBoundX_HwNm_s4p11[1][1]       -12288         12_AsstFWUprBoundX_HwNm_s4p11[1][2]       -10240         12_AsstFWUprBoundX_HwNm_s4p11[1][3]       -8192         12_AsstFWUprBoundX_HwNm_s4p11[1][4]       -6144         12_AsstFWUprBoundX_HwNm_s4p11[1][5]       -4096	t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][2] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[1][3] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[1][4] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[1][5] -4096	t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][3] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[1][4] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[1][5] -4096	t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[1][5] -4096	t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][5] -4096	t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
, , , , , , , , , , , , , , , , , , , ,	t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
t2 AcetEWI IntRoundY Huybin c4p11[1][6] 2049	t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
12_nooii vvopiDouiiun_1iviviii_0+p+1[1][0] -2040	t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
12_AsstFWUprBoundX_HwNm_s4p11[1][7] 0	t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8] 2048	t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
12_AsstFWUprBoundX_HwNm_s4p11[1][9] 4096	t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
12_AsstFWUprBoundX_HwNm_s4p11[1][10] 6144	t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
12_AsstFWUprBoundX_HwNm_s4p11[2][0] -2048	t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048
12_AsstFWUprBoundX_HwNm_s4p11[2][1] 0	t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2] 2048	t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_Asst: WopiBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
12_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
	· ·
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-24576	
t2_Asst WopiBoundY_MtrNm_s4p11[1][1]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-26624	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-24576	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-12288	
:2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-10240	
	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]		
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0	
	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]		
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-28672	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-22528	
	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]		
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240	
	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]		
2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	14336	
- 4		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4] t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	16384 18432	



Name	Input Value		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576		
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672		
:_AsstFWDefltAssistX_HwNm_u8p8[0]	205		
t_AsstFWDefltAssistX_HwNm_u8p8[1]	230		
t_AsstFWDefltAssistX_HwNm_u8p8[2]	256		
t_AsstFWDefltAssistX_HwNm_u8p8[3]	282		
:_AsstFWDefltAssistX_HwNm_u8p8[4]	307		
t_AsstFWDefltAssistX_HwNm_u8p8[5]	333		
t_AsstFWDefltAssistX_HwNm_u8p8[6]	358		
:_AsstFWDefltAssistX_HwNm_u8p8[7]	384		
t_AsstFWDefltAssistX_HwNm_u8p8[8]	410		
t_AsstFWDefltAssistX_HwNm_u8p8[9]	435		
:_AsstFWDefltAssistX_HwNm_u8p8[10]	461		
t_AsstFWDefltAssistX_HwNm_u8p8[11]	486		
t_AsstFWDefltAssistX_HwNm_u8p8[12]	512		
t_AsstFWDefltAssistX_HwNm_u8p8[13]	538		
t_AsstFWDefltAssistX_HwNm_u8p8[14]	563		
t_AsstFWDefltAssistX_HwNm_u8p8[15]	589		
t AsstFWDefltAssistX HwNm u8p8[16]	614		
t AsstFWDefltAssistX HwNm u8p8[17]	640		
t_AsstFWDefltAssistX_HwNm_u8p8[18]	666		
t AsstFWDefltAssistX HwNm u8p8[19]	691		
t_AsstFWDefitAssistY_mwnin_uopo[19]	3482		
t_AsstFWDefitAssistY_MtrNm_s4p11[0]  t_AsstFWDefitAssistY_MtrNm_s4p11[1]	3686		
	3891		
t_AsstFWDefitAssistY_MtrNm_s4p11[2]			
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096		
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4301		
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4506		
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4710		
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4915		
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5120		
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5325		
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5530		
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5734		
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5939		
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6144		
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6349		
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6554		
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6758		
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6963		
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7168		
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7373		
t_AsstFWPstepNstepThresh_Cnt_u16[0]	129		
t_AsstFWPstepNstepThresh_Cnt_u16[1]	235		
t_AsstFWVehSpd_Kph_u9p7[0]	22016		
t_AsstFWVehSpd_Kph_u9p7[1]	22144		
t_AsstFWVehSpd_Kph_u9p7[2]	22272		
t_AsstFWVehSpd_Kph_u9p7[3]	22400		
t_AsstFWVehSpd_Kph_u9p7[4]	22528		
t_AsstFWVehSpd_Kph_u9p7[5]	22656		
t_AsstFWVehSpd_Kph_u9p7[6]	22784		
	22912		
t_AsstFWVehSpd_Kph_u9p7[7]			
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	0		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	80.1999969		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallAct		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmo		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssis	t_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	lt tgt_AssistFirewall_Per1_Defeat_AsstTbl	_Service_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist	_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwI	Nm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisCom	p_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_	Cnt_enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_l		
Name	Actual Value	Expected Value	Resu
		EADCOLCU FAIUC	



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveRawAcc_Cnt_M_u16	235	235 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.60009766	3.60009766 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.46399999	1.46399999 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.33400011	4.33400011 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.9460001	7.9460001 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.60009766	3.60009766 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	<b>~</b>
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	<b>✓</b>

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.099999
Assist irewall_ActiveKSV_M_str.K_UIs_f32	0.090000036
Assisti rewall_ActiveRoV_M_str.N_ois_i32	109
	1
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.079999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.8999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0700000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0099999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
:_AsstFWInpLimitBaseAsst_MtrNm_f32	4
:_AsstFWInpLimitHFA_MtrNm_f32	2.5
:_AsstFWInpLimitHysComp_MtrNm_f32	3.78999996
x_AsstFWNstep_Cnt_u16	3928
z_AsstFWPstep_Cnt_u16	1107
_RestoreThresh_MtrNm_f32	1.8999998
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
2 AsstFWUprBoundX HwNm s4p11[0][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-8192
2_AsstFWUprBoundX_HWNm_s4p11[1][2] 2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-6144
z_AsstFWUprBoundX_HwNm_s4p11[1][3] 2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][0] 2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0 2048



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-16384
	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288
t2 AsstFWUprBoundY MtrNm s4p11[5][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
TEL 1000 TOPIDOUNG I _WILLIAM _ 54P I I[I][4]	0.02



t2_AsstFWUprBoundY_MtrNm_s4p11[7][5] t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	
	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	230
t_AsstFWDefltAssistX_HwNm_u8p8[1]	256
t_AsstFWDefltAssistX_HwNm_u8p8[2]	282
t_AsstFWDefltAssistX_HwNm_u8p8[3]	307
t_AsstFWDefltAssistX_HwNm_u8p8[4]	333
t_AsstFWDefltAssistX_HwNm_u8p8[5]	358
t_AsstFWDefltAssistX_HwNm_u8p8[6]	384
t_AsstFWDefltAssistX_HwNm_u8p8[7]	410
t_AsstFWDefltAssistX_HwNm_u8p8[8]	435
t_AsstFWDefltAssistX_HwNm_u8p8[9]	461 486
t_AsstFWDefltAssistX_HwNm_u8p8[10]	512
t_AsstFWDefltAssistX_HwNm_u8p8[11]	538
t_AsstFWDefltAssistX_HwNm_u8p8[12]	
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	563 589
t_AsstFWDefitAssistX_HwNm_u8p8[14]  t_AsstFWDefitAssistX_HwNm_u8p8[15]	614
t_AsstFWDefitAssistX_HwNm_u8p8[16]	640
t_AsstFWDefitAssistX_mwnm_uopo[16] t_AsstFWDefitAssistX_HwNm_u8p8[17]	666
t_AsstFWDefitAssistX_HwNm_u8p8[18]	691
t_AsstFWDefitAssistX_HwNm_u8p8[19]	717
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7578
t_AsstFWPstepNstepThresh_Cnt_u16[0]	130
t_AsstFWPstepNstepThresh_Cnt_u16[1]	239
t_AsstFWVehSpd_Kph_u9p7[0]	24960
t_AsstFWVehSpd_Kph_u9p7[1]	25088
t_AsstFWVehSpd_Kph_u9p7[2]	25216
t_AsstFWVehSpd_Kph_u9p7[3]	25344
t_AsstFWVehSpd_Kph_u9p7[4]	25472
t_AsstFWVehSpd_Kph_u9p7[5]	25600
t_AsstFWVehSpd_Kph_u9p7[6]	25728
t_AsstFWVehSpd_Kph_u9p7[7]	25856
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.5
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	9
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90.0100021
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	
	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	A A A SECTION OF THE
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
• • • • • • • • • • • • • • • • • • • •	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.82099986	2.8210001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	239	239 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.70019531	3.70019531 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.63199997	2.63199997 ± 4.88E-04	<b>~</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.2329998	5.2329998 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.11900008	1.11899996 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.70019531	3.70019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T ·				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.10 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3
AssistFirewall ActiveKSV M str.K Uls f32	0.0099999978
AssistFirewall_ActiveRawAcc_Cnt_M_u16	112
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall CombAsstSV MtrNm M f32	-1.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00899999961
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.1000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.0080000038
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00200000009
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.0999999
k AsstFWInpLimitHFA MtrNm f32	2.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	4.28000021
k_AsstFWNstep_Cnt_u16	3804
k_AsstFWPstep_Cnt_u16	1230
k RestoreThresh MtrNm f32	2
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2 AsstFWUprBoundX HwNm s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2 AsstFWUprBoundX HwNm s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-18432
	1 10 102



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240
	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-12288
	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	4096
12_AsstFWUprBoundX_HwNm_s4p11[4][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	2048



	• 1	
Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-20480	
	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]		
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480	
	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]		
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096	
	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240	
	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]		
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192	
t2_AsstrWUprBoundY_MtrNm_s4p11[7][0]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	256
t_AsstFWDefltAssistX_HwNm_u8p8[1]	282
t_AsstFWDefltAssistX_HwNm_u8p8[2]	307
t_AsstFWDefltAssistX_HwNm_u8p8[3]	333
t_AsstFWDefltAssistX_HwNm_u8p8[4]	358
t_AsstFWDefltAssistX_HwNm_u8p8[5]	384 410
t_AsstFWDefitAssistX_HwNm_u8p8[6] t_AsstFWDefitAssistX_HwNm_u8p8[7]	435
t_AsstFWDefitAssistX_HwNm_u8p8[8]	461
t_AsstFWDefitAssistX_HwNm_u8p8[9]	486
t_AsstFWDefitAssistX_HwNm_u8p8[10]	512
t AsstFWDefltAssistX HwNm u8p8[11]	538
t_AsstFWDefltAssistX_HwNm_u8p8[12]	563
t_AsstFWDefltAssistX_HwNm_u8p8[13]	589
t_AsstFWDefltAssistX_HwNm_u8p8[14]	614
t_AsstFWDefltAssistX_HwNm_u8p8[15]	640
t_AsstFWDefltAssistX_HwNm_u8p8[16]	666
t_AsstFWDefltAssistX_HwNm_u8p8[17]	691
t_AsstFWDefltAssistX_HwNm_u8p8[18]	717
t_AsstFWDefltAssistX_HwNm_u8p8[19]	742
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7168 7373
t_AsstFWDefltAssistY_MtrNm_s4p11[17] t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7578
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	7782
t_AsstFWPstepNstepThresh_Cnt_u16[0]	131
t_AsstFWPstepNstepThresh_Cnt_u16[1]	243
t_AsstFWVehSpd_Kph_u9p7[0]	27904
t_AsstFWVehSpd_Kph_u9p7[1]	28032
t_AsstFWVehSpd_Kph_u9p7[2]	28160
t_AsstFWVehSpd_Kph_u9p7[3]	28288
t_AsstFWVehSpd_Kph_u9p7[4]	28416
t_AsstFWVehSpd_Kph_u9p7[5]	28544
t_AsstFWVehSpd_Kph_u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7]	28800
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.5
gt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	10.1999998
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tot Die land An AngletEnguell A. 1981 II B. 4.11 E	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.97000003	2.97000003 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	243	243 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.89990234	1.89990234 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.97660005	1.97660005 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0079999	5.0079999 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	0.987999976	0.987999976 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	1.89990234	1.89990234 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T ·				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.11 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	5.0999999
AssistFirewall ActiveKSV M str.K Uls f32	0.0060000005
AssistFirewall_ActiveRawAcc_Cnt_M_u16	115
AssistFirewall AsstReducedPerfSV Cnt M Iqc	1
AssistFirewall CombAsstSV MtrNm M f32	-1.29999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0599999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.090000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.099999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.029999993
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.4000001
k_AsstFWInpLimitHFA_MtrNm_f32	2.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	4.76999998
k_AsstFWNstep_Cnt_u16	3680
k_AsstFWPstep_Cnt_u16	1353
k_RestoreThresh_MtrNm_f32	2.0999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384



	( =# := 10=10
Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
, , , , , , , , , , , , , , , , , , , ,	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2 AsstFWUprBoundX HwNm s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_Asst WopiBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_Asst WopiBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
:z_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144
12_1 10011 11 Opt 20011010 1p 1 1[0][2]	
	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336	
	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-8192	
	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]		
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240	
	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	282
t_AsstFWDefltAssistX_HwNm_u8p8[1]	307
t_AsstFWDefltAssistX_HwNm_u8p8[2]	333
t_AsstFWDefltAssistX_HwNm_u8p8[3]	358
t_AsstFWDefltAssistX_HwNm_u8p8[4]	384
t_AsstFWDefltAssistX_HwNm_u8p8[5]	410
t_AsstFWDefltAssistX_HwNm_u8p8[6]	435
t_AsstFWDefltAssistX_HwNm_u8p8[7]	461
t_AsstFWDefltAssistX_HwNm_u8p8[8]	486
t_AsstFWDefltAssistX_HwNm_u8p8[9]	512
t_AsstFWDefltAssistX_HwNm_u8p8[10]	538
t_AsstFWDefltAssistX_HwNm_u8p8[11]	563
t_AsstFWDefltAssistX_HwNm_u8p8[12]	589
t_AsstFWDefltAssistX_HwNm_u8p8[13]	614
t_AsstFWDefltAssistX_HwNm_u8p8[14]	640
t_AsstFWDefltAssistX_HwNm_u8p8[15]	666
t_AsstFWDefltAssistX_HwNm_u8p8[16]	691
t_AsstFWDefltAssistX_HwNm_u8p8[17]	717
t_AsstFWDefltAssistX_HwNm_u8p8[18]	742
t_AsstFWDefltAssistX_HwNm_u8p8[19]	768
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7782
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	7987
t_AsstFWPstepNstepThresh_Cnt_u16[0]	132
t_AsstFWPstepNstepThresh_Cnt_u16[1]	247
t_AsstFWVehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1]	30976 31104
t_AsstFWVehSpd_Kph_u9p7[2] t_AsstFWVehSpd_Kph_u9p7[3]	31104 31232
t_AsstFWVenSpd_kpn_usp7[3] t_AsstFWVehSpd_kph_usp7[4]	31360
t_AsstFWVehSpd_Kph_u9p7[5]	31488
t_AsstFWVehSpd_Kph_u9p7[6]	31616
t_AsstFWVehSpd_Kph_u9p7[7]	31744
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_BaseAssistCmd_mtmm_r32.value  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-10
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	22.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_li	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32
-3	-0-7



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.06939983	5.06939983 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	247	247 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.89990234	-3.89990234 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.25	4.25 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.459999979	0.460000008 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.85699987	2.85700011 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-3.89990234	-3.89990234 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.12 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	6.0999999
AssistFirewall ActiveKSV M str.K Uls f32	0.00700000022
AssistFirewall_ActiveRawAcc_Cnt_M_u16	118
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall CombAsstSV MtrNm M f32	-1.3999998
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00800000038
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.02999997
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2
AssistFirewall LwrBoundKSV M str.K Uls f32	0.0049999989
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.099999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.039999991
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.70000005
k_AsstFWInpLimitHFA_MtrNm_f32	2.5
k_AsstFWInpLimitHysComp_MtrNm_f32	5.26000023
k_AsstFWNstep_Cnt_u16	3556
k_AsstFWPstep_Cnt_u16	1476
k RestoreThresh MtrNm f32	2.2000005
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	4096
ı∠_ASSLEVVUPI BOUNU T_IVILININ_S4PTT[U][b]	4090



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240	
	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]		
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-10240	
2 AsstFWUprBoundY MtrNm s4p11[2][5]	-8192	
:2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-6144	
	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]		
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-20480	
	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]		
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-4096	
t2 AsstFWUprBoundY MtrNm s4p11[4][9]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096	
	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]		
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240	
	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240	
2 AcctEM/IntPoundV MtrNm c4p11[7][1]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-6144	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096
	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefltAssistX_HwNm_u8p8[0]	307
t_AsstFWDefltAssistX_HwNm_u8p8[1]	333
t_AsstFWDefltAssistX_HwNm_u8p8[2]	358
t_AsstFWDefltAssistX_HwNm_u8p8[3]	384
t_AsstFWDefltAssistX_HwNm_u8p8[4]	410
t AsstFWDefltAssistX HwNm u8p8[5]	435
t_AsstFWDefltAssistX_HwNm_u8p8[6]	461
t_AsstFWDefltAssistX_HwNm_u8p8[7]	486
t_AsstFWDefitAssistX_HwNm_u8p8[8]	512
	538
t_AsstFWDefltAssistX_HwNm_u8p8[9]	
t_AsstFWDefltAssistX_HwNm_u8p8[10]	563
t_AsstFWDefltAssistX_HwNm_u8p8[11]	589
t_AsstFWDefltAssistX_HwNm_u8p8[12]	614
t_AsstFWDefltAssistX_HwNm_u8p8[13]	640
t_AsstFWDefltAssistX_HwNm_u8p8[14]	666
t_AsstFWDefltAssistX_HwNm_u8p8[15]	691
t_AsstFWDefltAssistX_HwNm_u8p8[16]	717
t AsstFWDefltAssistX HwNm u8p8[17]	742
t_AsstFWDefitAssistX_HwNm_u8p8[18]	768
	794
t_AsstFWDefltAssistX_HwNm_u8p8[19]	
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	6144
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	6349
t_AsstFWDefitAssistY_MtrNm_s4p11[11]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	8192
t_AsstFWPstepNstepThresh_Cnt_u16[0]	133
t AsstFWPstepNstepThresh Cnt u16[1]	251
t_AsstFWVehSpd_Kph_u9p7[0]	33792
t_AsstFWVehSpd_Kph_u9p7[1]	33920
t_AsstFWVehSpd_Kph_u9p7[2]	34048
t_AsstFWVehSpd_Kph_u9p7[3]	34176
t_AsstFWVehSpd_Kph_u9p7[4]	34304
t_AsstFWVehSpd_Kph_u9p7[5]	34432
t_AsstFWVehSpd_Kph_u9p7[6]	34560
t_AsstFWVehSpd_Kph_u9p7[7]	34688
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2.20000005
·	10
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	33.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.05730009	6.05730009 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	251	251 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	4	4 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.13119984	5.13119984 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.00999999	2.00999999 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.17600012	4.17600012 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4	4 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>~</b>

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.13 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	1
AssistFirewall ActiveKSV M str.K Uls f32	0.00800000038
AssistFirewall_ActiveRawAcc_Cnt_M_u16	121
AssistFirewall AsstReducedPerfSV Cnt M Iqc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00899999961
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.03999996
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00600000005
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0500000007
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3
k_AsstFWInpLimitHFA_MtrNm_f32	4.5
k_AsstFWInpLimitHysComp_MtrNm_f32	5.75
k_AsstFWNstep_Cnt_u16	3432
k_AsstFWPstep_Cnt_u16	1599
k_RestoreThresh_MtrNm_f32	2.2999995
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288



	(
Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_Asst WopiBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_Asst WopiBoundX_HwNm_s4p11[5][0]	-8192
t2_Asst WopiBoundX_HwNm_s4p11[5][1]	-6144
	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2 AsstFWUprBoundX HwNm s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4] t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2040 0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4] t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	4096 6144



Name	Input Value	
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t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144	
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t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048	
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t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240	
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t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432	
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2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048	
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2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048	
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2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144	
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t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048	
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2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288	
	14336	
2 AcctEM/IntRoundV Mirkim canadicitadi	14550	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0] 2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192 -6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192	



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2. Jean Phylipson Chem. ps. 1179   944   2. Jean Phylipson Chem. ps. 1179   944   2. Jean Phylipson Chem. ps. 1179   944   2. Jean Phylipson Chem. ps. 1179   942   2. Jean Phylipson Chem. ps. 1179   942   2. Jean Phylipson Chem. ps. 1179   942   2. Jean Phylipson Chem. ps. 1179   943   2. Jean Phylipson Chem. ps. 1179   943   3. Jean Phylipson Chem. ps. 1179   943   3. Jean Phylipson Chem. ps. 1179   943   3. Jean Phylipson Chem. ps. 1179   944   3. Jean Phylipson Chem. ps. 1179   945   3. Jean Phylipson Chem. ps. 1179	t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	
PLANSPLY  Flat SAMP   JAMPS   1541   T   1541   T   1544   T   1	t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
2. Aces*Ps/Upfordown/ Jubbes sets/1919  1920   2. Aces*Ps/Upfordown/ Jubbes sets/1919  1920   3. Aces*Ps/Upfordown/ Jubbes sets/1919  1930   3. Aces*Ps/Upfordown/ Jubbes sets/1919  1932   3. Aces*Ps/Upfordown/ Jubbes sets/1919  1932   3. Aces*Ps/Upfordown/ Jubbes sets/1919  1932   3. Aces*Ps/Upfordown/ Jubbes sets/1919  1930   3. Aces*Ps/Upfordown/ J	t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
2 Acces*Victoritacions**, Numbrus.sps*117(19)   10280   1028	t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
2 AGENT/VORTHOGENERAL   Nathron   Ling   1979   338	t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
Death Victor March Service   The Name	t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
LaserWorkindessitk Hebrin upplied   410   420	t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
Least Worldwaser, Hawlen, Lapid    410    - Least Worldwaser, Hawlen, Lapid    512    - Least Worldwaser, Hawlen, Lapid    513    - Least Worldwaser, Hawlen, Lapid    513    - Least Worldwaser, Hawlen, Lapid    513    - Least Worldwaser, Hawlen, Lapid    614    - Least Worldwaser, Hawlen, Lapid    614    - Least Worldwaser, Hawlen, Lapid    616    - Least Worldwaser, Hawlen, Lapid    616    - Least Worldwaser, Hawlen, Lapid    616    - Least Worldwaser, Hawlen, Lapid    617    - Least Worldwaser, Marken, Lapid    617    - Least Worldwaser, Ma	t_AsstFWDefltAssistX_HwNm_u8p8[0]	333
Laser Worldwaser, Namou, app85   455	t_AsstFWDefltAssistX_HwNm_u8p8[1]	358
1 AcesTV-PolithAssist, Harbys (1998)	t_AsstFWDefltAssistX_HwNm_u8p8[2]	384
Acest World Assert   Henhru upplig    466		
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Laser North Assett A Profit m. 1988   14   881     Laser North Assett A Profit m. 1988   15   777     Laser North Assett A Profit m. 1988   15   777     Laser North Assett A Profit m. 1988   178   788     Laser North Assett A Profit m. 1988   179   788     Laser North Assett A Profit m. 1988   179   788     Laser North Assett A Profit m. 1988   179   788     Laser North Assett A Profit m. 1988   179   789   7		
LastPVDHTAsistX, HeNn, usp8[14]   991		
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LASSE/Wichfacksik/ Minkin_s4p110		
LassFWDeltAssietX, Hwhm. s4p110	· · ·	
LassFWDeltAssir/ Minkm.sqn110		
LassFWDefihassixY_Mrkm_s4p11[2]		
LassIPWDelflassistY_Mrkm_s4p11[3] 512  LAssIPWDelflassistY_Mrkm_s4p11[6] 5325  LAssIPWDelflassistY_Mrkm_s4p11[6] 5336  LassIPWDelflassistY_Mrkm_s4p11[6] 5344  LassIPWDelflassistY_Mrkm_s4p11[7] 5939  LassIPWDelflassistY_Mrkm_s4p11[7] 6444  LassIPWDelflassistY_Mrkm_s4p11[8] 644  LassIPWDelflassistY_Mrkm_s4p11[8] 6554  LassIPWDelflassistY_Mrkm_s4p11[8] 6554  LassIPWDelflassistY_Mrkm_s4p11[8] 6554  LassIPWDelflassistY_Mrkm_s4p11[8] 758  LassIPWDelflassistY_Mrkm_s4p1[8] 758  LassIPWDelflassistY_Mrkm_s4p1[8] 758  LassIPWDelfl		
LassFWDethAssiaY Minkm_stp11[3]   5520   5530   5		4915
LASSIFWDeftNassistY_MtrNm_s4p11[9]   5530   5734		5120
CASSIFWDeftNasistY_Mirkm_s4p11[6]   5724	t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5325
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L AssFWDelftAssistY_MtrNm_s4p11[10]	t_AsstFWDefltAssistY_MtrNm_s4p11[8]	6144
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L AssiFWDelflAssistY_MtrNm_s4p11[12]	t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6554
L AssiFWDelftAssistY MtrNm_s4p11[13] 7737 L AssiFWDelftAssistY MtrNm_s4p11[16] 7788 L AssiFWDelftAssistY MtrNm_s4p11[17] 7782 L AssiFWDelftAssistY MtrNm_s4p11[17] 7987 L AssiFWDelftAssistY MtrNm_s4p11[17] 7987 L AssiFWDelftAssistY MtrNm_s4p11[18] 8192 L AssiFWDelftAssistY MtrNm_s4p11[19] 8397 L AssiFWDelftAssistY MtrNm_s4p11[19] 255 L AssiFWDelftAssistY MtrNm_s4p11[19] 255 L AssiFWDelftAssistY MtrNm_s4p11[19] 255 L AssiFWDelftAssistY MtrNm_s4p11[19] 36864 L AssiFWDelftAssistY MtrNm_s4p11[19] 36864 L AssiFWDelftAssistY MtrNm_s4p11[19] 36864 L AssiFWDelftAssistY MtrNm_s4p11[19] 36864 L AssiFWDelftAssistY MtrNm_s4p1[1] 36864 L AssiFWDelftAssistY MtrNm_s4p1[1] 36864 L AssiFWDelftAssistY MtrNm_s4p1[1] 37120 L AssiFWDelftAssistY MtrNm_s4p1[1] 37120 L AssiFWDelftAssistY MtrNm_s4p1[1] 37120 L AssiFWDelftAssistY MtrNm_s4p1[1] 37364 L AssiFWDelftAssitY MtrNm_s4p1[1] 37364 L AssifYDelftAssitY MtrNm_s4p1[1] 37364 L AssifYDelftAssitY MtrNm_s4p1[1] 37364 L AssifYDelftAssitY MtrNm_s4p1[1] 37364 L AssifYDelftAssitYDelftAss	t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6758
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tgt_Rte_Inst_Ap_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_let_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum		0
tgt_Rte_Inst_Ap_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgt tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	44.2000008
tgt_Rte_Inst_Ap_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgt tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MSC_Counter_Cnt_enum	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgt tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgt tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum	$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_leadstarted and the state of $	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
	, , , , , , , , , , , , , , , , , , , ,	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_VehicleSpeed_Kph_f32 tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32	-	1
	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32





Name	Input Value	
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048	
	0	
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]		
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336	
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288	
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096	
t2 AsstFWUprBoundX HwNm s4p11[4][2]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048	
	0	
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]		
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	12288	
	12200	



	(
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-12288
	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	0
t2 AsstFWUprBoundY MtrNm s4p11[4][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288
:2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336
, , , , , , , , , , , , , , , , , , , ,	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
	16384
	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144



	, , , , , , , , , , , , , , , , , , , ,
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	358
t_AsstFWDefltAssistX_HwNm_u8p8[1]	384
t_AsstFWDefltAssistX_HwNm_u8p8[2]	410
t_AsstFWDefltAssistX_HwNm_u8p8[3]	435
t_AsstFWDefltAssistX_HwNm_u8p8[4]	461
t_AsstFWDefltAssistX_HwNm_u8p8[5]	486
t_AsstFWDefltAssistX_HwNm_u8p8[6]	512
t_AsstFWDefltAssistX_HwNm_u8p8[7]	538
t_AsstFWDefltAssistX_HwNm_u8p8[8]	563
t_AsstFWDefltAssistX_HwNm_u8p8[9]	589
t_AsstFWDefltAssistX_HwNm_u8p8[10]	614
t_AsstFWDefltAssistX_HwNm_u8p8[11]	640
t_AsstFWDefltAssistX_HwNm_u8p8[12]	666
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	691 717
t_AsstFWDefitAssistX_HwNm_u8p8[14] t_AsstFWDefitAssistX_HwNm_u8p8[15]	742
t AsstFWDefitAssistX HwNm u8p8[16]	768
t_AsstFWDefitAssistX_HwNm_u8p8[17]	794
t_AsstFWDefltAssistX_HwNm_u8p8[18]	819
t_AsstFWDefltAssistX_HwNm_u8p8[19]	845
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	8602
t_AsstFWPstepNstepThresh_Cnt_u16[0]	135
t_AsstFWPstepNstepThresh_Cnt_u16[1]	259
t_AsstFWVehSpd_Kph_u9p7[0]	39680
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	39808 39936
t_AsstFWVehSpd_Kph_u9p7[3]	40064
t AsstFWVehSpd Kph u9p7[4]	40192
t_AsstFWVehSpd_Kph_u9p7[5]	40320
t_AsstFWVehSpd_Kph_u9p7[6]	40448
t_AsstFWVehSpd_Kph_u9p7[7]	40576
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5.5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	55.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.98199999	1.98199999 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	259	259 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.20019531	4.20019531 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.07500005	1.07500005 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.97550011	3.97550011 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.27399969	6.27400017 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4.20019531	4.20019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.15 (Repeat Count = 1)	· ·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3
AssistFirewall ActiveKSV M str.K Uls f32	0.0099999978
AssistFirewall_ActiveRawAcc_Cnt_M_u16	127
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.70000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.019999996
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.05999994
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00800000038
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.070000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.5999999
k_AsstFWInpLimitHFA_MtrNm_f32	1.60000002
k_AsstFWInpLimitHysComp_MtrNm_f32	6.73000002
k_AsstFWNstep_Cnt_u16	3184
k_AsstFWPstep_Cnt_u16	1845
k_RestoreThresh_MtrNm_f32	2.5
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_Asst WorlboundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048
	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][3] t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_Asst WopiboundX_1WNIII_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	
	8192



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-10240
:2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-8192
	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	6144
	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
, , , , , , , , , , , , , , , , , , , ,	18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
, 11 Obi poduja i _iviti i i i i	
2 AcetEM/I IntRoundV MtrNm 04p44177141	10
	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	0 2048 4096



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	384
t_AsstFWDefltAssistX_HwNm_u8p8[1]	410
t_AsstFWDefltAssistX_HwNm_u8p8[2]	435
t_AsstFWDefltAssistX_HwNm_u8p8[3]	461
t_AsstFWDefltAssistX_HwNm_u8p8[4]	486
t_AsstFWDefltAssistX_HwNm_u8p8[5]	512
t_AsstFWDefltAssistX_HwNm_u8p8[6] t_AsstFWDefltAssistX_HwNm_u8p8[7]	538 563
t_AsstFWDefitAssistX_HwNm_u8p8[8]	589
t_AsstFWDefltAssistX_HwNm_u8p8[9]	614
t_AsstFWDefltAssistX_HwNm_u8p8[10]	640
t_AsstFWDefltAssistX_HwNm_u8p8[11]	666
t AsstFWDefltAssistX HwNm u8p8[12]	691
t_AsstFWDefltAssistX_HwNm_u8p8[13]	717
t_AsstFWDefltAssistX_HwNm_u8p8[14]	742
t_AsstFWDefltAssistX_HwNm_u8p8[15]	768
t_AsstFWDefltAssistX_HwNm_u8p8[16]	794
t_AsstFWDefltAssistX_HwNm_u8p8[17]	819
t_AsstFWDefltAssistX_HwNm_u8p8[18]	845
t_AsstFWDefltAssistX_HwNm_u8p8[19]	870
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	6349 6554
t_AsstFWDefltAssistY_MtrNm_s4p11[8] t_AsstFWDefltAssistY_MtrNm_s4p11[9]	6758
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	6963
t_AsstFWDefitAssistY_MtrNm_s4p11[11]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	8806
t_AsstFWPstepNstepThresh_Cnt_u16[0]	136
t_AsstFWPstepNstepThresh_Cnt_u16[1]	263
t_AsstFWVehSpd_Kph_u9p7[0]	42624
t_AsstFWVehSpd_Kph_u9p7[1]	42752
t_AsstFWVehSpd_Kph_u9p7[2]	42880
t_AsstFWVehSpd_Kph_u9p7[3]	43008
t_AsstFWVehSpd_Kph_u9p7[4]	43136
t_AsstFWVehSpd_Kph_u9p7[5]	43264
t_AsstFWVehSpd_Kph_u9p7[6]	43392
t_AsstFWVehSpd_Kph_u9p7[7] tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	43520 2.20000005
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.6999981
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	66.4000015
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_le	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_Hw1orque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstrWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
t2 AsstFWUprBoundX HwNm s4p11[5][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
tz_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	8192
	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	16384



	· ·	
Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192	
	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]		
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-28672	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-26624	
	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]		
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144	
	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-8192	
	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]		
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336	
12_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144	



	( 10.70
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	410
t_AsstFWDefltAssistX_HwNm_u8p8[1]	435
t_AsstFWDefltAssistX_HwNm_u8p8[2]	461
t_AsstFWDefltAssistX_HwNm_u8p8[3]	486
t_AsstFWDefltAssistX_HwNm_u8p8[4]	512
t_AsstFWDefltAssistX_HwNm_u8p8[5]	538
t_AsstFWDefltAssistX_HwNm_u8p8[6]	563
t_AsstFWDefltAssistX_HwNm_u8p8[7]	589
t_AsstFWDefltAssistX_HwNm_u8p8[8]	614
	640
t_AsstFWDefltAssistX_HwNm_u8p8[9]	
t_AsstFWDefltAssistX_HwNm_u8p8[10]	666
t_AsstFWDefltAssistX_HwNm_u8p8[11]	691
t_AsstFWDefltAssistX_HwNm_u8p8[12]	717
t_AsstFWDefltAssistX_HwNm_u8p8[13]	742
t_AsstFWDefltAssistX_HwNm_u8p8[14]	768
t_AsstFWDefltAssistX_HwNm_u8p8[15]	794
t_AsstFWDefltAssistX_HwNm_u8p8[16]	819
t AsstFWDefltAssistX HwNm u8p8[17]	845
t_AsstFWDefitAssistX_HwNm_u8p8[18]	870
	896
t_AsstFWDefltAssistX_HwNm_u8p8[19]	
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	9011
t_AsstFWPstepNstepThresh_Cnt_u16[0]	137
t AsstFWPstepNstepThresh Cnt u16[1]	267
_ , , ;	
t_AsstFWVehSpd_Kph_u9p7[0]	45568
t_AsstFWVehSpd_Kph_u9p7[1]	45696
t_AsstFWVehSpd_Kph_u9p7[2]	45824
t_AsstFWVehSpd_Kph_u9p7[3]	45952
t_AsstFWVehSpd_Kph_u9p7[4]	46080
t_AsstFWVehSpd_Kph_u9p7[5]	46208
t_AsstFWVehSpd_Kph_u9p7[6]	46336
t_AsstFWVehSpd_Kph_u9p7[7]	46464
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3.099999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.099999
· .	
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-8.80000019
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	77.1999969
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNr	m_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNi	· ·
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrN	m_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_en tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f3:	



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.92000008	3.92000008 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	267	267 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-2.89990234	-2.89990234 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.01799989	3.01799989 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.8829999	5.8829999 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.07999992	2.07999992 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-2.89990234	-2.89990234 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5
AssistFirewall_ActiveKSV_M_str.K_UIs_f32	0.029999993
AssistFirewall_ActiveRawAcc_Cnt_M_u16	133
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.89999998
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.039999991
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.08000004
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0099999978
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.090000036
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
<_AsstFWInpLimitBaseAsst_MtrNm_f32	4.19999981
c_AsstFWInpLimitHFA_MtrNm_f32	2
C_AsstFWInpLimitHysComp_MtrNm_f32	1.70000005
c_AsstFWNstep_Cnt_u16	2936
C_AsstFWPstep_Cnt_u16	2091
c_RestoreThresh_MtrNm_f32	2.70000005
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
12_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
2 AsstFWUprBoundX HwNm s4p11[6][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	4096
:2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	8192
:2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	10240
:2_AsstFWUprBoundY_MtrNm_s4p11[0][3] :2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	12288
	14336
2 AcctEM/IntRoundV M+rNm c4c44[0][5]	14550
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	16384





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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	22528
t_AsstFWDefltAssistX_HwNm_u8p8[0]	435
t_AsstFWDefltAssistX_HwNm_u8p8[1]	461
t_AsstFWDefltAssistX_HwNm_u8p8[2]	486
t_AsstFWDefltAssistX_HwNm_u8p8[3]	512
t_AsstFWDefltAssistX_HwNm_u8p8[4]	538
t_AsstFWDefltAssistX_HwNm_u8p8[5]	563
t_AsstFWDefltAssistX_HwNm_u8p8[6]	589
t_AsstFWDefltAssistX_HwNm_u8p8[7]	614
t_AsstFWDefltAssistX_HwNm_u8p8[8]	640
t_AsstFWDefltAssistX_HwNm_u8p8[9]	666
t_AsstFWDefltAssistX_HwNm_u8p8[10]	691
t_AsstFWDefltAssistX_HwNm_u8p8[11]	717 742
t_AsstFWDefltAssistX_HwNm_u8p8[12]	
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	768 794
t_AsstFWDefitAssistX_HwNm_u8p8[14] t_AsstFWDefitAssistX_HwNm_u8p8[15]	819
t AsstFWDefitAssistX HwNm u8p8[16]	845
t_AsstFWDefitAssistX_HwNm_u8p8[17]	870
t_AsstFWDefltAssistX_HwNm_u8p8[18]	896
t_AsstFWDefltAssistX_HwNm_u8p8[19]	922
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	9216
t_AsstFWPstepNstepThresh_Cnt_u16[0]	138
t_AsstFWPstepNstepThresh_Cnt_u16[1]	271
t_AsstFWVehSpd_Kph_u9p7[0]	27904
t_AsstFWVehSpd_Kph_u9p7[1]	28032 28160
t_AsstFWVehSpd_Kph_u9p7[2] t_AsstFWVehSpd_Kph_u9p7[3]	28288
t AsstFWVehSpd Kph u9p7[4]	28416
t_AsstFWVehSpd_Kph_u9p7[5]	28544
t_AsstFWVehSpd_Kph_u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7]	28800
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.80000019
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	88.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4.8499999	4.8499999 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	271	271 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.89990234	-3.89990234 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.11199999	4.11199999 ± 4.88E-04	<b>~</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.8499999	6.8499999 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.91000009	2.91000009 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-3.89990234	-3.89990234 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.18 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6
AssistFirewall ActiveKSV M str.K Uls f32	0.039999991
AssistFirewall_ActiveRawAcc_Cnt_M_u16	136
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.09000003
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0199999996
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.100000001
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.5
k_AsstFWInpLimitHFA_MtrNm_f32	2.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	2.0999999
k_AsstFWNstep_Cnt_u16	2812
k_AsstFWPstep_Cnt_u16	2214
k RestoreThresh MtrNm f32	2.79999995
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	20480



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	26624
	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-22528
, , , , , , , , , , , , , , , , , , , ,	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	12288
	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	18432
, , , , , , , , , , , , , , , , , , , ,	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	10240



	(
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576
t_AsstFWDefltAssistX_HwNm_u8p8[0]	461
t_AsstFWDefltAssistX_HwNm_u8p8[1]	486
t_AsstFWDefltAssistX_HwNm_u8p8[2]	512
t_AsstFWDefltAssistX_HwNm_u8p8[3]	538
t_AsstFWDefltAssistX_HwNm_u8p8[4]	563
t_AsstFWDefltAssistX_HwNm_u8p8[5]	589
t_AsstFWDefltAssistX_HwNm_u8p8[6]	614
t_AsstFWDefltAssistX_HwNm_u8p8[7]	640
t_AsstFWDefltAssistX_HwNm_u8p8[8]	666
t_AsstFWDefltAssistX_HwNm_u8p8[9]	691
t_AsstFWDefltAssistX_HwNm_u8p8[10]	717
t_AsstFWDefltAssistX_HwNm_u8p8[11]	742
t_AsstFWDefltAssistX_HwNm_u8p8[12]	768
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	794 819
t_AsstFWDefitAssistX_HwNm_u8p8[14] t_AsstFWDefitAssistX_HwNm_u8p8[15]	819
t_AsstFWDefitAssistX_HwNm_u8p8[16]	870
t_AsstFWDefltAssistX_HwNm_u8p8[17]	896
t_AsstFWDefltAssistX_HwNm_u8p8[18]	922
t_AsstFWDefltAssistX_HwNm_u8p8[19]	947
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	9421
t_AsstFWPstepNstepThresh_Cnt_u16[0]	139
t_AsstFWPstepNstepThresh_Cnt_u16[1]	275
t_AsstFWVehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	30976 31104
t_AsstFWVehSpd_Kph_u9p7[3]	31232
t_AsstFWVehSpd_Kph_u9p7[4]	31360
t_AsstFWVehSpd_Kph_u9p7[5]	31488
t_AsstFWVehSpd_Kph_u9p7[6]	31616
t_AsstFWVehSpd_Kph_u9p7[7]	31744
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	0
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	99.3000031
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFi$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.76000023	5.76000023 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	275	275 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.60009766	-4.60009766 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.07499981	5.07499981 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.65999985	7.65999985 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.9000001	3.9000001 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-4.60009766	-4.60009766 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.19 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7
AssistFirewall ActiveKSV M str.K Uls f32	0.0500000007
AssistFirewall_ActiveRawAcc_Cnt_M_u16	139
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0599999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall LwrBoundKSV M str.K Uls f32	0.029999993
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.200000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.80000019
k_AsstFWInpLimitHFA_MtrNm_f32	2.4000001
k_AsstFWInpLimitHysComp_MtrNm_f32	2.43000007
k_AsstFWNstep_Cnt_u16	2688
k_AsstFWPstep_Cnt_u16	2337
k_RestoreThresh_MtrNm_f32	2.9000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2 AsstFWUprBoundX HwNm s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundX_HWNm_s4p11[7][0] t2 AsstFWUprBoundX HwNm s4p11[7][1]	
	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	22528



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1] t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-14336 -12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	26624 28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	12288



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	26624
t_AsstFWDefltAssistX_HwNm_u8p8[0]	486
t_AsstFWDefltAssistX_HwNm_u8p8[1]	512
t_AsstFWDefltAssistX_HwNm_u8p8[2]	538
t_AsstFWDefltAssistX_HwNm_u8p8[3]	563
t_AsstFWDefltAssistX_HwNm_u8p8[4]	589
t_AsstFWDefltAssistX_HwNm_u8p8[5]	614
t_AsstFWDefltAssistX_HwNm_u8p8[6]	640
t_AsstFWDefltAssistX_HwNm_u8p8[7]	666
t_AsstFWDefltAssistX_HwNm_u8p8[8]	691
t_AsstFWDefltAssistX_HwNm_u8p8[9]	717
t_AsstFWDefltAssistX_HwNm_u8p8[10]	742
t_AsstFWDefltAssistX_HwNm_u8p8[11]	768 794
t_AsstFWDefltAssistX_HwNm_u8p8[12]	
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	819 845
t_AsstFWDefitAssistX_HwNm_u8p8[14] t_AsstFWDefitAssistX_HwNm_u8p8[15]	845 870
t AsstFWDefitAssistX HwNm u8p8[16]	896
t_AsstFWDefltAssistX_HwNm_u8p8[17]	922
t_AsstFWDefltAssistX_HwNm_u8p8[18]	947
t_AsstFWDefltAssistX_HwNm_u8p8[19]	973
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	9421
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	9626
t_AsstFWPstepNstepThresh_Cnt_u16[0]	140
t_AsstFWPstepNstepThresh_Cnt_u16[1]	279
t_AsstFWVehSpd_Kph_u9p7[0]	33792
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	33920 34048
t_AsstFWVehSpd_Kph_u9p7[3]	34176
t AsstFWVehSpd Kph u9p7[4]	34304
t_AsstFWVehSpd_Kph_u9p7[5]	34432
t_AsstFWVehSpd_Kph_u9p7[6]	34560
t_AsstFWVehSpd_Kph_u9p7[7]	34688
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.099999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	123.099998
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFirewal$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.6500001	6.6500001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	279	279 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.70019531	-4.70019531 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.21780014	6.21780014 ± 4.88E-04	<b>~</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.76700002	0.76700002 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.80000019	4.80000019 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-4.70019531	-4.70019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.20 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8
AssistFirewall ActiveKSV M str.K Uls f32	0.059999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	142
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	1.2999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0700000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.20000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.2000005
AssistFirewall LwrBoundKSV M str.K Uls f32	0.039999991
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.300000012
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.0999999
k AsstFWInpLimitHFA MtrNm f32	2.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	2.77999997
k_AsstFWNstep_Cnt_u16	2564
k_AsstFWPstep_Cnt_u16	2460
k RestoreThresh MtrNm f32	3
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2 AsstFWUprBoundX HwNm s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192
t2 AsstFWUprBoundX HwNm s4p11[1][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384
	1000



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-4096
F	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288
	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
t2 AsstFWUprBoundY MtrNm s4p11[4][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192
	-6192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5] t2 AsstFWUprBoundY MtrNm s4p11[5][6]	
	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240
t2_AsstrWUprBoundY_MtrNm_s4p11[0][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	10240
	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	14336



	(14 11 10110
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	512
t_AsstFWDefltAssistX_HwNm_u8p8[1]	538
t_AsstFWDefltAssistX_HwNm_u8p8[2]	563
t_AsstFWDefltAssistX_HwNm_u8p8[3]	589
t_AsstFWDefltAssistX_HwNm_u8p8[4]	614
t_AsstFWDefltAssistX_HwNm_u8p8[5]	640
t_AsstFWDefltAssistX_HwNm_u8p8[6]	666
t_AsstFWDefltAssistX_HwNm_u8p8[7]	691
t_AsstFWDefitAssistX_HwNm_u8p8[8]	717
	742
t_AsstFWDefltAssistX_HwNm_u8p8[9]	
t_AsstFWDefltAssistX_HwNm_u8p8[10]	768
t_AsstFWDefltAssistX_HwNm_u8p8[11]	794
t_AsstFWDefltAssistX_HwNm_u8p8[12]	819
t_AsstFWDefltAssistX_HwNm_u8p8[13]	845
t_AsstFWDefltAssistX_HwNm_u8p8[14]	870
t_AsstFWDefltAssistX_HwNm_u8p8[15]	896
t_AsstFWDefltAssistX_HwNm_u8p8[16]	922
t AsstFWDefltAssistX HwNm u8p8[17]	947
t_AsstFWDefitAssistX_HwNm_u8p8[18]	973
	998
t_AsstFWDefltAssistX_HwNm_u8p8[19]	
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	9830
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t_AsstFWPstepNstepThresh_Cnt_u16[0]	141
t_AsstFWPstepNstepThresh_Cnt_u16[1]	283
t_AsstFWVehSpd_Kph_u9p7[0]	36736
t_AsstFWVehSpd_Kph_u9p7[1]	36864
t_AsstFWVehSpd_Kph_u9p7[2]	36992
t_AsstFWVehSpd_Kph_u9p7[3]	37120
t_AsstFWVehSpd_Kph_u9p7[4]	37248
t_AsstFWVehSpd_Kph_u9p7[5]	37376
t_AsstFWVehSpd_Kph_u9p7[6]	37504
t_AsstFWVehSpd_Kph_u9p7[7]	37632
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1
•	
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-6
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	234.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f3	
•	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cr	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	
• • • • • • • • • • • • • • • • • • • •	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
• • • • • • • • • • • • • • • • • • • •	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7.51999998	7.51999998 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	283	283 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.79980469	-4.79980469 ± 4.88E-04	<b>~</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.56739998	6.56739998 ± 4.88E-04	<b>~</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.19200015	2.19199991 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.79999971	1.79999995 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-4.79980469	-4.79980469 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>~</b>
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.21 (Repeat Count = 1)	✓
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall ActiveKSV M str.K Uls f32	0.0700000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	123
AssistFirewall AsstReducedPerfSV Cnt M Iqc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.3999998
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	8
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.079999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.29999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.050000007
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.40000006
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.4000001
k_AsstFWInpLimitHFA_MtrNm_f32	2.7999995
k_AsstFWInpLimitHysComp_MtrNm_f32	3.13000011
k_AsstFWNstep_Cnt_u16	2440
k_AsstFWPstep_Cnt_u16	2583
k_RestoreThresh_MtrNm_f32	3.099999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336
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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2 AsstFWUprBoundX HwNm s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_Asst WopiBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2 AsstFWUprBoundX HwNm s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstrWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3] t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-2048



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9] t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240
	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12200
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
	-16384 -14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384



	( 14 15 16 16
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	538
t_AsstFWDefltAssistX_HwNm_u8p8[1]	563
t_AsstFWDefltAssistX_HwNm_u8p8[2]	589
t_AsstFWDefltAssistX_HwNm_u8p8[3]	614
t_AsstFWDefltAssistX_HwNm_u8p8[4]	640
t_AsstFWDefltAssistX_HwNm_u8p8[5]	666
t_AsstFWDefltAssistX_HwNm_u8p8[6]	691
t_AsstFWDefltAssistX_HwNm_u8p8[7]	717
t_AsstFWDefltAssistX_HwNm_u8p8[8]	742
· · · ·	768
t_AsstFWDefltAssistX_HwNm_u8p8[9]	
t_AsstFWDefltAssistX_HwNm_u8p8[10]	794
t_AsstFWDefltAssistX_HwNm_u8p8[11]	819
t_AsstFWDefltAssistX_HwNm_u8p8[12]	845
t_AsstFWDefltAssistX_HwNm_u8p8[13]	870
t_AsstFWDefltAssistX_HwNm_u8p8[14]	896
t_AsstFWDefltAssistX_HwNm_u8p8[15]	922
t_AsstFWDefltAssistX_HwNm_u8p8[16]	947
t AsstFWDefltAssistX HwNm u8p8[17]	973
t_AsstFWDefitAssistX_HwNm_u8p8[18]	998
	1024
t_AsstFWDefltAssistX_HwNm_u8p8[19]	
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	10035
t_AsstFWPstepNstepThresh_Cnt_u16[0]	142
• • • • • • • • • • • • • • • • • • • •	
t_AsstFWPstepNstepThresh_Cnt_u16[1]	287
t_AsstFWVehSpd_Kph_u9p7[0]	39680
t_AsstFWVehSpd_Kph_u9p7[1]	39808
t_AsstFWVehSpd_Kph_u9p7[2]	39936
t_AsstFWVehSpd_Kph_u9p7[3]	40064
t_AsstFWVehSpd_Kph_u9p7[4]	40192
t_AsstFWVehSpd_Kph_u9p7[5]	40320
t_AsstFWVehSpd_Kph_u9p7[6]	40448
t_AsstFWVehSpd_Kph_u9p7[7]	40576
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2
	0
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igc.value	
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-7
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	0
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	•
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cr	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	
tet Die last An AssistEisewell AssistEisewell Doct 11 T	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f3:	2 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f3: tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.023	1.023 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	287	287 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.89990234	-4.89990234 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.90399981	7.90399981 ± 4.88E-04	<b>~</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.79499984	2.79500008 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.19999981	2.20000005 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-4.89990234	-4.89990234 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T ✓				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.22 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	2.20000005
AssistFirewall ActiveKSV M str.K Uls f32	0.079999982
AssistFirewall_ActiveRawAcc_Cnt_M_u16	246
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall CombAsstSV MtrNm M f32	1.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.090000036
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.3999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.5
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.69999981
k_AsstFWInpLimitHFA_MtrNm_f32	3
k_AsstFWInpLimitHysComp_MtrNm_f32	3.48000002
k_AsstFWNstep_Cnt_u16	2316
k_AsstFWPstep_Cnt_u16	2706
k_RestoreThresh_MtrNm_f32	3.20000005
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_Asst WopiBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_Asst WoprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3] t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_Asst WorlboundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
tz_AsstFWUprBoundX_HwNm_s4p11[7][6] t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	2048
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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	6144
	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144
	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-20480
t2_AsstFWUprBoundY_mitrNm_s4p11[5][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192
12_1.0041 AAONIDORUG I TINITIAIII 20+h I I[1][9]	-0192



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
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t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	563
t_AsstFWDefltAssistX_HwNm_u8p8[1]	589
t_AsstFWDefltAssistX_HwNm_u8p8[2]	614
t_AsstFWDefltAssistX_HwNm_u8p8[3]	640
t_AsstFWDefltAssistX_HwNm_u8p8[4]	666
t_AsstFWDefltAssistX_HwNm_u8p8[5]	691
t_AsstFWDefltAssistX_HwNm_u8p8[6]	717
t_AsstFWDefltAssistX_HwNm_u8p8[7]	742
t_AsstFWDefltAssistX_HwNm_u8p8[8]	768
t_AsstFWDefltAssistX_HwNm_u8p8[9]	794
t_AsstFWDefltAssistX_HwNm_u8p8[10]	819
t_AsstFWDefltAssistX_HwNm_u8p8[11]	845
t_AsstFWDefltAssistX_HwNm_u8p8[12]	870
t_AsstFWDefltAssistX_HwNm_u8p8[13]	896
t_AsstFWDefltAssistX_HwNm_u8p8[14]	922
t_AsstFWDefltAssistX_HwNm_u8p8[15]	947
t_AsstFWDefltAssistX_HwNm_u8p8[16]	973
t AsstFWDefltAssistX HwNm u8p8[17]	998
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1050
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	6349
t_AsstFWDefitAssistY_MtrNm_s4p11[1]	6554
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	10240
t_AsstFWPstepNstepThresh_Cnt_u16[0]	143
t AsstFWPstepNstepThresh Cnt u16[1]	291
t_AsstFWVehSpd_Kph_u9p7[0]	42624
t_AsstFWVehSpd_Kph_u9p7[1]	42752
t_AsstFWVehSpd_Kph_u9p7[2]	4280
t_AsstFWVehSpd_Kph_u9p7[3]	43008
t_Asstrwvenspd_kpn_usp7[3] t_AsstFWVehSpd_kph_usp7[4]	43136
_	
t_AsstFWVehSpd_Kph_u9p7[5]	43264
t_AsstFWVehSpd_Kph_u9p7[6]	43392
t_AsstFWVehSpd_Kph_u9p7[7]	43520
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4.099999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	255
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cn	_tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_inst_Ap_assistFirewall.AssistFirewall_Per1_HighFreqassist_MtrNm_f32_	
• • • • • • • • • • • • • • • • • • • •	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.02400017	2.02399993 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	291	291 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5	-5 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.81100011	1.81099999 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.61399984	3.61400008 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1	1 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-5	-5 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.23 (Repeat Count = 1)  ✓		
Name	Input Value	
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.0999999	
AssistFirewall ActiveKSV M str.K Uls f32	0.00600000005	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	369	
AssistFirewall AsstReducedPerfSV Cnt M lgc	1	
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.6000002	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0599999987	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998	
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.090000036	
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.0999999	
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.029999993	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6	
k_AsstFWInpLimitHFA_MtrNm_f32	3.20000005	
k_AsstFWInpLimitHysComp_MtrNm_f32	3.82999992	
k_AsstFWNstep_Cnt_u16	2192	
k_AsstFWPstep_Cnt_u16	2829	
k_RestoreThresh_MtrNm_f32	3.2999995	
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336	
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288	
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-12288	
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240	



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-4096
	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
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2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
2 AsstFWUprBoundX HwNm s4p11[6][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
	-2040
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	4096



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	26624	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	28672	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-12288	
:2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048	
t2 AsstFWUprBoundY MtrNm s4p11[2][9]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	6144	
	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-28672	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-26624	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-12288	
	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]		
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	589
t_AsstFWDefltAssistX_HwNm_u8p8[1]	614
t_AsstFWDefltAssistX_HwNm_u8p8[2]	640
t_AsstFWDefltAssistX_HwNm_u8p8[3]	666
t_AsstFWDefltAssistX_HwNm_u8p8[4]	691
t_AsstFWDefltAssistX_HwNm_u8p8[5]	717
t_AsstFWDefltAssistX_HwNm_u8p8[6]	742
t_AsstFWDefltAssistX_HwNm_u8p8[7]	768
t_AsstFWDefltAssistX_HwNm_u8p8[8]	794
t_AsstFWDefltAssistX_HwNm_u8p8[9]	819
t_AsstFWDefltAssistX_HwNm_u8p8[10]	845
t_AsstFWDefltAssistX_HwNm_u8p8[11]	870
t_AsstFWDefltAssistX_HwNm_u8p8[12]	896
t_AsstFWDefltAssistX_HwNm_u8p8[13]	922
t_AsstFWDefltAssistX_HwNm_u8p8[14]	947
t_AsstFWDefltAssistX_HwNm_u8p8[15]	973
t_AsstFWDefltAssistX_HwNm_u8p8[16]	998
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1075
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	10445
t_AsstFWPstepNstepThresh_Cnt_u16[0]	144
t_AsstFWPstepNstepThresh_Cnt_u16[1]	295
t_AsstFWVehSpd_Kph_u9p7[0]	45568
t_AsstFWVehSpd_Kph_u9p7[1]	45696
t_AsstFWVehSpd_Kph_u9p7[2]	45824
t_AsstFWVehSpd_Kph_u9p7[3]	45952
t_AsstFWVehSpd_Kph_u9p7[4]	46080
t_AsstFWVehSpd_Kph_u9p7[5]	46208
t_AsstFWVehSpd_Kph_u9p7[6]	46336
t_AsstFWVehSpd_Kph_u9p7[7]	46464
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-10
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	22.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_li	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32
191_110_1101_pp_nooioti ilewaii.nooioti ilewaii_r et i_veliitileopeeti_npii_132	tgr_notion inewall_reliationeopedu_rvpil_loz



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.06939983	5.06939983 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	295	295 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.10009766	-5.10009766 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.46600008	4.46600008 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.459999979	0.460000008 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.85699987	2.85700011 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-5.10009766	-5.10009766 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.24 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall ActiveKSV M str.K Uls f32	0.059999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	492
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	1.7000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0089999961
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.60000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.0999999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.079999982
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.059999987
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6.30000019
k AsstFWInpLimitHFA MtrNm f32	3.4000001
k_AsstFWInpLimitHysComp_MtrNm_f32	4.17999983
k_AsstFWNstep_Cnt_u16	2068
k_AsstFWPstep_Cnt_u16	2952
k RestoreThresh MtrNm f32	3.4000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2 AsstFWUprBoundX HwNm s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192
	1 0.00



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][4] t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][8] t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
	2048
t2 AsstFWUprBoundY MtrNm s4p11[0][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	4096



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240	
	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]		
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-2048	
	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]		
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-4096	
2 AsstFWUprBoundY MtrNm s4p11[2][5]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	0	
:2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336	
	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]		
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	26624	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-26624	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-24576	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048	
, , , , , , , , , , , , , , , , , , , ,		
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288	
	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]		
2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384 18432	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	16384 18432 20480	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	16384 18432 20480 -10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]  2_AsstFWUprBoundY_MtrNm_s4p11[6][8]  2_AsstFWUprBoundY_MtrNm_s4p11[6][9]  2_AsstFWUprBoundY_MtrNm_s4p11[6][10]  2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	16384 18432 20480	
12_AsstFWUprBoundY_MtrNm_s4p11[6][7] 12_AsstFWUprBoundY_MtrNm_s4p11[6][8] 12_AsstFWUprBoundY_MtrNm_s4p11[6][9] 12_AsstFWUprBoundY_MtrNm_s4p11[6][10] 12_AsstFWUprBoundY_MtrNm_s4p11[7][0] 12_AsstFWUprBoundY_MtrNm_s4p11[7][1] 12_AsstFWUprBoundY_MtrNm_s4p11[7][1] 12_AsstFWUprBoundY_MtrNm_s4p11[7][2]	16384 18432 20480 -10240	



	(
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096
	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefltAssistX_HwNm_u8p8[0]	614
t_AsstFWDefltAssistX_HwNm_u8p8[1]	640
t_AsstFWDefltAssistX_HwNm_u8p8[2]	666
t_AsstFWDefltAssistX_HwNm_u8p8[3]	691
t_AsstFWDefltAssistX_HwNm_u8p8[4]	717
t AsstFWDefltAssistX HwNm u8p8[5]	742
t_AsstFWDefltAssistX_HwNm_u8p8[6]	768
t_AsstFWDefltAssistX_HwNm_u8p8[7]	794
t_AsstFWDefltAssistX_HwNm_u8p8[8]	819
	845
t_AsstFWDefltAssistX_HwNm_u8p8[9]	
t_AsstFWDefltAssistX_HwNm_u8p8[10]	870
t_AsstFWDefltAssistX_HwNm_u8p8[11]	896
t_AsstFWDefltAssistX_HwNm_u8p8[12]	922
t_AsstFWDefltAssistX_HwNm_u8p8[13]	947
t_AsstFWDefltAssistX_HwNm_u8p8[14]	973
t_AsstFWDefltAssistX_HwNm_u8p8[15]	998
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1024
t AsstFWDefltAssistX HwNm u8p8[17]	1050
t_AsstFWDefitAssistX_HwNm_u8p8[18]	1075
	1101
t_AsstFWDefltAssistX_HwNm_u8p8[19]	
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	8806
	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	10650
t_AsstFWPstepNstepThresh_Cnt_u16[0]	145
t_AsstFWPstepNstepThresh_Cnt_u16[1]	299
t_AsstFWVehSpd_Kph_u9p7[0]	0
t_AsstFWVehSpd_Kph_u9p7[1]	0
t_AsstFWVehSpd_Kph_u9p7[2]	0
t_AsstFWVehSpd_Kph_u9p7[3]	0
t_AsstFWVehSpd_Kph_u9p7[4]	0
t_AsstFWVehSpd_Kph_u9p7[5]	0
t_AsstFWVehSpd_Kph_u9p7[6]	0
t_AsstFWVehSpd_Kph_u9p7[7]	0
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igc.value	0
•	
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.099999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	10.1999998
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_	_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_	
tgt_Rte_Inst_Ap_AssistInewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_t	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tot Dto Inot An AppintEirough AppintEirough Daniel Handard Communication	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_ tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enur tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.85399985	3.85400009 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	299	299 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.29980469	3.29980469 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.17559981	3.17560005 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.61199999	5.61199999 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.18799996	2.18799996 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.29980469	3.29980469 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

T			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.25 (Repeat Count = 1)	· ·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall ActiveKSV M str.K Uls f32	0.00800000038
AssistFirewall_ActiveRawAcc_Cnt_M_u16	615
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	1,7999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0099999978
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.70000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0900000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0700000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6.5999999
k_AsstFWInpLimitHFA_MtrNm_f32	3.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	4.53000021
k_AsstFWNstep_Cnt_u16	1944
k_AsstFWPstep_Cnt_u16	3075
k_RestoreThresh_MtrNm_f32	3.5
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384
12_Asst WoprBoundX_rwini_s4p11[4][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
2 AsstFWUprBoundX HwNm s4p11[6][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
2 AsstFWUprBoundX HwNm s4p11[6][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
O A JEMAN B. INVASOR CONTROL	-6144
	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096 -2048
i2_AsstFWUprBoundY_MtrNm_s4p11[0][1] i2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	
i2_AsstFWUprBoundY_MtrNm_s4p11[0][1] i2_AsstFWUprBoundY_MtrNm_s4p11[0][2] i2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
12_AsstFWUprBoundY_MtrNm_s4p11[0][0] 12_AsstFWUprBoundY_MtrNm_s4p11[0][1] 12_AsstFWUprBoundY_MtrNm_s4p11[0][2] 12_AsstFWUprBoundY_MtrNm_s4p11[0][3] 12_AsstFWUprBoundY_MtrNm_s4p11[0][4] 12_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048 0 2048



Name	Innut Value
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10] t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144 -4096
t2 AcctEM/InrRoundV MtrNm c4c44[7][2]	74417711
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048



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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	640
t_AsstFWDefltAssistX_HwNm_u8p8[1]	666
t_AsstFWDefltAssistX_HwNm_u8p8[2]	691
t_AsstFWDefltAssistX_HwNm_u8p8[3]	717
t_AsstFWDefltAssistX_HwNm_u8p8[4]	742
t_AsstFWDefltAssistX_HwNm_u8p8[5]	768
t_AsstFWDefltAssistX_HwNm_u8p8[6]	794
t_AsstFWDefltAssistX_HwNm_u8p8[7]	819
t_AsstFWDefltAssistX_HwNm_u8p8[8]	845
t_AsstFWDefltAssistX_HwNm_u8p8[9]	870
t_AsstFWDefltAssistX_HwNm_u8p8[10]	896
t_AsstFWDefltAssistX_HwNm_u8p8[11] t AsstFWDefltAssistX HwNm u8p8[12]	922 947
,	
t_AsstFWDefltAssistX_HwNm_u8p8[13]	973 998
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[15] t_AsstFWDefltAssistX_HwNm_u8p8[16]	1050
t_AsstFWDefitAssistX_HwNm_u8p8[17]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1101
t_AsstFWDefitAssistX_HwNm_u8p8[19]	1126
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	10854
t_AsstFWPstepNstepThresh_Cnt_u16[0]	146
t_AsstFWPstepNstepThresh_Cnt_u16[1]	303
t_AsstFWVehSpd_Kph_u9p7[0]	65408
t_AsstFWVehSpd_Kph_u9p7[1]	65408
t_AsstFWVehSpd_Kph_u9p7[2] t_AsstFWVehSpd_Kph_u9p7[3]	65408 65409
t AsstFWVehSpd Kph u9p7[4]	65408 65408
t_AsstFWVehSpd_Kph_u9p7[5]	65408
t AsstFWVehSpd Kph u9p7[6]	65408
t_AsstFWVehSpd_Kph_u9p7[7]	65408
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	20.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.05919981	5.05919981 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	303	303 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.39990234	3.39990234 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.17000008	4.17000008 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.63999987	4.63999987 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.09299994	3.09299994 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.39990234	3.39990234 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•

Τ				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.26 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.099999
AssistFirewall ActiveKSV M str.K Uls f32	0.0089999961
AssistFirewall_ActiveRawAcc_Cnt_M_u16	738
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	1.89999998
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.019999996
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall LwrBoundKSV M str.K Uls f32	0.059999987
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.079999982
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6.9000001
k AsstFWInpLimitHFA MtrNm f32	3.79999995
k_AsstFWInpLimitHysComp_MtrNm_f32	4.88000011
k_AsstFWNstep_Cnt_u16	1820
k_AsstFWPstep_Cnt_u16	3198
k RestoreThresh MtrNm f32	3.5999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2 AsstFWUprBoundX HwNm s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0	
2 AsstFWUprBoundY MtrNm s4p11[2][5]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-28672	
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-26624	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-16384	
	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]		
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	0	
2 AsstFWUprBoundY MtrNm s4p11[4][9]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048	
===		



Input Value
2048
4096
6144
8192
10240
12288
14336
666
691
717
742
768
794
819
845
870 896
922
947
973
998
1024
1050
1075
1101
1126
1152
7168
7373
7578
7782
7987
8192
8397
8602
8806
9011
9216
9421
9626
9830
10035
10240
10445
10650
10854
11059
147 307
12800
12800
12800
12800
12800
12800
12800
12800
12800 7
7
7 0
7 0 2
7 0 2 3
7 0 2 3 5.0999999
7 0 2 3 5.0999999
7 0 2 3 5.0999999 1 0.78125
7 0 2 3 5.0999999 1 0.78125 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
7 0 2 3 5.0999999 1 0.78125 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
7 0 2 3 5.0999999 1 0.78125 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
7 0 2 3 5.0999999 1 0.78125 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
7 0 2 3 5.0999999 1 0.78125 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
7 0 2 3 5.0999999 1 0.78125 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.04509974	6.04510021 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	307	307 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.89990234	3.89990234 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.2736001	5.2736001 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.69999981	5.69999981 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.17199993	4.17199993 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.89990234	3.89990234 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.27 (Repeat Count = 1)  ✓		
Name	Input Value	
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	4	
AssistFirewall ActiveKSV M str.K Uls f32	0.0099999978	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	861	
AssistFirewall AsstReducedPerfSV Cnt M lqc	1	
AssistFirewall_CombAsstSV_MtrNm_M_f32	-2.0999999	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.0999999	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.029999993	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.8999998	
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00800000038	
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999	
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.090000036	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
k_AsstFWInpLimitBaseAsst_MtrNm_f32	7.19999981	
k_AsstFWInpLimitHFA_MtrNm_f32	4	
k_AsstFWInpLimitHysComp_MtrNm_f32	5.23000002	
k_AsstFWNstep_Cnt_u16	1696	
k_AsstFWPstep_Cnt_u16	3321	
k_RestoreThresh_MtrNm_f32	3.70000005	
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-20480	
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-20480	
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-20480	
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-20480	
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-20480	
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-20480	
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-20480	
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-20480	
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-20480	
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	-20480	
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	-20480	
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-20480	
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-20480	
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-20480	
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-20480	
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-20480	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-20480	
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-20480	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-20480	
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-20480	
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	-20480	
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	-20480	
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-20480	



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-20480
t2_Asst WopiBoundX_HwNm_s4p11[5][5]	-20480
:2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-20480
	-20480
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288
	· · · · · · · · · · · · · · · · · · ·



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432	
	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]		
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048	
2 AsstFWUprBoundY MtrNm s4p11[2][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144	
	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]		
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-18432	
12_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-10240	
	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]		
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	691
t_AsstFWDefltAssistX_HwNm_u8p8[1]	717
t_AsstFWDefltAssistX_HwNm_u8p8[2]	742
t_AsstFWDefltAssistX_HwNm_u8p8[3]	768
t_AsstFWDefltAssistX_HwNm_u8p8[4]	794
t_AsstFWDefltAssistX_HwNm_u8p8[5]	819
t_AsstFWDefltAssistX_HwNm_u8p8[6]	845
t_AsstFWDefltAssistX_HwNm_u8p8[7]	870
t_AsstFWDefltAssistX_HwNm_u8p8[8]	896
t_AsstFWDefltAssistX_HwNm_u8p8[9]	922
t_AsstFWDefltAssistX_HwNm_u8p8[10]	947
t_AsstFWDefltAssistX_HwNm_u8p8[11]	973
t_AsstFWDefltAssistX_HwNm_u8p8[12]	998
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	1024 1050
t_AsstFWDefitAssistX_HwNm_u8p8[14] t_AsstFWDefitAssistX_HwNm_u8p8[15]	1075
t AsstFWDefitAssistX HwNm u8p8[16]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1178
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	11264
t_AsstFWPstepNstepThresh_Cnt_u16[0]	148
t_AsstFWPstepNstepThresh_Cnt_u16[1]	311
t_AsstFWVehSpd_Kph_u9p7[0]	1408
t_AsstFWVehSpd_Kph_u9p7[1]	1536 1664
t_AsstFWVehSpd_Kph_u9p7[2] t_AsstFWVehSpd_Kph_u9p7[3]	1792
t_AsstFWVehSpd_Kph_u9p7[4]	1920
t_AsstFWVehSpd_Kph_u9p7[5]	2048
t AsstFWVehSpd Kph u9p7[6]	2176
t_AsstFWVehSpd_Kph_u9p7[7]	2304
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	40.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFirewal$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.96000004	3.96000004 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	311	311 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.89990234	4.89990234 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.37989998	6.37989998 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.96799994	6.96799994 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.37099981	4.37099981 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	•
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4.89990234	4.89990234 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	•
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.28 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5
AssistFirewall ActiveKSV M str.K Uls f32	0.019999996
AssistFirewall_ActiveRawAcc_Cnt_M_u16	984
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall CombAsstSV MtrNm M f32	-2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.039999991
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall LwrBoundKSV M str.K Uls f32	0.00899999961
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.099999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.100000001
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	7.5
k AsstFWInpLimitHFA MtrNm f32	4.19999981
k_AsstFWInpLimitHysComp_MtrNm_f32	5.57999992
k_AsstFWNstep_Cnt_u16	1572
k_AsstFWPstep_Cnt_u16	3444
k RestoreThresh MtrNm f32	3.79999995
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	20480
t2 AsstFWUprBoundX HwNm s4p11[0][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	20480
t2 AsstFWUprBoundX HwNm s4p11[1][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	20480
	1-2



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	20480
t2 AsstFWUprBoundX HwNm s4p11[2][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	20480
t2 AsstFWUprBoundX HwNm s4p11[6][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	8192
LE_, 1001 VV OPI DOUNG I _IVILIVIII_SHP I I[U][U]	
t2 AsstEWI InrBoundY MtrNm s4n11[0][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	10240 12288 14336



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
, , , , , , , , , , , , , , , , , , , ,	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336
	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	0
	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	18432
12_AsstFWUprBoundY_MtrNm_s4p11[6][8]         12_AsstFWUprBoundY_MtrNm_s4p11[6][9]         12_AsstFWUprBoundY_MtrNm_s4p11[6][10]         12_AsstFWUprBoundY_MtrNm_s4p11[7][0]         12_AsstFWUprBoundY_MtrNm_s4p11[7][1]         12_AsstFWUprBoundY_MtrNm_s4p11[7][2]	18432 0



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	717
t_AsstFWDefltAssistX_HwNm_u8p8[1]	742
t_AsstFWDefltAssistX_HwNm_u8p8[2]	768
t_AsstFWDefltAssistX_HwNm_u8p8[3]	794
t_AsstFWDefltAssistX_HwNm_u8p8[4]	819
t_AsstFWDefltAssistX_HwNm_u8p8[5]	845
t_AsstFWDefltAssistX_HwNm_u8p8[6]	870
t_AsstFWDefltAssistX_HwNm_u8p8[7]	896
t_AsstFWDefltAssistX_HwNm_u8p8[8]	922
t_AsstFWDefltAssistX_HwNm_u8p8[9]	947
t_AsstFWDefltAssistX_HwNm_u8p8[10]	973
t_AsstFWDefltAssistX_HwNm_u8p8[11]	998
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	1050 1075
t_AsstFWDefitAssistX_HwNm_u8p8[14] t AsstFWDefitAssistX_HwNm_u8p8[15]	1101
t_AsstFWDefitAssistX_HwNm_u8p8[16]	1126
t_AsstFWDefitAssistX_HwNm_u8p8[17]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1203
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	11469
t_AsstFWPstepNstepThresh_Cnt_u16[0]	149
t_AsstFWPstepNstepThresh_Cnt_u16[1]	315
t_AsstFWVehSpd_Kph_u9p7[0] t_AsstFWVehSpd_Kph_u9p7[1]	4352 4480
	4608
t_AsstFWVehSpd_Kph_u9p7[2] t_AsstFWVehSpd_Kph_u9p7[3]	4736
t_AsstFWVehSpd_kph_u9p7[4]	4864
t_AsstFWVehSpd_Kph_u9p7[5]	4992
t_AsstFWVehSpd_Kph_u9p7[6]	5120
t_AsstFWVehSpd_Kph_u9p7[7]	5248
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	50.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFi$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4.9000001	4.9000001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	315	315 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.60009766	5.60009766 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.08400011	4.08400011 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.9369998	7.9369998 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.38999987	5.38999987 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	5.60009766	5.60009766 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

<b>T</b>				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.29 (Repeat Count = 1)	▼
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6
AssistFirewall ActiveKSV M str.K Uls f32	0.029999993
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1107
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-2.29999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0099999978
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.20000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	7.80000019
k_AsstFWInpLimitHFA_MtrNm_f32	4.400001
k_AsstFWInpLimitHysComp_MtrNm_f32	5.92999983
k_AsstFWNstep_Cnt_u16	1448
k_AsstFWPstep_Cnt_u16	3567
k_RestoreThresh_MtrNm_f32	3.9000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	0
t2 AsstFWUprBoundX HwNm s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2 AsstFWUprBoundX HwNm s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	18432
= , , , ,	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0] t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2] t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	14336



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	742
t_AsstFWDefltAssistX_HwNm_u8p8[1]	768
t_AsstFWDefltAssistX_HwNm_u8p8[2]	794
t_AsstFWDefltAssistX_HwNm_u8p8[3]	819
t_AsstFWDefltAssistX_HwNm_u8p8[4]	845
t_AsstFWDefltAssistX_HwNm_u8p8[5]	870
t_AsstFWDefltAssistX_HwNm_u8p8[6]	896
t_AsstFWDefltAssistX_HwNm_u8p8[7]	922
t_AsstFWDefltAssistX_HwNm_u8p8[8]	947
t_AsstFWDefltAssistX_HwNm_u8p8[9]	973
t_AsstFWDefltAssistX_HwNm_u8p8[10]	998
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[13] t AsstFWDefltAssistX HwNm u8p8[14]	11075
t_AsstFWDefitAssistX_HwNm_u8p8[14] t_AsstFWDefitAssistX_HwNm_u8p8[15]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1152
t_AsstFWDefitAssistX_HwNm_u8p8[17]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1203
t AsstFWDefltAssistX HwNm u8p8[19]	1229
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	11674
t_AsstFWPstepNstepThresh_Cnt_u16[0]	150
t_AsstFWPstepNstepThresh_Cnt_u16[1]	319
t_AsstFWVehSpd_Kph_u9p7[0]	7296 7424
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	7552
t_AsstFWVehSpd_Kph_u9p7[3]	7680
t AsstFWVehSpd Kph u9p7[4]	7808
t_AsstFWVehSpd_Kph_u9p7[5]	7936
t_AsstFWVehSpd_Kph_u9p7[6]	8064
t_AsstFWVehSpd_Kph_u9p7[7]	8192
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2.20000005
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-6
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	60.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFi$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.82000017	5.82000017 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	319	319 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.70019531	-5.70019531 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.17999983	5.17999983 ± 4.88E-04	<b>~</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.199	1.199 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1	1 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-5.70019531	-5.70019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Τ				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7
AssistFirewall_ActiveKSV_M_str.K_UIs_f32	0.039999991
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1230
AssistFirewall_ActiveRawAcc_Citt_ivi_u16 AssistFirewall AsstReducedPerfSV Cnt M lgc	1230
AssistFirewall_AssiReducedPenSv_Cnt_M_gc AssistFirewall CombAsstSV MtrNm M f32	-2.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6 0.0599999987
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.02999997
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0199999996
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.300000012
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
<_AsstFWInpLimitBaseAsst_MtrNm_f32	8.10000038
<_AsstFWInpLimitHFA_MtrNm_f32	4.5999999
<_AsstFWInpLimitHysComp_MtrNm_f32	6.28000021
<_AsstFWNstep_Cnt_u16	1324
c_AsstFWPstep_Cnt_u16	3690
c_RestoreThresh_MtrNm_f32	4
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2 AsstFWUprBoundX HwNm s4p11[6][4]	8192
t2 AsstFWUprBoundX HwNm s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	
t2_AsstFWUprBoundX_HWNm_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	6144
	19



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-4096	
	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]		
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240	
2 AsstFWUprBoundY MtrNm s4p11[2][5]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192	
	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]		
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192	
t2 AsstFWUprBoundY MtrNm s4p11[4][9]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144	
	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]		
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528	
	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	768
t_AsstFWDefltAssistX_HwNm_u8p8[1]	794
t_AsstFWDefltAssistX_HwNm_u8p8[2]	819
t_AsstFWDefltAssistX_HwNm_u8p8[3]	845
t_AsstFWDefltAssistX_HwNm_u8p8[4]	870
t_AsstFWDefltAssistX_HwNm_u8p8[5]	896
t_AsstFWDefltAssistX_HwNm_u8p8[6]	922
t_AsstFWDefltAssistX_HwNm_u8p8[7]	947
t_AsstFWDefltAssistX_HwNm_u8p8[8]	973
t_AsstFWDefltAssistX_HwNm_u8p8[9]	998
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	1101
t_AsstFWDefitAssistX_HwNm_u8p8[14] t_AsstFWDefitAssistX_HwNm_u8p8[15]	1152
t_AsstFWDefitAssistX_HwNm_u8p8[16]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1254
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	11878
t_AsstFWPstepNstepThresh_Cnt_u16[0]	151
t_AsstFWPstepNstepThresh_Cnt_u16[1]	323
t_AsstFWVehSpd_Kph_u9p7[0]	10240
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	10368 10496
t_AsstFWVehSpd_Kph_u9p7[3]	10624
t_AsstFWVehSpd_kph_u9p7[4]	10752
t_AsstFWVehSpd_Kph_u9p7[5]	10880
t_AsstFWVehSpd_Kph_u9p7[6]	11008
t_AsstFWVehSpd_Kph_u9p7[7]	11136
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3.099999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-7
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	70.1999969
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFi$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.71999979	6.71999979 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	323	323 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.79980469	-5.79980469 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.28200006	6.28200006 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.09599996	2.09599996 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.2999995	2.29999995 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-5.79980469	-5.79980469 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Τ				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.31 (Repeat Count = 1)	✓
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8
AssistFirewall ActiveKSV M str.K Uls f32	0.0500000007
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1353
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-2.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.070000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.03999996
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.029999993
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.40000006
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	8.39999962
k_AsstFWInpLimitHFA_MtrNm_f32	4.80000019
k_AsstFWInpLimitHysComp_MtrNm_f32	6.63000011
k_AsstFWNstep_Cnt_u16	1200
k_AsstFWPstep_Cnt_u16	3813
k_RestoreThresh_MtrNm_f32	4.0999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-20480



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	-2048 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10] t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-20480
t2_Asst WoprBoundX_HwNm_s4p11[3][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-18432 -16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2] t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6] t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7] t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	-2046
t2_Asst WopiBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstrWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-2048
t2_AsstrWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-2048	
	0	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]		
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	14336	
:2_Asst WopiBoundY_MtrNm_s4p11[2][6]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-14336	
	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096	
t2 AsstFWUprBoundY MtrNm s4p11[4][6]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-4096	
	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]		
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576	
O A - 45 A		
	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]		



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	794
t_AsstFWDefltAssistX_HwNm_u8p8[1]	819
t_AsstFWDefltAssistX_HwNm_u8p8[2]	845
t_AsstFWDefltAssistX_HwNm_u8p8[3]	870
t_AsstFWDefltAssistX_HwNm_u8p8[4]	896
t_AsstFWDefltAssistX_HwNm_u8p8[5]	922
	947
t_AsstFWDefltAssistX_HwNm_u8p8[6]	973
t_AsstFWDefltAssistX_HwNm_u8p8[7]	
t_AsstFWDefltAssistX_HwNm_u8p8[8]	998
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1280
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	9830
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	10240
	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	12083
t_AsstFWPstepNstepThresh_Cnt_u16[0]	152
t_AsstFWPstepNstepThresh_Cnt_u16[1]	327
t_AsstFWVehSpd_Kph_u9p7[0]	13184
t_AsstFWVehSpd_Kph_u9p7[1]	13312
t_AsstFWVehSpd_Kph_u9p7[2]	13440
t_AsstFWVehSpd_Kph_u9p7[3]	13568
t_AsstFWVehSpd_Kph_u9p7[4]	13696
t_AsstFWVehSpd_Kph_u9p7[5]	13824
t_AsstFWVehSpd_Kph_u9p7[6]	13952
t_AsstFWVehSpd_Kph_u9p7[7]	14080
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
~	
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	80.099985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
	that Assess Second Bank Bakest AssetThi Condes Out Inc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7.5999999	7.5999999 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	327	327 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.89990234	-5.89990234 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.41300011	7.41300011 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.8269999	2.8269999 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.20000005	3.20000005 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-5.89990234	-5.89990234 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.32 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.1000002
AssistFirewall ActiveKSV M str.K Uls f32	0.059999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1476
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	-2.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	8
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.079999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.04999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.099999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.039999991
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.5
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2
k AsstFWInpLimitHFA MtrNm f32	5
k_AsstFWInpLimitHysComp_MtrNm_f32	0.200000003
k_AsstFWNstep_Cnt_u16	1076
k_AsstFWPstep_Cnt_u16	3936
k RestoreThresh MtrNm f32	4.1999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2 AsstFWUprBoundX HwNm s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2 AsstFWUprBoundX HwNm s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288
	,



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2 AsstFWUprBoundX HwNm s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstrWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
t2_Asst WopfboundX_HwNm_s4p11[5][1]	2048
t2_AsstrWUprBoundX_HwNm_s4p11[5][2]	4096
	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3] t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_Asst WopiBoundX_HwNm_s4p11[7][4]	4096
t2_AsstrWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
tz_AsstFWUprBoundX_HWNm_s4p11[7][6] t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-32768



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-32768
	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-32768
	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-32768
	1 11
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-32768
:2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	
E 7.00% TO ONE OWING ENTREED BY THE TOTAL	
	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-32768 -32768
i2_AsstFWUprBoundY_MtrNm_s4p11[6][0] i2_AsstFWUprBoundY_MtrNm_s4p11[6][1] i2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-32768 -32768 -32768
i2_AsstFWUprBoundY_MtrNm_s4p11[6][0] i2_AsstFWUprBoundY_MtrNm_s4p11[6][1] i2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-32768 -32768
i2_AsstFWUprBoundY_MtrNm_s4p11[6][0] i2_AsstFWUprBoundY_MtrNm_s4p11[6][1] i2_AsstFWUprBoundY_MtrNm_s4p11[6][2] i2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-32768 -32768 -32768
i2_AsstFWUprBoundY_MtrNm_s4p11[6][0] i2_AsstFWUprBoundY_MtrNm_s4p11[6][1] i2_AsstFWUprBoundY_MtrNm_s4p11[6][2] i2_AsstFWUprBoundY_MtrNm_s4p11[6][3] i2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-32768 -32768 -32768 -32768
i2_AsstFWUprBoundY_MtrNm_s4p11[6][0] i2_AsstFWUprBoundY_MtrNm_s4p11[6][1] i2_AsstFWUprBoundY_MtrNm_s4p11[6][2] i2_AsstFWUprBoundY_MtrNm_s4p11[6][3] i2_AsstFWUprBoundY_MtrNm_s4p11[6][4] i2_AsstFWUprBoundY_MtrNm_s4p11[6][4] i2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-32768 -32768 -32768 -32768 -32768 -32768
12_AsstFWUprBoundY_MtrNm_s4p11[6][0] 12_AsstFWUprBoundY_MtrNm_s4p11[6][1] 12_AsstFWUprBoundY_MtrNm_s4p11[6][2] 12_AsstFWUprBoundY_MtrNm_s4p11[6][3] 12_AsstFWUprBoundY_MtrNm_s4p11[6][4] 12_AsstFWUprBoundY_MtrNm_s4p11[6][5] 12_AsstFWUprBoundY_MtrNm_s4p11[6][5] 12_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768
12_AsstFWUprBoundY_MtrNm_s4p11[6][0] 12_AsstFWUprBoundY_MtrNm_s4p11[6][1] 12_AsstFWUprBoundY_MtrNm_s4p11[6][2] 12_AsstFWUprBoundY_MtrNm_s4p11[6][3] 12_AsstFWUprBoundY_MtrNm_s4p11[6][4] 12_AsstFWUprBoundY_MtrNm_s4p11[6][5] 12_AsstFWUprBoundY_MtrNm_s4p11[6][6] 12_AsstFWUprBoundY_MtrNm_s4p11[6][6] 12_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768
12_AsstFWUprBoundY_MtrNm_s4p11[6][0] 12_AsstFWUprBoundY_MtrNm_s4p11[6][1] 12_AsstFWUprBoundY_MtrNm_s4p11[6][2] 12_AsstFWUprBoundY_MtrNm_s4p11[6][3] 12_AsstFWUprBoundY_MtrNm_s4p11[6][4] 12_AsstFWUprBoundY_MtrNm_s4p11[6][5] 12_AsstFWUprBoundY_MtrNm_s4p11[6][6] 12_AsstFWUprBoundY_MtrNm_s4p11[6][6] 12_AsstFWUprBoundY_MtrNm_s4p11[6][7] 12_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768
12_AsstFWUprBoundY_MtrNm_s4p11[6][0] 12_AsstFWUprBoundY_MtrNm_s4p11[6][1] 12_AsstFWUprBoundY_MtrNm_s4p11[6][2] 12_AsstFWUprBoundY_MtrNm_s4p11[6][3] 12_AsstFWUprBoundY_MtrNm_s4p11[6][4] 12_AsstFWUprBoundY_MtrNm_s4p11[6][5] 12_AsstFWUprBoundY_MtrNm_s4p11[6][6] 12_AsstFWUprBoundY_MtrNm_s4p11[6][7] 12_AsstFWUprBoundY_MtrNm_s4p11[6][7] 12_AsstFWUprBoundY_MtrNm_s4p11[6][8] 12_AsstFWUprBoundY_MtrNm_s4p11[6][8]	-32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	-32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	-32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	-32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768
12_AsstFWUprBoundY_MtrNm_s4p11[6][0] 12_AsstFWUprBoundY_MtrNm_s4p11[6][1] 12_AsstFWUprBoundY_MtrNm_s4p11[6][2] 12_AsstFWUprBoundY_MtrNm_s4p11[6][3] 12_AsstFWUprBoundY_MtrNm_s4p11[6][4] 12_AsstFWUprBoundY_MtrNm_s4p11[6][5] 12_AsstFWUprBoundY_MtrNm_s4p11[6][6] 12_AsstFWUprBoundY_MtrNm_s4p11[6][7] 12_AsstFWUprBoundY_MtrNm_s4p11[6][8] 12_AsstFWUprBoundY_MtrNm_s4p11[6][9] 12_AsstFWUprBoundY_MtrNm_s4p11[6][9] 12_AsstFWUprBoundY_MtrNm_s4p11[6][10] 12_AsstFWUprBoundY_MtrNm_s4p11[7][0] 12_AsstFWUprBoundY_MtrNm_s4p11[7][0] 12_AsstFWUprBoundY_MtrNm_s4p11[7][1] 12_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768



Name	Inc. 4 Malica
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-32768 -32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	-32768
t_AsstFWDefltAssistX_HwNm_u8p8[0]	819
t_AsstFWDefitAssistX_HwNm_u8p8[1]	845
t_AsstFWDefitAssistX_HwNm_u8p8[2]	870
t_AsstFWDefitAssistX_HwNm_u8p8[3]	896
t_AsstFWDefltAssistX_HwNm_u8p8[4]	922
t_AsstFWDefltAssistX_HwNm_u8p8[5]	947
t_AsstFWDefltAssistX_HwNm_u8p8[6]	973
t_AsstFWDefltAssistX_HwNm_u8p8[7]	998
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1101
t AsstFWDefltAssistX HwNm u8p8[12]	1126
t_AsstFWDefitAssistX_HwNm_u8p8[13]	1152
t_AsstFWDefitAssistX_HwNm_u8p8[14]	1178
t_AsstFWDefitAssistX_HwNm_u8p8[15]	1203
t_AsstFWDefitAssistX_HwNm_u8p8[16]	1229
t AsstFWDefltAssistX HwNm u8p8[17]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1280
t_AsstFWDefitAssistX_HwNm_u8p8[19]	1306
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	9216
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	9421
t_AsstFWDefitAssistY_MtrNm_s4p11[6]	9626
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	9830
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	10035
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	11264
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	11674
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	12288
t_AsstFWPstepNstepThresh_Cnt_u16[0]	153
t_AsstFWPstepNstepThresh_Cnt_u16[1]	331
t_AsstFWVehSpd_Kph_u9p7[0]	16128
t_AsstFWVehSpd_Kph_u9p7[1]	16256
t_AsstFWVehSpd_Kph_u9p7[2]	16384
t_AsstFWVehSpd_Kph_u9p7[3]	16512
t_AsstFWVehSpd_Kph_u9p7[4]	16640
t_AsstFWVehSpd_Kph_u9p7[5]	16768
t_AsstFWVehSpd_Kph_u9p7[6]	16896
t_AsstFWVehSpd_Kph_u9p7[7]	17024
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-9
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90.1999969
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt lo	tgt_assist-irewaii_peri_deteat_asstidi Service Unt igc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Itgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall Per1_HighFreqAssist_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Itgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_Deteat_Assit bl_Service_Cnt_igc  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.03400004	1.03400004 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	331	331 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6	-6 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.93599987	7.93599987 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.57599974	4.57600021 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-4.5	-4.5 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-6	-6 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

lacksquare				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.33 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall ActiveKSV M str.K Uls f32	0.070000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1599
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	-2.70000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.090000036
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.05999994
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.0500000007
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.600000024
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1
k AsstFWInpLimitHFA MtrNm f32	5.19999981
k_AsstFWInpLimitHysComp_MtrNm_f32	0.230000004
k_AsstFWNstep_Cnt_u16	952
k_AsstFWPstep_Cnt_u16	4059
k RestoreThresh MtrNm f32	4.30000019
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
t2 AsstFWUprBoundX HwNm s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
:2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
:2_AsstFWUprBoundX_HwNm_s4p11[6][4]	
	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	32767
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	32767
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	32767
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	32767
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	32767



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	32767	
	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]		
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	32767	
	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	32767	
t2 AsstFWUprBoundY MtrNm s4n11[7][1]	32/6/	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	32767 32767	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	32767 32767 32767	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	32767
t_AsstFWDefltAssistX_HwNm_u8p8[0]	845
t_AsstFWDefltAssistX_HwNm_u8p8[1]	870
t_AsstFWDefltAssistX_HwNm_u8p8[2]	896
t_AsstFWDefltAssistX_HwNm_u8p8[3]	922
t_AsstFWDefltAssistX_HwNm_u8p8[4]	947
t_AsstFWDefltAssistX_HwNm_u8p8[5]	973
t_AsstFWDefltAssistX_HwNm_u8p8[6]	998
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	1178 1203
t_AsstFWDefitAssistX_HwNm_u8p8[14] t_AsstFWDefitAssistX_HwNm_u8p8[15]	1229
t_AsstFWDefitAssistX_HwNm_u8p8[16]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1331
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	12288
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	12493
t_AsstFWPstepNstepThresh_Cnt_u16[0]	154
t_AsstFWPstepNstepThresh_Cnt_u16[1]	335
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	19200 19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
t_AsstFWVehSpd_Kph_u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.099999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	11.3000002
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFirewal$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.046	2.046 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	335	335 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.20019531	4.20019531 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.21070004	1.21070004 ± 4.88E-04	<b>~</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.04502439	4.04502439 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	12.7997074	12.7997074 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4.20019531	4.20019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T ·				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.34 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4
AssistFirewall ActiveKSV M str.K Uls f32	0.0799999982
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1722
AssistFirewall AsstReducedPerfSV Cnt M Igc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-2.79999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00800000038
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.07000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0599999987
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.10000002
k_AsstFWInpLimitHFA_MtrNm_f32	5.4000001
k_AsstFWInpLimitHysComp_MtrNm_f32	0.430000007
k_AsstFWNstep_Cnt_u16	828
k_AsstFWPstep_Cnt_u16	4182
k_RestoreThresh_MtrNm_f32	4.400001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2 AsstFWUprBoundX HwNm s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	
	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	0
2_1.00OpiDodiid 1_initi 111_04p 1 1[0][1]	1



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
	0
t2 AsstEWUnrBoundY MtrNm s4n11[6][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	0
	0 0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0 0 0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0 0 0 0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0 0 0



	(
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
12_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
12_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
12_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	0
t_AsstFWDefltAssistX_HwNm_u8p8[0]	870
t_AsstFWDefltAssistX_HwNm_u8p8[1]	896
t_AsstFWDefltAssistX_HwNm_u8p8[2]	922
t_AsstFWDefltAssistX_HwNm_u8p8[3]	947
t_AsstFWDefltAssistX_HwNm_u8p8[4]	973
t_AsstFWDefltAssistX_HwNm_u8p8[5]	998
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1254
t AsstFWDefltAssistX HwNm u8p8[16]	1280
t AsstFWDefltAssistX HwNm u8p8[17]	1306
t_AsstFWDefitAssistX_HwNm_u8p8[18]	1331
t_AsstFWDefitAssistX_HwNm_u8p8[19]	1357
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	8806
t_AsstFWDefitAssistY_MtrNm_s4p11[1]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	12698
t_AsstFWPstepNstepThresh_Cnt_u16[0]	155
t_AsstFWPstepNstepThresh_Cnt_u16[1]	339
t_AsstFWVehSpd_Kph_u9p7[0]	22016
t_AsstFWVehSpd_Kph_u9p7[1]	22144
t_Asstrwverispd_kpin_usp7[1] t_AsstFWVehSpd_Kph_u9p7[2]	22272
t_AsstFWVehSpd_Kph_u9p7[2] t_AsstFWVehSpd_Kph_u9p7[3]	22400
t_Asstrwvenspd_kpn_usp7[3] t_AsstFWVehSpd_Kph_u9p7[4]	22528
t_AsstFWVehSpd_Kph_u9p7[5]	22656
t_AsstFWVehSpd_Kph_u9p7[6]	22784
t_AsstFWVehSpd_Kph_u9p7[7]	22912
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3.099999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tet AssistFirewall Dord VahialaCased Kah (22 value	22.1000004
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	tot AssistFirewell Bord AsstFirewellAstive IIIs 422
tgt_Assistrirewaii_rei1_veriicleSpeed_kpri_i32.value tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	1
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.68000007	3.68000007 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	339	339 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.29980469	-4.29980469 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.21864009	2.21864009 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.73399973	5.73400021 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.03400004	1.03400004 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-4.29980469	-4.29980469 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.35 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	5
AssistFirewall ActiveKSV M str.K Uls f32	0.090000036
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1845
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	-2.9000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00899999961
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.08000004
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0700000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0700000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	5.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	3.48000002
k_AsstFWNstep_Cnt_u16	704
k_AsstFWPstep_Cnt_u16	4305
k_RestoreThresh_MtrNm_f32	4.5
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
12_Asst WorlboundX_TWNII_s4p11[5][4] 12_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7] t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288
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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9] t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432 20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10] t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	12288 14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288 14336 16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288 14336 16384 18432 20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	12288 14336 16384 18432 20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	12288 14336 16384 18432 20480 0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	12288 14336 16384 18432 20480 0 2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	12288 14336 16384 18432 20480 0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288 14336 16384 18432 20480 0 2048 4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	12288 14336 16384 18432 20480 0 2048 4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288 14336 16384 18432 20480 0 2048 4096 6144 8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288 14336 16384 18432 20480 0 2048 4096 6144 8192 10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288 14336 16384 18432 20480 0 2048 4096 6144 8192 10240 12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	12288 14336 16384 18432 20480 0 2048 4096 6144 8192 10240 12288 14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	12288 14336 16384 18432 20480 0 2048 4096 6144 8192 10240 12288 14336 16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288 14336 16384 18432 20480 0 2048 4096 6144 8192 10240 12288 14336 16384 18432 20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288 14336 16384 18432 20480 0 2048 4096 6144 8192 10240 12288 14336 16384 18432 20480 0



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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	896
t_AsstFWDefltAssistX_HwNm_u8p8[1]	922
t_AsstFWDefltAssistX_HwNm_u8p8[2]	947
t_AsstFWDefltAssistX_HwNm_u8p8[3]	973
t_AsstFWDefltAssistX_HwNm_u8p8[4]	998
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1382
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	12698
t_AsstFWDeftrAssistY_MtrNm_s4p11[19]	12902
t_AsstFWPstepNstepThresh_Cnt_u16[0]	156
t_AsstFWPstepNstepThresh_Cnt_u16[1]	343
t_AsstFWVehSpd_Kph_u9p7[0]	24960
t_AsstFWVehSpd_Kph_u9p7[1]	25088 25216
t_AsstFWVehSpd_Kph_u9p7[2]	
t_AsstFWVehSpd_Kph_u9p7[3] t AsstFWVehSpd Kph u9p7[4]	25344
	25472
t_AsstFWVehSpd_Kph_u9p7[5] t_AsstFWVehSpd_Kph_u9p7[6]	25600 25728
t_AsstFWVehSpd_Kph_u9p7[7] tqt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	25856
tgt_AssistFirewall_Per1_BaseAssistCmd_intrinm_132.value  tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_Deteat_Assist_bt_Service_Cnt_igc.value  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4.0999999
tgt_AssistFirewail_Per1_HighFreqAssist_MtrNm_f32.value  tgt_AssistFirewail_Per1_HwTorque_HwNm_f32.value	4.03999999
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	33.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_inst_Ap_AssistFirewali.AssistFirewali_Per1_AsstFirewaliActive_Uis_132 tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_132	tgt_AssistFirewall_Per1_Asstr-IrewallActive_Uis_132 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_inst_Ap_AssistFireWall.AssistFireWall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_inst_Ap_AssistFireWall.AssistFireWall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_wtrNm_r32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_r32
tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_Assist_Mit/Nffi_i32  tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_l	1
tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_beleat_AssistDi_service_Crit_i tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_intf\tilifi1i32 tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32
J	0



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4.55000019	4.55000019 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	343	343 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.39990234	-4.39990234 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.05022001	4.05022001 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.370000005	0.370000005 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.18600011	2.18600011 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-4.39990234	-4.39990234 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Τ				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.36 (Repeat Count = 1)		
Name	Input Value	
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6	
AssistFirewall ActiveKSV M str.K Uls f32	0.00499999989	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1968	
AssistFirewall AsstReducedPerfSV Cnt M lqc	1	
AssistFirewall_CombAsstSV_MtrNm_M_f32	2.0999999	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0099999978	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.09000003	
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0799999982	
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4	
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0799999982	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.0999999	
k_AsstFWInpLimitHFA_MtrNm_f32	5.80000019	
k_AsstFWInpLimitHysComp_MtrNm_f32	3.82999992	
k_AsstFWNstep_Cnt_u16	580	
k_AsstFWPstep_Cnt_u16	4428	
k_RestoreThresh_MtrNm_f32	4.5999999	
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336	
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288	
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096	



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240 -8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-14336
	-14336 -12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	
t2 AcctEM/IntRoundV MtrNm c4n44[0][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-10240 -8192



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-16384 -14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4] t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2046
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-14336



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	-2048
t_AsstFWDefltAssistX_HwNm_u8p8[0]	922
t_AsstFWDefltAssistX_HwNm_u8p8[1]	947
t_AsstFWDefltAssistX_HwNm_u8p8[2]	973
t_AsstFWDefltAssistX_HwNm_u8p8[3]	998
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1382
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1408
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	13107
t_AsstFWPstepNstepThresh_Cnt_u16[0]	157
t_AsstFWPstepNstepThresh_Cnt_u16[1]	347
t_AsstFWVehSpd_Kph_u9p7[0]	27904
t_AsstFWVehSpd_Kph_u9p7[1]	28032 28160
t_AsstFWVehSpd_Kph_u9p7[2]	
t_AsstFWVehSpd_Kph_u9p7[3] t AsstFWVehSpd Kph u9p7[4]	28288
	28416 28544
t_AsstFWVehSpd_Kph_u9p7[5] t_AsstFWVehSpd_Kph_u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7] tqt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	28800
tgt_AssistFirewall_Per1_BaseAssistCmd_intrinm_132.value  tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_Deteat_Assist_bt_Service_Cnt_igc.value  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999
tgt_AssistFirewail_Per1_HighFreqAssist_MtrNm_f32.value  tgt_AssistFirewail_Per1_HwTorque_HwNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	44.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_DaseAssistCinio_MithInf_i32 tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_Assist_Mit/Nffi_i32  tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_l	•
tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_beleat_AssistDi_service_Crit_i tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_intf\tilifi1i32 tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32
J	0 =



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.96999979	5.96999979 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	347	347 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.89990234	4.89990234 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.03299999	5.03299999 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.63999987	2.6400001 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.51999998	3.51999998 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4.89990234	4.89990234 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.37 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6
AssistFirewall ActiveKSV M str.K Uls f32	0.0700000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	3321
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	-3.2999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.900001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0099999978
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0500000007
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-16
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00800000038
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.70000005
k_AsstFWInpLimitHFA_MtrNm_f32	8
k_AsstFWInpLimitHysComp_MtrNm_f32	0.430000007
k_AsstFWNstep_Cnt_u16	4305
k_AsstFWPstep_Cnt_u16	861
k_RestoreThresh_MtrNm_f32	5.69999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2 AsstFWUprBoundX HwNm s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-26624
	-24576
t2 AsstFWUnrBoundY MtrNm s4n11[0][3]	27070
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-22528 -20480
	-22528 -20480 -18432



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6] t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8] t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144



Input Value
8192
10240
12288
14336
16384
18432
20480
947
973
998
1024
1050
1075
1101
1126
1152
1178
1203
1229
1254
1280
1306
1331
1357
1382
1408
1434
9421
9626
9830
10035
10240
10445
10650
10854
11059
11264
11469
11674
11878
12083
12288
12493
12698
12902
13107
13312
158
351
30848
30976
31104
31232
31360
31488
31616
31744
6.0999999
0
3.0999999
-8
3.0999999
0
40.0999985
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igc
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.57999992	5.57999992 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	351	351 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6.5	-6.5 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.89330006	6.89330006 ± 4.88E-04	<b>~</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.09499979	5.09499979 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-15.9919996	-15.9919996 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-6.5	-6.5 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>~</b>

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.38 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5
AssistFirewall ActiveKSV M str.K Uls f32	0.079999982
AssistFirewall_ActiveRawAcc_Cnt_M_u16	3444
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	-3.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0199999996
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.02999997
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	15.9995003
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00899999961
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6
k_AsstFWInpLimitHFA_MtrNm_f32	1.29999995
k_AsstFWInpLimitHysComp_MtrNm_f32	3.48000002
k_AsstFWNstep_Cnt_u16	4428
k_AsstFWPstep_Cnt_u16	984
k_RestoreThresh_MtrNm_f32	5.80000019
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-16384
	111



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096	
	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]		
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288	
	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-30720	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-28672	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	8192	



	(14 11 10 10
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	22528
t_AsstFWDefltAssistX_HwNm_u8p8[0]	77
t_AsstFWDefltAssistX_HwNm_u8p8[1]	102
t_AsstFWDefltAssistX_HwNm_u8p8[2]	128
t_AsstFWDefltAssistX_HwNm_u8p8[3]	154
t_AsstFWDefltAssistX_HwNm_u8p8[4]	179
t_AsstFWDefltAssistX_HwNm_u8p8[5]	205
t_AsstFWDefltAssistX_HwNm_u8p8[6]	230
t_AsstFWDefltAssistX_HwNm_u8p8[7]	256
t_AsstFWDefltAssistX_HwNm_u8p8[8]	282
t_AsstFWDefltAssistX_HwNm_u8p8[9]	307
t_AsstFWDefltAssistX_HwNm_u8p8[10]	333
t_AsstFWDefltAssistX_HwNm_u8p8[11]	358
t_AsstFWDefItAssistX_HwNm_u8p8[12]	384
t_AsstFWDefltAssistX_HwNm_u8p8[13]	410
t_AsstFWDefltAssistX_HwNm_u8p8[14]	435
t AsstFWDefltAssistX HwNm u8p8[15]	461
t AsstFWDefltAssistX HwNm u8p8[16]	486
t_AsstFWDefitAssistX_HwNm_u8p8[17]	512
t_AsstFWDefltAssistX_HwNm_u8p8[18]	538
t_AsstFWDefltAssistX_HwNm_u8p8[19]	563
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	11059
	11264
t_AsstFWDeftAssistY_MtrNm_s4p11[8]	
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	13517
t_AsstFWPstepNstepThresh_Cnt_u16[0]	159
t_AsstFWPstepNstepThresh_Cnt_u16[1]	355
t_AsstFWVehSpd_Kph_u9p7[0]	33792
t_AsstFWVehSpd_Kph_u9p7[1]	33920
t_AsstFWVehSpd_Kph_u9p7[2]	34048
t_AsstFWVehSpd_Kph_u9p7[3]	34176
t AsstFWVehSpd Kph u9p7[4]	34304
	34432
t_AsstFWVehSpd_Kph_u9p7[5]	
t_AsstFWVehSpd_Kph_u9p7[6]	34560
t_AsstFWVehSpd_Kph_u9p7[7]	34688
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-9
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	50.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
•	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
•	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_le	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lq	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_letgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lqtgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4.5999999	4.5999999 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	355	355 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6.60009766	-6.60009766 ± 4.88E-04	<b>~</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.58560002	1.58560002 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.97399998	5.97399998 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	15.7295046	15.7295046 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-6.60009766	-6.60009766 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	<b>~</b>
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Τ				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.39 (Repeat Count = 1)	v
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5
AssistFirewall ActiveKSV M str.K Uls f32	0.090000036
AssistFirewall_ActiveRawAcc_Cnt_M_u16	3567
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.029999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.03999996
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0700000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	0
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0099999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	8
k_AsstFWInpLimitHFA_MtrNm_f32	2.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	0.10000001
k_AsstFWNstep_Cnt_u16	4551
k_AsstFWPstep_Cnt_u16	1107
k_RestoreThresh_MtrNm_f32	5.9000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384



	( - # - 10-10
Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_Asst WopiboundX_1WNIII_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144
t2_Asst WopiboundX_1WNIII_s4p11[5][0] t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096
	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2 AsstFWUprBoundX HwNm s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
12_Asst WopiBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-20480
iz_Assii Wopibodiidi_Militiii_s+pii[o][o]	
	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-18432 -16384



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	4096
42 Appt [MI   p p D c cond.] Marking a 4 p 4 4 [7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	8192



	(
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576
t_AsstFWDefltAssistX_HwNm_u8p8[0]	26
t_AsstFWDefltAssistX_HwNm_u8p8[1]	51
t_AsstFWDefltAssistX_HwNm_u8p8[2]	77
t_AsstFWDefltAssistX_HwNm_u8p8[3]	102
t_AsstFWDefltAssistX_HwNm_u8p8[4]	128
t_AsstFWDefltAssistX_HwNm_u8p8[5]	154
t_AsstFWDefltAssistX_HwNm_u8p8[6]	179
t_AsstFWDefltAssistX_HwNm_u8p8[7]	205
t_AsstFWDefltAssistX_HwNm_u8p8[8]	230
t_AsstFWDefltAssistX_HwNm_u8p8[9]	256
t_AsstFWDefltAssistX_HwNm_u8p8[10]	282
t_AsstFWDefltAssistX_HwNm_u8p8[11]	307
t_AsstFWDefltAssistX_HwNm_u8p8[12]	333
t_AsstFWDefltAssistX_HwNm_u8p8[13]	358
t_AsstFWDefltAssistX_HwNm_u8p8[14]	384
t_AsstFWDefltAssistX_HwNm_u8p8[15]	410
t_AsstFWDefltAssistX_HwNm_u8p8[16]	435
t_AsstFWDefltAssistX_HwNm_u8p8[17]	461
t_AsstFWDefltAssistX_HwNm_u8p8[18]	486
t_AsstFWDefltAssistX_HwNm_u8p8[19]	512
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	13722
t_AsstFWPstepNstepThresh_Cnt_u16[0]	160
t_AsstFWPstepNstepThresh_Cnt_u16[1]	359
t_AsstFWVehSpd_Kph_u9p7[0]	36736
t_AsstFWVehSpd_Kph_u9p7[1]	36864
t_AsstFWVehSpd_Kph_u9p7[2]	36992
t_AsstFWVehSpd_Kph_u9p7[3]	37120
t_AsstFWVehSpd_Kph_u9p7[4]	37248
t_AsstFWVehSpd_Kph_u9p7[5]	37376
t_AsstFWVehSpd_Kph_u9p7[6]	37504
t_AsstFWVehSpd_Kph_u9p7[7]	37632
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	60.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lawerserve$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-4.55000019	-4.55000019 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	359	359 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.70019531	5.70019531 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.97900009	4.97900009 ± 4.88E-04	<b>~</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.72300005	4.72300005 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-0.109999999	-0.109999999 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	5.70019531	5.70019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>~</b>

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.40 (Repeat Count = 1)	ranga kanangan kanan
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	1
AssistFirewall ActiveKSV M str.K Uls f32	0.0599999987
AssistFirewall ActiveRawAcc Cnt M u16	3690
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.039999991
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.04999995
AssistFirewall LwrBoundKSV M str.SV Uls f32	5.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0799999982
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0199999996
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	7
k_AsstFWInpLimitHFA_MtrNm_f32	1.3999998
k_AsstFWInpLimitHysComp_MtrNm_f32	1.10000002
k_AsstFWNstep_Cnt_u16	4674
k_AsstFWPstep_Cnt_u16	1230
k_RestoreThresh_MtrNm_f32	6
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336
= , , , , = = = 1	1



	(
Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4] t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
t2 AsstFWUprBoundX HwNm s4p11[5][10]	16384
t2_AsstrWUprBoundX_HwNm_s4p11[3][10]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-14336 -12288



-8192 -6144
-6144
-4096
2048
4096
6144
8192
10240
12288
14336
16384
18432
20480
22528
-2048
0
2048
4096
6144
8192
10240
12288
14336
16384
18432
2048
4096
6144
8192
10240
12288
14336
16384
18432
20480
22528
-2048
0
2048
4096
6144
8192
10240
12288
14336
16384
18432



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	51
t_AsstFWDefltAssistX_HwNm_u8p8[1]	77
t_AsstFWDefltAssistX_HwNm_u8p8[2]	102
t_AsstFWDefltAssistX_HwNm_u8p8[3]	128
t_AsstFWDefltAssistX_HwNm_u8p8[4]	154
t_AsstFWDefltAssistX_HwNm_u8p8[5]	179
t_AsstFWDefltAssistX_HwNm_u8p8[6]	205
t_AsstFWDefltAssistX_HwNm_u8p8[7]	230
t_AsstFWDefltAssistX_HwNm_u8p8[8]	256
t_AsstFWDefltAssistX_HwNm_u8p8[9]	282
t_AsstFWDefltAssistX_HwNm_u8p8[10]	307
t_AsstFWDefltAssistX_HwNm_u8p8[11]	333
t_AsstFWDefltAssistX_HwNm_u8p8[12]	358
t_AsstFWDefltAssistX_HwNm_u8p8[13]	384
t_AsstFWDefltAssistX_HwNm_u8p8[14]	410
t_AsstFWDefltAssistX_HwNm_u8p8[15]	435
t_AsstFWDefltAssistX_HwNm_u8p8[16]	461
t_AsstFWDefltAssistX_HwNm_u8p8[17]	486
t_AsstFWDefltAssistX_HwNm_u8p8[18]	512
t_AsstFWDefltAssistX_HwNm_u8p8[19]	538
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[12] t AsstFWDefltAssistY_MtrNm_s4p11[13]	12493 12698
	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[15] t_AsstFWDefltAssistY_MtrNm_s4p11[16]	13312
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	13517
t AsstFWDefitAssistY MtrNm s4p11[18]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	13926
t_AsstFWPstepNstepThresh_Cnt_u16[0]	161
t_AsstFWPstepNstepThresh_Cnt_u16[1]	363
t_AsstFWVehSpd_Kph_u9p7[0]	39680
t_AsstFWVehSpd_Kph_u9p7[1]	39808
t_AsstFWVehSpd_Kph_u9p7[2]	39936
t_AsstFWVehSpd_Kph_u9p7[3]	40064
t_AsstFWVehSpd_Kph_u9p7[4]	40192
t_AsstFWVehSpd_Kph_u9p7[5]	40320
t_AsstFWVehSpd_Kph_u9p7[6]	40448
t_AsstFWVehSpd_Kph_u9p7[7]	40576
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	70.4000015
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_li	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32
-3sp reside wereaut toolet nettan_rest_vernoleopeed_repr_102	-2 "ona"- or one obsord this los



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.93999998	0.93999998 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	363	363 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6.70019531	-6.70019531 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-4.57999992	-4.57999992 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.4920001	5.4920001 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.1500001	5.1500001 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.93999998	0.939999998 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-6.70019531	-6.70019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.41 (Repeat Count = 1)		
Name	Input Value	
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2	
AssistFirewall ActiveKSV M str.K Uls f32	0.090000036	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	3813	
AssistFirewall AsstReducedPerfSV Cnt M lgc	1	
AssistFirewall CombAsstSV MtrNm M f32	-3.70000005	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.05999994	
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.099999	
AssistFirewall LwrBoundKSV M str.K Uls f32	0.090000036	
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.5	
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.20000003	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2	
k_AsstFWInpLimitHFA_MtrNm_f32	1.60000002	
k_AsstFWInpLimitHysComp_MtrNm_f32	1.3999998	
k_AsstFWNstep_Cnt_u16	3567	
k_AsstFWPstep_Cnt_u16	1353	
k RestoreThresh MtrNm f32	6.099999	
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432	
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384	
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336	
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288	
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384	
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288	





Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384	
	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]		
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144	
	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]		
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480	
	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288	
2 AsstFWUprBoundY MtrNm s4p11[5][3]		
	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]		
	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048 4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	2048 4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048 4096 6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]  2_AsstFWUprBoundY_MtrNm_s4p11[6][2]  2_AsstFWUprBoundY_MtrNm_s4p11[6][3]  2_AsstFWUprBoundY_MtrNm_s4p11[6][4]  2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048 4096 6144 8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]  2_AsstFWUprBoundY_MtrNm_s4p11[6][2]  2_AsstFWUprBoundY_MtrNm_s4p11[6][3]  2_AsstFWUprBoundY_MtrNm_s4p11[6][4]  2_AsstFWUprBoundY_MtrNm_s4p11[6][5]  2_AsstFWUprBoundY_MtrNm_s4p11[6][6]  2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048 4096 6144 8192 10240 12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]  2_AsstFWUprBoundY_MtrNm_s4p11[6][2]  2_AsstFWUprBoundY_MtrNm_s4p11[6][3]  2_AsstFWUprBoundY_MtrNm_s4p11[6][4]  2_AsstFWUprBoundY_MtrNm_s4p11[6][5]  2_AsstFWUprBoundY_MtrNm_s4p11[6][6]  2_AsstFWUprBoundY_MtrNm_s4p11[6][6]  2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048 4096 6144 8192 10240 12288 14336	
12_AsstFWUprBoundY_MtrNm_s4p11[6][1] 12_AsstFWUprBoundY_MtrNm_s4p11[6][2] 12_AsstFWUprBoundY_MtrNm_s4p11[6][3] 12_AsstFWUprBoundY_MtrNm_s4p11[6][4] 12_AsstFWUprBoundY_MtrNm_s4p11[6][5] 12_AsstFWUprBoundY_MtrNm_s4p11[6][6] 12_AsstFWUprBoundY_MtrNm_s4p11[6][6] 12_AsstFWUprBoundY_MtrNm_s4p11[6][7] 12_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048 4096 6144 8192 10240 12288 14336	
12_AsstFWUprBoundY_MtrNm_s4p11[6][1] 12_AsstFWUprBoundY_MtrNm_s4p11[6][2] 12_AsstFWUprBoundY_MtrNm_s4p11[6][3] 12_AsstFWUprBoundY_MtrNm_s4p11[6][4] 12_AsstFWUprBoundY_MtrNm_s4p11[6][5] 12_AsstFWUprBoundY_MtrNm_s4p11[6][6] 12_AsstFWUprBoundY_MtrNm_s4p11[6][7] 12_AsstFWUprBoundY_MtrNm_s4p11[6][7] 12_AsstFWUprBoundY_MtrNm_s4p11[6][8] 12_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048 4096 6144 8192 10240 12288 14336 16384	
12_AsstFWUprBoundY_MtrNm_s4p11[6][1] 12_AsstFWUprBoundY_MtrNm_s4p11[6][2] 12_AsstFWUprBoundY_MtrNm_s4p11[6][3] 12_AsstFWUprBoundY_MtrNm_s4p11[6][4] 12_AsstFWUprBoundY_MtrNm_s4p11[6][5] 12_AsstFWUprBoundY_MtrNm_s4p11[6][6] 12_AsstFWUprBoundY_MtrNm_s4p11[6][7] 12_AsstFWUprBoundY_MtrNm_s4p11[6][7] 12_AsstFWUprBoundY_MtrNm_s4p11[6][8] 12_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048 4096 6144 8192 10240 12288 14336	
12_AsstFWUprBoundY_MtrNm_s4p11[6][1] 12_AsstFWUprBoundY_MtrNm_s4p11[6][2] 12_AsstFWUprBoundY_MtrNm_s4p11[6][3] 12_AsstFWUprBoundY_MtrNm_s4p11[6][4] 12_AsstFWUprBoundY_MtrNm_s4p11[6][5] 12_AsstFWUprBoundY_MtrNm_s4p11[6][6] 12_AsstFWUprBoundY_MtrNm_s4p11[6][7] 12_AsstFWUprBoundY_MtrNm_s4p11[6][7] 12_AsstFWUprBoundY_MtrNm_s4p11[6][8] 12_AsstFWUprBoundY_MtrNm_s4p11[6][9] 12_AsstFWUprBoundY_MtrNm_s4p11[6][9] 12_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048 4096 6144 8192 10240 12288 14336 16384	
12_AsstFWUprBoundY_MtrNm_s4p11[6][1] 12_AsstFWUprBoundY_MtrNm_s4p11[6][2] 12_AsstFWUprBoundY_MtrNm_s4p11[6][3] 12_AsstFWUprBoundY_MtrNm_s4p11[6][4] 12_AsstFWUprBoundY_MtrNm_s4p11[6][5] 12_AsstFWUprBoundY_MtrNm_s4p11[6][6] 12_AsstFWUprBoundY_MtrNm_s4p11[6][7] 12_AsstFWUprBoundY_MtrNm_s4p11[6][8] 12_AsstFWUprBoundY_MtrNm_s4p11[6][9] 12_AsstFWUprBoundY_MtrNm_s4p11[6][9] 12_AsstFWUprBoundY_MtrNm_s4p11[6][10] 12_AsstFWUprBoundY_MtrNm_s4p11[6][10]	2048 4096 6144 8192 10240 12288 14336 16384 18432 20480	
L_asstFWUprBoundY_MtrNm_s4p11[6][1]  12_AsstFWUprBoundY_MtrNm_s4p11[6][2]  12_AsstFWUprBoundY_MtrNm_s4p11[6][3]  12_AsstFWUprBoundY_MtrNm_s4p11[6][4]  12_AsstFWUprBoundY_MtrNm_s4p11[6][5]  12_AsstFWUprBoundY_MtrNm_s4p11[6][6]  12_AsstFWUprBoundY_MtrNm_s4p11[6][7]  12_AsstFWUprBoundY_MtrNm_s4p11[6][8]  12_AsstFWUprBoundY_MtrNm_s4p11[6][9]  12_AsstFWUprBoundY_MtrNm_s4p11[6][9]  12_AsstFWUprBoundY_MtrNm_s4p11[6][10]  12_AsstFWUprBoundY_MtrNm_s4p11[7][0]  12_AsstFWUprBoundY_MtrNm_s4p11[7][0]  12_AsstFWUprBoundY_MtrNm_s4p11[7][1]  12_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048 4096 6144 8192 10240 12288 14336 16384 18432 20480 -2048	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	77
t_AsstFWDefltAssistX_HwNm_u8p8[1]	102
t_AsstFWDefltAssistX_HwNm_u8p8[2]	128
t_AsstFWDefltAssistX_HwNm_u8p8[3]	154
t_AsstFWDefltAssistX_HwNm_u8p8[4]	179 205
t_AsstFWDefltAssistX_HwNm_u8p8[5] t_AsstFWDefltAssistX_HwNm_u8p8[6]	230
t_AsstFWDefltAssistX_HwNm_u8p8[7]	256
t_AsstFWDefltAssistX_HwNm_u8p8[8]	282
t_AsstFWDefltAssistX_HwNm_u8p8[9]	307
t_AsstFWDefltAssistX_HwNm_u8p8[10]	333
t_AsstFWDefltAssistX_HwNm_u8p8[11]	358
t_AsstFWDefltAssistX_HwNm_u8p8[12]	384
t_AsstFWDefltAssistX_HwNm_u8p8[13]	410
t_AsstFWDefltAssistX_HwNm_u8p8[14]	435
t_AsstFWDefltAssistX_HwNm_u8p8[15]	461
t_AsstFWDefltAssistX_HwNm_u8p8[16]	486
t_AsstFWDefltAssistX_HwNm_u8p8[17]	512
t_AsstFWDefltAssistX_HwNm_u8p8[18]	538
t_AsstFWDefltAssistX_HwNm_u8p8[19]	563
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288 12493
t_AsstFWDefltAssistY_MtrNm_s4p11[11] t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12698
t_AsstFWDefitAssistY_MtrNm_s4p11[13]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	14131
t_AsstFWPstepNstepThresh_Cnt_u16[0]	162
t_AsstFWPstepNstepThresh_Cnt_u16[1]	367
t_AsstFWVehSpd_Kph_u9p7[0]	42624
t_AsstFWVehSpd_Kph_u9p7[1]	42752
t_AsstFWVehSpd_Kph_u9p7[2]	42880
t_AsstFWVehSpd_Kph_u9p7[3]	43008
t_AsstFWVehSpd_Kph_u9p7[4]	43136
t_AsstFWVehSpd_Kph_u9p7[5]	43264
t_AsstFWVehSpd_Kph_u9p7[6]	43392
t_AsstFWVehSpd_Kph_u9p7[7]	43520
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1 00 000005
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	80.099985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_kterner.  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFregAssist_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.81999993	1.82000005 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	367	367 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6.89990234	-6.89990234 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.14999998	1.14999998 ± 4.88E-04	<b>~</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.64099979	5.64099979 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.4000001	-5.4000001 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-6.89990234	-6.89990234 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.42 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3
AssistFirewall ActiveKSV M str.K Uls f32	0.10000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	3936
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.79999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0599999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.07000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.059999987
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00125584798
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1
k_AsstFWInpLimitHFA_MtrNm_f32	2
k_AsstFWInpLimitHysComp_MtrNm_f32	1.29999995
k_AsstFWNstep_Cnt_u16	3690
k_AsstFWPstep_Cnt_u16	1476
k_RestoreThresh_MtrNm_f32	6.19999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2 AsstFWUprBoundX HwNm s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2 AsstFWUprBoundX HwNm s4p11[6][3]	0
t2 AsstFWUprBoundX HwNm s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2 AsstFWUprBoundX HwNm s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2 AsstFWUprBoundX HwNm s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-16384
10. A - of FAMIL - D - or olly Marks	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-12288



News	Innuid Value
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	6144
	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144



	(
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	102
t_AsstFWDefltAssistX_HwNm_u8p8[1]	128
t_AsstFWDefltAssistX_HwNm_u8p8[2]	154
t_AsstFWDefltAssistX_HwNm_u8p8[3]	179
t_AsstFWDefltAssistX_HwNm_u8p8[4]	205
t_AsstFWDefltAssistX_HwNm_u8p8[5]	230
t_AsstFWDefltAssistX_HwNm_u8p8[6]	256
t_AsstFWDefltAssistX_HwNm_u8p8[7]	282
t_AsstFWDefltAssistX_HwNm_u8p8[8]	307
t_AsstFWDefltAssistX_HwNm_u8p8[9]	333
t_AsstFWDefltAssistX_HwNm_u8p8[10]	358
t_AsstFWDefltAssistX_HwNm_u8p8[11]	384
t_AsstFWDefltAssistX_HwNm_u8p8[12]	410
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	435 461
t_AsstFWDefitAssistX_HwNm_u8p8[14] t_AsstFWDefitAssistX_HwNm_u8p8[15]	486
t_AsstFWDefitAssistX_HwNm_u8p8[16]	512
t_AsstFWDefltAssistX_HwNm_u8p8[17]	538
t_AsstFWDefltAssistX_HwNm_u8p8[18]	563
t_AsstFWDefltAssistX_HwNm_u8p8[19]	589
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	14336
t_AsstFWPstepNstepThresh_Cnt_u16[0]	163
t_AsstFWPstepNstepThresh_Cnt_u16[1]	371
t_AsstFWVehSpd_Kph_u9p7[0]	45568
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	45696 45824
t_AsstFWVehSpd_Kph_u9p7[3]	45952
t AsstFWVehSpd Kph u9p7[4]	46080
t_AsstFWVehSpd_Kph_u9p7[5]	46208
t_AsstFWVehSpd_Kph_u9p7[6]	46336
t_AsstFWVehSpd_Kph_u9p7[7]	46464
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90.1999969
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFirewal$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.70000005	2.70000005 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	371	371 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	7	7 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.13800001	2.13800001 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.05999994	5.05999994 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	0.99874413	0.99874413 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	7	7 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4
AssistFirewall_ActiveKSV_M_str.SV_Uis_132	0.20000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4059
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1 -3.900001
AssistFirewall_CombAsstSV_MtrNm_M_f32	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0700000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.08000004
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.090000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.715390444
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
<_AsstFWInpLimitBaseAsst_MtrNm_f32	1.10000002
c_AsstFWInpLimitHFA_MtrNm_f32	4
C_AsstFWInpLimitHysComp_MtrNm_f32	2.0999999
c_AsstFWNstep_Cnt_u16	3813
C_AsstFWPstep_Cnt_u16	1599
c_RestoreThresh_MtrNm_f32	6.30000019
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192



	( =# := 10=10
Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_Asst WopiBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_Asst WopiBoundX_HwNm_s4p11[6][3]	2048
, , , , , , , , , , , , , , , , , , , ,	
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-18432
:2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-16384
t2_Asst WopiBoundY_MtrNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-14330
, 11 Upi Doung i Militin 3 TP   1   U    U	
	I <sub>-1</sub> 0240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-10240 -8102
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-10240 -8192 -6144



	1 1 1
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	20480
t2 AsstFWUprBoundY MtrNm s4p11[2][9]	22528
	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096
	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	8192



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	22528
t_AsstFWDefltAssistX_HwNm_u8p8[0]	128
t_AsstFWDefltAssistX_HwNm_u8p8[1]	154
t_AsstFWDefltAssistX_HwNm_u8p8[2]	179
t_AsstFWDefltAssistX_HwNm_u8p8[3]	205
t_AsstFWDefltAssistX_HwNm_u8p8[4]	230
t_AsstFWDefltAssistX_HwNm_u8p8[5]	256
t_AsstFWDefltAssistX_HwNm_u8p8[6]	282
t_AsstFWDefltAssistX_HwNm_u8p8[7]	307
t_AsstFWDefltAssistX_HwNm_u8p8[8]	333
t_AsstFWDefltAssistX_HwNm_u8p8[9]	358
t_AsstFWDefltAssistX_HwNm_u8p8[10]	384
t_AsstFWDefltAssistX_HwNm_u8p8[11]	410
t_AsstFWDefltAssistX_HwNm_u8p8[12]	435
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	461 486
t_AsstFWDefitAssistX_HwNm_u8p8[14] t_AsstFWDefitAssistX_HwNm_u8p8[15]	512
t_AsstFWDefltAssistX_HwNm_u8p8[16]	538
t_AsstFWDefltAssistX_HwNm_u8p8[17]	563
t_AsstFWDefltAssistX_HwNm_u8p8[18]	589
t_AsstFWDefltAssistX_HwNm_u8p8[19]	614
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	14131
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	14541
t_AsstFWPstepNstepThresh_Cnt_u16[0]	164
t_AsstFWPstepNstepThresh_Cnt_u16[1]	375
t_AsstFWVehSpd_Kph_u9p7[0]	1408
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	1536 1664
t_AsstFWVehSpd_Kph_u9p7[3]	1792
t_AsstFWVehSpd_Kph_u9p7[4]	1920
t_AsstFWVehSpd_Kph_u9p7[5]	2048
t_AsstFWVehSpd_Kph_u9p7[6]	2176
t_AsstFWVehSpd_Kph_u9p7[7]	2304
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	11.1000004
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFirewal$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.20000005	3.20000005 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	375	375 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.10009766	7.10009766 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.22399998	3.22399998 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.82562494	5.82562494 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.95528805	1.95528805 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	7.10009766	7.10009766 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.44 (Repeat Count = 1)	· ·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5
AssistFirewall ActiveKSV M str.K Uls f32	0.300000012
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4182
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.09000003
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.5
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.20000005
k_AsstFWInpLimitHFA_MtrNm_f32	5
k_AsstFWInpLimitHysComp_MtrNm_f32	2.29999995
k_AsstFWNstep_Cnt_u16	3936
k_AsstFWPstep_Cnt_u16	1722
k_RestoreThresh_MtrNm_f32	6.4000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
:2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-14336
t2_Asst WopiBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	4096
12_AsstFWUprBoundX_HwNm_s4p11[4][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-4096



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144	
	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]		
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048	
t2 AsstFWUprBoundY MtrNm s4p11[4][6]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0	
t2 AsstFWUprBoundY MtrNm s4p11[5][6]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	10240	



	(
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576
t_AsstFWDefltAssistX_HwNm_u8p8[0]	154
t_AsstFWDefltAssistX_HwNm_u8p8[1]	179
t_AsstFWDefltAssistX_HwNm_u8p8[2]	205
t_AsstFWDefltAssistX_HwNm_u8p8[3]	230
t_AsstFWDefltAssistX_HwNm_u8p8[4]	256
t_AsstFWDefltAssistX_HwNm_u8p8[5]	282
t_AsstFWDefltAssistX_HwNm_u8p8[6]	307
t_AsstFWDefltAssistX_HwNm_u8p8[7]	333
t_AsstFWDefltAssistX_HwNm_u8p8[8]	358
t_AsstFWDefltAssistX_HwNm_u8p8[9]	384
t_AsstFWDefltAssistX_HwNm_u8p8[10]	410
t_AsstFWDefltAssistX_HwNm_u8p8[11]	435
t_AsstFWDefltAssistX_HwNm_u8p8[12]	461
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	486 512
t_AsstFWDefitAssistX_HwNm_u8p8[14] t_AsstFWDefitAssistX_HwNm_u8p8[15]	538
t_AsstFWDefitAssistX_HwNm_u8p8[16]	563
t_AsstFWDefitAssistX_HwNm_u8p8[17]	589
t_AsstFWDefltAssistX_HwNm_u8p8[18]	614
t AsstFWDefltAssistX HwNm u8p8[19]	640
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	14746
t_AsstFWPstepNstepThresh_Cnt_u16[0]	165
t_AsstFWPstepNstepThresh_Cnt_u16[1]	379
t_AsstFWVehSpd_Kph_u9p7[0]	4352
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	4480 4608
t_AsstFWVehSpd_Kph_u9p7[3]	4736
t_AsstFWVehSpd_Kph_u9p7[4]	4864
t_AsstFWVehSpd_Kph_u9p7[5]	4992
t_AsstFWVehSpd_Kph_u9p7[6]	5120
t_AsstFWVehSpd_Kph_u9p7[7]	5248
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	22.3999996
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_legendering the property of th$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.5	3.5 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	379	379 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.20019531	7.20019531 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.28000021	4.28000021 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.9000001	6.9000001 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.5	2.5 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	7.20019531	7.20019531 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.45 (Repeat Count = 1)	Innut Value
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.400000006
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4305
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.090000036
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-8.80000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.200000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00499999989
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.20000005
k_AsstFWInpLimitHFA_MtrNm_f32	2
<_AsstFWInpLimitHysComp_MtrNm_f32	2.5
x_AsstFWNstep_Cnt_u16	4059
<pre>c_AsstFWPstep_Cnt_u16</pre>	1845
RestoreThresh MtrNm f32	6.5
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
	4096
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2 AsstFWUprBoundX HwNm s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240
	-8192 6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	0
op.20aa	17



	<u> </u>	
Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240	
t2 AsstFWUprBoundY MtrNm s4p11[2][9]	12288	
	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0	
, , , , , , , , , , , , , , , , , , , ,		
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	6144	
	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	12288	



	MACILAU
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	26624
t_AsstFWDefltAssistX_HwNm_u8p8[0]	179
t_AsstFWDefltAssistX_HwNm_u8p8[1]	205
t_AsstFWDefltAssistX_HwNm_u8p8[2]	230
t_AsstFWDefltAssistX_HwNm_u8p8[3]	256
t_AsstFWDefltAssistX_HwNm_u8p8[4]	282
t_AsstFWDefltAssistX_HwNm_u8p8[5]	307
t_AsstFWDefltAssistX_HwNm_u8p8[6]	333
t_AsstFWDefltAssistX_HwNm_u8p8[7]	358
t_AsstFWDefltAssistX_HwNm_u8p8[8]	384
t_AsstFWDefltAssistX_HwNm_u8p8[9]	410 435
t_AsstFWDefltAssistX_HwNm_u8p8[10]	461
t_AsstFWDefltAssistX_HwNm_u8p8[11] t_AsstFWDefltAssistX_HwNm_u8p8[12]	486
t AsstFWDefitAssistX HwNm u8p8[13]	512
t_AsstFWDefitAssistX_HwNm_u8p8[14]	538
t_AsstFWDefltAssistX_HwNm_u8p8[15]	563
t_AsstFWDefltAssistX_HwNm_u8p8[16]	589
t_AsstFWDefltAssistX_HwNm_u8p8[17]	614
t_AsstFWDefltAssistX_HwNm_u8p8[18]	640
t_AsstFWDefltAssistX_HwNm_u8p8[19]	666
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[17] t_AsstFWDefltAssistY_MtrNm_s4p11[18]	14541 14746
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	14950
t_AsstFWPstepNstepThresh_Cnt_u16[0]	166
t_AsstFWPstepNstepThresh_Cnt_u16[1]	383
t_AsstFWVehSpd_Kph_u9p7[0]	7296
t_AsstFWVehSpd_Kph_u9p7[1]	7424
t_AsstFWVehSpd_Kph_u9p7[2]	7552
t_AsstFWVehSpd_Kph_u9p7[3]	7680
t_AsstFWVehSpd_Kph_u9p7[4]	7808
t_AsstFWVehSpd_Kph_u9p7[5]	7936
t_AsstFWVehSpd_Kph_u9p7[6]	8064
t_AsstFWVehSpd_Kph_u9p7[7]	8192
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	33.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.5999999	3.5999999 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	383	383 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.29980469	7.29980469 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.0630002	5.0630002 ± 4.88E-04	<b>~</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.64000034	-5.63999987 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.99499989	3.99499989 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	7.29980469	7.29980469 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.46 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7
AssistFirewall ActiveKSV M str.K Uls f32	0.5
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4428
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00800000038
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.20000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8.80000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.300000012
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00600000005
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.5
k_AsstFWInpLimitHFA_MtrNm_f32	1
k_AsstFWInpLimitHysComp_MtrNm_f32	2.70000005
k_AsstFWNstep_Cnt_u16	4182
k_AsstFWPstep_Cnt_u16	1968
k_RestoreThresh_MtrNm_f32	6.599999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	2048



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-12288	
t2_AsstrWUprBoundY_MtrNm_s4p11[1][1]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-30720	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-28672	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144	
	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-30720	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-28672	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096	
t2_Asst WoprBoundY_MtrNm_s4p11[5][1]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0	
t2_Asst WoprBoundY_MtrNm_s4p11[5][4]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240	
t2_Asst WopiBoundY_MtrNm_s4p11[7][0]	8192	
	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	14336	



Moura	Innut Value
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5] t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	205
t_AsstFWDefltAssistX_HwNm_u8p8[1]	230
t_AsstFWDefltAssistX_HwNm_u8p8[2]	256
t_AsstFWDefltAssistX_HwNm_u8p8[3]	282
t_AsstFWDefltAssistX_HwNm_u8p8[4]	307
t_AsstFWDefltAssistX_HwNm_u8p8[5]	333
t_AsstFWDefltAssistX_HwNm_u8p8[6]	358
t_AsstFWDefltAssistX_HwNm_u8p8[7]	384
t_AsstFWDefltAssistX_HwNm_u8p8[8]	410
t_AsstFWDefltAssistX_HwNm_u8p8[9]	435
t_AsstFWDefltAssistX_HwNm_u8p8[10]	461
t_AsstFWDefltAssistX_HwNm_u8p8[11]	486
t_AsstFWDefltAssistX_HwNm_u8p8[12]	512
t_AsstFWDefltAssistX_HwNm_u8p8[13]	538
t_AsstFWDefltAssistX_HwNm_u8p8[14]	563
t_AsstFWDefltAssistX_HwNm_u8p8[15]	589
t_AsstFWDefltAssistX_HwNm_u8p8[16]	614
t_AsstFWDefltAssistX_HwNm_u8p8[17]	640
t_AsstFWDefltAssistX_HwNm_u8p8[18]	666
t_AsstFWDefltAssistX_HwNm_u8p8[19]	691
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	11264 11469
t_AsstFWDefitAssistY_MtrNm_s4p11[1]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[2] t_AsstFWDefltAssistY_MtrNm_s4p11[3]	11878
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	12083
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	15155
t_AsstFWPstepNstepThresh_Cnt_u16[0]	167
t_AsstFWPstepNstepThresh_Cnt_u16[1]	387
t_AsstFWVehSpd_Kph_u9p7[0]	10240
t_AsstFWVehSpd_Kph_u9p7[1]	10368
t_AsstFWVehSpd_Kph_u9p7[2]	10496
t_AsstFWVehSpd_Kph_u9p7[3]	10624
t_AsstFWVehSpd_Kph_u9p7[4]	10752
t_AsstFWVehSpd_Kph_u9p7[5]	10880
t_AsstFWVehSpd_Kph_u9p7[6]	11008
t_AsstFWVehSpd_Kph_u9p7[7]  tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	11136 1.10000002
tgt_AssistFirewall_Per1_Defeat_AssistCmd_intinfm_i32.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-6
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	44.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_le	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
• • • • •	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_Assisti ilewaii_Fei1_11w10ique_11w1tii1_132
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.5	3.5 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	387	387 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.39990234	-7.39990234 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.99039984	5.99039984 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.96000004	4.96000004 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.93400002	4.93400002 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.39990234	-7.39990234 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

lacksquare				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.47 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8
AssistFirewall ActiveKSV M str.K Uls f32	0.600000024
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4551
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00899999961
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.29999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0
AssistFirewall LwrBoundKSV M str.K Uls f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00700000022
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.60000002
k_AsstFWInpLimitHFA_MtrNm_f32	4
k_AsstFWInpLimitHysComp_MtrNm_f32	2.9000001
k_AsstFWNstep_Cnt_u16	4305
k_AsstFWPstep_Cnt_u16	2091
k RestoreThresh MtrNm f32	6.69999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2 AsstFWUprBoundX HwNm s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2046
	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240 -8192
	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	



		(11, 10, 10, 10, 10, 10, 10, 10, 10, 10,
Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-28672	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-26624	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-24576	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144	
	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-28672	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0	
	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]		
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336	
	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	230
t_AsstFWDefltAssistX_HwNm_u8p8[1]	256
t_AsstFWDefltAssistX_HwNm_u8p8[2]	282
t_AsstFWDefltAssistX_HwNm_u8p8[3]	307
t_AsstFWDefltAssistX_HwNm_u8p8[4]	333
t_AsstFWDefltAssistX_HwNm_u8p8[5]	358
t_AsstFWDefltAssistX_HwNm_u8p8[6]	384
t_AsstFWDefltAssistX_HwNm_u8p8[7]	410
t_AsstFWDefltAssistX_HwNm_u8p8[8]	435
t_AsstFWDefltAssistX_HwNm_u8p8[9]	461
t_AsstFWDefltAssistX_HwNm_u8p8[10]	486
t_AsstFWDefltAssistX_HwNm_u8p8[11]	512
t_AsstFWDefltAssistX_HwNm_u8p8[12]	538
t_AsstFWDefltAssistX_HwNm_u8p8[13]	563
t_AsstFWDefltAssistX_HwNm_u8p8[14]	589
t_AsstFWDefltAssistX_HwNm_u8p8[15]	614
t_AsstFWDefltAssistX_HwNm_u8p8[16]	640
t_AsstFWDefltAssistX_HwNm_u8p8[17]	666
t_AsstFWDefltAssistX_HwNm_u8p8[18]	691
t_AsstFWDefltAssistX_HwNm_u8p8[19]	717
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	15360
t_AsstFWPstepNstepThresh_Cnt_u16[0]	168
t_AsstFWPstepNstepThresh_Cnt_u16[1]	391
t_AsstFWVehSpd_Kph_u9p7[0]	13184
t_AsstFWVehSpd_Kph_u9p7[1]	13312
t_AsstFWVehSpd_Kph_u9p7[2]	13440
t_AsstFWVehSpd_Kph_u9p7[3]	13568
t_AsstFWVehSpd_Kph_u9p7[4]	13696
t_AsstFWVehSpd_Kph_u9p7[5]	13824
t_AsstFWVehSpd_Kph_u9p7[6]	13952
t_AsstFWVehSpd_Kph_u9p7[7]	14080
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2.20000005
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-7
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	55.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_legers_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_legers_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_legers_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_legers_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_legers_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_legers_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_legers_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_legers_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_legers_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_legers_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_legers_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_legers_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_legers_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_legers_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_legers_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.19999981	3.20000005 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	391	391 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.5	-7.5 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.01350021	7.01350021 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-2	-2 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.92299986	5.92299986 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.5	-7.5 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•

$ ilde{ au}$				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.48 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.1000002
AssistFirewall ActiveKSV M str.K Uls f32	0.40000006
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4674
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall CombAsstSV MtrNm M f32	4.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	8
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0099999978
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.3999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0080000038
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.7000005
k AsstFWInpLimitHFA MtrNm f32	2.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	3.0999999
k_AsstFWNstep_Cnt_u16	4428
k_AsstFWPstep_Cnt_u16	2214
k RestoreThresh MtrNm f32	6.80000019
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2 AsstFWUprBoundX HwNm s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192
t2 AsstFWUprBoundX HwNm s4p11[1][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-18432
	1 10 102



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192 C444
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3] t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2 AsstFWUprBoundX HwNm s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10] t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2 AsstFWUprBoundX HwNm s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2 AsstFWUprBoundX HwNm s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	6144



	· ·	
Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240	
	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]		
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240	
	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192	
= -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1		



	(14 11 10 10
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
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t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	256
t_AsstFWDefltAssistX_HwNm_u8p8[1]	282
t_AsstFWDefltAssistX_HwNm_u8p8[2]	307
t_AsstFWDefltAssistX_HwNm_u8p8[3]	333
t_AsstFWDefltAssistX_HwNm_u8p8[4]	358
t_AsstFWDefltAssistX_HwNm_u8p8[5]	384
t_AsstFWDefltAssistX_HwNm_u8p8[6]	410
t_AsstFWDefltAssistX_HwNm_u8p8[7]	435
t_AsstFWDefltAssistX_HwNm_u8p8[8]	461
t_AsstFWDefltAssistX_HwNm_u8p8[9]	486
t_AsstFWDefltAssistX_HwNm_u8p8[10]	512
t_AsstFWDefltAssistX_HwNm_u8p8[11]	538
t_AsstFWDefltAssistX_HwNm_u8p8[12]	563
t_AsstFWDefltAssistX_HwNm_u8p8[13]	589
t_AsstFWDefltAssistX_HwNm_u8p8[14]	614
t_AsstFWDefltAssistX_HwNm_u8p8[15]	640
t_AsstFWDefltAssistX_HwNm_u8p8[16]	666
t AsstFWDefltAssistX HwNm u8p8[17]	691
t_AsstFWDefltAssistX_HwNm_u8p8[18]	717
t_AsstFWDefltAssistX_HwNm_u8p8[19]	742
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	15565
t_AsstFWPstepNstepThresh_Cnt_u16[0]	169
t AsstFWPstepNstepThresh Cnt u16[1]	395
t_AsstFWVehSpd_Kph_u9p7[0]	16128
t_AsstFWVehSpd_Kph_u9p7[1]	16256
t_AsstrWVehSpd_Kph_u9p7[2]	16384
t_AsstFWVehSpd_Kph_u9p7[3]	16512
t_AsstFWVenSpd_kpn_u9p7[3] t_AsstFWVehSpd_kph_u9p7[4]	
	16640
t_AsstFWVehSpd_Kph_u9p7[5]	16768
t_AsstFWVehSpd_Kph_u9p7[6]	16896
t_AsstFWVehSpd_Kph_u9p7[7]	17024
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	66.5
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	2 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f3	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cr	nt_lt tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1 HighFreqAssist MtrNm f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
• • • • • • • • • • • • • • • • • • • •	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.659999967	0.660000026 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	395	395 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.60009766	-7.60009766 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.98999977	7.98999977 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-0.25	-0.25 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.91200018	6.91200018 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.659999967	0.660000026 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.60009766	-7.60009766 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

$ ilde{ au}$				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.49 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	2.2000005
AssistFirewall ActiveKSV M str.K Uls f32	0.100000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4797
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall CombAsstSV MtrNm M f32	4.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.1000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.019999996
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.5
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.600000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00899999961
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.79999995
k_AsstFWInpLimitHFA_MtrNm_f32	3.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	3.29999995
k_AsstFWNstep_Cnt_u16	4551
k_AsstFWPstep_Cnt_u16	2337
k RestoreThresh MtrNm f32	6.9000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7] t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9] t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10] t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0] t2 AsstFWUprBoundX HwNm s4p11[7][1]	-4096 -2048
	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2] t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7] t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8] t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144 -4006
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
	0
	2040
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
	2048 4096 6144



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144



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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	282
t_AsstFWDefltAssistX_HwNm_u8p8[1]	307
t_AsstFWDefltAssistX_HwNm_u8p8[2]	333
t_AsstFWDefltAssistX_HwNm_u8p8[3]	358
t_AsstFWDefltAssistX_HwNm_u8p8[4]	384
t_AsstFWDefltAssistX_HwNm_u8p8[5]	410
t_AsstFWDefltAssistX_HwNm_u8p8[6]	435
t_AsstFWDefltAssistX_HwNm_u8p8[7]	461
t_AsstFWDefltAssistX_HwNm_u8p8[8]	486
t_AsstFWDefltAssistX_HwNm_u8p8[9]	512
t_AsstFWDefltAssistX_HwNm_u8p8[10]	538
t_AsstFWDefltAssistX_HwNm_u8p8[11]	563
t_AsstFWDefltAssistX_HwNm_u8p8[12]	589
t_AsstFWDefltAssistX_HwNm_u8p8[13]	614 640
t_AsstFWDefltAssistX_HwNm_u8p8[14] t_AsstFWDefltAssistX_HwNm_u8p8[15]	666
t_AsstFWDefitAssistX_HwNm_u8p8[16]	691
t_AsstFWDefitAssistX_HwNm_u8p8[17]	717
t_AsstFWDefltAssistX_HwNm_u8p8[18]	742
t_AsstFWDefitAssistX_HwNm_u8p8[19]	768
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	15770
t_AsstFWPstepNstepThresh_Cnt_u16[0]	170
t_AsstFWPstepNstepThresh_Cnt_u16[1]	399
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	19200 19328
t_AsstFWVehSpd_Kph_u9p7[3] t AsstFWVehSpd Kph u9p7[4]	19456 19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
t_AsstFWVehSpd_Kph_u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-9
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	77.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.98000002	1.98000002 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	246	246 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	4	4 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.15799999	1.15799999 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-6.4000001	-6.4000001 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.90100002	7.90100002 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4	4 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x00	0x00	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	<b>~</b>

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.50 (Repeat Count = 1)		
Name	Input Value	
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.0999999	
AssistFirewall ActiveKSV M str.K Uls f32	0.5	
AssistFirewall ActiveRawAcc Cnt M u16	4920	
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.69999981	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.20000005	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.029999993	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.60000002	
AssistFirewall LwrBoundKSV M str.SV Uls f32	5	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00125584798	
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002	
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0099999978	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.89999998	
k_AsstFWInpLimitHFA_MtrNm_f32	1.10000002	
k_AsstFWInpLimitHysComp_MtrNm_f32	3.5	
k_AsstFWNstep_Cnt_u16	4674	
k_AsstFWPstep_Cnt_u16	2460	
k_RestoreThresh_MtrNm_f32	7	
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384	
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432	
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480	
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336	
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288	
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336	
tz_asst-wuprboundx_hwnm_s4p11[2][0]	-14336	



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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_Asst WopiBoundX_HwNm_s4p11[5][2]	-8192
	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_Asst WopiboundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
	2048
	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048	
	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]		
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480	
	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]		
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048	
	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-18432	
	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]		
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240	
	-10240 -8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]		
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144	
12_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192	
t2_Asst WopiBoundY_MtrNm_s4p11[7][2]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-4096	



	(
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefltAssistX_HwNm_u8p8[0]	307
t_AsstFWDefltAssistX_HwNm_u8p8[1]	333
t_AsstFWDefltAssistX_HwNm_u8p8[2]	358
t_AsstFWDefltAssistX_HwNm_u8p8[3]	384
t_AsstFWDefltAssistX_HwNm_u8p8[4]	410
t_AsstFWDefltAssistX_HwNm_u8p8[5]	435
t_AsstFWDefltAssistX_HwNm_u8p8[6]	461
t_AsstFWDefltAssistX_HwNm_u8p8[7]	486
t_AsstFWDefltAssistX_HwNm_u8p8[8]	512
t_AsstFWDefltAssistX_HwNm_u8p8[9]	538
t_AsstFWDefltAssistX_HwNm_u8p8[10]	563
t_AsstFWDefltAssistX_HwNm_u8p8[11]	589
t_AsstFWDefltAssistX_HwNm_u8p8[12]	614
t_AsstFWDefltAssistX_HwNm_u8p8[13]	640
t_AsstFWDefltAssistX_HwNm_u8p8[14]	666
t_AsstFWDefltAssistX_HwNm_u8p8[15]	691
t_AsstFWDefltAssistX_HwNm_u8p8[16]	717
t_AsstFWDefltAssistX_HwNm_u8p8[17]	742
t_AsstFWDefltAssistX_HwNm_u8p8[18]	768
t_AsstFWDefltAssistX_HwNm_u8p8[19]	794
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	13722 13926
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	14131 14336
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[12] t AsstFWDefltAssistY_MtrNm_s4p11[13]	14746
t_AsstFWDefitAssistY_MtrNm_s4p11[14]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	15565
t AsstFWDefltAssistY MtrNm s4p11[18]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	15974
t_AsstFWPstepNstepThresh_Cnt_u16[0]	171
t_AsstFWPstepNstepThresh_Cnt_u16[1]	403
t_AsstFWVehSpd_Kph_u9p7[0]	22016
t_AsstFWVehSpd_Kph_u9p7[1]	22144
t_AsstFWVehSpd_Kph_u9p7[2]	22272
t_AsstFWVehSpd_Kph_u9p7[3]	22400
t AsstFWVehSpd Kph u9p7[4]	22528
t_AsstFWVehSpd_Kph_u9p7[5]	22656
t_AsstFWVehSpd_Kph_u9p7[6]	22784
t_AsstFWVehSpd_Kph_u9p7[7]	22912
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	88.0800018
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.54999995	1.54999995 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	403	403 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	•
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.89990234	5.89990234 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.31700015	2.31699991 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.99497652	4.99497652 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.08899999	1.08899999 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	5.89990234	5.89990234 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Input Value
2.7999995
0.090000036
5043
1
4.80000019
3.099999
0.039999991
1.7000005
6
0.715390444
0
2.20000005
0.019999996
tgt Rte Inst Ap AssistFirewall
2
2.20000005
3.7000005
3567
2583
7.0999999
-18432
-16384
-14336
-12288
-10240
-8192
-6144
-4096
-2048
0
2048
-12288
-10240
-8192
-6144
-4096
-2048
0
2048
4096
6144
8192
-12288



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7] t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8] t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HWNm_s4p11[6][10] t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HWNm_s4p11[7][0] t2 AsstFWUprBoundX HwNm s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HWNm_s4p11[7][2] t2 AsstFWUprBoundX HwNm s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3] t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][4] t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
	2048
t2 AsstEWI InrRoundV MtrNm s4n41[0][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4006
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-2048
	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	333
t_AsstFWDefltAssistX_HwNm_u8p8[1]	358
t_AsstFWDefltAssistX_HwNm_u8p8[2]	384
t_AsstFWDefltAssistX_HwNm_u8p8[3]	410
t_AsstFWDefltAssistX_HwNm_u8p8[4]	435
t_AsstFWDefltAssistX_HwNm_u8p8[5]	461
t_AsstFWDefltAssistX_HwNm_u8p8[6]	486
t_AsstFWDefltAssistX_HwNm_u8p8[7]	512
t_AsstFWDefltAssistX_HwNm_u8p8[8]	538
t_AsstFWDefltAssistX_HwNm_u8p8[9]	563
t_AsstFWDefltAssistX_HwNm_u8p8[10]	589
t_AsstFWDefltAssistX_HwNm_u8p8[11]	614
t_AsstFWDefltAssistX_HwNm_u8p8[12]	640
t_AsstFWDefltAssistX_HwNm_u8p8[13]	666
t_AsstFWDefltAssistX_HwNm_u8p8[14]	691
t_AsstFWDefltAssistX_HwNm_u8p8[15]	717
t_AsstFWDefltAssistX_HwNm_u8p8[16]	742
t_AsstFWDefltAssistX_HwNm_u8p8[17]	768
t_AsstFWDefltAssistX_HwNm_u8p8[18]	794
t_AsstFWDefltAssistX_HwNm_u8p8[19]	819
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	13926 14131
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	14336 14541
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[12] t AsstFWDefltAssistY_MtrNm_s4p11[13]	14950
t_AsstFWDefitAssistY_MtrNm_s4p11[14]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	15770
t AsstFWDefltAssistY MtrNm s4p11[18]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	16179
t_AsstFWPstepNstepThresh_Cnt_u16[0]	172
t_AsstFWPstepNstepThresh_Cnt_u16[1]	407
t_AsstFWVehSpd_Kph_u9p7[0]	24960
t_AsstFWVehSpd_Kph_u9p7[1]	25088
t_AsstFWVehSpd_Kph_u9p7[2]	25216
t_AsstFWVehSpd_Kph_u9p7[3]	25344
t AsstFWVehSpd Kph u9p7[4]	25472
t_AsstFWVehSpd_Kph_u9p7[5]	25600
t_AsstFWVehSpd_Kph_u9p7[6]	25728
t_AsstFWVehSpd_Kph_u9p7[7]	25856
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.099999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	99.0299988
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.54799986	2.5480001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1476	1476 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6.70019531	-6.70019531 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.29199982	3.29200006 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.4462471	-5.4462471 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.296	2.296 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-6.70019531	-6.70019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.52 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall ActiveKSV M str.K Uls f32	0.100000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	5166
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	4.900001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.7999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall LwrBoundKSV M str.K Uls f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.029999993
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.0999999
k AsstFWInpLimitHFA MtrNm f32	3.29999995
k_AsstFWInpLimitHysComp_MtrNm_f32	3.9000001
k_AsstFWNstep_Cnt_u16	3690
k_AsstFWPstep_Cnt_u16	2706
k RestoreThresh MtrNm f32	7.19999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2 AsstFWUprBoundX HwNm s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2 AsstFWUprBoundX HwNm s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240
E_, SSS. 1. Op. SSSSSSSS_TRESS_OPP. TELEOJ	1.02.0



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2 AsstFWUprBoundX HwNm s4p11[6][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
:2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
2 AsstFWUprBoundX HwNm s4p11[6][7]	8192
:z_AsstFWUprBoundX_HwNm_s4p11[6][7] :2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
:2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
:z_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	-18432
:2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][2] t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	
	-12288 -10240
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240 -8192
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240
12_AsstFWUprBoundY_MtrNm_s4p11[0][5] 12_AsstFWUprBoundY_MtrNm_s4p11[0][6] 12_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288 14336



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048
	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-16384
, , , , , , , , , , , , , , , , , , , ,	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144
	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-14336
	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-6144
	-0144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144
:2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192
:2_Asst WopiBoundY_MtrNm_s4p11[6][3]	10240
12_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	40.400
	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480 22528 24576
i2_AsstFWUprBoundY_MtrNm_s4p11[6][7] i2_AsstFWUprBoundY_MtrNm_s4p11[6][8] i2_AsstFWUprBoundY_MtrNm_s4p11[6][9] i2_AsstFWUprBoundY_MtrNm_s4p11[6][10] i2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	20480 22528 24576 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	20480 22528 24576



	(
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	358
t_AsstFWDefltAssistX_HwNm_u8p8[1]	384
t_AsstFWDefltAssistX_HwNm_u8p8[2]	410
t_AsstFWDefltAssistX_HwNm_u8p8[3]	435
t_AsstFWDefltAssistX_HwNm_u8p8[4]	461
t_AsstFWDefltAssistX_HwNm_u8p8[5]	486
t_AsstFWDefltAssistX_HwNm_u8p8[6]	512
t_AsstFWDefltAssistX_HwNm_u8p8[7]	538
t_AsstFWDefltAssistX_HwNm_u8p8[8]	563
t_AsstFWDefltAssistX_HwNm_u8p8[9]	589 614
t_AsstFWDefltAssistX_HwNm_u8p8[10]	640
t_AsstFWDefltAssistX_HwNm_u8p8[11] t AsstFWDefltAssistX HwNm u8p8[12]	666
t_AsstFWDefitAssistX_HwNm_u8p8[13]	691
t_AsstFWDefltAssistX_HwNm_u8p8[14]	717
t_AsstFWDefitAssistX_HwNm_u8p8[15]	742
t_AsstFWDefltAssistX_HwNm_u8p8[16]	768
t_AsstFWDefltAssistX_HwNm_u8p8[17]	794
t_AsstFWDefltAssistX_HwNm_u8p8[18]	819
t_AsstFWDefltAssistX_HwNm_u8p8[19]	845
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	15770
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	16384
t_AsstFWPstepNstepThresh_Cnt_u16[0] t_AsstFWPstepNstepThresh_Cnt_u16[1]	173 411
	27904
t_AsstFWVehSpd_Kph_u9p7[0] t_AsstFWVehSpd_Kph_u9p7[1]	28032
t_AsstFWVehSpd_Kph_u9p7[2]	28160
t_AsstFWVehSpd_Kph_u9p7[3]	28288
t AsstFWVehSpd Kph u9p7[4]	28416
t_AsstFWVehSpd_Kph_u9p7[5]	28544
t_AsstFWVehSpd_Kph_u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7]	28800
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	123.010002
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	
5	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cn tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32  tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AssiTbl_Service_Cn tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AssiTbl_Service_Cntgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AssiTbl_Service_Cn tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.99000001	0.99000001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1476	1476 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.70019531	-7.70019531 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.30499983	4.30499983 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-2	-2 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.1869998	3.18700004 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.99000001	0.99000001 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.70019531	-7.70019531 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Name	
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	
AssistFirewall_ActiveKSV_M_str.K_Uls_f32         0.20000003           AssistFirewall_ActiveRawAcc_Cnt_M_u16         5289           AssistFirewall_ActiveRawAcc_Cnt_M_lgc         1           AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32         -4.0999999           AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32         5.0999999           AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32         0.059999987           AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32         1.8999998           AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32         8           AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32         0.090000036           AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32         4.099999           AssistFirewall_UprBoundKSV_M_str.K_Uls_f32         0.039999991           AssistFirewall_UprBoundKSV_M_str.K_Uls_f32         0.039999991           Re_Inst_Ap_AssistFirewall         tgt_Re_Inst_Ap_AssistFirewall           k_AsstFWInpLimitBaseAsst_MtrNm_f32         2.20000005           k_AsstFWInpLimitHPA_MtrNm_f32         4.099999           k_AsstFWInpLimitHysComp_MtrNm_f32         4.0999999           k_AsstFWINpt_Cnt_u16         3813           k_AsstFWINpt_Cnt_u16         2829           k_RestoreThresh_MtrNm_f32         7.30000019           t_AsstFWUprBoundX_HwNm_s4p11[0][0]         -14336	
AssistFirewall_ActiveRawAcc_Cnt_M_u16 5289 AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc 1 AssistFirewall_CombAsstSV_MtrNm_M_f32 -4.0999999 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32 5.0999999 AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32 0.059999987 AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32 1.8999998 AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32 8 AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32 0.090000036 AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32 0.090000036 AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 4.099999 AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 4.099999 AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 0.039999991 Rte_Inst_Ap_AssistFirewall L_AssitFirewall_UprBoundKSV_M_str.SV_Uls_f32 0.039999991 Rte_Inst_Ap_AssistFirewall L_AssitFWInpLimitBaseAsst_MtrNm_f32 2.2000005 L_AssitFWInpLimitHS_MtrNm_f32 4.400001 L_AssitFWInpLimitHS_Cmp_MtrNm_f32 4.909999 AssistFWInpLimitHS_Cmp_MtrNm_f32 4.909999 AssistFWInpLimitHS_Cmp_MtrNm_f32 4.00001 AssitFWPstep_Cnt_u16 2829 L_AssitFWPstep_Cnt_u16 2829 L_RestoreThresh_MtrNm_f32 7.3000019 2_AssitFWUprBoundX_HwNm_s4p11[0][0] -14336	
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc       1         AssistFirewall_CombAsstSV_MtrNm_M_f32       -4.0999999         AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32       5.0999999         AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32       0.059999987         AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32       1.8999998         AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32       8         AssistFirewall_wBoundKSV_M_str.K_Uls_f32       0.090000036         AssistFirewall_PNCountStatus_Cnt_M_lgc       1         AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32       4.0999999         AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32       0.039999991         Rte_Inst_Ap_AssistFirewall       tgt_Rte_Inst_Ap_AssistFirewall         k_AsstFWInpLimitBaseAsst_MtrNm_f32       2.20000005         k_AsstFWInpLimitHFA_MtrNm_f32       4.009001         k_AsstFWINStep_Cnt_u16       3813         k_AsstFWPstep_Cnt_u16       2829         k_RestoreThresh_MtrNm_f32       7.3000019         t_AsstFWUpBoundX_HwNm_s4p1[0][0]       -14336	
AssistFirewall_CombAsstSV_MtrNm_M_f32 -4.0999999 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32 5.0999999 AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32 0.059999987 AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32 1.8999998 AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32 8 AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32 0.090000036 AssistFirewall_PNCountStatus_Cnt_M_lgc 1 1 AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 4.099999 AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 0.039999991 AssistFirewall_UprBoundKSV_M_str.K_Uls_f32 0.039999991 Rte_Inst_Ap_AssistFirewall	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32       5.0999999         AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32       0.0599999987         AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32       1.89999998         AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32       8         AssistFirewall_PNCountStatus_Cnt_M_lgc       1         AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32       4.0999999         AssistFirewall_UprBoundKSV_M_str.K_Uls_f32       0.039999991         Rte_Inst_Ap_AssistFirewall       tgt_Rte_Inst_Ap_AssistFirewall         k_AsstFWInpLimitBaseAsst_MtrNm_f32       2.20000005         k_AsstFWInpLimitHysComp_MtrNm_f32       4.0999999         k_AsstFWIstep_Cnt_u16       3813         k_AsstFWPstep_Cnt_u16       2829         k_RestoreThresh_MtrNm_f32       7.30000019         t_AsstFWUprBoundX_HwNm_s4p11[0][0]       -14336	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32       0.0599999987         AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32       1.89999998         AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32       8         AssistFirewall_PNCountStatus_Cnt_M_lgc       1         AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32       4.0999999         AssistFirewall_UprBoundKSV_M_str.K_Uls_f32       0.039999991         Rte_Inst_Ap_AssistFirewall       tgt_Rte_Inst_Ap_AssistFirewall         k_AsstFWInpLimitBaseAsst_MtrNm_f32       2.20000005         k_AsstFWInpLimitHysComp_MtrNm_f32       4.0999999         k_AsstFWIstep_Cnt_u16       3813         k_AsstFWPstep_Cnt_u16       2829         k_RestoreThresh_MtrNm_f32       7.30000019         t_AsstFWUprBoundX_HwNm_s4p11[0][0]       -14336	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32       1.89999998         AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32       8         AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32       0.090000036         AssistFirewall_PNCountStatus_Cnt_M_lgc       1         AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32       4.0999999         AssistFirewall_UprBoundKSV_M_str.K_Uls_f32       0.039999991         Rte_Inst_Ap_AssistFirewall       tgt_Rte_Inst_Ap_AssistFirewall         k_AsstFWInpLimitBaseAsst_MtrNm_f32       2.20000005         k_AsstFWInpLimitHysComp_MtrNm_f32       4.000001         k_AsstFWInpLimitHysComp_MtrNm_f32       4.0999999         k_AsstFWPstep_Cnt_u16       3813         k_RestoreThresh_MtrNm_f32       7.30000019         t_AsstFWUprBoundX_HwNm_s4p11[0][0]       -14336	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32       8         AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32       0.0900000036         AssistFirewall_PNCountStatus_Cnt_M_lgc       1         AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32       4.0999999         AssistFirewall_UprBoundKSV_M_str.K_Uls_f32       0.039999991         Rte_Inst_Ap_AssistFirewall       tgt_Rte_Inst_Ap_AssistFirewall         k_AsstFWInpLimitBaseAsst_MtrNm_f32       2.20000005         k_AsstFWInpLimitHyA_MtrNm_f32       4.4000001         k_AsstFWInpLimitHysComp_MtrNm_f32       4.0999999         k_AsstFWNstep_Cnt_u16       3813         k_AsstFWPstep_Cnt_u16       2829         k_RestoreThresh_MtrNm_f32       7.30000019         t2_AsstFWUprBoundX_HwNm_s4p11[0][0]       -14336	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32       0.090000036         AssistFirewall_PNCountStatus_Cnt_M_lgc       1         AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32       4.0999999         AssistFirewall_UprBoundKSV_M_str.K_Uls_f32       0.039999991         Rte_Inst_Ap_AssistFirewall       tgt_Rte_Inst_Ap_AssistFirewall         k_AsstFWInpLimitBaseAsst_MtrNm_f32       2.20000005         k_AsstFWInpLimitHysComp_MtrNm_f32       4.000001         k_AsstFWIntep_Cnt_u16       3813         k_AsstFWPstep_Cnt_u16       2829         k_RestoreThresh_MtrNm_f32       7.30000019         t_AsstFWUprBoundX_HwNm_s4p11[0][0]       -14336	
AssistFirewall_PNCountStatus_Cnt_M_lgc       1         AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32       4.0999999         AssistFirewall_UprBoundKSV_M_str.K_Uls_f32       0.039999991         Rte_Inst_Ap_AssistFirewall       tgt_Rte_Inst_Ap_AssistFirewall         k_AsstFWInpLimitBaseAsst_MtrNm_f32       2.20000005         k_AsstFWInpLimitHys_Comp_MtrNm_f32       4.4000001         k_AsstFWInpLimitHysComp_MtrNm_f32       4.0999999         k_AsstFWNstep_Cnt_u16       3813         k_AsstFWPstep_Cnt_u16       2829         k_RestoreThresh_MtrNm_f32       7.30000019         t_AsstFWUprBoundX_HwNm_s4p11[0][0]       -14336	
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32       4.0999999         AssistFirewall_UprBoundKSV_M_str.K_Uls_f32       0.0399999991         Rte_Inst_Ap_AssistFirewall       tgt_Rte_Inst_Ap_AssistFirewall         k_AsstFWInpLimitBaseAsst_MtrNm_f32       2.20000005         k_AsstFWInpLimitHFA_MtrNm_f32       4.4000001         k_AsstFWInpLimitHysComp_MtrNm_f32       4.0999999         k_AsstFWNstep_Cnt_u16       3813         k_AsstFWPstep_Cnt_u16       2829         k_RestoreThresh_MtrNm_f32       7.30000019         t2_AsstFWUprBoundX_HwNm_s4p11[0][0]       -14336	
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32       0.0399999991         Rte_Inst_Ap_AssistFirewall       tgt_Rte_Inst_Ap_AssistFirewall         k_AsstFWInpLimitBaseAsst_MtrNm_f32       2.20000005         k_AsstFWInpLimitHFA_MtrNm_f32       4.4000001         k_AsstFWInpLimitHysComp_MtrNm_f32       4.0999999         k_AsstFWNstep_Cnt_u16       3813         k_AsstFWPstep_Cnt_u16       2829         k_RestoreThresh_MtrNm_f32       7.30000019         t2_AsstFWUprBoundX_HwNm_s4p11[0][0]       -14336	
Rte_Inst_Ap_AssistFirewall         tgt_Rte_Inst_Ap_AssistFirewall           k_AsstFWInpLimitBaseAsst_MtrNm_f32         2.20000005           k_AsstFWInpLimitHFA_MtrNm_f32         4.4000001           k_AsstFWInpLimitHysComp_MtrNm_f32         4.0999999           k_AsstFWNstep_Cnt_u16         3813           k_AsstFWPstep_Cnt_u16         2829           k_RestoreThresh_MtrNm_f32         7.30000019           t2_AsstFWUprBoundX_HwNm_s4p11[0][0]         -14336	
k_AsstFWInpLimitHFA_MtrNm_f32       4.4000001         k_AsstFWInpLimitHysComp_MtrNm_f32       4.0999999         k_AsstFWNstep_Cnt_u16       3813         k_AsstFWPstep_Cnt_u16       2829         k_RestoreThresh_MtrNm_f32       7.30000019         t2_AsstFWUprBoundX_HwNm_s4p11[0][0]       -14336	
k_AsstFWInpLimitHysComp_ltrNm_f32       4.0999999         k_AsstFWNstep_Cnt_u16       3813         k_AsstFWPstep_Cnt_u16       2829         k_RestoreThresh_MtrNm_f32       7.30000019         t2_AsstFWUprBoundX_HwNm_s4p11[0][0]       -14336	
k_AsstFWNstep_Cnt_u16       3813         k_AsstFWPstep_Cnt_u16       2829         k_RestoreThresh_MtrNm_f32       7.30000019         t2_AsstFWUprBoundX_HwNm_s4p11[0][0]       -14336	
k_AsstFWNstep_Cnt_u16       3813         k_AsstFWPstep_Cnt_u16       2829         k_RestoreThresh_MtrNm_f32       7.30000019         t2_AsstFWUprBoundX_HwNm_s4p11[0][0]       -14336	
k_AsstFWPstep_Cnt_u16       2829         k_RestoreThresh_MtrNm_f32       7.30000019         t2_AsstFWUprBoundX_HwNm_s4p11[0][0]       -14336	
k_RestoreThresh_MtrNm_f32       7.30000019         t2_AsstFWUprBoundX_HwNm_s4p11[0][0]       -14336	
, , , , , , ,	
, , , , , , ,	
t2_AsstFWUprBoundX_HwNm_s4p11[0][1] -12288	
12_AsstFWUprBoundX_HwNm_s4p11[0][2] -10240	
12_AsstFWUprBoundX_HwNm_s4p11[0][3] -8192	
12_AsstFWUprBoundX_HwNm_s4p11[0][4] -6144	
12_AsstFWUprBoundX_HwNm_s4p11[0][5] -4096	
12_AsstFWUprBoundX_HwNm_s4p11[0][6] -2048	
12_AsstFWUprBoundX_HwNm_s4p11[0][7] 0	
12_AsstFWUprBoundX_HwNm_s4p11[0][8] 2048	
12_AsstFWUprBoundX_HwNm_s4p11[0][9] 4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][10] 6144	
12_AsstFWUprBoundX_HwNm_s4p11[1][0] -8192	
12_AsstFWUprBoundX_HwNm_s4p11[1][1] -6144	
12_AsstFWUprBoundX_HwNm_s4p11[1][2] -4096	
12_AsstFWUprBoundX_HwNm_s4p11[1][3] -2048	
12_AsstFWUprBoundX_HwNm_s4p11[1][4] 0	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5] 2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][6] 4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7] 6144	
12_AsstFWUprBoundX_HwNm_s4p11[1][8] 8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][9] 10240	
t2_AsstFWUprBoundX_HwNm_s4p11[1][10] 12288	
t2_AsstFWUprBoundX_HwNm_s4p11[2][0] -8192	



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
:2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
	-2046
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240
	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
12_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
:2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	4096
:2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	6144
:2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240 12288
O ApptEM/Hardonady Markley - 4-445055	LT 2 788
I2_AsstFWUprBoundY_MtrNm_s4p11[0][4] I2_AsstFWUprBoundY_MtrNm_s4p11[0][5] I2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	14336 16384



	• "	
Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096	
	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]		
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336	
	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]		
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	8192	
	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-12288	
	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]		
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-4096	
	-4096 -2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]		
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0	
	2048	
12_AsstFWUprBoundY_MtrNm_s4p11[6][4]		
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	384
t_AsstFWDefltAssistX_HwNm_u8p8[1]	410
t_AsstFWDefltAssistX_HwNm_u8p8[2]	435
t_AsstFWDefltAssistX_HwNm_u8p8[3]	461
t_AsstFWDefltAssistX_HwNm_u8p8[4]	486
t_AsstFWDefltAssistX_HwNm_u8p8[5]	512
t_AsstFWDefltAssistX_HwNm_u8p8[6]	538
t_AsstFWDefltAssistX_HwNm_u8p8[7] t_AsstFWDefltAssistX_HwNm_u8p8[8]	563 589
t_AsstFWDefitAssistX_HwNm_u8p8[9]	614
t_AsstFWDefitAssistX_HwNm_u8p8[10]	640
t AsstFWDefitAssistX HwNm u8p8[11]	666
t_AsstFWDefltAssistX_HwNm_u8p8[12]	691
t_AsstFWDefltAssistX_HwNm_u8p8[13]	717
t_AsstFWDefitAssistX_HwNm_u8p8[14]	742
t AsstFWDefltAssistX HwNm u8p8[15]	768
t_AsstFWDefltAssistX_HwNm_u8p8[16]	794
t_AsstFWDefltAssistX_HwNm_u8p8[17]	819
t_AsstFWDefltAssistX_HwNm_u8p8[18]	845
t_AsstFWDefltAssistX_HwNm_u8p8[19]	870
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[15] t_AsstFWDefltAssistY_MtrNm_s4p11[16]	15770 15974
t_AsstFWDefltAssistY_MtrNm_s4p11[17] t_AsstFWDefltAssistY_MtrNm_s4p11[18]	16179 16384
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	16589
t_AsstFWPstepNstepThresh_Cnt_u16[0]	174
t_AsstFWPstepNstepThresh_Cnt_u16[1]	415
t_AsstFWVehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1]	30976
t_AsstFWVehSpd_Kph_u9p7[2]	31104
t_AsstFWVehSpd_Kph_u9p7[3]	31232
t_AsstFWVehSpd_Kph_u9p7[4]	31360
t_AsstFWVehSpd_Kph_u9p7[5]	31488
t_AsstFWVehSpd_Kph_u9p7[6]	31616
t_AsstFWVehSpd_Kph_u9p7[7]	31744
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	234.050003
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_le	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-7.03999996	-7.03999996 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	415	415 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.10009766	8.10009766 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.42399979	5.42399979 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.82999992	6.82999992 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.41599989	4.41599989 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.10009766	8.10009766 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8.80000019
Assisti ilewali_ActiveKSV_M_str.K_UIs_f32	0.30000019
AssistFirewall_ActiveRawAcc_Cnt_M_u16	5412
AssistFirewall_ActiveRawAcc_Cnt_M_u16 AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_AsstReducedPenSv_Cnt_M_igc AssistFirewall CombAsstSV MtrNm M f32	-4.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.0999999 0.070000003
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.0099999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0500000007
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
x_AsstFWInpLimitBaseAsst_MtrNm_f32	2.29999995
x_AsstFWInpLimitHFA_MtrNm_f32	5.5
x_AsstFWInpLimitHysComp_MtrNm_f32	4.30000019
x_AsstFWNstep_Cnt_u16	3936
x_AsstFWPstep_Cnt_u16	2952
c_RestoreThresh_MtrNm_f32	7.4000001
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][7] t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
t2_AsstFWUprBoundX_FIWNIII_S4p11[5][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2 AsstFWUprBoundX HwNm s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
t2 AsstFWUprBoundX HwNm s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	14336
	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10304
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	18432



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	26624	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240	
	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]		
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	6144	
	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	28672	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192	
	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]		
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192	
	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]		
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	410
t_AsstFWDefltAssistX_HwNm_u8p8[1]	435
t_AsstFWDefltAssistX_HwNm_u8p8[2]	461
t_AsstFWDefltAssistX_HwNm_u8p8[3]	486
t_AsstFWDefltAssistX_HwNm_u8p8[4]	512
t_AsstFWDefltAssistX_HwNm_u8p8[5]	538
t_AsstFWDefltAssistX_HwNm_u8p8[6]	563
t_AsstFWDefltAssistX_HwNm_u8p8[7]	589
t_AsstFWDefltAssistX_HwNm_u8p8[8]	614
t_AsstFWDefltAssistX_HwNm_u8p8[9]	640
t_AsstFWDefltAssistX_HwNm_u8p8[10]	666
t_AsstFWDefltAssistX_HwNm_u8p8[11]	691 717
t_AsstFWDefltAssistX_HwNm_u8p8[12]	
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	742 768
t_AsstFWDefitAssistX_HwNm_u8p8[14] t_AsstFWDefitAssistX_HwNm_u8p8[15]	794
t_AsstFWDefitAssistX_mwnm_uopo[15]	819
t_AsstFWDefltAssistX_HwNm_u8p8[17]	845
t_AsstFWDefltAssistX_HwNm_u8p8[18]	870
t_AsstFWDefltAssistX_HwNm_u8p8[19]	896
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	16589
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	16794
t_AsstFWPstepNstepThresh_Cnt_u16[0]	175
t_AsstFWPstepNstepThresh_Cnt_u16[1]	419 33792
t_AsstFWVehSpd_Kph_u9p7[0]	33920
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	34048
t_AsstFWVehSpd_Kph_u9p7[3]	34176
t AsstFWVehSpd Kph u9p7[4]	34304
t_AsstFWVehSpd_Kph_u9p7[5]	34432
t AsstFWVehSpd Kph u9p7[6]	34560
t_AsstFWVehSpd_Kph_u9p7[7]	34688
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	24.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFi$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.15999985	6.15999985 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	419	419 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	6.29980469	6.29980469 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.97399998	5.97399998 ± 4.88E-04	<b>~</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.189999998	0.189999998 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.34499979	5.34499979 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	6.29980469	6.29980469 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.55 (Repeat Count = 1)	variation of the state of the
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0
AssistFirewall ActiveKSV M str.K Uls f32	0.059999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	5535
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.200000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0599999987
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.4000001
k_AsstFWInpLimitHFA_MtrNm_f32	6.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	4.5
k_AsstFWNstep_Cnt_u16	4059
k_AsstFWPstep_Cnt_u16	3075
k_RestoreThresh_MtrNm_f32	7.5
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144
t2_Asst WoprBoundX_HwNm_s4p11[3][8]	8192
	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	16384
t2 AsstFWUprBoundX HwNm s4p11[5][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2 AsstFWUprBoundX HwNm s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	10240
	12288
t2 AsstEWUprBoundy Mirrim s4n11101121	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	



Nama	Innut Value
Name	Input Value 24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8] t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4] t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	14336



	, , , , , , , , , , , , , , , , , , , ,
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	435
t_AsstFWDefltAssistX_HwNm_u8p8[1]	461
t_AsstFWDefltAssistX_HwNm_u8p8[2]	486
t_AsstFWDefltAssistX_HwNm_u8p8[3]	512
t_AsstFWDefltAssistX_HwNm_u8p8[4]	538
t_AsstFWDefltAssistX_HwNm_u8p8[5]	563
t_AsstFWDefltAssistX_HwNm_u8p8[6]	589
t_AsstFWDefltAssistX_HwNm_u8p8[7]	614
t_AsstFWDefltAssistX_HwNm_u8p8[8]	640
t_AsstFWDefltAssistX_HwNm_u8p8[9]	666
t_AsstFWDefltAssistX_HwNm_u8p8[10]	691
t_AsstFWDefltAssistX_HwNm_u8p8[11]	717 742
t_AsstFWDefltAssistX_HwNm_u8p8[12]	
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	768 794
t_AsstFWDefitAssistX_HwNm_u8p8[14] t_AsstFWDefitAssistX_HwNm_u8p8[15]	819
t_AsstFWDefltAssistX_HwNm_u8p8[16]	845
t_AsstFWDefitAssistX_HwNm_u8p8[17]	870
t_AsstFWDefltAssistX_HwNm_u8p8[18]	896
t_AsstFWDefltAssistX_HwNm_u8p8[19]	922
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	16998
t_AsstFWPstepNstepThresh_Cnt_u16[0]	176
t_AsstFWPstepNstepThresh_Cnt_u16[1]	423
t_AsstFWVehSpd_Kph_u9p7[0]	36736
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	36864 36992
t_AsstFWVehSpd_Kph_u9p7[3]	37120
t AsstFWVehSpd Kph u9p7[4]	37248
t_AsstFWVehSpd_Kph_u9p7[5]	37376
t_AsstFWVehSpd_Kph_u9p7[6]	37504
t_AsstFWVehSpd_Kph_u9p7[7]	37632
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	57.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFi$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0	0 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1476	1476 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6.70019531	-6.70019531 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.43200004	1.43200004 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-0.440000057	-0.439999998 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.15399981	6.15399981 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-6.70019531	-6.70019531 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x00	0x00	•
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.56 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.5
AssistFirewall ActiveKSV M str.K Uls f32	0.070000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	5658
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	-4.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.090000036
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.02999997
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.099999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.30000012
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0700000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.5
k AsstFWInpLimitHFA MtrNm f32	7.69999981
k_AsstFWInpLimitHysComp_MtrNm_f32	4.69999981
k_AsstFWNstep_Cnt_u16	4182
k_AsstFWPstep_Cnt_u16	3198
k RestoreThresh MtrNm f32	7.5999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2 AsstFWUprBoundX HwNm s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048
	1 20 10



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2 AsstFWUprBoundX HwNm s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2 AsstFWUprBoundX HwNm s4p11[7][0]	-10240
t2 AsstFWUprBoundX HwNm s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_Asst WoprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240
	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	6144
tz_asst=wuprboundY_mtrNm_s4p11[0][4] t2_asstFWUprBoundY_mtrNm_s4p11[0][5] t2_asstFWUprBoundY_mtrNm_s4p11[0][6]	-6144 -4096



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-8192
	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	6144
2 AsstFWUprBoundY MtrNm s4p11[2][9]	8192
	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048
	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	· · · · · · · · · · · · · · · · · · ·
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	6144
t2 AsstFWUprBoundY MtrNm s4p11[4][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-12288 -10240



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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	461
t_AsstFWDefltAssistX_HwNm_u8p8[1]	486
t_AsstFWDefltAssistX_HwNm_u8p8[2]	512
t_AsstFWDefltAssistX_HwNm_u8p8[3]	538
t_AsstFWDefltAssistX_HwNm_u8p8[4]	563
t_AsstFWDefltAssistX_HwNm_u8p8[5]	589
t_AsstFWDefltAssistX_HwNm_u8p8[6]	614
t_AsstFWDefltAssistX_HwNm_u8p8[7]	640
t_AsstFWDefltAssistX_HwNm_u8p8[8]	666
t_AsstFWDefltAssistX_HwNm_u8p8[9]	691
t_AsstFWDefltAssistX_HwNm_u8p8[10]	717
t_AsstFWDefltAssistX_HwNm_u8p8[11]	742
t_AsstFWDefltAssistX_HwNm_u8p8[12]	768
t_AsstFWDefltAssistX_HwNm_u8p8[13]	794
t_AsstFWDefltAssistX_HwNm_u8p8[14]	819
t_AsstFWDefltAssistX_HwNm_u8p8[15]	845
t_AsstFWDefltAssistX_HwNm_u8p8[16]	870
t_AsstFWDefltAssistX_HwNm_u8p8[17]	896
t_AsstFWDefltAssistX_HwNm_u8p8[18]	922
t_AsstFWDefltAssistX_HwNm_u8p8[19]	947
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	17203
t_AsstFWPstepNstepThresh_Cnt_u16[0]	177
t_AsstFWPstepNstepThresh_Cnt_u16[1]	427
t_AsstFWVehSpd_Kph_u9p7[0]	39680
t_AsstFWVehSpd_Kph_u9p7[1]	39808
t_AsstFWVehSpd_Kph_u9p7[2]	39936
t_AsstFWVehSpd_Kph_u9p7[3] t AsstFWVehSpd Kph u9p7[4]	40064
	40192 40320
t_AsstFWVehSpd_Kph_u9p7[5] t_AsstFWVehSpd_Kph_u9p7[6]	40448
t_AsstFWVehSpd_Kph_u9p7[7]	4046
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_BaseAssistCmd_intrinm_132.value  tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_Deteat_Assist_bt_Service_Cnt_igc.value  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3
tgt_AssistFirewail_Per1_HighFreqAssist_MtrNm_f32.value  tgt_AssistFirewail_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	89.0699997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_AssistFirewallActive_ois_i32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_DaseAssistCinio_MithInf_i32 tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_Assist_Mit/Nffi_i32  tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_l	
tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_beleat_AssistDi_service_Crit_i tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_intf\tilifi1i32 tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32
J	0



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.11499977	5.11499977 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	427	427 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.70019531	-7.70019531 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.58500004	2.58500004 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.46999979	2.47000003 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	0.439999998	0.43999998 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.70019531	-7.70019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

au				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.57 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.5
AssistFirewall ActiveKSV M str.K Uls f32	0.0799999982
AssistFirewall_ActiveRawAcc_Cnt_M_u16	5781
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.200000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.03999996
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0799999982
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.5999999
k_AsstFWInpLimitHFA_MtrNm_f32	3.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	4.9000001
k_AsstFWNstep_Cnt_u16	4305
k_AsstFWPstep_Cnt_u16	3321
k_RestoreThresh_MtrNm_f32	7.69999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	10240
	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2 AsstFWUprBoundX HwNm s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	
	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-8192
	-6144
t2 AcctEM/I IntRoundV MtrNim c4n11[0][4]	170144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-4096 -2048



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2] t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3] t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192



	(10.00)
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	486
t_AsstFWDefltAssistX_HwNm_u8p8[1]	512
t_AsstFWDefltAssistX_HwNm_u8p8[2]	538
t_AsstFWDefltAssistX_HwNm_u8p8[3]	563
t_AsstFWDefltAssistX_HwNm_u8p8[4]	589
t_AsstFWDefltAssistX_HwNm_u8p8[5]	614
t_AsstFWDefltAssistX_HwNm_u8p8[6]	640
t_AsstFWDefltAssistX_HwNm_u8p8[7]	666
t_AsstFWDefltAssistX_HwNm_u8p8[8]	691
t_AsstFWDefltAssistX_HwNm_u8p8[9]	717
t_AsstFWDefltAssistX_HwNm_u8p8[10]	742
t_AsstFWDefltAssistX_HwNm_u8p8[11]	768
t_AsstFWDefltAssistX_HwNm_u8p8[12]	794
t_AsstFWDefltAssistX_HwNm_u8p8[13]	819
t_AsstFWDefltAssistX_HwNm_u8p8[14]	845
t_AsstFWDefltAssistX_HwNm_u8p8[15]	870
t AsstFWDefltAssistX HwNm u8p8[16]	896
t AsstFWDefltAssistX HwNm u8p8[17]	922
t_AsstFWDefltAssistX_HwNm_u8p8[18]	947
t_AsstFWDefltAssistX_HwNm_u8p8[19]	973
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	13722
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	17408
t_AsstFWPstepNstepThresh_Cnt_u16[0]	178
t AsstFWPstepNstepThresh Cnt u16[1]	431
t_AsstFWVehSpd_Kph_u9p7[0]	42624
t_AsstFWVehSpd_Kph_u9p7[1]	42752
t_AsstFWVehSpd_Kph_u9p7[2]	4280
t_AsstFWVehSpd_Kph_u9p7[3]	43008
t_AsstFWVenSpd_kpn_u9p7[3] t_AsstFWVenSpd_kpn_u9p7[4]	43136
t_AsstFWVehSpd_Kph_u9p7[5]	43264
t_AsstFWVehSpd_Kph_u9p7[6]	43392
t_AsstFWVehSpd_Kph_u9p7[7]	43520
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	10.1000004
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cn	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_rtte_mat_Ap_Assisti irewali.Assisti irewali_i eri Tilqili reqAssist ivitivili 132	
• • • • • • • • • • • • • • • • • • • •	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Ont_enum	



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.05999994	-5.05999994 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	431	431 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.5	8.5 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.53999996	4.53999996 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.26000023	5.26000023 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.84000003	1.84000003 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.5	8.5 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

au				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.58 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	5
AssistFirewall ActiveKSV M str.K Uls f32	0.00125584798
AssistFirewall_ActiveRawAcc_Cnt_M_u16	5904
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.300000012
AssistFirewall HiFreqKSV M str.CF Uls f32	1.04999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3
AssistFirewall UprBoundKSV M str.K Uls f32	0.090000036
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.70000005
k_AsstFWInpLimitHFA_MtrNm_f32	3.4000001
k_AsstFWInpLimitHysComp_MtrNm_f32	5.0999999
k_AsstFWNstep_Cnt_u16	4428
k_AsstFWPstep_Cnt_u16	3444
k RestoreThresh MtrNm f32	7.80000019
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384



	(
Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_Asst WopiBoundX_HwNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_Asst WopiBoundX_HwNm_s4p11[5][1]	-14336
t2_Asst WopiBoundX_HwNm_s4p11[5][1]	-12288
	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2 AsstFWUprBoundX HwNm s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstrWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-4096 -2048



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288	
	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	2048	
	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	14336	
	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]		
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288	
	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144	



	(
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	512
t_AsstFWDefltAssistX_HwNm_u8p8[1]	538
t_AsstFWDefltAssistX_HwNm_u8p8[2]	563
t_AsstFWDefltAssistX_HwNm_u8p8[3]	589
t_AsstFWDefltAssistX_HwNm_u8p8[4]	614
t_AsstFWDefltAssistX_HwNm_u8p8[5]	640
t_AsstFWDefltAssistX_HwNm_u8p8[6]	666
t_AsstFWDefltAssistX_HwNm_u8p8[7]	691
t_AsstFWDefltAssistX_HwNm_u8p8[8]	717
t_AsstFWDefltAssistX_HwNm_u8p8[9]	742
t_AsstFWDefltAssistX_HwNm_u8p8[10]	768
t_AsstFWDefltAssistX_HwNm_u8p8[11]	794
t_AsstFWDefltAssistX_HwNm_u8p8[12]	819
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	845 870
t_AsstFWDefitAssistX_HwNm_u8p8[14] t_AsstFWDefitAssistX_HwNm_u8p8[15]	896
t_AsstFWDefltAssistX_HwNm_u8p8[16]	922
t_AsstFWDefitAssistX_HwNm_u8p8[17]	947
t_AsstFWDefltAssistX_HwNm_u8p8[18]	973
t_AsstFWDefltAssistX_HwNm_u8p8[19]	998
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	17408
t_AsstFWDeftAssistY_MtrNm_s4p11[19]	17613
t_AsstFWPstepNstepThresh_Cnt_u16[0]	179
t_AsstFWPstepNstepThresh_Cnt_u16[1]	435
t_AsstFWVehSpd_Kph_u9p7[0]	45568
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	45696 45824
t_AsstFWVehSpd_Kph_u9p7[3]	45952
t AsstFWVehSpd Kph u9p7[4]	46980
t_AsstFWVehSpd_Kph_u9p7[5]	46208
t_AsstFWVehSpd_Kph_u9p7[6]	46336
t_AsstFWVehSpd_Kph_u9p7[7]	46464
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	40.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32$	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_locations and the property of $	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4.99372053	4.99372053 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	435	435 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.70019531	-7.70019531 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.75	4.75 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.04999995	3.04999995 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.19000006	2.19000006 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.70019531	-7.70019531 ± 9.77E-04	<b>~</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•

T			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.59 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6
AssistFirewall ActiveKSV M str.K Uls f32	0.715390444
AssistFirewall_ActiveRawAcc_Cnt_M_u16	6027
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	-4.69999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.40000006
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.05999994
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.0999999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.60000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0049999989
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.79999995
k AsstFWInpLimitHFA MtrNm f32	3.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	5.30000019
k_AsstFWNstep_Cnt_u16	4551
k_AsstFWPstep_Cnt_u16	3567
k RestoreThresh MtrNm f32	7.9000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2 AsstFWUprBoundX HwNm s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2 AsstFWUprBoundX HwNm s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336
2_1001 1. Optibodilov_1111111_0-p11[2][0]	



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
	-2040 0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	-14336
, , , , , , , , , , , , , , , , , , , ,	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2 AsstFWUprBoundX HwNm s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	4096
- 1	



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-24576	
	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]		
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048	
	-2040	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-4096	
	-1000	



lame  2_AsstFWUprBoundY_MtrNm_s4p11[7][4]  2_AsstFWUprBoundY_MtrNm_s4p11[7][5]  2_AsstFWUprBoundY_MtrNm_s4p11[7][6]  2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	Input Value -2048
P_AsstFWUprBoundY_MtrNm_s4p11[7][5] P_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
	4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
_AsstFWDefltAssistX_HwNm_u8p8[0]	538
_AsstFWDefltAssistX_HwNm_u8p8[1]	563
_AsstFWDefltAssistX_HwNm_u8p8[2]	589
_AsstFWDefltAssistX_HwNm_u8p8[3]	614
_AsstFWDefltAssistX_HwNm_u8p8[4]	640
_AsstFWDefltAssistX_HwNm_u8p8[5]	666
_AsstFWDefltAssistX_HwNm_u8p8[6]	691
_AsstFWDefltAssistX_HwNm_u8p8[7]	717
_AsstFWDefltAssistX_HwNm_u8p8[8]	742
_AsstFWDefltAssistX_HwNm_u8p8[9]	768
_AsstFWDefltAssistX_HwNm_u8p8[10]	794
_AsstFWDefltAssistX_HwNm_u8p8[11]	819
_AsstFWDefltAssistX_HwNm_u8p8[12]	845
_AsstFWDefltAssistX_HwNm_u8p8[13]	870
_AsstFWDefltAssistX_HwNm_u8p8[14]	896
_AsstFWDefltAssistX_HwNm_u8p8[15]	922
_AsstFWDefltAssistX_HwNm_u8p8[16]	947
_AsstFWDefltAssistX_HwNm_u8p8[17]	973
_AsstFWDefltAssistX_HwNm_u8p8[18]	998
_AsstFWDefltAssistX_HwNm_u8p8[19]	1024
_AsstFWDefltAssistY_MtrNm_s4p11[0]	13926
_AsstFWDefltAssistY_MtrNm_s4p11[1]	14131
_AsstFWDefltAssistY_MtrNm_s4p11[2]	14336
_AsstFWDefltAssistY_MtrNm_s4p11[3]	14541
_AsstFWDefltAssistY_MtrNm_s4p11[4]	14746
AsstFWDefltAssistY_MtrNm_s4p11[5]	14950
AsstFWDefltAssistY_MtrNm_s4p11[6]	15155
AsstFWDefltAssistY_MtrNm_s4p11[7]	15360
AsstFWDefltAssistY_MtrNm_s4p11[8]	15565
AsstFWDefltAssistY_MtrNm_s4p11[9]	15770
AsstFWDefltAssistY_MtrNm_s4p11[10]	15974
AsstFWDefltAssistY_MtrNm_s4p11[11]	16179
AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
AsstFWDefltAssistY_MtrNm_s4p11[13]	16589
AsstFWDefltAssistY_MtrNm_s4p11[14]	16794
AsstFWDefltAssistY_MtrNm_s4p11[15]	16998
AsstFWDefitAssistY_MtrNm_s4p11[16]	17203
AsstFWDefltAssistY_MtrNm_s4p11[17]	17408
AsstFWDefltAssistY_MtrNm_s4p11[18]	17613
AsstFWDefltAssistY_MtrNm_s4p11[19]	17818
AsstFWPstepNstepThresh_Cnt_u16[0]	180
AsstFWPstepNstepThresh_Cnt_u16[1]	439
AsstFWVehSpd_Kph_u9p7[0]	1408
AsstFWVehSpd_Kph_u9p7[1]	1536
AsstFWVehSpd_Kph_u9p7[1] AsstFWVehSpd_Kph_u9p7[2]	1664
AsstFWVehSpd_Kph_u9p7[3]	1792
AsstFWVehSpd_Kph_u9p7[4]	1920
AsstFWVehSpd_Kph_u9p7[5]	2048
AsstFWVehSpd_Kph_u9p7[6]	2176
AsstFWVehSpd_Kph_u9p7[7]	2304
rt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2.20000005
pt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
pt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.099999
pt_AssistFirewall_Per1_HighFreqAssist_MtrNm_r32.value pt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	6.0999999
pt_AssistFirewall_Per1_mwTorque_mwNrn_i3z.value pt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3
	3  1
t_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	
pt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	50.2999992
pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt	
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.70765734	1.70765722 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	439	439 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.70019531	8.70019531 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.51999998	6.51999998 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.44000006	5.44000006 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.9849999	3.9849999 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.70019531	8.70019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.60 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7
AssistFirewall ActiveKSV M str.K Uls f32	0.5
AssistFirewall ActiveRawAcc Cnt M u16	6150
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.5
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.07000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.090000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00600000005
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.9000001
k_AsstFWInpLimitHFA_MtrNm_f32	3.79999995
k_AsstFWInpLimitHysComp_MtrNm_f32	5.5
k_AsstFWNstep_Cnt_u16	4674
k_AsstFWPstep_Cnt_u16	3690
k_RestoreThresh_MtrNm_f32	8
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3] t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	2048
	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	6144



		( 10
Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-12288	
	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]		
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096	
	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]		
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048	



Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] 12288 t_AsstFWDefltAssistX_HwNm_u8p8[0] 563 t_AsstFWDefltAssistX_HwNm_u8p8[1] 589 t_AsstFWDefltAssistX_HwNm_u8p8[2] 614 t_AsstFWDefltAssistX_HwNm_u8p8[3] 640 t_AsstFWDefltAssistX_HwNm_u8p8[4] 666 t_AsstFWDefltAssistX_HwNm_u8p8[6] 717 t_AsstFWDefltAssistX_HwNm_u8p8[6] 717 t_AsstFWDefltAssistX_HwNm_u8p8[7] 742 t_AsstFWDefltAssistX_HwNm_u8p8[8] 768 t_AsstFWDefltAssistX_HwNm_u8p8[9] 794 t_AsstFWDefltAssistX_HwNm_u8p8[10] 819 t_AsstFWDefltAssistX_HwNm_u8p8[11] 845 t_AsstFWDefltAssistX_HwNm_u8p8[12] 870	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] 12288 t_AsstFWDefitAssistX_HwNm_u8p8[0] 563 t_AsstFWDefitAssistX_HwNm_u8p8[1] 589 t_AsstFWDefitAssistX_HwNm_u8p8[2] 614 t_AsstFWDefitAssistX_HwNm_u8p8[3] 640 t_AsstFWDefitAssistX_HwNm_u8p8[4] 666 t_AsstFWDefitAssistX_HwNm_u8p8[5] 691 t_AsstFWDefitAssistX_HwNm_u8p8[6] 717 t_AsstFWDefitAssistX_HwNm_u8p8[7] 742 t_AsstFWDefitAssistX_HwNm_u8p8[8] 768 t_AsstFWDefitAssistX_HwNm_u8p8[9] 794 t_AsstFWDefitAssistX_HwNm_u8p8[10] 819 t_AsstFWDefitAssistX_HwNm_u8p8[11] 845 t_AsstFWDefitAssistX_HwNm_u8p8[12] 870	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] 12288 t_AsstFWDefltAssistX_HwNm_u8p8[0] 563 t_AsstFWDefltAssistX_HwNm_u8p8[1] 589 t_AsstFWDefltAssistX_HwNm_u8p8[2] 614 t_AsstFWDefltAssistX_HwNm_u8p8[3] 640 t_AsstFWDefltAssistX_HwNm_u8p8[4] 666 t_AsstFWDefltAssistX_HwNm_u8p8[5] 691 t_AsstFWDefltAssistX_HwNm_u8p8[6] 717 t_AsstFWDefltAssistX_HwNm_u8p8[7] 742 t_AsstFWDefltAssistX_HwNm_u8p8[8] 768 t_AsstFWDefltAssistX_HwNm_u8p8[9] 794 t_AsstFWDefltAssistX_HwNm_u8p8[10] 819 t_AsstFWDefltAssistX_HwNm_u8p8[11] 845 t_AsstFWDefltAssistX_HwNm_u8p8[12] 870	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]       10240         t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]       12288         t_AsstFWDefltAssistX_HwNm_u8p8[0]       563         t_AsstFWDefltAssistX_HwNm_u8p8[1]       589         t_AsstFWDefltAssistX_HwNm_u8p8[2]       614         t_AsstFWDefltAssistX_HwNm_u8p8[3]       640         t_AsstFWDefltAssistX_HwNm_u8p8[4]       666         t_AsstFWDefltAssistX_HwNm_u8p8[5]       691         t_AsstFWDefltAssistX_HwNm_u8p8[6]       717         t_AsstFWDefltAssistX_HwNm_u8p8[7]       742         t_AsstFWDefltAssistX_HwNm_u8p8[8]       768         t_AsstFWDefltAssistX_HwNm_u8p8[9]       794         t_AsstFWDefltAssistX_HwNm_u8p8[10]       819         t_AsstFWDefltAssistX_HwNm_u8p8[11]       845         t_AsstFWDefltAssistX_HwNm_u8p8[12]       870	
12_AsstFWUprBoundY_MtrNm_s4p11[7][10]       12288         t_AsstFWDefltAssistX_HwNm_u8p8[0]       563         t_AsstFWDefltAssistX_HwNm_u8p8[1]       589         t_AsstFWDefltAssistX_HwNm_u8p8[2]       614         t_AsstFWDefltAssistX_HwNm_u8p8[3]       640         t_AsstFWDefltAssistX_HwNm_u8p8[4]       666         t_AsstFWDefltAssistX_HwNm_u8p8[5]       691         t_AsstFWDefltAssistX_HwNm_u8p8[6]       717         t_AsstFWDefltAssistX_HwNm_u8p8[7]       742         t_AsstFWDefltAssistX_HwNm_u8p8[8]       768         t_AsstFWDefltAssistX_HwNm_u8p8[10]       819         t_AsstFWDefltAssistX_HwNm_u8p8[11]       845         t_AsstFWDefltAssistX_HwNm_u8p8[12]       870	
t_AsstFWDefitAssistX_HwNm_u8p8[0]       563         t_AsstFWDefitAssistX_HwNm_u8p8[1]       589         t_AsstFWDefitAssistX_HwNm_u8p8[2]       614         t_AsstFWDefitAssistX_HwNm_u8p8[3]       640         t_AsstFWDefitAssistX_HwNm_u8p8[4]       666         t_AsstFWDefitAssistX_HwNm_u8p8[5]       691         t_AsstFWDefitAssistX_HwNm_u8p8[6]       717         t_AsstFWDefitAssistX_HwNm_u8p8[7]       742         t_AsstFWDefitAssistX_HwNm_u8p8[8]       768         t_AsstFWDefitAssistX_HwNm_u8p8[9]       794         t_AsstFWDefitAssistX_HwNm_u8p8[10]       819         t_AsstFWDefitAssistX_HwNm_u8p8[11]       845         t_AsstFWDefitAssistX_HwNm_u8p8[12]       870	
t_AsstFWDefitAssistX_HwNm_u8p8[1]       589         t_AsstFWDefitAssistX_HwNm_u8p8[2]       614         t_AsstFWDefitAssistX_HwNm_u8p8[3]       640         t_AsstFWDefitAssistX_HwNm_u8p8[4]       666         t_AsstFWDefitAssistX_HwNm_u8p8[5]       691         t_AsstFWDefitAssistX_HwNm_u8p8[6]       717         t_AsstFWDefitAssistX_HwNm_u8p8[7]       742         t_AsstFWDefitAssistX_HwNm_u8p8[8]       768         t_AsstFWDefitAssistX_HwNm_u8p8[9]       794         t_AsstFWDefitAssistX_HwNm_u8p8[10]       819         t_AsstFWDefitAssistX_HwNm_u8p8[11]       845         t_AsstFWDefitAssistX_HwNm_u8p8[12]       870	
t_AsstFWDefitAssistX_HwNm_u8p8[2]       614         t_AsstFWDefitAssistX_HwNm_u8p8[3]       640         t_AsstFWDefitAssistX_HwNm_u8p8[4]       666         t_AsstFWDefitAssistX_HwNm_u8p8[5]       691         t_AsstFWDefitAssistX_HwNm_u8p8[6]       717         t_AsstFWDefitAssistX_HwNm_u8p8[7]       742         t_AsstFWDefitAssistX_HwNm_u8p8[8]       768         t_AsstFWDefitAssistX_HwNm_u8p8[9]       794         t_AsstFWDefitAssistX_HwNm_u8p8[10]       819         t_AsstFWDefitAssistX_HwNm_u8p8[11]       845         t_AsstFWDefitAssistX_HwNm_u8p8[12]       870	
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t_AsstFWDefltAssistX_HwNm_u8p8[4] 666 t_AsstFWDefltAssistX_HwNm_u8p8[5] 691 t_AsstFWDefltAssistX_HwNm_u8p8[6] 717 t_AsstFWDefltAssistX_HwNm_u8p8[7] 742 t_AsstFWDefltAssistX_HwNm_u8p8[8] 768 t_AsstFWDefltAssistX_HwNm_u8p8[9] 794 t_AsstFWDefltAssistX_HwNm_u8p8[10] 819 t_AsstFWDefltAssistX_HwNm_u8p8[11] 845 t_AsstFWDefltAssistX_HwNm_u8p8[12] 870	
t_AsstFWDefltAssistX_HwNm_u8p8[5]       691         t_AsstFWDefltAssistX_HwNm_u8p8[6]       717         t_AsstFWDefltAssistX_HwNm_u8p8[7]       742         t_AsstFWDefltAssistX_HwNm_u8p8[8]       768         t_AsstFWDefltAssistX_HwNm_u8p8[9]       794         t_AsstFWDefltAssistX_HwNm_u8p8[10]       819         t_AsstFWDefltAssistX_HwNm_u8p8[11]       845         t_AsstFWDefltAssistX_HwNm_u8p8[12]       870	
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t_AsstFWDefltAssistX_HwNm_u8p8[7]       742         t_AsstFWDefltAssistX_HwNm_u8p8[8]       768         t_AsstFWDefltAssistX_HwNm_u8p8[9]       794         t_AsstFWDefltAssistX_HwNm_u8p8[10]       819         t_AsstFWDefltAssistX_HwNm_u8p8[11]       845         t_AsstFWDefltAssistX_HwNm_u8p8[12]       870	
t_AsstFWDefltAssistX_HwNm_u8p8[8]       768         t_AsstFWDefltAssistX_HwNm_u8p8[9]       794         t_AsstFWDefltAssistX_HwNm_u8p8[10]       819         t_AsstFWDefltAssistX_HwNm_u8p8[11]       845         t_AsstFWDefltAssistX_HwNm_u8p8[12]       870	
t_AsstFWDefltAssistX_HwNm_u8p8[9]       794         t_AsstFWDefltAssistX_HwNm_u8p8[10]       819         t_AsstFWDefltAssistX_HwNm_u8p8[11]       845         t_AsstFWDefltAssistX_HwNm_u8p8[12]       870	
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t_AsstFWDefitAssistY_MtrNm_s4p11[18] 17818	
t_AsstFWDefitAssistY_MtrNm_s4p11[19] 18022	
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t_AsstFWVehSpd_Kph_u9p7[0] 4352	
t_AsstFWVehSpd_Kph_u9p7[1] 4480	
t_AsstFWVehSpd_Kph_u9p7[2] 4608	
t_AsstFWVehSpd_Kph_u9p7[3] 4736	
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t_AsstFWVehSpd_Kph_u9p7[6] 5120	
t_AsstFWVehSpd_Kph_u9p7[7] 5248	
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value 3.0999999	
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value 0	
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value 1	
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value 3	
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value 2	
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value 2	
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value 60.4000015	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32	



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.5	3.5 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1476	1476 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.70019531	7.70019531 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.85000014	1.85000002 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.26999998	1.26999998 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.96999979	4.96999979 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	7.70019531	7.70019531 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>~</b>

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8
AssistFirewall ActiveKSV M str.K Uls f32	0.100000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	6273
AssistFirewall_ActiveNawAcc_Cit_M_uT0	1
AssistFirewall_AssixTeducedFeH3V_CHI_W_igc	-4.9000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-52.7999992
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.60000024
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.08000004
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2
AssistFirewall LwrBoundKSV M str.K Uls f32	0.100000001
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00700000022
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
<_AsstFWInpLimitBaseAsst_MtrNm_f32	3
AsstFWInpLimitHFA MtrNm f32	4
<_AsstFWInpLimitHysComp_MtrNm_f32	5.69999981
<_AsstFWNstep_Cnt_u16	3567
<_AsstFWPstep_Cnt_u16	3813
RestoreThresh MtrNm f32	8.10000038
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
2 AsstFWUprBoundX HwNm s4p11[0][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_Asst WopiBoundX_HwNm_s4p11[6][2]	-2048
	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
12_ASSII WODIDOUNUT_WITHIN_S4PTT[O][O]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048 0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048 0



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-2048	
	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]		
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	16384	
12_Asst WorlboundY_MtrNm_s4p11[2][8]	18432	
12_ASSIFWOPIBOUNDY_MINNIT_S4P11[2][8] 12_ASSIFWUprBoundY_MtrNm_s4p11[2][9]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240	
	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240	
	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]		
12_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144	
t2_Asst WoprBoundY_MtrNm_s4p11[7][0]	-6144	
	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	0	



2.ABSPW_ADBROACH_AD	Name	Input Value
P. ASSPENIQUEDONIA, Minthon, 19911795   9144   D. ASSPENIQUEDONIA, Minthon, 19911795   9144   D. ASSPENIQUEDONIA, Minthon, 19911795   9192   D. ASSPENIQUEDONIA, Minthon, 19911795   9192   D. ASSPENIQUEDONIA, Minthon, 19911795   9192   D. ASSPENIQUEDONIA, Minthon, 19911795   9193   D. ASSPENIQUEDONIA, Minthon, 19911796   9193   D. ASSPENIQUEDONIA, Minthon, 19911796   9194   D. ASSPENIQUEDONIA, Minthon, 19911797   9194   D. ASSPENIQUEDONIA, Minthon, 19911797   9194   D. ASSPENIQUEDONIA, Minthon, 19911797   9194   D. ASSPENIQUEDONIA, Minthon, 1991179   9194   D. ASSPEN		
12. AGENTYURPROSENTY   Minima _psi_11719    1942   2. AGENTYURPROSENTY   Minima _psi_11719    1928   3. AGENTYURPROSENTY   Minima _psi_11719    1928   3. AGENTYURPROSENTY   Minima _psi_11719    1928   4. AGENTYURPROSENTY   Minima _psi_11719    1928   4. AGENTYURPROSENTY   Minima _psi_11719    1928   4. AGENTYURPROSENTY   Minima _psi_11719    1929   4. AGENTYURPROSENTY   Minima _psi_11719		
2. AGENTYUJIPOGONY   JAMPA   SEPTITIFE    1040		
20. ASPER   10. ASPECT   10.		
2.4881FW/pitcours/_Nofem_step11799   1298		
12.848FW/MASSACK, Jankin, Jankin   14336   1	, , , , , , , , , , , , , , , , , , , ,	
Laces Proceins ages   Leven		
Laces TVORIRADARS, JANNIN, LapiR10]		
Least PVORHASSIEN, Harbinuipi012  066   Acces PVORHASSIEN, Harbinuipi012  077   Acces PVORHASSIEN, Harbinuipi012  772   Acces PVORHASSIEN, Harbinuipi012  784   Acces PVORHASSIEN, Harbinuipi012  784   Acces PVORHASSIEN, Harbinuipi012  784   Acces PVORHASSIEN, Harbinuipi012  784   Acces PVORHASSIEN, Harbinuipi012  819   Acces PVORHASSIEN, Harbinuipi012  819   Acces PVORHASSIEN, Harbinuipi013  922   Acces PVORHASSIEN, Harbinuipi013  922   Acces PVORHASSIEN, Harbinuipi013  922   Acces PVORHASSIEN, Harbinuipi013  922   Acces PVORHASSIEN, Harbinuipi013  927   Acces PVORHASSIEN, Harbinuipi013  927   Acces PVORHASSIEN, Harbinuipi013  937   Acces PVORHASSIEN, H	t_AsstFWDefltAssistX_HwNm_u8p8[0]	589
LABSET/VERHÖRSSET, HANNIN, 1998 01   001   LABSET/VERHÖRSSET, HANNIN, 1998 01   742   LABSET/VERHÖRSSET, HANNIN, 1998 01   742   LABSET/VERHÖRSSET, HANNIN, 1998 01   742   LABSET/VERHÖRSSET, HANNIN, 1998 01   743   LABSET/VERHÖRSSET, HANNIN, 1998 01   045   LABSET/VERHÖRSSET, HANNIN, 1998 01   045   LABSET/VERHÖRSSET, HANNIN, 1998 01   070   LABSET/VERHÖRSSET, HANNIN, 1999 01   070   LABSET/VERHÖRSSET, HANN	t_AsstFWDefltAssistX_HwNm_u8p8[1]	614
CARST WORTHASSEN, EARN-DUBBES   717   72   72   73   74   74   75   75   75   75   75   75	t_AsstFWDefltAssistX_HwNm_u8p8[2]	640
Laces FW0elfastes News   Legist	t_AsstFWDefltAssistX_HwNm_u8p8[3]	666
Aces   North-Aces   North-Ace	t_AsstFWDefltAssistX_HwNm_u8p8[4]	691
AssENDentAssist Newhon upplips	t AsstFWDefltAssistX HwNm u8p8[5]	717
Asset NOPHARASEK Harbin Lipid   744   Asset North Asset Name   Asset Name   Asset North Asset Name   Asse		
LABST WORTASSICK HANNIN Lippil (1)		
Laser Worlflasseist, Hwhen   Lapel 10   945   945   945   946   945   946	· · · ·	
Laser WorthAssist J. Hwhm   ubg8[1]   870     Assist WorthAssist J. Hwhm   ubg8[1]   870     Assist WorthAssist J. Hwhm   ubg8[1]   870     Assist WorthAssist J. Hwhm   ubg8[1]   971     Laser WorthAssist J. Hwhm   ubg8[1]   972     Laser WorthAssist J. Hwhm   ubg8[1]   973     Assist WorthAssist J. Hwhm   ubg8[1]   973     Assist WorthAssist J. Hwhm   ubg8[1]   1024     Assist WorthAssist J. Hwhm   ubg8[1]   1024     Assist WorthAssist J. Hwhm   ubg8[1]   1025     Assist WorthAssist J. Hwhm   ubg8[1]   1075     Assist WorthAssist J. Hwhm   ubg9[1]   1494     Laser WorthAssist J. Hwhm   ubg9[1]   1495     Assist WorthAssist J. Hwhm   ubg9[1]   1495     Assist WorthAssist J. Hwhm   ubg9[1]   1590     Assist WorthAssist J. Hwhm   ubg9[1]   1590     Assist WorthAssist J. Hwhm   ubg9[1]   1590     Assist WorthAssist J. Hwhm   ubg9[1]   1677     Assist WorthAssist J. Hwhm   ubg9[1]   1679     Assist WorthAssist J. Hwhm   ubg9[1]		
AssiTVPORHASSIST, HwbM, ubg8112  870   AssiTVPORHASSIST, HwbM, ubg812  896   AssiTVPORHASSIST, HwbM, ubg813  922   AssiTVPORHASSIST, HwbM, ubg813  927   AssiTVPORHASSIST, HwbM, ubg813  928   AssiTVPORHASSIST, HwbM, ubg813  928   AssiTVPORHASSIST, HwbM, ubg813  1050   AssiTVPORHASSIST, HwbM, ubg913  1050   AssiTVPORHASSIST, MwbM, ubg913  14336   AssiTVPORHASSIST, MwbM, ubg913  1456   AssiTVPORHASSIST, MwbM, ubg913  1556   AssiTVPORHASSIST, MwbM, ubg913  1556   AssiTVPORHASSIST, MwbM, ubg913  1556   AssiTVPORHASSIST, MwbM, ubg913  1556   AssiTVPORHASSIST, MwbM, ubg913  15570   AssiTVPORHASSIST, MwbM, ubg913  15570   AssiTVPORHASSIST, MwbM, ubg913  15770   AssiTVPORHASSIST, MwbM, ubg9		
LastFVPOMIAsaistX Hwhm usp8[12]   886     LastFVPOMIAsaistX Hwhm usp8[13]   92     LastFVPOMIAsaistX Hwhm usp8[14]   947     LastFVPOMIAsaistX Hwhm usp8[14]   947     LastFVPOMIAsaistX Hwhm usp8[15]   1024     LastFVPOMIAsaistX Hwhm usp8[17]   1024     LastFVPOMIAsaistX Hwhm usp8[17]   1024     LastFVPOMIAsaistX Hwhm usp8[18]   1050     LastFVPOMIAsaistX Hwhm usp8[19]   1075     LastFVPOMIAsaistX Hwhm usp8[19]   1076     LastFVPOMIAsaistX Hwhm usp8[19]   1076     LastFVPOMIAsaistX Hwhm usp8[19]   14541     LastFVPOMIAsaistX Hwhm usp8[19]   14540     LastFVPOMIAsaistX Hwhm usp8[19]   14590     LastFVPOMIAsaistX Hwhm usp8[19]   14590     LastFVPOMIAsaistX Hwhm usp8[19]   14590     LastFVPOMIAsaistX Hwhm usp8[19]   14590     LastFVPOMIAsaistX Hwhm usp8[19]   15790     LastFVPOMIAsaistX Hwhm usp8[19]   15790     LastFVPOMIAsaistX Hwhm usp8[19]   15790     LastFVPOMIAsaistX Hwhm usp8[19]   16790     LastFVPOMIAsaistX Hwhm usp8[19]   17406     LastFVPOMIAsaistX Hwhm usp8[19]   17		
Asser/PodenAssiex/ Hewhr up9813  92   Asser/PodenAssiex/ Hewhr up9814  967   Asser/PodenAssiex/ Hewhr up9814  973   Asser/PodenAssiex/ Hewhr up9817  1024   Asser/PodenAssiex/ Minh up9817  1036   Asser/PodenAssiex/ Minh up9817  1136   Asser/PodenAssiex/ Minh up9817  11436   Asser/PodenAssiex/ Minh up9817  1156   Asser/PodenAssiex/ Minh up9817  1157   Asser/PodenAssiex/ Minh up9817  1158   Asser/PodenAssiex/ Minh up9818  1159   Asser/Pode	t_AsstFWDefltAssistX_HwNm_u8p8[11]	870
LassIPVDelfiAssistX_HeNm_usQR1143   947	t_AsstFWDefltAssistX_HwNm_u8p8[12]	896
LassiPVDRIBASSIX   Mehru   Lipi0[15]   973	t_AsstFWDefltAssistX_HwNm_u8p8[13]	922
LassFWPMRAssiX   Mehru   1981 15    1050	t_AsstFWDefltAssistX_HwNm_u8p8[14]	947
LassPNPMRAssisX, Hohm.uspR16]	t_AsstFWDefltAssistX_HwNm_u8p8[15]	973
L AssEPWDelfAssistX, Hwhm_usbplt19		
LASSIFWDelflAcsistY, Minkin_s4p110		
LassiFWoelhAssistY_Minkm_s4p110    14356	, ; ;	
LASSIP/DelftAssistY_Minns_s4p110    14336   14366		
LASSIFW/DelfiAssistY_Minkm_s4p11[2]   14541   14746		
LASSIFW/DelfAssistY_Minkm_sdp11[2]		
LASSIFWDelftAssistY_Minkm_sip11[4]   1555	,	
AssiFWDeltAssistY_MtrNm_s4p116    15155   15360	t_AsstFWDefltAssistY_MtrNm_s4p11[2]	14746
AssIFWDelftAssistY_MtrNm_s4p11[6]   15360   15565   15565   15565   15565   15565   15565   15565   15565   15565   15565   15565   15570	t_AsstFWDefltAssistY_MtrNm_s4p11[3]	14950
AssiFWDefitAssistY_Mrthm_sdp11[6]   15565   15770	t_AsstFWDefltAssistY_MtrNm_s4p11[4]	15155
LASSIFWDeftNassistY_MirNm_s4p11 0  15974	t_AsstFWDefltAssistY_MtrNm_s4p11[5]	15360
LASSIFWORTHASSISTY_MITNITN_s4p11 8    1679	t_AsstFWDefltAssistY_MtrNm_s4p11[6]	15565
LASSIFWOERTASSISY_MITNIN_s4p11[8]   1679   16179   16384   1	t AsstFWDefltAssistY MtrNm s4p11[7]	15770
LASSIFWDeftNasistry_MtrNm_s4p11[10] 16394  LASSIFWDeftNasistry_MtrNm_s4p11[11] 16589  LASSIFWDeftNasistry_MtrNm_s4p11[12] 16794  LASSIFWDeftNasistry_MtrNm_s4p11[13] 16998  LASSIFWDeftNasistry_MtrNm_s4p11[14] 17203  LASSIFWDeftNasistry_MtrNm_s4p11[15] 17408  LASSIFWDeftNasistry_MtrNm_s4p11[16] 17613  LASSIFWDeftNasistry_MtrNm_s4p11[16] 17613  LASSIFWDeftNasistry_MtrNm_s4p11[17] 17818  LASSIFWDeftNasistry_MtrNm_s4p11[17] 17818  LASSIFWDeftNasistry_MtrNm_s4p11[19] 18227  LASSIFWDeftNasistry_MtrNm		
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L AssIFWDefitAssistY_MtrNm_s4p11[17]	t_AsstFWDefltAssistY_MtrNm_s4p11[15]	17408
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LAsstFWDefthAssistY_MtrNm_s4p11[19]	t_AsstFWDefltAssistY_MtrNm_s4p11[17]	17818
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L AssIFWPstepNstepThresh_Cnt_u16[0]		18227
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tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value  0  70.0999985  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AssistFirewall_Per1_BaseAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_AssistFirewall_Per1_AsstFirewall_Per1_LighFreqAssist_MtrNm_f32  tgt_AssistFirewall_Per1_LysteresisComp_MtrNm_f32  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
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tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_AssistFirewall_Per1_AsstFirewall_Per1_BaseAssistCmd_MtrNm_f32  tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32  tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Servic	•	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AssistDl_Service_Cnt_lt tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lt tgt_AssistFirewall_	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	70.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_k  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_k  tgt_AssistFirewall_Per1_LysteresisComp_MtrNm_f32  tgt_AssistFirewall_Per1_LysteresisComp_MtrNm_f32  tgt_AssistFirewall_Per1_LysteresisComp_MtrNm_f32  tgt_AssistFirewall_Per1_LysteresisComp_MtrNm_f32	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	2 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f3	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f:	32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32	•	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32	-	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32	• • • • • • • • • • • • • • • • • • • •	
		, , ,
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32	-	



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7.19999981	7.19999981 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	447	447 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.70019531	8.70019531 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-16.3199997	-16.3199997 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.0999999	2.0999999 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.96500015	5.96500015 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.70019531	8.70019531 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>~</b>

Τ				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Name	Step 2.62 (Repeat Count = 1)	v v
AssistFirewall_ActiveRawAcc_Cnt_M_u16 6396 AssistFirewall_AssiReducedPerfSV_Cnt_M_gc 1 AssistFirewall_CombAssiSV_MtrNn_M_132 5 AssistFirewall_HiFreqKSV_M_str_LPF_Str_SV_UIs_132 5 AssistFirewall_HiFreqKSV_M_str_LPF_Str_SV_UIs_132 0.090000036 AssistFirewall_HiFreqKSV_M_str_LPF_Str_SV_UIs_132 0.090000036 AssistFirewall_HiFreqKSV_M_str_LPF_Str_SV_UIs_132 1.09000003 AssistFirewall_LwrBoundKSV_M_str_LPF_Str_SV_UIs_132 3 AssistFirewall_LwrBoundKSV_M_str_LPF_Str_SV_UIs_132 1.09000003 AssistFirewall_LwrBoundKSV_M_str_K_UIs_132 0.20000003 AssistFirewall_LyrBoundKSV_M_str_K_UIs_132 0.20000003 AssistFirewall_UprBoundKSV_M_str_SV_UIs_132 7 AssistFirewall_UprBoundKSV_M_str_SV_UIs_132 7 AssistFirewall_UprBoundKSV_M_str_SV_UIs_132 7 AssistFirewall_UprBoundKSV_M_str_SV_UIs_132 7 AssistFirewall_UprBoundKSV_M_str_SV_UIs_132 1.000000000000000000000000000000000000		Input Value
AssistFirewall ActiveRsvAc_Cnt_M_u16 6396 AssistFirewall_ActiveRawAc_Cnt_M_u16 6396 AssistFirewall_AssistAeducedFotSv_Cnt_M_u16 1 AssistFirewall_AssistAeducedFotSv_Cnt_M_u16 1 AssistFirewall_HiFreqKSv_M_str_LPF_Str_Sv_Uls_J32 5.7999992 AssistFirewall_HiFreqKSv_M_str_LPF_Str_Sv_Uls_J32 0.090000036 AssistFirewall_HiFreqKSv_M_str_LPF_Str_Sv_Uls_J32 1.09000003 AssistFirewall_LwrBoundKSv_M_str_LPF_Str_Sv_Uls_J32 1.09000003 AssistFirewall_LwrBoundKSv_M_str_K_Uls_J32 0.20000003 AssistFirewall_WrBoundKSv_M_str_K_Uls_J32 1.09000003 AssistFirewall_UwrBoundKSv_M_str_K_Uls_J32 0.20000003 AssistFirewall_UwrBoundKSv_M_str_Sv_Uls_J32 7 AssistFirewall_UprBoundKSv_M_str_Sv_Uls_J32 7 AssistFirewall_UprBoundKSv_M_str_Sv_Uls_J32 7 AssistFirewall_UprBoundKSv_M_str_Sv_Uls_J32 7 AssistFirewall_UprBoundKSv_M_str_Sv_Uls_J32 0.0080000038 Rte_Inst_D_A_SsistFirewall 1 tgt_Re_Inst_D_A_ssistFirewall k_AsstFWInpLimitBaseAsst_MtrNm_J32 3.099999 k_AsstFWInpLimitBaseAsst_MtrNm_J32 4.1999981 k_AsstFWInpLimitHyAComp_MtrNm_J32 4.1999981 k_AsstFWInpLimitHyAComp_MtrNm_J32 8.19999981 k_AsstFWDstep_Cnt_u16 3936 k_AsstFWDstep	irewall ActiveKSV M str.SV Uls f32	·
AssistFirewall_ActiveRawAcc_Cnt_M_u16 AssistFirewall_CombAsstSV_Mrtm_M_132 AssistFirewall_CombAsstSV_Mrtm_M_132 AssistFirewall_HiFreqKSV_M_str.LPF_Str.Sv_Uls_132 AssistFirewall_HiFreqKSV_M_str.LPF_Str.Sv_Uls_132 AssistFirewall_HiFreqKSV_M_str.LPF_Str.Sv_Uls_132 AssistFirewall_LifereqKSV_M_str.LPF_Str.Sv_Uls_132 AssistFirewall_LifereqKSV_M_str.LP_Uls_132 AssistFirewall_LwrBoundKSV_M_str.Sv_Uls_132 AssistFirewall_LwrBoundKSV_M_str.Sv_Uls_132 AssistFirewall_LwrBoundKSV_M_str.Sv_Uls_132 AssistFirewall_UrpBoundKSV_M_str.Sv_Uls_132 AssistFirewall_UprBoundKSV_M_str.Sv_Uls_132 AssistFirewall_UprBoundK_HiMn_f32 AssistFirewall_UprBoundK_HiMn_f32 AssistFirewall_UprBoundK_HiMn_s4p11[0][0] AssistFirewall_UprBoundX_HiMn_s4p11[0][0] AssistFirewall_UprBoundX_Himn_s4p11[0]		
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc		
AssistFirewall_UnFoundKsty_M_str.LPF_Str.Sv_Uis_f32 52.799992 AssistFirewall_HiFreqKSV_M_str.LPF_Str.Sv_Uis_f32 0.090000036 AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uis_f32 1.09000003 AssistFirewall_HiFreqKSV_M_str.CF_Uis_f32 1.09000003 AssistFirewall_LwrBoundKSV_M_str.Sv_Uis_f32 3.AssistFirewall_LwrBoundKSV_M_str.Sv_Uis_f32 3.AssistFirewall_LwrBoundKSV_M_str.Sv_Uis_f32 0.200000003 AssistFirewall_UnFoundKSV_M_str.K_Uis_f32 0.200000003 AssistFirewall_UprBoundKSV_M_str.K_Uis_f32 7.AssistFirewall_UprBoundKSV_M_str.K_Uis_f32 7.AssistFirewall_UprBoundKSV_M_str.K_Uis_f32 0.0080000038 Rte_Inst_Ap_AssistFirewall UprBoundKSV_M_str.K_Uis_f32 0.0080000038 Rte_Inst_Ap_AssistFirewall LyrBoundKSV_M_str.K_Uis_f32 1.0999999 k_AsstFWInpLimitHsAp_Assist_MitNm_f32 1.9999999999 k_AsstFWInpLimitHsAp_Assist_MitNm_f32 1.999999999999999999999999999999999999		
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	•	
AssistFirewall_HiFreqKSV_M_str.CF_Str.K_Uls_f32		52.7999992
AssistFirewall_LHrPeqKSV_M_str.CF_Uls_f32         1.09000003           AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32         0.200000003           AssistFirewall_PNCountStatus_Cnt_M_lgc         1           AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32         7           AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32         7           AssistFirewall_UprBoundKSV_M_str.K_Uls_f32         0.0080000038           Rte_Inst_Ap_AssistFirewall         tgt_Rte_Inst_Ap_AssistFirewall           k_AsstFWInpLimitHFA_MtrNm_f32         3.0999999           k_AsstFWInpLimitHFA_MtrNm_f32         4.19999981           k_AsstFWInpLimitHysComp_MtrNm_f32         5.9000001           k_AsstFWInpLoundX_HwNm_s4p11[0][0]         3936           k_AsstFWUprBo_cnt_u16         3999981           k_AsstFWUprBoundX_HwNm_s4p11[0][0]         -16384           t2_AsstFWUprBoundX_HwNm_s4p11[0][0]         -14336           t2_AsstFWUprBoundX_HwNm_s4p11[0][1]         -14288           t2_AsstFWUprBoundX_HwNm_s4p11[0][3]         -10240           t2_AsstFWUprBoundX_HwNm_s4p11[0][4]         -8192           t2_AsstFWUprBoundX_HwNm_s4p11[0][6]         -4096           t2_AsstFWUprBoundX_HwNm_s4p11[0][6]         -4096           t2_AsstFWUprBoundX_HwNm_s4p11[0][8]         0           t2_AsstFWUprBoundX_HwNm_s4p11[0][8]         0 <tr< td=""><td>•</td><td>0.090000036</td></tr<>	•	0.090000036
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32 0.20000003 AssistFirewall_PNCountStatus_Cnt_M_lgc 1 AssistFirewall_UprBoundKSV_M_str.K_Uls_f32 7 AssistFirewall_UprBoundKSV_M_str.K_Uls_f32 7 AssistFirewall_UprBoundKSV_M_str.K_Uls_f32 7 AssistFirewall_UprBoundKSV_M_str.K_Uls_f32 0.0080000038 Rte_Inst_Ap_AssistFirewall tgt_Rte_Inst_Ap_AssistFirewall tgt_Rte_Inst_Ap_AssistFirew	•	1.09000003
AssistFirewall_PNCountStatus_Cnt_N_lgc	•	3
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 7 AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 7 AssistFirewall_UprBoundKSV_M_str.K_Uls_f32 0.00800000038  Rte_Inst_Ap_AssistFirewall tgt_Rte_Inst_Ap_AssistFirewall k_AsstFWInpLimitBaseAsst_MtrNm_f32 3.099999 k_AsstFWInpLimitHFA_MtrNm_f32 4.1999981 k_AsstFWInpLimitHysComp_MtrNm_f32 5.9000001 k_AsstFWNstep_Cnt_u16 3690 k_AsstFWPstep_Cnt_u16 3936 k_RestoreThresh_MtrNm_f32 8.1999981 t2_AsstFWDtpBoundX_HwNm_s4p11[0][0] -16384 t2_AsstFWDtpBoundX_HwNm_s4p11[0][1] -14336 t2_AsstFWDtpBoundX_HwNm_s4p11[0][2] -12288 t2_AsstFWUprBoundX_HwNm_s4p11[0][3] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[0][4] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[0][6] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[0][6] -6048 t2_AsstFWUprBoundX_H	irewall LwrBoundKSV M str.K Uls f32	0.200000003
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32 7 AssistFirewall_UprBoundKSV_M_str.K_Uls_f32 0.0080000038 Rte_Inst_Ap_AssistFirewall tgt_Rte_Inst_Ap_AssistFirewall tgt_Rte_Inst_Ap_AssistFirew		1
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32		7
Rte_Inst_Ap_AssistFirewall       tgt_Rte_Inst_Ap_AssistFirewall         k_AsstFWInpLimitBaseAsst_MtrNm_f32       3.0999999         k_AsstFWInpLimitHysComp_MtrNm_f32       4.1999981         k_AsstFWNstep_Cnt_u16       3690         k_AsstFWPstep_Cnt_u16       3936         k_RestoreThresh_MtrNm_f32       8.19999981         t2_AsstFWUprBoundX_HwNm_s4p11[0][0]       -16384         t2_AsstFWUprBoundX_HwNm_s4p11[0][1]       -14336         t2_AsstFWUprBoundX_HwNm_s4p11[0][2]       -12288         t2_AsstFWUprBoundX_HwNm_s4p11[0][3]       -10240         t2_AsstFWUprBoundX_HwNm_s4p11[0][4]       -8192         t2_AsstFWUprBoundX_HwNm_s4p11[0][5]       -6144         t2_AsstFWUprBoundX_HwNm_s4p11[0][6]       -4096         t2_AsstFWUprBoundX_HwNm_s4p11[0][7]       -2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][8]       0         t2_AsstFWUprBoundX_HwNm_s4p11[0][8]       0         t2_AsstFWUprBoundX_HwNm_s4p11[0][9]       2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][9]       2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][9]       2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][9]       4096	·	
k_AsstFWInpLimitHFA_MtrNm_f32       4.19999981         k_AsstFWInpLimitHysComp_MtrNm_f32       5.9000001         k_AsstFWNstep_Cnt_u16       3690         k_AsstFWPstep_Cnt_u16       3936         k_RestoreThresh_MtrNm_f32       8.19999981         t2_AsstFWUprBoundX_HwNm_s4p11[0][0]       -16384         t2_AsstFWUprBoundX_HwNm_s4p11[0][1]       -14336         t2_AsstFWUprBoundX_HwNm_s4p11[0][2]       -12288         t2_AsstFWUprBoundX_HwNm_s4p11[0][3]       -10240         t2_AsstFWUprBoundX_HwNm_s4p11[0][4]       -8192         t2_AsstFWUprBoundX_HwNm_s4p11[0][5]       -6144         t2_AsstFWUprBoundX_HwNm_s4p11[0][6]       -4096         t2_AsstFWUprBoundX_HwNm_s4p11[0][7]       -2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][8]       0         t2_AsstFWUprBoundX_HwNm_s4p11[0][9]       2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][10]       4096	·	
k_AsstFWInpLimitHFA_MtrNm_f32       4.19999981         k_AsstFWInpLimitHysComp_MtrNm_f32       5.9000001         k_AsstFWNstep_Cnt_u16       3690         k_AsstFWPstep_Cnt_u16       3936         k_RestoreThresh_MtrNm_f32       8.19999981         t2_AsstFWUprBoundX_HwNm_s4p11[0][0]       -16384         t2_AsstFWUprBoundX_HwNm_s4p11[0][1]       -14336         t2_AsstFWUprBoundX_HwNm_s4p11[0][2]       -12288         t2_AsstFWUprBoundX_HwNm_s4p11[0][3]       -10240         t2_AsstFWUprBoundX_HwNm_s4p11[0][4]       -8192         t2_AsstFWUprBoundX_HwNm_s4p11[0][5]       -6144         t2_AsstFWUprBoundX_HwNm_s4p11[0][6]       -4096         t2_AsstFWUprBoundX_HwNm_s4p11[0][7]       -2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][8]       0         t2_AsstFWUprBoundX_HwNm_s4p11[0][9]       2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][10]       4096	·	3.0999999
k_AsstFWInpLimitHysComp_MtrNm_f32       5.9000001         k_AsstFWNstep_Cnt_u16       3690         k_RestoreThresh_MtrNm_f32       8.19999981         t2_AsstFWUprBoundX_HwNm_s4p11[0][0]       -16384         t2_AsstFWUprBoundX_HwNm_s4p11[0][1]       -14336         t2_AsstFWUprBoundX_HwNm_s4p11[0][2]       -12288         t2_AsstFWUprBoundX_HwNm_s4p11[0][3]       -10240         t2_AsstFWUprBoundX_HwNm_s4p11[0][4]       -8192         t2_AsstFWUprBoundX_HwNm_s4p11[0][5]       -6144         t2_AsstFWUprBoundX_HwNm_s4p11[0][6]       -4096         t2_AsstFWUprBoundX_HwNm_s4p11[0][7]       -2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][8]       0         t2_AsstFWUprBoundX_HwNm_s4p11[0][9]       2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][10]       4096		
k_AsstFWNstep_Cnt_u16       3690         k_AsstFWPstep_Cnt_u16       3936         k_RestoreThresh_MtrNm_f32       8.19999981         t2_AsstFWUprBoundX_HwNm_s4p11[0][0]       -16384         t2_AsstFWUprBoundX_HwNm_s4p11[0][1]       -14336         t2_AsstFWUprBoundX_HwNm_s4p11[0][2]       -12288         t2_AsstFWUprBoundX_HwNm_s4p11[0][3]       -10240         t2_AsstFWUprBoundX_HwNm_s4p11[0][4]       -8192         t2_AsstFWUprBoundX_HwNm_s4p11[0][5]       -6144         t2_AsstFWUprBoundX_HwNm_s4p11[0][6]       -4096         t2_AsstFWUprBoundX_HwNm_s4p11[0][7]       -2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][8]       0         t2_AsstFWUprBoundX_HwNm_s4p11[0][9]       2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][10]       4096	·	5.9000001
k_AsstFWPstep_Cnt_u16       3936         k_RestoreThresh_MtrNm_f32       8.19999981         t2_AsstFWUprBoundX_HwNm_s4p11[0][0]       -16384         t2_AsstFWUprBoundX_HwNm_s4p11[0][1]       -14336         t2_AsstFWUprBoundX_HwNm_s4p11[0][2]       -12288         t2_AsstFWUprBoundX_HwNm_s4p11[0][3]       -10240         t2_AsstFWUprBoundX_HwNm_s4p11[0][4]       -8192         t2_AsstFWUprBoundX_HwNm_s4p11[0][5]       -6144         t2_AsstFWUprBoundX_HwNm_s4p11[0][6]       -4096         t2_AsstFWUprBoundX_HwNm_s4p11[0][7]       -2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][8]       0         t2_AsstFWUprBoundX_HwNm_s4p11[0][9]       2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][10]       4096	· · · ·	3690
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	·	3936
t2_AsstFWUprBoundX_HwNm_s4p11[0][1] -14336 t2_AsstFWUprBoundX_HwNm_s4p11[0][2] -12288 t2_AsstFWUprBoundX_HwNm_s4p11[0][3] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[0][4] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[0][5] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[0][6] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[0][7] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[0][8] 0 t2_AsstFWUprBoundX_HwNm_s4p11[0][8] 0 t2_AsstFWUprBoundX_HwNm_s4p11[0][9] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[0][10] 4096	•	8.19999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][1] -14336 t2_AsstFWUprBoundX_HwNm_s4p11[0][2] -12288 t2_AsstFWUprBoundX_HwNm_s4p11[0][3] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[0][4] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[0][5] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[0][6] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[0][7] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[0][8] 0 t2_AsstFWUprBoundX_HwNm_s4p11[0][8] 0 t2_AsstFWUprBoundX_HwNm_s4p11[0][9] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[0][10] 4096	tFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][3] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[0][4] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[0][5] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[0][6] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[0][7] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[0][8] 0 t2_AsstFWUprBoundX_HwNm_s4p11[0][9] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[0][9] 4096		-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][4] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[0][5] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[0][6] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[0][7] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[0][8] 0 t2_AsstFWUprBoundX_HwNm_s4p11[0][9] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[0][10] 4096	tFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][5] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[0][6] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[0][7] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[0][8] 0 t2_AsstFWUprBoundX_HwNm_s4p11[0][9] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[0][10] 4096	tFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[0][7] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[0][8] 0 t2_AsstFWUprBoundX_HwNm_s4p11[0][9] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[0][10] 4096	tFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[0][8] 0 t2_AsstFWUprBoundX_HwNm_s4p11[0][9] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[0][10] 4096	tFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8] 0 t2_AsstFWUprBoundX_HwNm_s4p11[0][9] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[0][10] 4096	tFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[0][10] 4096	tFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10] 4096	tFWUprBoundX_HwNm_s4p11[0][8]	0
, , , , , , , , , , , , , , , , , , , ,	tFWUprBoundX_HwNm_s4p11[0][9]	2048
t2 AsstFWUprBoundX HwNm s4p11[1][0] -18432	rFWUprBoundX_HwNm_s4p11[0][10]	4096
	tFWUprBoundX_HwNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][1] -16384	tFWUprBoundX_HwNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][2] -14336	rFWUprBoundX_HwNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][3] -12288	rFWUprBoundX_HwNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4] -10240	rFWUprBoundX_HwNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][5] -8192	rFWUprBoundX_HwNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6] -6144	rFWUprBoundX_HwNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7] -4096	rFWUprBoundX_HwNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8] -2048	rFWUprBoundX_HwNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9] 0	rFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10] 2048	FWUprBoundX_HwNm_s4p11[1][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0] -8192	:FWUprBoundX_HwNm_s4p11[2][0]	-8192



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240 -8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7] t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_11WNIn_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2 AsstFWUprBoundX HwNm s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	8192
	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	



		(12.10.10.10
Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-6144	
	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]		
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336	
	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-30720	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-28672	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-26624	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-24576	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0	
	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096	



lame ?_AsstFWUprBoundY_MtrNm_s4p11[7][4]	
	Input Value
	6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
P_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
_AsstFWDefltAssistX_HwNm_u8p8[0]	614
_AsstFWDefltAssistX_HwNm_u8p8[1]	640
_AsstFWDefltAssistX_HwNm_u8p8[2]	666
_AsstFWDefltAssistX_HwNm_u8p8[3]	691
_AsstFWDefltAssistX_HwNm_u8p8[4]	717
_AsstFWDefltAssistX_HwNm_u8p8[5]	742
_AsstFWDefltAssistX_HwNm_u8p8[6]	768
_AsstFWDefltAssistX_HwNm_u8p8[7]	794
_AsstFWDefltAssistX_HwNm_u8p8[8]	819
_AsstFWDefltAssistX_HwNm_u8p8[9]	845
_AsstFWDefltAssistX_HwNm_u8p8[10]	870
_AsstFWDefltAssistX_HwNm_u8p8[11]	896
_AsstFWDefltAssistX_HwNm_u8p8[12]	922
_AsstFWDefltAssistX_HwNm_u8p8[13]	947
_AsstFWDefltAssistX_HwNm_u8p8[14]	973
_AsstFWDefltAssistX_HwNm_u8p8[15]	998
_AsstFWDefltAssistX_HwNm_u8p8[16]	1024
_AsstFWDefltAssistX_HwNm_u8p8[17]	1050
_AsstFWDefltAssistX_HwNm_u8p8[18]	1075
_AsstFWDefltAssistX_HwNm_u8p8[19]	1101
_AsstFWDefltAssistY_MtrNm_s4p11[0]	14541
_AsstFWDefltAssistY_MtrNm_s4p11[1]	14746
_AsstFWDefltAssistY_MtrNm_s4p11[2]	14950
_AsstFWDefltAssistY_MtrNm_s4p11[3]	15155
_AsstFWDefltAssistY_MtrNm_s4p11[4]	15360
_AsstFWDefltAssistY_MtrNm_s4p11[5]	15565
_AsstFWDefltAssistY_MtrNm_s4p11[6]	15770
_AsstFWDefltAssistY_MtrNm_s4p11[7]	15974
_AsstFWDefltAssistY_MtrNm_s4p11[8]	16179
_AsstFWDefltAssistY_MtrNm_s4p11[9]	16384
_AsstFWDefltAssistY_MtrNm_s4p11[10]	16589
_AsstFWDefltAssistY_MtrNm_s4p11[11]	16794
_AsstFWDefltAssistY_MtrNm_s4p11[12]	16998
_AsstFWDefltAssistY_MtrNm_s4p11[13]	17203
_AsstFWDefltAssistY_MtrNm_s4p11[14]	17408
_AsstFWDefltAssistY_MtrNm_s4p11[15]	17613
_AsstFWDefltAssistY_MtrNm_s4p11[16]	17818
_AsstFWDefltAssistY_MtrNm_s4p11[17]	18022
_AsstFWDefltAssistY_MtrNm_s4p11[18]	18227
_AsstFWDefltAssistY_MtrNm_s4p11[19]	18432
_AsstFWPstepNstepThresh_Cnt_u16[0]	183
_AsstFWPstepNstepThresh_Cnt_u16[1]	451
_AsstFWVehSpd_Kph_u9p7[0]	10240
AsstFWVehSpd_Kph_u9p7[1]	10368
_AsstFWVehSpd_Kph_u9p7[2]	10496
AsstFWVehSpd_Kph_u9p7[3]	10624
_AsstFWVehSpd_Kph_u9p7[4]	10752
AsstFWVehSpd_Kph_u9p7[5]	10880
_AsstFWVehSpd_Kph_u9p7[6]	11008
AsstFWVehSpd_Kph_u9p7[7]	11136
pt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.0999999
pt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
pt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3
pt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5
pt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4
pt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
t_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	80.1999969
,	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	•
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cn	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 t_ttgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cn pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 t_lt tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnipt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cn pt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_AssistFirewall_Per1_HwTorque_HwNm_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.550000012	0.550000012 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	451	451 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	48.9570007	48.9570007 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.2734375	2.2734375 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.00349998	7.00349998 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.550000012	0.550000012 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.63 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall ActiveKSV M str.K Uls f32	0.090000036
AssistFirewall_ActiveRawAcc_Cnt_M_u16	6519
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	0
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.100000001
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.70000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.300000012
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00899999961
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.20000005
k_AsstFWInpLimitHFA_MtrNm_f32	4.4000001
k_AsstFWInpLimitHysComp_MtrNm_f32	6.0999999
k_AsstFWNstep_Cnt_u16	3813
k_AsstFWPstep_Cnt_u16	4059
k_RestoreThresh_MtrNm_f32	8.30000019
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	14336



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	10240	
	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]		
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	22528	
t2 AsstFWUprBoundY MtrNm s4p11[2][9]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-28672	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096	
	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	U144	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	640
t_AsstFWDefltAssistX_HwNm_u8p8[1]	666
t_AsstFWDefltAssistX_HwNm_u8p8[2]	691
t_AsstFWDefltAssistX_HwNm_u8p8[3]	717
t_AsstFWDefltAssistX_HwNm_u8p8[4]	742
t_AsstFWDefltAssistX_HwNm_u8p8[5]	768
t_AsstFWDefltAssistX_HwNm_u8p8[6]	794
t_AsstFWDefltAssistX_HwNm_u8p8[7]	819
t_AsstFWDefltAssistX_HwNm_u8p8[8]	845
t_AsstFWDefltAssistX_HwNm_u8p8[9]	870
t_AsstFWDefltAssistX_HwNm_u8p8[10]	896
t_AsstFWDefltAssistX_HwNm_u8p8[11]	922 947
t_AsstFWDefltAssistX_HwNm_u8p8[12]	
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	973 998
t_AsstFWDefitAssistX_HwNm_u8p8[14] t_AsstFWDefitAssistX_HwNm_u8p8[15]	1024
t_AsstFWDefitAssistX_mwnm_uopo[15]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1126
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	18637
t_AsstFWPstepNstepThresh_Cnt_u16[0]	184
t_AsstFWPstepNstepThresh_Cnt_u16[1]	455
t_AsstFWVehSpd_Kph_u9p7[0]	13184
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	13312 13440
t_AsstFWVehSpd_Kph_u9p7[3]	13568
t_AsstFWVehSpd_kph_u9p7[4]	13696
t_AsstFWVehSpd_Kph_u9p7[5]	13824
t AsstFWVehSpd Kph u9p7[6]	13952
t_AsstFWVehSpd_Kph_u9p7[7]	14080
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-6
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFi$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.00200009	2.00200009 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	455	455 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019	-8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.03000009	1.02999997 ± 4.88E-04	<b>~</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-0.200000286	-0.200000003 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.9369998	7.9369998 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-8.80000019	-8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Τ				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.64 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.099999
AssistFirewall ActiveKSV M str.K Uls f32	0.100000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	6642
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	5.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00499999989
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0099999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.29999995
k_AsstFWInpLimitHFA_MtrNm_f32	4.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	6.30000019
k_AsstFWNstep_Cnt_u16	3936
k_AsstFWPstep_Cnt_u16	4182
k_RestoreThresh_MtrNm_f32	8.39999962
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2 AsstFWUprBoundX HwNm s4p11[6][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	8192
L 11 Opt Dodn'd 1 _Multin_34p i i[o][o]	10240
t2 AsstEWUnrBoundY MtrNm s4n11[0][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288 14336



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096	
	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]		
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	28672	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384	
	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	18432	
t2_AsstrWUprBoundY_MtrNm_s4p11[4][6]		
	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	28672	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	2048	
2 AsstFWUprBoundY MtrNm s4p11[5][3]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6144	
	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]		
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240	
	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	6144 8192	



t2_AsstFWUprBoundY_MtrNm_s4p11[7][4] t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] t_AsstFWUprBoundY_MtrNm_u8p8[0] t_AsstFWDefltAssistX_HwNm_u8p8[1] t_AsstFWDefltAssistX_HwNm_u8p8[2]	Input Value  10240  12288  14336  16384  18432  20480  22528  666
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5] t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] t_AsstFWUprBoundY_MtrNm_u8p8[0] t_AsstFWDefltAssistX_HwNm_u8p8[1] t_AsstFWDefltAssistX_HwNm_u8p8[2]	12288 14336 16384 18432 20480 22528 666
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] t_AsstFWUprBoundY_MtrNm_u8p8[0] t_AsstFWDefltAssistX_HwNm_u8p8[1] t_AsstFWDefltAssistX_HwNm_u8p8[2]	14336 16384 18432 20480 22528 666
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] t_AsstFWDefltAssistX_HwNm_u8p8[0] t_AsstFWDefltAssistX_HwNm_u8p8[1] t_AsstFWDefltAssistX_HwNm_u8p8[2]	18432 20480 22528 666
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] t_AsstFWDefltAssistX_HwNm_u8p8[0] t_AsstFWDefltAssistX_HwNm_u8p8[1] t_AsstFWDefltAssistX_HwNm_u8p8[2]	20480       22528       666
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] t_AsstFWDefltAssistX_HwNm_u8p8[0] t_AsstFWDefltAssistX_HwNm_u8p8[1] t_AsstFWDefltAssistX_HwNm_u8p8[2]	20480       22528       666
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] t_AsstFWDefltAssistX_HwNm_u8p8[0] t_AsstFWDefltAssistX_HwNm_u8p8[1] t_AsstFWDefltAssistX_HwNm_u8p8[2]	666
t_AsstFWDefltAssistX_HwNm_u8p8[1] t_AsstFWDefltAssistX_HwNm_u8p8[2]	
t_AsstFWDefltAssistX_HwNm_u8p8[2]	004
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1.1.1	973
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	1024
	1050
	1075
	1101
	1126
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1152
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	16179
	16384
,	16589
	16794
, ; ;	16998
	17203
, ; ;	17408 17613
	17818
	18022
	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	18432
	18637
	18842
	185
t_AsstFWPstepNstepThresh_Cnt_u16[1]	459
	16128
t_AsstFWVehSpd_Kph_u9p7[1]	16256
t_AsstFWVehSpd_Kph_u9p7[2]	16384
t_AsstFWVehSpd_Kph_u9p7[3]	16512
t_AsstFWVehSpd_Kph_u9p7[4]	16640
t_AsstFWVehSpd_Kph_u9p7[5]	16768
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	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.78999996	2.78999996 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	459	459 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019	-8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.52099991	5.52099991 ± 4.88E-04	<b>~</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-1.4000001	-1.39999998 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.09899998	1.09899998 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-8.80000019	-8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Τ				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.65 (Repeat Count = 1)	v
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.7999995
AssistFirewall ActiveKSV M str.K Uls f32	0.20000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	6765
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.039999991
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.8999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0199999996
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.4000001
k_AsstFWInpLimitHFA_MtrNm_f32	4.80000019
k_AsstFWInpLimitHysComp_MtrNm_f32	6.5
k_AsstFWNstep_Cnt_u16	4059
k_AsstFWPstep_Cnt_u16	4305
k_RestoreThresh_MtrNm_f32	8.5
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_riwNm_s4p11[7][0]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	18432
	10.02



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336 -12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4] t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	10240



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576
t_AsstFWDefltAssistX_HwNm_u8p8[0]	691
t_AsstFWDefltAssistX_HwNm_u8p8[1]	717
t_AsstFWDefltAssistX_HwNm_u8p8[2]	742
t_AsstFWDefltAssistX_HwNm_u8p8[3]	768
t_AsstFWDefltAssistX_HwNm_u8p8[4]	794
t_AsstFWDefltAssistX_HwNm_u8p8[5]	819
t_AsstFWDefltAssistX_HwNm_u8p8[6]	845
t_AsstFWDefltAssistX_HwNm_u8p8[7]	870
t_AsstFWDefltAssistX_HwNm_u8p8[8]	896
t_AsstFWDefltAssistX_HwNm_u8p8[9]	922
t_AsstFWDefltAssistX_HwNm_u8p8[10]	947
t_AsstFWDefltAssistX_HwNm_u8p8[11]	973
t_AsstFWDefltAssistX_HwNm_u8p8[12]	998
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1178
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	19046
t_AsstFWPstepNstepThresh_Cnt_u16[0]	186
t_AsstFWPstepNstepThresh_Cnt_u16[1]	463
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
t_AsstFWVehSpd_Kph_u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	22.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.24000001	2.24000001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	463	463 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019	-8.80000019 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-4.8039999	-4.8039999 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-3	-3 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.1960001	2.1960001 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-8.80000019	-8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>~</b>

Τ				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.66 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall ActiveKSV M str.K Uls f32	0.300000012
AssistFirewall_ActiveRawAcc_Cnt_M_u16	6888
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00125584798
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall LwrBoundKSV M str.K Uls f32	0.600000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.029999993
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.5
k_AsstFWInpLimitHFA_MtrNm_f32	5
k_AsstFWInpLimitHysComp_MtrNm_f32	6.69999981
k_AsstFWNstep_Cnt_u16	4182
k_AsstFWPstep_Cnt_u16	4428
k_RestoreThresh_MtrNm_f32	8.60000038
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2 AsstFWUprBoundX HwNm s4p11[6][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
2 AsstFWUprBoundX HwNm s4p11[7][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_Asst WorlboundX_TWMin_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
:2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
:2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
:2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7] t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
.z_AsstFWUprBoundX_HwNm_s4p11[7][6] .2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
:2_AsstFWUprBoundX_HwNm_s4p11[7][9] :2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
12_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	4096



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	4096	
	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]		
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144	
2 AsstFWUprBoundY MtrNm s4p11[2][5]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336	
	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]		
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	717
t_AsstFWDefltAssistX_HwNm_u8p8[1]	742
t_AsstFWDefltAssistX_HwNm_u8p8[2]	768
t_AsstFWDefltAssistX_HwNm_u8p8[3]	794
t_AsstFWDefltAssistX_HwNm_u8p8[4]	819
t_AsstFWDefltAssistX_HwNm_u8p8[5]	845
t_AsstFWDefltAssistX_HwNm_u8p8[6]	870
t_AsstFWDefltAssistX_HwNm_u8p8[7]	896
t_AsstFWDefltAssistX_HwNm_u8p8[8]	922
t_AsstFWDefltAssistX_HwNm_u8p8[9]	947
t_AsstFWDefltAssistX_HwNm_u8p8[10]	973
t_AsstFWDefltAssistX_HwNm_u8p8[11]	998
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1203
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[12] t AsstFWDefltAssistY_MtrNm_s4p11[13]	17818 18022
, , ,	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[14] t AsstFWDefltAssistY_MtrNm_s4p11[15]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	19251
t_AsstFWPstepNstepThresh_Cnt_u16[0]	187
t AsstFWPstepNstepThresh Cnt u16[1]	467
t_AsstFWVehSpd_Kph_u9p7[0]	22016
t_AsstFWVehSpd_Kph_u9p7[1]	22144
t_AsstFWVehSpd_Kph_u9p7[2]	22272
t_AsstFWVehSpd_Kph_u9p7[3]	22400
t AsstFWVehSpd Kph u9p7[4]	22528
t_AsstFWVehSpd_Kph_u9p7[5]	22656
t_AsstFWVehSpd_Kph_u9p7[6]	22784
t_AsstFWVehSpd_Kph_u9p7[7]	22912
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-9
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	33.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32
·	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.769999981	0.769999981 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	467	467 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	•
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019	-8.80000019 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.00891638	7.00891638 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-0.800000191	-0.800000012 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.88699985	2.88700008 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.769999981	0.769999981 ± 3.05E-05	•
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-8.80000019	-8.80000019 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	•
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.67 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7
AssistFirewall ActiveKSV M str.K Uls f32	0.059999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	7011
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall CombAsstSV MtrNm M f32	5.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	8
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.715390444
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.090000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0399999991
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.5999999
k_AsstFWInpLimitHFA_MtrNm_f32	5.19999981
k_AsstFWInpLimitHysComp_MtrNm_f32	6.900001
k_AsstFWNstep_Cnt_u16	4305
k_AsstFWPstep_Cnt_u16	4551
k_RestoreThresh_MtrNm_f32	8.69999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-18432



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3] t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240 -8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_Asst WopiBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9] t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2 AsstFWUprBoundX HwNm s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
10. A - 4 FIAM I - D - 11 AV AMAN A 44 FOR FOR	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	00.40
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	8192	
	-30720	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-28672	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	8192	
	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]		
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	742
t_AsstFWDefltAssistX_HwNm_u8p8[1]	768
t_AsstFWDefltAssistX_HwNm_u8p8[2]	794
t_AsstFWDefltAssistX_HwNm_u8p8[3]	819
t_AsstFWDefltAssistX_HwNm_u8p8[4]	845
t_AsstFWDefltAssistX_HwNm_u8p8[5]	870
t_AsstFWDefltAssistX_HwNm_u8p8[6]	896
t_AsstFWDefltAssistX_HwNm_u8p8[7]	922
t_AsstFWDefltAssistX_HwNm_u8p8[8]	947
t_AsstFWDefltAssistX_HwNm_u8p8[9]	973
t_AsstFWDefltAssistX_HwNm_u8p8[10]	998
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	1075 1101
t_AsstFWDefitAssistX_HwNm_u8p8[14] t_AsstFWDefitAssistX_HwNm_u8p8[15]	1126
t_AsstFWDefitAssistX_HwNm_u8p8[16]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1203
t AsstFWDefltAssistX HwNm u8p8[19]	1229
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	19456
t_AsstFWPstepNstepThresh_Cnt_u16[0]	188
t_AsstFWPstepNstepThresh_Cnt_u16[1]	471
t_AsstFWVehSpd_Kph_u9p7[0]	24960
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	25088 25216
t_AsstFWVehSpd_Kph_u9p7[3]	25344
t_AsstFWVehSpd_kph_u9p7[4]	25472
t_AsstFWVehSpd_Kph_u9p7[5]	25600
t_AsstFWVehSpd_Kph_u9p7[6]	25728
t_AsstFWVehSpd_Kph_u9p7[7]	25856
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	44.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFi$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.57999992	6.57999992 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	471	471 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.60009766	7.60009766 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	9.28770256	9.28770256 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.36999989	7.36999989 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.97599983	3.97600007 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	7.60009766	7.60009766 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.68 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.070000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	7134
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.5
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.04999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.050000007
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.70000005
k_AsstFWInpLimitHFA_MtrNm_f32	5.4000001
k_AsstFWInpLimitHysComp_MtrNm_f32	7.0999999
k_AsstFWNstep_Cnt_u16	4428
k_AsstFWPstep_Cnt_u16	4674
k_RestoreThresh_MtrNm_f32	1.12
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384



2. AssiPU/DjefourK, Nebm. spi11294   4952   5144	
2. ASSEPUL/BEDOMEN HAND: sel-10[26]   6144   2. ASSEPUL/BEDOMEN HAND: sel-10[27]   2048   2. ASSEPUL/BEDOMEN HAND: sel-10[27]   2048   2. ASSEPUL/BEDOMEN HAND: sel-10[27]   2048   2. ASSEPUL/BEDOMEN HAND: sel-10[28]   0   2. ASSEPUL/BEDOMEN HAND: sel-10[28]   2048   2. ASSEPUL/BEDOMEN HAND: sel-10[28]   2048   2. ASSEPUL/BEDOMEN HAND: sel-10[28]   1406   2. ASSEPUL/BEDOMEN HAND: sel-10[38]   1428   2. ASSEPUL/BEDOMEN HAND: sel-10[38]   1409   2. ASSEPUL/BEDOMEN HAND: sel-10[38]   2048   2. ASSEPUL/BEDOMEN HAND: sel-10[38]   4098   2. ASSEPUL/BEDOMEN HAN	
2. ABSIPUL/PSBOUNDX. Hah/m. s.	
22_ABSF/WUPSCHOOK_Hebm_sel112 7    2048	
22_ASSEPUVEBBOURK_Hebrn_sep11281   0	
2 ASSE/VURBOUNDX HANN: seb112[0] 2049 2 ASSE/VURBOUNDX HANN: seb112[0] 4059 2 ASSE/VURBOUNDX HANN: seb112[0] 4059 2 ASSE/VURBOUNDX HANN: seb113[0] 14336 2 ASSE/VURBOUNDX HANN: seb113[0] 1528 2 ASSE/VURBOUNDX HANN: seb113[0] 1528 2 ASSE/VURBOUNDX HANN: seb113[0] 1528 2 ASSE/VURBOUNDX HANN: seb113[0] 1529 2 ASSE/VURBOUNDX HANN: seb113[0] 1533 2 ASSE/VURBOUNDX HANN: seb113[0	
2. AssERVUPDEOMIX HAMPL spot 1029   2048   2. AssERVUPDEOMIX HAMPL spot 1021   1049   14596   2. AssERVUPDEOMIX HAMPL spot 1021   14288   14288   2. AssERVUPDEOMIX HAMPL spot 1021   14288   14288   2. AssERVUPDEOMIX HAMPL spot 1022   14288   14288   2. AssERVUPDEOMIX HAMPL spot 1022   14288   14288   2. AssERVUPDEOMIX HAMPL spot 1022   142888   14288   14288   14288   14288   14288   14288   14288   14288   14288   14288   14288   1	
2. ASSE/WipfoomX, Havins, 494112[10]	
12. ASSE/Wijchountk, Hwhm. schot   19 11   10200   1	
2_AssFWUpDounX, Hwhm, s40113  2    10240	
2. AssFWUpBoundX_Hwhm_spir1[3]	
2_AssEWUpDounX_HwNm_sdp11[3]	
2. AssEWUpfboundX. HwNm. s4p11(3) 5	
2_AssEWUproduck Hwkm_s4pt1[3]8]   2048   2_AssEWUproduck Hwkm_s4pt1[3]8]   2048   2_AssEWUproduck Hwkm_s4pt1[3]8]   2048   2_AssEWUproduck Hwkm_s4pt1[3]8]   4096   2_AssEWUproduck Hwkm_s4pt1[3]8]   4096	
22 AssEFWUprBouncX, HwNm_sep11(3)  7	
2. AssEWUprBounck	
2. ASSEWUPBOUNDX_HWNN_sep11(3) 9    2. ASSEWUPBOUNDX_HWNN_sep11(3) 10    2. ASSEWUPBOUNDX_HWNN_sep11(4) 11    2. ASSEWUPBOUNDX_HWNN_sep11(4) 11    2. ASSEWUPBOUNDX_HWNN_sep11(4) 11    2. ASSEWUPBOUNDX_HWNN_sep11(4) 12    2. ASSEWUPBOUNDX_HWNN_sep11(4) 13    3. ExastewupBoundX_HWNN_sep11(4) 14    4. ExastewupBoundX_HWNN_sep11(4) 15    2. ASSEWUPBOUNDX_HWNN_sep11(4) 16    3. ExastewupBoundX_HWNN_sep11(4) 16    3. ExastewupBoundX_HWNN_sep11(4) 16    4. ASSEWUPBOUNDX_HWNN_sep11(4) 16    5. ASSEWUPBOUNDX_HWNN_sep11(4) 16    6. LASSEWUPBOUNDX_HWNN_sep11(4) 16    7. ASSEWUPBOUNDX_HWNN_sep11(4) 16    7. ASSEWUPBOUNDX_HWNN_sep11(4) 16    7. ASSEWUPBOUNDX_HWNN_sep11(4) 16    8. ASSEWUPBOUNDX_HWNN_sep11(5) 16    8. ASSEWUPBOUNDX_HWNN_sep11(5) 16    9. ASSEWUPBOUNDX_HWNN_sep11(5) 16    10. ASSEWUPBOUNDX_HWNN_sep11	
22. ASSEWUDPBOUNDX_HWNm_s4p11[4][0]   0   0   0   0   0   0   0   0   0	
2. AssFWUprBoundX_HwNm_s4p114[1]   2048   12. AssFWUprBoundX_HwNm_s4p114[1]   2048   12. AssFWUprBoundX_HwNm_s4p114[1]   2048   12. AssFWUprBoundX_HwNm_s4p114[1]   2048   2048   2. AssFWUprBoundX_HwNm_s4p114[1]   8192   2. AssFWUprBoundX_HwNm_s4p114[1]   8192   2. AssFWUprBoundX_HwNm_s4p114[1]   10240   122888   12288   12288   122888   122888   122888   12288   12288   122888   122888   122888   1228	
12_AssFWUpRoundX_HwNm_s4p114  2    2_AssFWUpRoundX_HwNm_s4p114  4    3   102   2_AssFWUpRoundX_HwNm_s4p114  4    3   102   2_AssFWUpRoundX_HwNm_s4p114  5    2_AssFWUpRoundX_HwNm_s4p114  5    2_AssFWUpRoundX_HwNm_s4p114  7    2_AssFWUpRoundX_HwNm_s4p114  7    2_AssFWUpRoundX_HwNm_s4p114  8    2_AssFWUpRoundX_HwNm_s4p114  8    2_AssFWUpRoundX_HwNm_s4p114  8    2_AssFWUpRoundX_HwNm_s4p114  9    3   4832   2_AssFWUpRoundX_HwNm_s4p114  9    4_AssFWUpRoundX_HwNm_s4p115  9    2_AssFWUpRoundX_HwNm_s4p115  11    2_AssFWUpRoundX_HwNm_s4p115  1	
12_AssFWUprBoundX_HwNm_s4p114  12    2_AssFWUprBoundX_HwNm_s4p114  4    3   102   2_AssFWUprBoundX_HwNm_s4p114  4    3   102   2_AssFWUprBoundX_HwNm_s4p114  5    3_AssFWUprBoundX_HwNm_s4p114  5    3_AssFWUprBoundX_HwNm_s4p114  7    4_AssFWUprBoundX_HwNm_s4p114  7    4_AssFWUprBoundX_HwNm_s4p114  8    4_AssFWUprBoundX_HwNm_s4p114  8    4_AssFWUprBoundX_HwNm_s4p114  8    4_AssFWUprBoundX_HwNm_s4p114  9    4_AssFWUprBoundX_HwNm_s4p114  9    4_AssFWUprBoundX_HwNm_s4p114  9    4_AssFWUprBoundX_HwNm_s4p115  11    4_AssFWUprBoundX_HwNm_s4p115  11    4_AssFWUprBoundX_HwNm_s4p115  12    4_AssFWUprBoundX_HwNm_s4p115  13    4_AssFWUprBoundX_HwNm_s4p115  14    4_AssFWUprBoundX_HwNm_s4p115  15    4_AssFWUprBoundX_HwNm_s4p115  16    4_AssFWUprBoundX_Hw	
12_AssFWUprBoundX_Hwhm_s4p114  6     10240   12288   10240   12288   12288   10240   122888   122888   122888   122888   122888   122888   122888	
12_AssFWUprBoundX_HwNm_s4p11[4] 5    10240   122888   122888   12288   122888   12288   12288   12288   1228	
12.AssFWUprBoundX_HwNm_s4p11[4] 5   2.AssFWUprBoundX_HwNm_s4p11[4] 7   2.AssFWUprBoundX_HwNm_s4p11[4] 8   2.AssFWUprBoundX_HwNm_s4p11[4] 8   2.AssFWUprBoundX_HwNm_s4p11[4] 8   2.AssFWUprBoundX_HwNm_s4p11[8] 9   2.AssFWUprBoundX_HwNm_s4p11[8] 1   2.AssFWUprBoundX_HwNm_s4p11[8] 1   2.AssFWUprBoundX_HwNm_s4p11[8] 1   2.AssFWUprBoundX_HwNm_s4p11[8] 1   2.AssFWUprBoundX_HwNm_s4p11[8] 2   2.AssFWUprBoundX_HwNm_s4p11[8] 3   2.AssFWUprBoundX_HwNm_s4p11[8] 3   2.AssFWUprBoundX_HwNm_s4p11[8] 4   2.AssFWUprBoundX_HwNm_s4p11[8] 6   2.AssFWUprBoundX_HwNm_s4p11[8] 6   2.AssFWUprBoundX_HwNm_s4p11[8] 6   2.AssFWUprBoundX_HwNm_s4p11[8] 6   2.AssFWUprBoundX_HwNm_s4p11[8] 9   2.AssFWUprBoundX_HwNm_s4p11[8] 9   2.AssFWUprBoundX_HwNm_s4p11[8] 9   2.AssFWUprBoundX_HwNm_s4p11[8] 9   2.AssFWUprBoundX_HwNm_s4p11[8] 1   2.AssFWUprBou	
14336	
12_AsstFWUpRoundX_HwNm_s4p11[4] 8	
12_AsstFWUpFboundX_HwNm_s4p11[4][9]   18432   12_AsstFWUpFboundX_HwNm_s4p11[4][10]   20480   16384	
12_AsstFWUpfboundX_HwNm_s4p11[4][10] 12_AsstFWUpfboundX_HwNm_s4p11[5][0] 12_AsstFWUpfboundX_HwNm_s4p11[5][2] 12_AsstFWUpfboundX_HwNm_s4p11[5][2] 12_AsstFWUpfboundX_HwNm_s4p11[5][3] 12_AsstFWUpfboundX_HwNm_s4p11[5][3] 12_AsstFWUpfboundX_HwNm_s4p11[5][3] 12_AsstFWUpfboundX_HwNm_s4p11[5][6] 12_AsstFWUpfboundX_HwNm_s4p11[5][6] 12_AsstFWUpfboundX_HwNm_s4p11[6][6] 12_AsstFWUpfboundX_HwNm_s4p11[6][7] 12_AsstFWUpfboundX_HwNm_s4p11[6][7] 12_AsstFWUpfboundX_HwNm_s4p11[6][9] 12_AsstFWUpfboundX_HwNm_s4p11[6][9] 12_AsstFWUpfboundX_HwNm_s4p11[6][1] 12_AsstFWUpfboundX_HwNm_s4p11[6][1] 12_AsstFWUpfboundX_HwNm_s4p11[6][1] 12_AsstFWUpfboundX_HwNm_s4p11[6][1] 12_AsstFWUpfboundX_HwNm_s4p11[6][1] 12_AsstFWUpfboundX_HwNm_s4p11[6][1] 12_AsstFWUpfboundX_HwNm_s4p11[6][6] 12_AsstFWUpfboundX_HwNm_s4p11[6][6] 12_AsstFWUpfboundX_HwNm_s4p11[6][6] 12_AsstFWUpfboundX_HwNm_s4p11[6][6] 12_AsstFWUpfboundX_HwNm_s4p11[6][6] 12_AsstFWUpfboundX_HwNm_s4p11[6][6] 12_AsstFWUpfboundX_HwNm_s4p11[6][6] 12_AsstFWUpfboundX_HwNm_s4p11[6][7] 12_AsstFWUpfboundX_HwNm_s4p11[7][7] 12_AsstFWUpfboundX_HwNm_s4p11	
12_AsstFWUpfboundX_HwNm_s4p11[5][0]   -16384    -12_AsstFWUpfboundX_HwNm_s4p11[5][1]   -14356    -12_AsstFWUpfboundX_HwNm_s4p11[5][3]   -10240    -12_AsstFWUpfboundX_HwNm_s4p11[5][3]   -10240    -12_AsstFWUpfboundX_HwNm_s4p11[5][5]   -6144   -8192    -12_AsstFWUpfboundX_HwNm_s4p11[5][6]   -4096    -12_AsstFWUpfboundX_HwNm_s4p11[5][6]   -4096    -12_AsstFWUpfboundX_HwNm_s4p11[5][7]   -2048    -12_AsstFWUpfboundX_HwNm_s4p11[5][8]   0    -12_AsstFWUpfboundX_HwNm_s4p11[5][9]   -2048    -12_AsstFWUpfboundX_HwNm_s4p11[6][9]   -2048    -12_AsstFWUpfboundX_HwNm_s4p11[6][9]   -2048    -12_AsstFWUpfboundX_HwNm_s4p11[6][1]   -2048    -12_AsstFWUpfboundX_HwNm_s4p11[6][1]   -2048    -12_AsstFWUpfboundX_HwNm_s4p11[6][1]   -2048    -12_AsstFWUpfboundX_HwNm_s4p11[6][1]   -2048    -12_AsstFWUpfboundX_HwNm_s4p11[6][1]   -2048    -12_AsstFWUpfboundX_HwNm_s4p11[6][2]   -2048    -12_AsstFWUpfboundX_HwNm_s4p11[6][3]   -2048    -12_AsstFWUpfboundX_HwNm_s4p11[6][3]   -2048    -12_AsstFWUpfboundX_HwNm_s4p11[6][3]   -2048    -12_AsstFWUpfboundX_HwNm_s4p11[6][4]   -2048    -12_AsstFWUpfboundX_HwNm_s4p11[6][5]   -2048    -12_AsstFWUpfboundX_HwNm_s4p11[6][6]   -2048    -12_AsstFWUpfboundX_HwNm_s4p11[6][6]   -2048    -12_AsstFWUpfboundX_HwNm_s4p11[6][6]   -2048    -12_AsstFWUpfboundX_HwNm_s4p11[6][7]   -2288    -12_AsstFWUpfboundX_HwNm_s4p11[6][7]   -2288    -12_AsstFWUpfboundX_HwNm_s4p11[6][8]   -2385    -12_AsstFWUpfboundX_HwNm_s4p11[6][9]   -2385    -12_AsstFWUpfboundX_HwNm_s4p11[7][9]   -2485    -12_AsstFWUpfboundX_H	
12_AssIFWUpfBoundX_HwNm_s4p11[5][1] 12_AssIFWUpfBoundX_HwNm_s4p11[5][3] 12_AssIFWUpfBoundX_HwNm_s4p11[5][3] 12_AssIFWUpfBoundX_HwNm_s4p11[5][4] 12_AssIFWUpfBoundX_HwNm_s4p11[5][6] 12_AssIFWUpfBoundX_HwNm_s4p11[5][6] 12_AssIFWUpfBoundX_HwNm_s4p11[5][6] 12_AssIFWUpfBoundX_HwNm_s4p11[5][6] 12_AssIFWUpfBoundX_HwNm_s4p11[5][8] 12_AssIFWUpfBoundX_HwNm_s4p11[5][8] 12_AssIFWUpfBoundX_HwNm_s4p11[5][8] 12_AssIFWUpfBoundX_HwNm_s4p11[6][8] 12_AssIFWUpfBoundX_HwNm_s4p11[6][9] 12_AssIFWUpfBoundX_HwNm_s4p11[6][9] 12_AssIFWUpfBoundX_HwNm_s4p11[6][9] 12_AssIFWUpfBoundX_HwNm_s4p11[6][1] 0 12_AssIFWUpfBoundX_HwNm_s4p11[6][2] 12_AssIFWUpfBoundX_HwNm_s4p11[6][3] 12_AssIFWUpfBoundX_HwNm_s4p11[6][3] 12_AssIFWUpfBoundX_HwNm_s4p11[6][6] 12_AssIFWUpfBoundX_HwNm_s4p11[7][6] 12_AssIFWUpfBoundX_HwNm_s4p1	
12_AssIFWUprBoundX_HwNm_s4p11[5] 2   2_AssIFWUprBoundX_HwNm_s4p11[5] 3   2_AssIFWUprBoundX_HwNm_s4p11[5] 4   2_AssIFWUprBoundX_HwNm_s4p11[5] 5   2_AssIFWUprBoundX_HwNm_s4p11[5] 5   2_AssIFWUprBoundX_HwNm_s4p11[5] 6   2_AssIFWUprBoundX_HwNm_s4p11[5] 7   2_DassIFWUprBoundX_HwNm_s4p11[5] 9   2_AssIFWUprBoundX_HwNm_s4p11[5] 9   2_AssIFWUprBoundX_HwNm_s4p11[5] 9   2_AssIFWUprBoundX_HwNm_s4p11[5] 9   2_AssIFWUprBoundX_HwNm_s4p11[6] 0   2_AssIFWUprBoundX_HwNm_s4p11[6] 1   2_AssIFWUprBoundX_HwNm_s4p11[6] 1   2_AssIFWUprBoundX_HwNm_s4p11[6] 2   2_AssIFWUprBoundX_HwNm_s4p11[6] 2   2_AssIFWUprBoundX_HwNm_s4p11[6] 3   2_AssIFWUprBoundX_HwNm_s4p11[6] 5   2_AssIFWUprBoundX_HwNm_s4p11[6] 5   2_AssIFWUprBoundX_HwNm_s4p11[6] 5   2_AssIFWUprBoundX_HwNm_s4p11[6] 5   2_AssIFWUprBoundX_HwNm_s4p11[6] 5   2_AssIFWUprBoundX_HwNm_s4p11[6] 5   2_AssIFWUprBoundX_HwNm_s4p11[6] 6   2_AssIFWUprBoundX_HwNm_s4p11[6] 6   2_AssIFWUprBoundX_HwNm_s4p11[6] 9   2_AssIFWUprBoundX_HwNm_s4p11[6] 9   2_AssIFWUprBoundX_HwNm_s4p11[6] 9   2_AssIFWUprBoundX_HwNm_s4p11[6] 9   2_AssIFWUprBoundX_HwNm_s4p11[6] 9   2_AssIFWUprBoundX_HwNm_s4p11[6] 9   2_AssIFWUprBoundX_HwNm_s4p11[6] 10   2_AssIFWUprBoundX_HwNm_s4p11[6] 10   2_AssIFWUprBoundX_HwNm_s4p11[7] 1   2_DassIFWUprBoundX_HwNm_s4p11[7] 1   2_DassIFWUprBoundX_HwNm_s4p11[7] 1   2_AssIFWUprBoundX_HwNm_s4p11[7] 2   2_AssIFWUprBoundX_HwNm_s4p11[7] 2   2_AssIFWUprBoundX_HwNm_s4p11[7] 2   2_AssIFWUprBoundX_HwNm_s4p11[7] 2   2_AssIFWUprBoundX_HwNm_s4p11[7] 2   2_AssIFWUprBoundX_HwNm	
12. AsstFWUprBoundX_HwNm_s4p11[5][3]   -10240   -10240     -10240     -10240     -10240     -10240     -10240   -10240     -10240     -10240     -10240     -10240     -10240   -10240     -10240     -10240     -10240     -10240     -10240   -10240     -10240	
12. AsstFWUprBoundX_HwNm_s4p11[5][4] 12. AsstFWUprBoundX_HwNm_s4p11[5][6] 12. AsstFWUprBoundX_HwNm_s4p11[5][6] 12. AsstFWUprBoundX_HwNm_s4p11[5][7] 13. AsstFWUprBoundX_HwNm_s4p11[5][8] 14. AsstFWUprBoundX_HwNm_s4p11[5][8] 15. AsstFWUprBoundX_HwNm_s4p11[5][8] 16. AsstFWUprBoundX_HwNm_s4p11[6][10] 17. AsstFWUprBoundX_HwNm_s4p11[6][10] 18. AsstFWUprBoundX_HwNm_s4p11[6][10] 19. AsstFWUprBoundX_HwNm_s4p11[6][1] 19. AsstFWUprBoundX_HwNm_s4p11[6][1] 10. AsstFWUprBoundX_HwNm_s4p11[6][2] 10. AsstFWUprBoundX_HwNm_s4p11[6][3] 10. AsstFWUprBoundX_HwNm_s4p11[6][4] 11. AsstFWUprBoundX_HwNm_s4p11[6][6] 12. AsstFWUprBoundX_HwNm_s4p11[6][6] 13. AsstFWUprBoundX_HwNm_s4p11[6][6] 14. AsstFWUprBoundX_HwNm_s4p11[6][6] 15. AsstFWUprBoundX_HwNm_s4p11[6][6] 16. AsstFWUprBoundX_HwNm_s4p11[6][6] 17. AsstFWUprBoundX_HwNm_s4p11[6][6] 18. AsstFWUprBoundX_HwNm_s4p11[6][6] 19. AsstFWUprBoundX_HwNm_s4p11[6][6] 10. AsstFWUprBoundX_HwNm_s4p11[6][6] 10. AsstFWUprBoundX_HwNm_s4p11[6][6] 10. AsstFWUprBoundX_HwNm_s4p11[6][6] 10. AsstFWUprBoundX_HwNm_s4p11[6][6] 11. AsstFWUprBoundX_HwNm_s4p11[7][6] 12. AsstFWUprBoundX_HwNm_s4p11[7][6] 13. AsstFWUprBoundX_HwNm_s4p11[7][7] 14. AsstFWUprBoundX_HwNm_s4p11[7][7] 15. AsstFWUprBoundX_HwNm_s4p11[7][7] 16. AsstFWUprBoundX_HwNm_s4p11[7][7] 17. AsstFWUprBoundX_HwNm_s4p11[7][7] 18. Asst	
12_AsstFWUprBoundX_HwNm_s4p11[5][5]   -6144     12_AsstFWUprBoundX_HwNm_s4p11[5][6]   -4096     12_AsstFWUprBoundX_HwNm_s4p11[5][7]   -2048     12_AsstFWUprBoundX_HwNm_s4p11[5][8]   0     12_AsstFWUprBoundX_HwNm_s4p11[5][9]   2048     12_AsstFWUprBoundX_HwNm_s4p11[5][9]   2048     12_AsstFWUprBoundX_HwNm_s4p11[6][0]   -2048     12_AsstFWUprBoundX_HwNm_s4p11[6][0]   -2048     12_AsstFWUprBoundX_HwNm_s4p11[6][1]   0     12_AsstFWUprBoundX_HwNm_s4p11[6][1]   0     12_AsstFWUprBoundX_HwNm_s4p11[6][2]   2048     12_AsstFWUprBoundX_HwNm_s4p11[6][3]   4096     12_AsstFWUprBoundX_HwNm_s4p11[6][4]   6114     12_AsstFWUprBoundX_HwNm_s4p11[6][5]   8192     12_AsstFWUprBoundX_HwNm_s4p11[6][6]   10240     12_AsstFWUprBoundX_HwNm_s4p11[6][6]   14336     12_AsstFWUprBoundX_HwNm_s4p11[6][8]   14336     12_AsstFWUprBoundX_HwNm_s4p11[6][9]   16384     12_AsstFWUprBoundX_HwNm_s4p11[6][10]   18432     12_AsstFWUprBoundX_HwNm_s4p11[7][0]   0     12_AsstFWUprBoundX_HwNm_s4p11[7][1]   2048     12_AsstFWUprBoundX_HwNm_s4p11[7][1]   2048     12_AsstFWUprBoundX_HwNm_s4p11[7][1]   2048     12_AsstFWUprBoundX_HwNm_s4p11[7][1]   2048     12_AsstFWUprBoundX_HwNm_s4p11[7][6]   1228     12_AsstFWUprBoundX_HwNm_s4p11[7][6]   10240     12_AsstFWUprBoundX_HwNm_s4p11[7][6]   1228     12_AsstFWUprBoundX_HwNm	
12_AssIFWUprBoundX_HwNm_s4p11[5][6]   -4096   -2048	
12_AssIFWUprBoundX_HwNm_s4p11[5][7]   -2048     12_AssIFWUprBoundX_HwNm_s4p11[5][8]   0     12_AssIFWUprBoundX_HwNm_s4p11[5][9]   2048     12_AssIFWUprBoundX_HwNm_s4p11[5][10]   4096     12_AssIFWUprBoundX_HwNm_s4p11[6][10]   -2048     12_AssIFWUprBoundX_HwNm_s4p11[6][1]   0     12_AssIFWUprBoundX_HwNm_s4p11[6][1]   2048     12_AssIFWUprBoundX_HwNm_s4p11[6][3]   4096     12_AssIFWUprBoundX_HwNm_s4p11[6][3]   4096     12_AssIFWUprBoundX_HwNm_s4p11[6][4]   6144     12_AssIFWUprBoundX_HwNm_s4p11[6][5]   8192     12_AssIFWUprBoundX_HwNm_s4p11[6][6]   10240     12_AssIFWUprBoundX_HwNm_s4p11[6][7]   12288     12_AssIFWUprBoundX_HwNm_s4p11[6][8]   14336     12_AssIFWUprBoundX_HwNm_s4p11[6][9]   16384     12_AssIFWUprBoundX_HwNm_s4p11[6][9]   16384     12_AssIFWUprBoundX_HwNm_s4p11[7][0]   0     12_AssIFWUprBoundX_HwNm_s4p11[7][1]   2048     12_AssIFWUprBoundX_HwNm_s4p11[7][1]   2048     12_AssIFWUprBoundX_HwNm_s4p11[7][1]   8192     12_AssIFWUprBoundX_HwNm_s4p11[7][1]   8192     12_AssIFWUprBoundX_HwNm_s4p11[7][6]   12288     1	
12_AssIFWUprBoundX_HwNm_s4p11[5][8]       0         12_AssIFWUprBoundX_HwNm_s4p11[5][10]       2048         12_AssIFWUprBoundX_HwNm_s4p11[6][0]       4096         12_AssIFWUprBoundX_HwNm_s4p11[6][0]       -2048         12_AssIFWUprBoundX_HwNm_s4p11[6][1]       0         12_AssIFWUprBoundX_HwNm_s4p11[6][2]       2048         12_AssIFWUprBoundX_HwNm_s4p11[6][3]       4096         12_AssIFWUprBoundX_HwNm_s4p11[6][4]       6144         12_AssIFWUprBoundX_HwNm_s4p11[6][5]       8192         12_AssIFWUprBoundX_HwNm_s4p11[6][6]       10240         12_AssIFWUprBoundX_HwNm_s4p11[6][7]       12288         12_AssIFWUprBoundX_HwNm_s4p11[6][8]       14336         12_AssIFWUprBoundX_HwNm_s4p11[6][9]       16384         12_AssIFWUprBoundX_HwNm_s4p11[6][10]       18432         12_AssIFWUprBoundX_HwNm_s4p11[7][1]       2048         12_AssIFWUprBoundX_HwNm_s4p11[7][1]       4096         12_AssIFWUprBoundX_HwNm_s4p11[7][1]       10240         12_AssIFWUprBoundX_HwNm_s4p11[7][1]       10240         12_AssIFWUprBoundX_HwNm_s4p11[7][6]       1128         12_AssIFWUprBoundX_HwNm_s4p11[7][6]       1228         12_AssIFWUprBoundX_HwNm_s4p11[7][6]       1228         12_AssIFWUprBoundX_HwNm_s4p11[7][6]       1228         12_AssIFWUprBoundX_HwNm_s4p11[7	
12_AssIF-WUprBoundX_HwNm_s4p11[5][9]   2048     12_AssIF-WUprBoundX_HwNm_s4p11[5][10]   4096     12_AssIF-WUprBoundX_HwNm_s4p11[6][0]   -2048     12_AssIF-WUprBoundX_HwNm_s4p11[6][1]   0     12_AssIF-WUprBoundX_HwNm_s4p11[6][2]   2048     12_AssIF-WUprBoundX_HwNm_s4p11[6][2]   2048     12_AssIF-WUprBoundX_HwNm_s4p11[6][3]   4096     12_AssIF-WUprBoundX_HwNm_s4p11[6][4]   6144     12_AssIF-WUprBoundX_HwNm_s4p11[6][5]   8192     12_AssIF-WUprBoundX_HwNm_s4p11[6][6]   10240     12_AssIF-WUprBoundX_HwNm_s4p11[6][7]   12288     12_AssIF-WUprBoundX_HwNm_s4p11[6][8]   14336     12_AssIF-WUprBoundX_HwNm_s4p11[6][9]   16384     12_AssIF-WUprBoundX_HwNm_s4p11[6][10]   18432     12_AssIF-WUprBoundX_HwNm_s4p11[7][0]   0     12_AssIF-WUprBoundX_HwNm_s4p11[7][0]   0     12_AssIF-WUprBoundX_HwNm_s4p11[7][1]   2048     12_AssIF-WUprBoundX_HwNm_s4p11[7][2]   4096     12_AssIF-WUprBoundX_HwNm_s4p11[7][2]   4096     12_AssIF-WUprBoundX_HwNm_s4p11[7][4]   8192     12_AssIF-WUprBoundX_HwNm_s4p11[7][6]   12288     12_AssIF-WUprBoundX_HwNm_s4p11[7][6]   12288     12_AssIF-WUprBoundX_HwNm_s4p11[7][6]   18344     12_AssIF-WUprBoundX_HwNm_s4p11[7][6]   18342     12_AssIF-WUprBoundX_HwNm_s4p11[7][6]   18364     12_AssIF-WUprBoundX_HwNm_s4p11[7][6]   18432     12_AssIF-WUprB	
12_AsstFWUprBoundX_HwNm_s4p11[5] 10    2-048     12_AsstFWUprBoundX_HwNm_s4p11[6] 0    -2048     12_AsstFWUprBoundX_HwNm_s4p11[6] 1    0     12_AsstFWUprBoundX_HwNm_s4p11[6] 2    2048     12_AsstFWUprBoundX_HwNm_s4p11[6] 3    4096     12_AsstFWUprBoundX_HwNm_s4p11[6] 4    6144     12_AsstFWUprBoundX_HwNm_s4p11[6] 5    8192     12_AsstFWUprBoundX_HwNm_s4p11[6] 6    10240     12_AsstFWUprBoundX_HwNm_s4p11[6] 7    12288     12_AsstFWUprBoundX_HwNm_s4p11[6] 8    14336     12_AsstFWUprBoundX_HwNm_s4p11[6] 9    16384     12_AsstFWUprBoundX_HwNm_s4p11[6] 9    16384     12_AsstFWUprBoundX_HwNm_s4p11[6] 10    18432     12_AsstFWUprBoundX_HwNm_s4p11[7] 0    0     12_AsstFWUprBoundX_HwNm_s4p11[7] 1    2048     12_AsstFWUprBoundX_HwNm_s4p11[7] 2    4096     12_AsstFWUprBoundX_HwNm_s4p11[7] 3    6144     12_AsstFWUprBoundX_HwNm_s4p11[7] 3    6144     12_AsstFWUprBoundX_HwNm_s4p11[7] 4    8192     12_AsstFWUprBoundX_HwNm_s4p11[7] 6    12288     12_AsstFWUprBoundX_HwNm_s4p11[7] 6    12285     12_AsstFWUprBoundX_HwNm_s4p11[7] 6    12285     12_AsstFWUprBoundX_HwNm_s4p11[7] 6    12285     12_AsstFWUprBoundX_HwNm_s4p11[7] 6    12285     12_AsstFWUprBoundX_HwNm_s4p11[7] 6    12285	
12_AsstFWUprBoundX_HwNm_s4p11[6][0]   -2048     12_AsstFWUprBoundX_HwNm_s4p11[6][1]   0     12_AsstFWUprBoundX_HwNm_s4p11[6][2]   2048     12_AsstFWUprBoundX_HwNm_s4p11[6][3]   4096     12_AsstFWUprBoundX_HwNm_s4p11[6][4]   6144     12_AsstFWUprBoundX_HwNm_s4p11[6][5]   8192     12_AsstFWUprBoundX_HwNm_s4p11[6][6]   10240     12_AsstFWUprBoundX_HwNm_s4p11[6][7]   12288     12_AsstFWUprBoundX_HwNm_s4p11[6][8]   14336     12_AsstFWUprBoundX_HwNm_s4p11[6][9]   16384     12_AsstFWUprBoundX_HwNm_s4p11[6][10]   18432     12_AsstFWUprBoundX_HwNm_s4p11[7][0]   0     12_AsstFWUprBoundX_HwNm_s4p11[7][1]   2048     12_AsstFWUprBoundX_HwNm_s4p11[7][1]   2048     12_AsstFWUprBoundX_HwNm_s4p11[7][2]   4096     12_AsstFWUprBoundX_HwNm_s4p11[7][3]   6144     12_AsstFWUprBoundX_HwNm_s4p11[7][6]   10240     12_AsstFWUprBoundX_HwNm_s4p11[7][6]   12288     12_AsstFWUprBoundX_HwNm_s4p11[7][6]   12286     12_AsstFWUprBoundX_HwNm_s4p11[7][6]   12286     12_AsstFWUprBoundX_HwNm_s4p11[7][6]   12286     12_AsstFWUprBoundX_HwNm_s4p11[7][6]   20480     12_AsstFWUprBoundX_HwNm_s4p11[7][6]   20480     12_AsstFWUprBoundX_HwNm_s4p11[6][6]   20480     12_AsstFWUprBoundY_MtrNm_s4p11[6][6]   20480     12_AsstFWUprBoundY_MtrNm_s4p11[6][6]   20480     12_AsstFWUprBoundY_MtrNm_s4p11[6][6]   20480     12_AsstFWUprBoundY_MtrNm_s4p11[6][6]   20480     12_AsstFWUprBoundY_MtrNm_s4p11[6][6]   20480     12_AsstFWUprBoundY_MtrNm_s4p11[6][6]	
12_AsstFWUprBoundX_HwNm_s4p11[6][1]   0     12_AsstFWUprBoundX_HwNm_s4p11[6][2]   2048     12_AsstFWUprBoundX_HwNm_s4p11[6][3]   4096     12_AsstFWUprBoundX_HwNm_s4p11[6][4]   6144     12_AsstFWUprBoundX_HwNm_s4p11[6][6]   8192     12_AsstFWUprBoundX_HwNm_s4p11[6][6]   10240     12_AsstFWUprBoundX_HwNm_s4p11[6][7]   12288     12_AsstFWUprBoundX_HwNm_s4p11[6][8]   14336     12_AsstFWUprBoundX_HwNm_s4p11[6][9]   16384     12_AsstFWUprBoundX_HwNm_s4p11[6][10]   18432     12_AsstFWUprBoundX_HwNm_s4p11[7][0]   0     12_AsstFWUprBoundX_HwNm_s4p11[7][1]   2048     12_AsstFWUprBoundX_HwNm_s4p11[7][2]   4096     12_AsstFWUprBoundX_HwNm_s4p11[7][3]   6144     12_AsstFWUprBoundX_HwNm_s4p11[7][4]   8192     12_AsstFWUprBoundX_HwNm_s4p11[7][6]   10240     12_AsstFWUprBoundX_HwNm_s4p11[7][6]   10240     12_AsstFWUprBoundX_HwNm_s4p11[7][6]   12288     12_AsstFWUprBoundX_HwNm_s4p11[7][6]   12288     12_AsstFWUprBoundX_HwNm_s4p11[7][6]   12288     12_AsstFWUprBoundX_HwNm_s4p11[7][6]   1836     12_AsstFWUprBoundX_HwNm_s4p11[7][6]   18432     12_AsstFWUprBoundX_HwNm_s4p11[7][6]   18432     12_AsstFWUprBoundX_HwNm_s4p11[7][6]   18432     12_AsstFWUprBoundX_HwNm_s4p11[7][6]   20480     12_AsstFWUprBoundX_HwNm_s4p11[7][6]   20480     12_AsstFWUprBoundY_MtrNm_s4p11[6][0]   20480     12_AsstFWUprBoundY_MtrNm_s4p11[6][0]   20480     12_AsstFWUprBoundY_MtrNm_s4p11[6][1]   204872     12_AsstFWUprBoundY_MtrNm_s4p11[6][1]   20480     12_AsstFWUprBoundY_MtrNm_s4p11[6][6]   20480     12_AsstFWUprBoundY_MtrNm_s4p11[6][6]   20480     12_AsstFWUprBoundY_MtrNm_s4p11[6][6]   20480     12_AsstFWUprBoundY_MtrNm_s4p11[6][6]   20480   20480     12_AsstFWUprBoundY_MtrNm_s4p11[6][6]   20480   20480   20480   20480	
12_AsstFWUprBoundX_HwNm_s4p11[6][2]       2048         12_AsstFWUprBoundX_HwNm_s4p11[6][3]       4096         12_AsstFWUprBoundX_HwNm_s4p11[6][4]       6144         12_AsstFWUprBoundX_HwNm_s4p11[6][5]       8192         12_AsstFWUprBoundX_HwNm_s4p11[6][6]       10240         12_AsstFWUprBoundX_HwNm_s4p11[6][7]       12288         12_AsstFWUprBoundX_HwNm_s4p11[6][8]       14336         12_AsstFWUprBoundX_HwNm_s4p11[6][9]       16384         12_AsstFWUprBoundX_HwNm_s4p11[6][10]       18432         12_AsstFWUprBoundX_HwNm_s4p11[7][0]       0         12_AsstFWUprBoundX_HwNm_s4p11[7][1]       2048         12_AsstFWUprBoundX_HwNm_s4p11[7][2]       4096         12_AsstFWUprBoundX_HwNm_s4p11[7][3]       6144         12_AsstFWUprBoundX_HwNm_s4p11[7][4]       8192         12_AsstFWUprBoundX_HwNm_s4p11[7][5]       10240         12_AsstFWUprBoundX_HwNm_s4p11[7][6]       12288         12_AsstFWUprBoundX_HwNm_s4p11[7][7]       14336         12_AsstFWUprBoundX_HwNm_s4p11[7][8]       16384         12_AsstFWUprBoundX_HwNm_s4p11[7][9]       18432         12_AsstFWUprBoundX_HwNm_s4p11[7][9]       18432         12_AsstFWUprBoundX_HwNm_s4p11[7][9]       20480         12_AsstFWUprBoundY_MtrNm_s4p11[7][0]       30720         12_AsstFWUprBoundY_MtrN	
12_AsstFWUprBoundX_HwNm_s4p11[6][3]       4096         12_AsstFWUprBoundX_HwNm_s4p11[6][4]       6144         12_AsstFWUprBoundX_HwNm_s4p11[6][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[6][6]       10240         12_AsstFWUprBoundX_HwNm_s4p11[6][7]       12288         12_AsstFWUprBoundX_HwNm_s4p11[6][8]       14336         12_AsstFWUprBoundX_HwNm_s4p11[6][9]       16384         12_AsstFWUprBoundX_HwNm_s4p11[6][10]       18432         12_AsstFWUprBoundX_HwNm_s4p11[7][0]       0         12_AsstFWUprBoundX_HwNm_s4p11[7][1]       2048         12_AsstFWUprBoundX_HwNm_s4p11[7][2]       4096         12_AsstFWUprBoundX_HwNm_s4p11[7][3]       6144         12_AsstFWUprBoundX_HwNm_s4p11[7][4]       8192         12_AsstFWUprBoundX_HwNm_s4p11[7][6]       10240         12_AsstFWUprBoundX_HwNm_s4p11[7][6]       12288         12_AsstFWUprBoundX_HwNm_s4p11[7][7]       14336         12_AsstFWUprBoundX_HwNm_s4p11[7][8]       16384         12_AsstFWUprBoundX_HwNm_s4p11[7][9]       18432         12_AsstFWUprBoundX_HwNm_s4p11[7][9]       18432         12_AsstFWUprBoundX_HwNm_s4p11[7][0]       20480         12_AsstFWUprBoundY_MtrNm_s4p11[0][0]       30720         12_AsstFWUprBoundY_MtrNm_s4p11[0][0]       -26624         12_AsstFWUprBoundY_M	
12_AsstFWUprBoundX_HwNm_s4p11[6][4]       6144         12_AsstFWUprBoundX_HwNm_s4p11[6][5]       8192         12_AsstFWUprBoundX_HwNm_s4p11[6][6]       10240         12_AsstFWUprBoundX_HwNm_s4p11[6][7]       12288         12_AsstFWUprBoundX_HwNm_s4p11[6][8]       14336         12_AsstFWUprBoundX_HwNm_s4p11[6][9]       16384         12_AsstFWUprBoundX_HwNm_s4p11[7][0]       0         12_AsstFWUprBoundX_HwNm_s4p11[7][0]       0         12_AsstFWUprBoundX_HwNm_s4p11[7][1]       2048         12_AsstFWUprBoundX_HwNm_s4p11[7][2]       4096         12_AsstFWUprBoundX_HwNm_s4p11[7][4]       8192         12_AsstFWUprBoundX_HwNm_s4p11[7][4]       8192         12_AsstFWUprBoundX_HwNm_s4p11[7][6]       12288         12_AsstFWUprBoundX_HwNm_s4p11[7][6]       12288         12_AsstFWUprBoundX_HwNm_s4p11[7][8]       16384         12_AsstFWUprBoundX_HwNm_s4p11[7][9]       18432         12_AsstFWUprBoundX_HwNm_s4p11[7][9]       18432         12_AsstFWUprBoundX_HwNm_s4p11[7][0]       20480         12_AsstFWUprBoundY_MtrNm_s4p11[0][0]       -30720         12_AsstFWUprBoundY_MtrNm_s4p11[0][1]       -28672         12_AsstFWUprBoundY_MtrNm_s4p11[0][2]       -26624         12_AsstFWUprBoundY_MtrNm_s4p11[0][3]       -24576	
12_AsstFWUprBoundX_HwNm_s4p11[6][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[6][6]       10240         12_AsstFWUprBoundX_HwNm_s4p11[6][7]       12288         12_AsstFWUprBoundX_HwNm_s4p11[6][8]       14336         12_AsstFWUprBoundX_HwNm_s4p11[6][9]       16384         12_AsstFWUprBoundX_HwNm_s4p11[7][0]       0         12_AsstFWUprBoundX_HwNm_s4p11[7][0]       0         12_AsstFWUprBoundX_HwNm_s4p11[7][1]       2048         12_AsstFWUprBoundX_HwNm_s4p11[7][2]       4096         12_AsstFWUprBoundX_HwNm_s4p11[7][3]       6144         12_AsstFWUprBoundX_HwNm_s4p11[7][4]       8192         12_AsstFWUprBoundX_HwNm_s4p11[7][6]       12288         12_AsstFWUprBoundX_HwNm_s4p11[7][6]       12288         12_AsstFWUprBoundX_HwNm_s4p11[7][8]       16384         12_AsstFWUprBoundX_HwNm_s4p11[7][8]       16384         12_AsstFWUprBoundX_HwNm_s4p11[7][9]       18432         12_AsstFWUprBoundX_HwNm_s4p11[7][0]       20480         12_AsstFWUprBoundY_MtrNm_s4p11[0][0]       -30720         12_AsstFWUprBoundY_MtrNm_s4p11[0][0]       -26624         12_AsstFWUprBoundY_MtrNm_s4p11[0][0]       -26624         12_AsstFWUprBoundY_MtrNm_s4p11[0][0]       -26624         12_AsstFWUprBoundY_MtrNm_s4p11[0][0]       -26624         12_AsstFWUprBoun	
12_AsstFWUprBoundX_HwNm_s4p11[6][7]       10240         12_AsstFWUprBoundX_HwNm_s4p11[6][7]       12288         12_AsstFWUprBoundX_HwNm_s4p11[6][8]       14336         12_AsstFWUprBoundX_HwNm_s4p11[6][9]       16384         12_AsstFWUprBoundX_HwNm_s4p11[6][10]       18432         12_AsstFWUprBoundX_HwNm_s4p11[7][0]       0         12_AsstFWUprBoundX_HwNm_s4p11[7][1]       2048         12_AsstFWUprBoundX_HwNm_s4p11[7][2]       4096         12_AsstFWUprBoundX_HwNm_s4p11[7][3]       6144         12_AsstFWUprBoundX_HwNm_s4p11[7][4]       8192         12_AsstFWUprBoundX_HwNm_s4p11[7][5]       10240         12_AsstFWUprBoundX_HwNm_s4p11[7][6]       12288         12_AsstFWUprBoundX_HwNm_s4p11[7][7]       14336         12_AsstFWUprBoundX_HwNm_s4p11[7][8]       16384         12_AsstFWUprBoundX_HwNm_s4p11[7][9]       18432         12_AsstFWUprBoundX_HwNm_s4p11[7][9]       18432         12_AsstFWUprBoundY_HwNm_s4p11[7][0]       20480         12_AsstFWUprBoundY_MtrNm_s4p11[0][0]       -30720         12_AsstFWUprBoundY_MtrNm_s4p11[0][0]       -28672         12_AsstFWUprBoundY_MtrNm_s4p11[0][0]       -26624         12_AsstFWUprBoundY_MtrNm_s4p11[0][0]       -26624	
12_AsstFWUprBoundX_HwNm_s4p11[6][8]       14336         12_AsstFWUprBoundX_HwNm_s4p11[6][9]       16384         12_AsstFWUprBoundX_HwNm_s4p11[6][10]       18432         12_AsstFWUprBoundX_HwNm_s4p11[7][0]       0         12_AsstFWUprBoundX_HwNm_s4p11[7][1]       2048         12_AsstFWUprBoundX_HwNm_s4p11[7][2]       4096         12_AsstFWUprBoundX_HwNm_s4p11[7][3]       6144         12_AsstFWUprBoundX_HwNm_s4p11[7][4]       8192         12_AsstFWUprBoundX_HwNm_s4p11[7][5]       10240         12_AsstFWUprBoundX_HwNm_s4p11[7][6]       12288         12_AsstFWUprBoundX_HwNm_s4p11[7][7]       14336         12_AsstFWUprBoundX_HwNm_s4p11[7][8]       16384         12_AsstFWUprBoundX_HwNm_s4p11[7][9]       18432         12_AsstFWUprBoundX_HwNm_s4p11[7][0]       20480         12_AsstFWUprBoundY_MtrNm_s4p11[0][0]       -30720         12_AsstFWUprBoundY_MtrNm_s4p11[0][1]       -28672         12_AsstFWUprBoundY_MtrNm_s4p11[0][2]       -26624         12_AsstFWUprBoundY_MtrNm_s4p11[0][3]       -24576	
12_AsstFWUprBoundX_HwNm_s4p11[6][9]       16384         12_AsstFWUprBoundX_HwNm_s4p11[6][10]       18432         12_AsstFWUprBoundX_HwNm_s4p11[7][0]       0         12_AsstFWUprBoundX_HwNm_s4p11[7][1]       2048         12_AsstFWUprBoundX_HwNm_s4p11[7][2]       4096         12_AsstFWUprBoundX_HwNm_s4p11[7][3]       6144         12_AsstFWUprBoundX_HwNm_s4p11[7][4]       8192         12_AsstFWUprBoundX_HwNm_s4p11[7][5]       10240         12_AsstFWUprBoundX_HwNm_s4p11[7][6]       12288         12_AsstFWUprBoundX_HwNm_s4p11[7][7]       14336         12_AsstFWUprBoundX_HwNm_s4p11[7][8]       16384         12_AsstFWUprBoundX_HwNm_s4p11[7][9]       18432         12_AsstFWUprBoundX_HwNm_s4p11[7][0]       20480         12_AsstFWUprBoundY_MtrNm_s4p11[0][0]       -30720         12_AsstFWUprBoundY_MtrNm_s4p11[0][1]       -28672         12_AsstFWUprBoundY_MtrNm_s4p11[0][2]       -26624         12_AsstFWUprBoundY_MtrNm_s4p11[0][3]       -24576	
12_AsstFWUprBoundX_HwNm_s4p11[6][10]       18432         12_AsstFWUprBoundX_HwNm_s4p11[7][0]       0         12_AsstFWUprBoundX_HwNm_s4p11[7][1]       2048         12_AsstFWUprBoundX_HwNm_s4p11[7][2]       4096         12_AsstFWUprBoundX_HwNm_s4p11[7][3]       6144         12_AsstFWUprBoundX_HwNm_s4p11[7][4]       8192         12_AsstFWUprBoundX_HwNm_s4p11[7][5]       10240         12_AsstFWUprBoundX_HwNm_s4p11[7][6]       12288         12_AsstFWUprBoundX_HwNm_s4p11[7][7]       14336         12_AsstFWUprBoundX_HwNm_s4p11[7][8]       16384         12_AsstFWUprBoundX_HwNm_s4p11[7][9]       18432         12_AsstFWUprBoundX_HwNm_s4p11[7][0]       20480         12_AsstFWUprBoundY_MtrNm_s4p11[0][0]       -30720         12_AsstFWUprBoundY_MtrNm_s4p11[0][1]       -28672         12_AsstFWUprBoundY_MtrNm_s4p11[0][2]       -26624         12_AsstFWUprBoundY_MtrNm_s4p11[0][3]       -24576	
12_AsstFWUprBoundX_HwNm_s4p11[7][0]       0         12_AsstFWUprBoundX_HwNm_s4p11[7][1]       2048         12_AsstFWUprBoundX_HwNm_s4p11[7][2]       4096         12_AsstFWUprBoundX_HwNm_s4p11[7][3]       6144         12_AsstFWUprBoundX_HwNm_s4p11[7][4]       8192         12_AsstFWUprBoundX_HwNm_s4p11[7][5]       10240         12_AsstFWUprBoundX_HwNm_s4p11[7][6]       12288         12_AsstFWUprBoundX_HwNm_s4p11[7][7]       14336         12_AsstFWUprBoundX_HwNm_s4p11[7][8]       16384         12_AsstFWUprBoundX_HwNm_s4p11[7][9]       18432         12_AsstFWUprBoundX_HwNm_s4p11[7][10]       20480         12_AsstFWUprBoundY_MtrNm_s4p11[0][0]       -30720         12_AsstFWUprBoundY_MtrNm_s4p11[0][1]       -28672         12_AsstFWUprBoundY_MtrNm_s4p11[0][2]       -26624         12_AsstFWUprBoundY_MtrNm_s4p11[0][3]       -24576	
12_AsstFWUprBoundX_HwNm_s4p11[7][1]       2048         12_AsstFWUprBoundX_HwNm_s4p11[7][2]       4096         12_AsstFWUprBoundX_HwNm_s4p11[7][3]       6144         12_AsstFWUprBoundX_HwNm_s4p11[7][4]       8192         12_AsstFWUprBoundX_HwNm_s4p11[7][5]       10240         12_AsstFWUprBoundX_HwNm_s4p11[7][6]       12288         12_AsstFWUprBoundX_HwNm_s4p11[7][7]       14336         12_AsstFWUprBoundX_HwNm_s4p11[7][8]       16384         12_AsstFWUprBoundX_HwNm_s4p11[7][9]       18432         12_AsstFWUprBoundX_HwNm_s4p11[7][10]       20480         12_AsstFWUprBoundY_MtrNm_s4p11[0][0]       -30720         12_AsstFWUprBoundY_MtrNm_s4p11[0][1]       -28672         12_AsstFWUprBoundY_MtrNm_s4p11[0][2]       -26624         12_AsstFWUprBoundY_MtrNm_s4p11[0][3]       -24576	
12_AsstFWUprBoundX_HwNm_s4p11[7][2]       4096         12_AsstFWUprBoundX_HwNm_s4p11[7][3]       6144         12_AsstFWUprBoundX_HwNm_s4p11[7][4]       8192         12_AsstFWUprBoundX_HwNm_s4p11[7][5]       10240         12_AsstFWUprBoundX_HwNm_s4p11[7][6]       12288         12_AsstFWUprBoundX_HwNm_s4p11[7][7]       14336         12_AsstFWUprBoundX_HwNm_s4p11[7][8]       16384         12_AsstFWUprBoundX_HwNm_s4p11[7][9]       18432         12_AsstFWUprBoundX_HwNm_s4p11[7][10]       20480         12_AsstFWUprBoundY_MtrNm_s4p11[0][0]       -30720         12_AsstFWUprBoundY_MtrNm_s4p11[0][1]       -28672         12_AsstFWUprBoundY_MtrNm_s4p11[0][2]       -26624         12_AsstFWUprBoundY_MtrNm_s4p11[0][3]       -24576	
12_AsstFWUprBoundX_HwNm_s4p11[7][3]       6144         12_AsstFWUprBoundX_HwNm_s4p11[7][4]       8192         12_AsstFWUprBoundX_HwNm_s4p11[7][5]       10240         12_AsstFWUprBoundX_HwNm_s4p11[7][6]       12288         12_AsstFWUprBoundX_HwNm_s4p11[7][7]       14336         12_AsstFWUprBoundX_HwNm_s4p11[7][8]       16384         12_AsstFWUprBoundX_HwNm_s4p11[7][9]       18432         12_AsstFWUprBoundX_HwNm_s4p11[7][10]       20480         12_AsstFWUprBoundY_MtrNm_s4p11[0][0]       -30720         12_AsstFWUprBoundY_MtrNm_s4p11[0][1]       -28672         12_AsstFWUprBoundY_MtrNm_s4p11[0][2]       -26624         12_AsstFWUprBoundY_MtrNm_s4p11[0][3]       -24576	
12_AsstFWUprBoundX_HwNm_s4p11[7][4] 8192 12_AsstFWUprBoundX_HwNm_s4p11[7][5] 10240 12_AsstFWUprBoundX_HwNm_s4p11[7][6] 12288 12_AsstFWUprBoundX_HwNm_s4p11[7][7] 14336 12_AsstFWUprBoundX_HwNm_s4p11[7][8] 16384 12_AsstFWUprBoundX_HwNm_s4p11[7][9] 18432 12_AsstFWUprBoundX_HwNm_s4p11[7][10] 20480 12_AsstFWUprBoundY_MtrNm_s4p11[0][0] 20480 12_AsstFWUprBoundY_MtrNm_s4p11[0][1] -28672 12_AsstFWUprBoundY_MtrNm_s4p11[0][2] -26624 12_AsstFWUprBoundY_MtrNm_s4p11[0][3] -24576	
12_AsstFWUprBoundX_HwNm_s4p11[7][5]       10240         12_AsstFWUprBoundX_HwNm_s4p11[7][6]       12288         12_AsstFWUprBoundX_HwNm_s4p11[7][7]       14336         12_AsstFWUprBoundX_HwNm_s4p11[7][8]       16384         12_AsstFWUprBoundX_HwNm_s4p11[7][9]       18432         12_AsstFWUprBoundX_HwNm_s4p11[7][10]       20480         12_AsstFWUprBoundY_MtrNm_s4p11[0][0]       -30720         12_AsstFWUprBoundY_MtrNm_s4p11[0][1]       -28672         12_AsstFWUprBoundY_MtrNm_s4p11[0][2]       -26624         12_AsstFWUprBoundY_MtrNm_s4p11[0][3]       -24576	
12_AsstFWUprBoundX_HwNm_s4p11[7][6]       12288         12_AsstFWUprBoundX_HwNm_s4p11[7][7]       14336         12_AsstFWUprBoundX_HwNm_s4p11[7][8]       16384         12_AsstFWUprBoundX_HwNm_s4p11[7][9]       18432         12_AsstFWUprBoundX_HwNm_s4p11[7][10]       20480         12_AsstFWUprBoundY_MtrNm_s4p11[0][0]       -30720         12_AsstFWUprBoundY_MtrNm_s4p11[0][1]       -28672         12_AsstFWUprBoundY_MtrNm_s4p11[0][2]       -26624         12_AsstFWUprBoundY_MtrNm_s4p11[0][3]       -24576	
12_AsstFWUprBoundX_HwNm_s4p11[7][7]       14336         12_AsstFWUprBoundX_HwNm_s4p11[7][8]       16384         12_AsstFWUprBoundX_HwNm_s4p11[7][9]       18432         12_AsstFWUprBoundX_HwNm_s4p11[7][10]       20480         12_AsstFWUprBoundY_MtrNm_s4p11[0][0]       -30720         12_AsstFWUprBoundY_MtrNm_s4p11[0][1]       -28672         12_AsstFWUprBoundY_MtrNm_s4p11[0][2]       -26624         12_AsstFWUprBoundY_MtrNm_s4p11[0][3]       -24576	
12_AsstFWUprBoundX_HwNm_s4p11[7][8]     16384       12_AsstFWUprBoundX_HwNm_s4p11[7][9]     18432       12_AsstFWUprBoundX_HwNm_s4p11[7][10]     20480       12_AsstFWUprBoundY_MtrNm_s4p11[0][0]     -30720       12_AsstFWUprBoundY_MtrNm_s4p11[0][1]     -28672       12_AsstFWUprBoundY_MtrNm_s4p11[0][2]     -26624       12_AsstFWUprBoundY_MtrNm_s4p11[0][3]     -24576	
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]       18432         t2_AsstFWUprBoundX_HwNm_s4p11[7][10]       20480         t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]       -30720         t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]       -28672         t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]       -26624         t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]       -24576	
12_AsstFWUprBoundX_HwNm_s4p11[7][10]       20480         12_AsstFWUprBoundY_MtrNm_s4p11[0][0]       -30720         12_AsstFWUprBoundY_MtrNm_s4p11[0][1]       -28672         12_AsstFWUprBoundY_MtrNm_s4p11[0][2]       -26624         12_AsstFWUprBoundY_MtrNm_s4p11[0][3]       -24576	
12_AsstFWUprBoundY_MtrNm_s4p11[0][0]       -30720         12_AsstFWUprBoundY_MtrNm_s4p11[0][1]       -28672         12_AsstFWUprBoundY_MtrNm_s4p11[0][2]       -26624         12_AsstFWUprBoundY_MtrNm_s4p11[0][3]       -24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] -28672 t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] -26624 t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] -24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] -26624 t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] -24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] -24576	
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t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] -20480 t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] -18432	
tz_Asstr-wuprBoundY_mtrNm_s4p11[0][0] -18432 t2_AsstFWUprBoundY_mtrNm_s4p11[0][7] -16384	



	( ' ' ' ' ' ' ' ' ' ' ' ' ' ' ' ' ' ' '	
Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-12288	
	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]		
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192	
	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]		
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-2048	
2 AsstFWUprBoundY MtrNm s4p11[2][5]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-28672	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-10240	
	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]		
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096	
12_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0	
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t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0040	
	2048	
	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096 6144	
i2_AsstFWUprBoundY_MtrNm_s4p11[5][7] i2_AsstFWUprBoundY_MtrNm_s4p11[5][8] i2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096 6144 8192 10240	
i2_AsstFWUprBoundY_MtrNm_s4p11[5][7] i2_AsstFWUprBoundY_MtrNm_s4p11[5][8] i2_AsstFWUprBoundY_MtrNm_s4p11[5][9] i2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096 6144 8192 10240 12288	
i2_AsstFWUprBoundY_MtrNm_s4p11[5][7] i2_AsstFWUprBoundY_MtrNm_s4p11[5][8] i2_AsstFWUprBoundY_MtrNm_s4p11[5][9] i2_AsstFWUprBoundY_MtrNm_s4p11[5][10] i2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096 6144 8192 10240 12288 8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096 6144 8192 10240 12288 8192 10240	
i2_AsstFWUprBoundY_MtrNm_s4p11[5][7] i2_AsstFWUprBoundY_MtrNm_s4p11[5][8] i2_AsstFWUprBoundY_MtrNm_s4p11[5][9] i2_AsstFWUprBoundY_MtrNm_s4p11[5][10] i2_AsstFWUprBoundY_MtrNm_s4p11[6][0] i2_AsstFWUprBoundY_MtrNm_s4p11[6][1] i2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096 6144 8192 10240 12288 8192 10240 12288	
i2_AsstFWUprBoundY_MtrNm_s4p11[5][7] i2_AsstFWUprBoundY_MtrNm_s4p11[5][8] i2_AsstFWUprBoundY_MtrNm_s4p11[5][9] i2_AsstFWUprBoundY_MtrNm_s4p11[5][10] i2_AsstFWUprBoundY_MtrNm_s4p11[6][0] i2_AsstFWUprBoundY_MtrNm_s4p11[6][1] i2_AsstFWUprBoundY_MtrNm_s4p11[6][2] i2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096 6144 8192 10240 12288 8192 10240 12288 14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096 6144 8192 10240 12288 8192 10240 12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	4096 6144 8192 10240 12288 8192 10240 12288 14336	
12_AsstFWUprBoundY_MtrNm_s4p11[5][7] 12_AsstFWUprBoundY_MtrNm_s4p11[5][8] 12_AsstFWUprBoundY_MtrNm_s4p11[5][9] 12_AsstFWUprBoundY_MtrNm_s4p11[5][10] 12_AsstFWUprBoundY_MtrNm_s4p11[6][0] 12_AsstFWUprBoundY_MtrNm_s4p11[6][1] 12_AsstFWUprBoundY_MtrNm_s4p11[6][2] 12_AsstFWUprBoundY_MtrNm_s4p11[6][3] 12_AsstFWUprBoundY_MtrNm_s4p11[6][4] 12_AsstFWUprBoundY_MtrNm_s4p11[6][4] 12_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096 6144 8192 10240 12288 8192 10240 12288 14336 16384	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 2_AsstFWUprBoundY_MtrNm_s4p11[6][5] 2_AsstFWUprBoundY_MtrNm_s4p11[6][5] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096 6144 8192 10240 12288 8192 10240 12288 14336 16384 18432 20480	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 2_AsstFWUprBoundY_MtrNm_s4p11[6][5] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096 6144 8192 10240 12288 8192 10240 12288 14336 16384 18432 20480 22528	
12_AsstFWUprBoundY_MtrNm_s4p11[5][7] 12_AsstFWUprBoundY_MtrNm_s4p11[5][8] 12_AsstFWUprBoundY_MtrNm_s4p11[5][9] 12_AsstFWUprBoundY_MtrNm_s4p11[5][10] 12_AsstFWUprBoundY_MtrNm_s4p11[6][0] 12_AsstFWUprBoundY_MtrNm_s4p11[6][1] 12_AsstFWUprBoundY_MtrNm_s4p11[6][2] 12_AsstFWUprBoundY_MtrNm_s4p11[6][3] 12_AsstFWUprBoundY_MtrNm_s4p11[6][4] 12_AsstFWUprBoundY_MtrNm_s4p11[6][5] 12_AsstFWUprBoundY_MtrNm_s4p11[6][6] 12_AsstFWUprBoundY_MtrNm_s4p11[6][6] 12_AsstFWUprBoundY_MtrNm_s4p11[6][7] 12_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096 6144 8192 10240 12288 8192 10240 12288 14336 16384 18432 20480 22528 24576	
12_AsstFWUprBoundY_MtrNm_s4p11[5][7] 12_AsstFWUprBoundY_MtrNm_s4p11[5][8] 12_AsstFWUprBoundY_MtrNm_s4p11[5][9] 12_AsstFWUprBoundY_MtrNm_s4p11[6][0] 12_AsstFWUprBoundY_MtrNm_s4p11[6][1] 12_AsstFWUprBoundY_MtrNm_s4p11[6][2] 12_AsstFWUprBoundY_MtrNm_s4p11[6][3] 12_AsstFWUprBoundY_MtrNm_s4p11[6][4] 12_AsstFWUprBoundY_MtrNm_s4p11[6][4] 12_AsstFWUprBoundY_MtrNm_s4p11[6][5] 12_AsstFWUprBoundY_MtrNm_s4p11[6][6] 12_AsstFWUprBoundY_MtrNm_s4p11[6][7] 12_AsstFWUprBoundY_MtrNm_s4p11[6][7] 12_AsstFWUprBoundY_MtrNm_s4p11[6][8] 12_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096 6144 8192 10240 12288 8192 10240 12288 14336 16384 18432 20480 22528 24576 26624	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 2_AsstFWUprBoundY_MtrNm_s4p11[6][5] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096 6144 8192 10240 12288 8192 10240 12288 14336 16384 18432 20480 22528 24576 26624 28672	
12_AsstFWUprBoundY_MtrNm_s4p11[5][7] 12_AsstFWUprBoundY_MtrNm_s4p11[5][8] 12_AsstFWUprBoundY_MtrNm_s4p11[5][9] 12_AsstFWUprBoundY_MtrNm_s4p11[5][10] 12_AsstFWUprBoundY_MtrNm_s4p11[6][0] 12_AsstFWUprBoundY_MtrNm_s4p11[6][1] 12_AsstFWUprBoundY_MtrNm_s4p11[6][2] 12_AsstFWUprBoundY_MtrNm_s4p11[6][3] 12_AsstFWUprBoundY_MtrNm_s4p11[6][4] 12_AsstFWUprBoundY_MtrNm_s4p11[6][5] 12_AsstFWUprBoundY_MtrNm_s4p11[6][6] 12_AsstFWUprBoundY_MtrNm_s4p11[6][7] 12_AsstFWUprBoundY_MtrNm_s4p11[6][7] 12_AsstFWUprBoundY_MtrNm_s4p11[6][8] 12_AsstFWUprBoundY_MtrNm_s4p11[6][9] 12_AsstFWUprBoundY_MtrNm_s4p11[6][9] 12_AsstFWUprBoundY_MtrNm_s4p11[6][9] 12_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096 6144 8192 10240 12288 8192 10240 12288 14336 16384 18432 20480 22528 24576 26624	
12_AsstFWUprBoundY_MtrNm_s4p11[5][7] 12_AsstFWUprBoundY_MtrNm_s4p11[5][8] 12_AsstFWUprBoundY_MtrNm_s4p11[5][9] 12_AsstFWUprBoundY_MtrNm_s4p11[5][10] 12_AsstFWUprBoundY_MtrNm_s4p11[6][0] 12_AsstFWUprBoundY_MtrNm_s4p11[6][1] 12_AsstFWUprBoundY_MtrNm_s4p11[6][2] 12_AsstFWUprBoundY_MtrNm_s4p11[6][3] 12_AsstFWUprBoundY_MtrNm_s4p11[6][4] 12_AsstFWUprBoundY_MtrNm_s4p11[6][5] 12_AsstFWUprBoundY_MtrNm_s4p11[6][6] 12_AsstFWUprBoundY_MtrNm_s4p11[6][7] 12_AsstFWUprBoundY_MtrNm_s4p11[6][8] 12_AsstFWUprBoundY_MtrNm_s4p11[6][8] 12_AsstFWUprBoundY_MtrNm_s4p11[6][9] 12_AsstFWUprBoundY_MtrNm_s4p11[6][9] 12_AsstFWUprBoundY_MtrNm_s4p11[6][10] 12_AsstFWUprBoundY_MtrNm_s4p11[6][10] 12_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096 6144 8192 10240 12288 8192 10240 12288 14336 16384 18432 20480 22528 24576 26624 28672	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	4096 6144 8192 10240 12288 8192 10240 12288 14336 16384 18432 20480 22528 24576 26624 28672 0	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	768
t_AsstFWDefltAssistX_HwNm_u8p8[1]	794
t_AsstFWDefltAssistX_HwNm_u8p8[2]	819
t_AsstFWDefltAssistX_HwNm_u8p8[3]	845
t_AsstFWDefltAssistX_HwNm_u8p8[4]	870
t_AsstFWDefltAssistX_HwNm_u8p8[5]	896
t_AsstFWDefltAssistX_HwNm_u8p8[6]	922
t_AsstFWDefltAssistX_HwNm_u8p8[7]	947
t_AsstFWDefltAssistX_HwNm_u8p8[8]	973
	998
t_AsstFWDefltAssistX_HwNm_u8p8[9]	
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1178
t AsstFWDefltAssistX HwNm u8p8[17]	1203
t_AsstFWDefitAssistX_HwNm_u8p8[18]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1254
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	17613
,	
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	19661
t_AsstFWPstepNstepThresh_Cnt_u16[0]	189
t_AsstFWPstepNstepThresh_Cnt_u16[1]	475
t_AsstFWVehSpd_Kph_u9p7[0]	27904
t_AsstFWVehSpd_Kph_u9p7[1]	28032
t_AsstFWVehSpd_Kph_u9p7[2]	28160
t_AsstFWVehSpd_Kph_u9p7[3]	28288
t_AsstFWVehSpd_Kph_u9p7[4]	28416
t_AsstFWVehSpd_Kph_u9p7[5]	28544
t_AsstFWVehSpd_Kph_u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7]	28800
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	55.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCind_withVini_ tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_	-
·	•
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tot Die lant An AnnietEinswell AnnietEinswell Dand I bestannin Orenn Michigan	_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm	_ioz tgi_rosisti irewaii_i of i_riyateresiseetiip_ivitiviii_toz
tgt_Rte_inst_Ap_assist⊦irewali.assist⊦irewali_Per1_HysteresisComp_mtrnm. tgt_Rte_Inst_Ap_AssistFirewall.assistFirewall_Per1_MEC_Counter_Cnt_enur	





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-16384
	-10004



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-10240
	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288
	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
2 AsstFWUprBoundY MtrNm s4p11[2][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-6144
	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2 AsstFWUprBoundY MtrNm s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0
	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	
IO A (EIA) I I - D IV MINN	4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	22528
t_AsstFWDefltAssistX_HwNm_u8p8[0]	794
t_AsstFWDefltAssistX_HwNm_u8p8[1]	819
t_AsstFWDefltAssistX_HwNm_u8p8[2]	845
t_AsstFWDefltAssistX_HwNm_u8p8[3]	870
t_AsstFWDefltAssistX_HwNm_u8p8[4]	896
t_AsstFWDefltAssistX_HwNm_u8p8[5]	922
t_AsstFWDefltAssistX_HwNm_u8p8[6]	947
t_AsstFWDefltAssistX_HwNm_u8p8[7]	973
t_AsstFWDefltAssistX_HwNm_u8p8[8]	998
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	1126 1152
t_AsstFWDefitAssistX_HwNm_u8p8[14] t_AsstFWDefitAssistX_HwNm_u8p8[15]	1178
t_AsstFWDefitAssistX_HwNm_u8p8[16]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1254
t AsstFWDefltAssistX HwNm u8p8[19]	1280
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	19661
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	19866
t_AsstFWPstepNstepThresh_Cnt_u16[0]	190
t_AsstFWPstepNstepThresh_Cnt_u16[1]	479 30848
t_AsstFWVehSpd_Kph_u9p7[0]	
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	30976 31104
t_AsstFWVehSpd_Kph_u9p7[3]	31232
t_AsstFWVehSpd_kph_u9p7[4]	31360
t_AsstFWVehSpd_Kph_u9p7[5]	31488
t_AsstFWVehSpd_Kph_u9p7[6]	31616
t_AsstFWVehSpd_Kph_u9p7[7]	31744
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3.099999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	66.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFi$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.01200008	1.01199996 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	479	479 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.79980469	-7.79980469 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.9000001	2.9000001 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.76000023	3.75999999 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.89400005	4.89400005 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.79980469	-7.79980469 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.70 (Repeat Count = 1) Name	Imput Value
	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0099999978
AssistFirewall_ActiveRawAcc_Cnt_M_u16	7380
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.20000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	2.09537959
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.300000012
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0700000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.9000001
k_AsstFWInpLimitHFA_MtrNm_f32	5.80000019
k_AsstFWInpLimitHysComp_MtrNm_f32	7.5
c_AsstFWNstep_Cnt_u16	4674
c_AsstFWPstep_Cnt_u16	4920
c_RestoreThresh_MtrNm_f32	1.13999999
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288



	(
Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_Asst WopiBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_Asst WopiBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2 AsstFWUprBoundX HwNm s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][3] t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240 -8192
	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-20480
	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-18432 -16384
12_AsstFWUprBoundY_MtrNm_s4p11[0][4] 12_AsstFWUprBoundY_MtrNm_s4p11[0][5] 12_AsstFWUprBoundY_MtrNm_s4p11[0][6]	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-8192
t2_Asst WoprBoundY_MtrNm_s4p11[0][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-4096
	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
t2 AsstFWUprBoundY MtrNm s4p11[4][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
	0
2 AsstFWUprBoundY MtrNm s4p11[6][7]	
	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096 6144 4096



Active_Uls_f32
md_MtrNm_f32
sist_MtrNm_f32
Fbl_Service_Cnt_lgc
ist_MtrNm_f32
lwNm_f32
pmp_MtrNm_f32
er_Cnt_enum
d_Kph_f32
r



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.17799997	2.17799997 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	483	483 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.70019531	8.70019531 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.46000004	4.46000004 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.06999969	6.07000017 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.80999994	6.80999994 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.70019531	8.70019531 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.71 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.099999
AssistFirewall ActiveKSV M str.K Uls f32	0.0199999996
AssistFirewall_ActiveRawAcc_Cnt_M_u16	7503
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.9000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.300000012
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.5
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0799999982
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4
k_AsstFWInpLimitHFA_MtrNm_f32	6
k_AsstFWInpLimitHysComp_MtrNm_f32	7.69999981
k_AsstFWNstep_Cnt_u16	2812
k_AsstFWPstep_Cnt_u16	1476
k_RestoreThresh_MtrNm_f32	1.14999998
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2 AsstFWUprBoundX HwNm s4p11[6][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
:2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
:2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
:2_AsstFWUprBoundX_HwNm_s4p11[7][1] :2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240
12_AsstFWUprBoundX_HwNm_s4p11[7][2] 12_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192
:z_AsstFWUprBoundX_HWNm_s4p11[7][3] :2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144
:z_AsstFWUprBoundX_HWNm_s4p11[7][4] :2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
:z_AsstFWUprBoundX_HWNm_s4p11[7][5] :2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][7] 2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0
	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096 6144
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-16384
	-16384 -14336 -12288



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048	
	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]		
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-28672	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-16432 -16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	12288	
TEL 1997 ALONI DOMINO LEMININI TOAD LI LI LIOI	12200	



	, , , , , , , , , , , , , , , , , , , ,
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	26624
t_AsstFWDefltAssistX_HwNm_u8p8[0]	845
t_AsstFWDefltAssistX_HwNm_u8p8[1]	870
t_AsstFWDefltAssistX_HwNm_u8p8[2]	896
t_AsstFWDefltAssistX_HwNm_u8p8[3]	922
t_AsstFWDefltAssistX_HwNm_u8p8[4]	947
t_AsstFWDefltAssistX_HwNm_u8p8[5]	973
t_AsstFWDefltAssistX_HwNm_u8p8[6]	998
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	1178 1203
t_AsstFWDefitAssistX_HwNm_u8p8[14] t_AsstFWDefitAssistX_HwNm_u8p8[15]	1229
t_AsstFWDefitAssistX_HwNm_u8p8[16]	1254
t_AsstFWDefitAssistX_HwNm_u8p8[17]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1306
t AsstFWDefltAssistX HwNm u8p8[19]	1331
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	20275
t_AsstFWPstepNstepThresh_Cnt_u16[0]	192
t_AsstFWPstepNstepThresh_Cnt_u16[1]	487
t_AsstFWVehSpd_Kph_u9p7[0]	36736
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	36864 36992
t_AsstFWVehSpd_Kph_u9p7[3]	37120
t AsstFWVehSpd Kph u9p7[4]	37248
t_AsstFWVehSpd_Kph_u9p7[5]	37376
t_AsstFWVehSpd_Kph_u9p7[6]	37504
t_AsstFWVehSpd_Kph_u9p7[7]	37632
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	88.0699997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.03799987	3.03800011 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	487	487 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8	8 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.47000027	6.46999979 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.05999994	4.05999994 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	0.852000058	0.851999998 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8	8 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.72 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	3.099999
AssistFirewall ActiveKSV M str.K Uls f32	0.10000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	7626
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	-5,099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.7999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.090000036
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	6.19999981
k_AsstFWInpLimitHysComp_MtrNm_f32	0
k_AsstFWNstep_Cnt_u16	2688
k_AsstFWPstep_Cnt_u16	1599
k RestoreThresh MtrNm f32	1.15999997
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096
	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-8192



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096	
	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]		
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-18432	
	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096	
	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]		
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-26624	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192	
castFWUprBoundY_MtrNm_s4p11[6][2]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	14336	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	870
t_AsstFWDefltAssistX_HwNm_u8p8[1]	896
t_AsstFWDefltAssistX_HwNm_u8p8[2]	922
t_AsstFWDefltAssistX_HwNm_u8p8[3]	947
t_AsstFWDefltAssistX_HwNm_u8p8[4]	973
t_AsstFWDefltAssistX_HwNm_u8p8[5]	998
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	1203 1229
t_AsstFWDefitAssistX_HwNm_u8p8[14] t_AsstFWDefitAssistX_HwNm_u8p8[15]	1254
t_AsstFWDefitAssistX_HwNm_u8p8[16]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1331
t AsstFWDefltAssistX HwNm u8p8[19]	1357
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	20275
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	20480
t_AsstFWPstepNstepThresh_Cnt_u16[0]	193
t_AsstFWPstepNstepThresh_Cnt_u16[1]	491 39680
t_AsstFWVehSpd_Kph_u9p7[0]	
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	39808 39936
t_AsstFWVehSpd_Kph_u9p7[3]	40064
t_AsstFWVehSpd_Kph_u9p7[4]	40004
t_AsstFWVehSpd_Kph_u9p7[5]	40320
t_AsstFWVehSpd_Kph_u9p7[6]	40448
t_AsstFWVehSpd_Kph_u9p7[7]	40576
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.6500001
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	99.0500031
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFirewal$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.78999996	2.78999996 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	491	491 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.10009766	8.10009766 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.1500001	4.1500001 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5	5 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.82099986	1.82099998 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.10009766	8.10009766 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T ✓				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.73 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.7999995
AssistFirewall ActiveKSV M str.K Uls f32	0.20000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	7749
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-5.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0599999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.8999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.099999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.10000001
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.19999981
k_AsstFWInpLimitHFA_MtrNm_f32	6.400001
k_AsstFWInpLimitHysComp_MtrNm_f32	8.80000019
k_AsstFWNstep_Cnt_u16	2564
k_AsstFWPstep_Cnt_u16	1722
k_RestoreThresh_MtrNm_f32	1.16999996
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
	16384
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
12_Asst WorlboundX_TWNII_s4p11[5][4] 12_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
	0
:2_AsstFWUprBoundX_HwNm_s4p11[5][7] :2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-6144



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	6144	
	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]		
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-4096	
	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288	
t2 AsstFWUprBoundY MtrNm s4p11[4][6]	14336	
t2_Asst WopiBoundY_MtrNm_s4p11[4][0]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096	
	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]		
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288	
	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336	
	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240	



	MACILAU
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	896
t_AsstFWDefltAssistX_HwNm_u8p8[1]	922
t_AsstFWDefltAssistX_HwNm_u8p8[2]	947
t_AsstFWDefltAssistX_HwNm_u8p8[3]	973
t_AsstFWDefltAssistX_HwNm_u8p8[4]	998
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1382
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	20685
t_AsstFWPstepNstepThresh_Cnt_u16[0]	194
t_AsstFWPstepNstepThresh_Cnt_u16[1]	495
t_AsstFWVehSpd_Kph_u9p7[0]	42624
t_AsstFWVehSpd_Kph_u9p7[1]	42752
t_AsstFWVehSpd_Kph_u9p7[2]	42880
t_AsstFWVehSpd_Kph_u9p7[3]	43008
t_AsstFWVehSpd_Kph_u9p7[4]	43136
t_AsstFWVehSpd_Kph_u9p7[5]	43264
t_AsstFWVehSpd_Kph_u9p7[6]	43392
t_AsstFWVehSpd_Kph_u9p7[7]	43520
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.78000021
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-4
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	110.019997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_legendering the property of th$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tet Dte leet An AssistFirewell AssistFirewell Dard MEC Counter Cet anum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	\*



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.24000001	2.24000001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	495	495 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.20019531	8.20019531 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.87199974	4.87200022 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6	6 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.78999996	2.78999996 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.20019531	8.20019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T ✓				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.74 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall ActiveKSV M str.K Uls f32	0.30000012
AssistFirewall_ActiveRawAcc_Cnt_M_u16	7872
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-5.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0700000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall LwrBoundKSV M str.K Uls f32	0.600000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.109999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.30000019
k AsstFWInpLimitHFA MtrNm f32	6.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	6.38000011
k_AsstFWNstep_Cnt_u16	2440
k_AsstFWPstep_Cnt_u16	1845
k RestoreThresh MtrNm f32	1.17999995
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2 AsstFWUprBoundX HwNm s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384
	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2 AsstFWUprBoundX HwNm s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2 AsstFWUprBoundX HwNm s4p11[6][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-16384
	-14336
t2 AsstFWUprBoundY MtrNm s4p11[0][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-12288 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	20480	
	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]		
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	26624	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	28672	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048	
	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288	
	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]		
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-20480	
	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]		
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-8192	
t2 AsstFWUprBoundY MtrNm s4p11[5][8]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288	
	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192	



ame	Input Value
_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
AsstFWDefltAssistX_HwNm_u8p8[0]	922
AsstFWDefltAssistX_HwNm_u8p8[1]	947
AsstFWDefltAssistX_HwNm_u8p8[2]	973
AsstFWDefltAssistX_HwNm_u8p8[3]	998
AsstFWDefltAssistX_HwNm_u8p8[4]	1024
AsstFWDefltAssistX_HwNm_u8p8[5]	1050
AsstFWDefltAssistX_HwNm_u8p8[6]	1075
AsstFWDefltAssistX_HwNm_u8p8[7]	1101
AsstFWDefltAssistX_HwNm_u8p8[8]	1126
AsstFWDefltAssistX_HwNm_u8p8[9]	1152
AsstFWDefltAssistX_HwNm_u8p8[10]	1178
AsstFWDefltAssistX_HwNm_u8p8[11]	1203
AsstFWDefltAssistX_HwNm_u8p8[12]	1229
AsstFWDefltAssistX_HwNm_u8p8[13]	1254
AsstFWDefltAssistX_HwNm_u8p8[14]	1280
AsstFWDefltAssistX_HwNm_u8p8[15]	1306
AsstFWDefltAssistX_HwNm_u8p8[16]	1331
AsstFWDefltAssistX_HwNm_u8p8[17]	1357
AsstFWDefltAssistX_HwNm_u8p8[18]	1382
AsstFWDefltAssistX_HwNm_u8p8[19]	1408
AsstFWDefltAssistY_MtrNm_s4p11[0]	16998
AsstFWDefltAssistY_MtrNm_s4p11[1]	17203
AsstFWDefltAssistY_MtrNm_s4p11[2]	17408
AsstFWDefltAssistY_MtrNm_s4p11[3]	17613
AsstFWDefltAssistY_MtrNm_s4p11[4]	17818
AsstFWDefltAssistY_MtrNm_s4p11[5]	18022
AsstFWDefltAssistY_MtrNm_s4p11[6]	18227
AsstFWDefltAssistY_MtrNm_s4p11[7]	18432
AsstFWDefltAssistY_MtrNm_s4p11[8]	18637
AsstFWDefltAssistY_MtrNm_s4p11[9]	18842
AsstFWDefltAssistY_MtrNm_s4p11[10]	19046
AsstFWDefltAssistY_MtrNm_s4p11[11]	19251
AsstFWDefltAssistY_MtrNm_s4p11[12]	19456
AsstFWDefltAssistY_MtrNm_s4p11[13]	19661
AsstFWDefltAssistY_MtrNm_s4p11[14]	19866
AsstFWDefltAssistY_MtrNm_s4p11[15]	20070
AsstFWDefltAssistY_MtrNm_s4p11[16]	20275
AsstFWDefltAssistY_MtrNm_s4p11[17]	20480
AsstFWDefltAssistY_MtrNm_s4p11[18]	20685
AsstFWDefltAssistY_MtrNm_s4p11[19]	20890
AsstFWPstepNstepThresh_Cnt_u16[0]	195
AsstFWPstepNstepThresh_Cnt_u16[1]	499
AsstFWVehSpd_Kph_u9p7[0]	45568
AsstFWVehSpd_Kph_u9p7[1]	45696
AsstFWVehSpd_Kph_u9p7[2]	45824
AsstFWVehSpd_Kph_u9p7[3]	45952
AsstFWVehSpd_Kph_u9p7[4]	46080
AsstFWVehSpd_Kph_u9p7[5]	46208
AsstFWVehSpd_Kph_u9p7[6]	46336
AsstFWVehSpd_Kph_u9p7[7]	46464
t_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.90999985
t_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
t_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
t_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
t_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-6
t_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
t_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	121.029999
	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	
	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	
t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cn	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cn t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cn t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_AssistFirewall_Per1_HwTorque_HwNm_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.769999981	0.769999981 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	499	499 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	•
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.70019531	8.70019531 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.69399977	5.69399977 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7	7 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.75899982	3.75900006 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.769999981	0.769999981 ± 3.05E-05	•
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.70019531	8.70019531 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	•
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Τ				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.75 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall ActiveKSV M str.K Uls f32	0.059999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	7995
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.119999997
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.4000001
k_AsstFWInpLimitHFA_MtrNm_f32	0
k_AsstFWInpLimitHysComp_MtrNm_f32	4
k_AsstFWNstep_Cnt_u16	2316
k_AsstFWPstep_Cnt_u16	1968
k_RestoreThresh_MtrNm_f32	1.19000006
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384 18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480 -10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240 -8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1] t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2 AsstFWUprBoundX HwNm s4p11[6][3]	-2048
t2 AsstFWUprBoundX HwNm s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-8192
tz_Assti Wopi bound i _With Min_s+p i T[o][+]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144
	-6144 -4096



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0] t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
	-10240 -8192 -6144



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	947
t_AsstFWDefltAssistX_HwNm_u8p8[1]	973
t_AsstFWDefltAssistX_HwNm_u8p8[2]	998
t_AsstFWDefltAssistX_HwNm_u8p8[3]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[8] t_AsstFWDefltAssistX_HwNm_u8p8[9]	1152 1178
t_AsstFWDefitAssistX_HwNm_u8p8[10]	1203
t_AsstFWDefitAssistX_HwNm_u8p8[11]	1229
t AsstFWDefltAssistX HwNm u8p8[12]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1382
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1408
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1434
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	19046
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[13] t_AsstFWDefltAssistY_MtrNm_s4p11[14]	19866 20070
t_AsstFWDefitAssistY_MtrNm_s4p11[14]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	20480
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	21094
t_AsstFWPstepNstepThresh_Cnt_u16[0]	196
t_AsstFWPstepNstepThresh_Cnt_u16[1]	503
t_AsstFWVehSpd_Kph_u9p7[0]	1408
t_AsstFWVehSpd_Kph_u9p7[1]	1536
t_AsstFWVehSpd_Kph_u9p7[2]	1664
t_AsstFWVehSpd_Kph_u9p7[3]	1792
t_AsstFWVehSpd_Kph_u9p7[4]	1920
t_AsstFWVehSpd_Kph_u9p7[5]	2048
t_AsstFWVehSpd_Kph_u9p7[6]	2176
t_AsstFWVehSpd_Kph_u9p7[7]	2304
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.03999996
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2 132.039993
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MiththTi32  tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt	
	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tot Rte Inst An AssistFirewall AssistFirewall Per1 HighFredAssist MtrNm f22	1912 10000 NOWAIL OF THE HIGH TOP 10010 LIVILITY IN THE
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tat AssistFirewall Per1 HwTorque HwNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tqt AssistFirewall Per1 HysteresisComp MtrNm f32
,	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.91400003	2.91400003 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	503	503 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.43200004	1.43200004 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5	5 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.96799994	4.96799994 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.76 (Repeat Count = 1)	
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	2.79999995
AssistFirewall ActiveKSV M str.K Uls f32	0.10000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8118
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.050000007
AssistFirewall HiFreqKSV M str.CF Uls f32	1.7999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall UprBoundKSV M str.K Uls f32	0.129999995
Rte_Inst_Ap_AssistFirewall	tgt Rte Inst Ap AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.5
k_AsstFWInpLimitHFA_MtrNm_f32	8.80000019
k_AsstFWInpLimitHysComp_MtrNm_f32	6.38000011
k_AsstFWNstep_Cnt_u16	2192
k_AsstFWPstep_Cnt_u16	2091
k RestoreThresh MtrNm f32	2.2100004
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2 AsstFWUprBoundX HwNm s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
t2 AsstFWUprBoundX HwNm s4p11[2][0]	0
E_7.000 TTOPIDOUIUX_ITWINII_0TPTT[2][0]	I.S.



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][10] 2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432
	-1843 <i>Z</i> -16384
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288
12_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
2 AsstFWUprBoundX HwNm s4p11[6][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144
12_Asst WorlboundY_MtrNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-2048



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Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288	
	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0	
, , , , , , , , , , , , , , , , , , , ,		
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192	
	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]		
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240	
	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-4096	



	(
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefltAssistX_HwNm_u8p8[0]	128
t_AsstFWDefltAssistX_HwNm_u8p8[1]	154
t_AsstFWDefltAssistX_HwNm_u8p8[2]	179
t_AsstFWDefltAssistX_HwNm_u8p8[3]	205
t_AsstFWDefltAssistX_HwNm_u8p8[4]	230
t_AsstFWDefltAssistX_HwNm_u8p8[5]	256
t_AsstFWDefltAssistX_HwNm_u8p8[6]	282
t_AsstFWDefltAssistX_HwNm_u8p8[7]	307
t_AsstFWDefltAssistX_HwNm_u8p8[8]	333
t_AsstFWDefltAssistX_HwNm_u8p8[9]	358
t_AsstFWDefltAssistX_HwNm_u8p8[10]	384
t_AsstFWDefltAssistX_HwNm_u8p8[11]	410
t_AsstFWDefltAssistX_HwNm_u8p8[12]	435
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	461 486
t_AsstFWDefitAssistX_HwNm_u8p8[14] t_AsstFWDefitAssistX_HwNm_u8p8[15]	512
t_AsstFWDefitAssistX_HwNm_u8p8[16]	538
t_AsstFWDefitAssistX_HwNm_u8p8[17]	563
t_AsstFWDefltAssistX_HwNm_u8p8[18]	589
t_AsstFWDefltAssistX_HwNm_u8p8[19]	614
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	21299
t_AsstFWPstepNstepThresh_Cnt_u16[0]	197
t_AsstFWPstepNstepThresh_Cnt_u16[1]	507
t_AsstFWVehSpd_Kph_u9p7[0]	4352
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	4480 4608
t_AsstFWVehSpd_Kph_u9p7[3]	4736
t_AsstFWVehSpd_Kph_u9p7[4]	4864
t_AsstFWVehSpd_Kph_u9p7[5]	4992
t_AsstFWVehSpd_Kph_u9p7[6]	5120
t_AsstFWVehSpd_Kph_u9p7[7]	5248
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.17000008
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	143.059998
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AsstTbl\_Service\_Cnt\_Ap\_AssistFirewall\_AsstTbl\_Service\_Cnt\_Ap\_AssistFirewall\_AsstTbl\_Service\_Cnt\_AsstTb$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.51999998	2.51999998 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	507	507 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.26999998	4.26999998 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.5	5.5 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.51999998	1.51999998 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	-
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	<b>✓</b>
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.77 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall ActiveKSV M str.K Uls f32	0.20000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8241
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	-5.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.059999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.8999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall LwrBoundKSV M str.K Uls f32	0.60000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.140000001
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.5999999
k AsstFWInpLimitHFA MtrNm f32	3,20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	6.48999977
k_AsstFWNstep_Cnt_u16	2812
k_AsstFWPstep_Cnt_u16	2214
k RestoreThresh MtrNm f32	2.22000003
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2 AsstFWUprBoundX HwNm s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2 AsstFWUprBoundX HwNm s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_Asst WopiBoundX_HwNm_s4p11[2][7]	0
	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_Asst WopiBoundX_nwnin_s4p11[0][9] t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
12_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192
12_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144
t2_AsstrWUprBoundY_MtrNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	i e e e e e e e e e e e e e e e e e e e
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	2048



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	8192 -30720
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0] t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-18432 -16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8] t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-14336 -12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288
t2 AsstFWUprBoundY MtrNm s4p11[5][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048



	(
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	26
t_AsstFWDefltAssistX_HwNm_u8p8[1]	51
t_AsstFWDefltAssistX_HwNm_u8p8[2]	77
t_AsstFWDefltAssistX_HwNm_u8p8[3]	102
t_AsstFWDefltAssistX_HwNm_u8p8[4]	128
t_AsstFWDefltAssistX_HwNm_u8p8[5]	154
t_AsstFWDefltAssistX_HwNm_u8p8[6]	179
t_AsstFWDefltAssistX_HwNm_u8p8[7]	205
t_AsstFWDefltAssistX_HwNm_u8p8[8]	230 256
t_AsstFWDefltAssistX_HwNm_u8p8[9] t_AsstFWDefltAssistX_HwNm_u8p8[10]	282
t_AsstFWDefltAssistX_HwNm_u8p8[11]	307
t_AsstFWDefltAssistX_HwNm_u8p8[12]	333
t_AsstFWDefitAssistX_HwNm_u8p8[13]	358
t_AsstFWDefltAssistX_HwNm_u8p8[14]	384
t_AsstFWDefitAssistX_HwNm_u8p8[15]	410
t_AsstFWDefitAssistX_HwNm_u8p8[16]	435
t_AsstFWDefltAssistX_HwNm_u8p8[17]	461
t_AsstFWDefltAssistX_HwNm_u8p8[18]	486
t_AsstFWDefltAssistX_HwNm_u8p8[19]	512
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	21504
t_AsstFWPstepNstepThresh_Cnt_u16[0] t_AsstFWPstepNstepThresh_Cnt_u16[1]	198 511
t_AsstFWVehSpd_Kph_u9p7[0]	7296
t_AsstFWVehSpd_Kph_u9p7[0] t_AsstFWVehSpd_Kph_u9p7[1]	7424
t_AsstFWVehSpd_Kph_u9p7[2]	7552
t_AsstFWVehSpd_Kph_u9p7[3]	7680
t AsstFWVehSpd Kph u9p7[4]	7808
t_AsstFWVehSpd_Kph_u9p7[5]	7936
t_AsstFWVehSpd_Kph_u9p7[6]	8064
t_AsstFWVehSpd_Kph_u9p7[7]	8192
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.30000019
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.3999998
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	154.300003
·	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32$	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall.Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cn tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32  tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32  t_lt_tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cn tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 t_lt_tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cntgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 t_tt_tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cn tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 t_lt_tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.879999995	0.879999995 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	511	511 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.454	5.454 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.19999981	5.19999981 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.55999994	2.55999994 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.879999995	0.879999995 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.78 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.099999
AssistFirewall ActiveKSV M str.K Uls f32	0.30000012
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8364
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall CombAsstSV MtrNm M f32	-5.6999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.070000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.150000006
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	0
k AsstFWInpLimitHFA MtrNm f32	1
k_AsstFWInpLimitHysComp_MtrNm_f32	6.5999999
k_AsstFWNstep_Cnt_u16	2688
k_AsstFWPstep_Cnt_u16	2337
k RestoreThresh MtrNm f32	2.23000002
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2 AsstFWUprBoundX HwNm s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_Asst WopiBoundX_HwNm_s4p11[6][9]	16384
:z_AsstFWUprBoundX_HwNm_s4p11[6][10] :2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
tz_AsstFWUprBoundX_HWNm_s4p11[7][2] t2 AsstFWUprBoundX HwNm_s4p11[7][3]	0
_ , ,	
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144 8192
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	2048



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-10240	
, , , , , , , , , , , , , , , , , , , ,	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]		
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-28672	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-20480	
2 AsstFWUprBoundY MtrNm s4p11[2][5]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048	
	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-28672	
	-26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]		
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]		
	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528	
12_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048	



	(
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	51
t_AsstFWDefltAssistX_HwNm_u8p8[1]	77
t_AsstFWDefltAssistX_HwNm_u8p8[2]	102
t_AsstFWDefltAssistX_HwNm_u8p8[3]	128
t_AsstFWDefltAssistX_HwNm_u8p8[4]	154
t_AsstFWDefltAssistX_HwNm_u8p8[5]	179
t_AsstFWDefltAssistX_HwNm_u8p8[6]	205
t_AsstFWDefltAssistX_HwNm_u8p8[7]	230
t_AsstFWDefltAssistX_HwNm_u8p8[8]	256
t_AsstFWDefltAssistX_HwNm_u8p8[9]	282
t_AsstFWDefltAssistX_HwNm_u8p8[10]	307
t_AsstFWDefltAssistX_HwNm_u8p8[11]	333
t_AsstFWDefltAssistX_HwNm_u8p8[12]	358
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	384 410
t_AsstFWDefitAssistX_HwNm_u8p8[14] t_AsstFWDefitAssistX_HwNm_u8p8[15]	410
t_AsstFWDefitAssistX_HwNm_u8p8[16]	461
t_AsstFWDefitAssistX_HwNm_u8p8[17]	486
t_AsstFWDefltAssistX_HwNm_u8p8[18]	512
t AsstFWDefltAssistX HwNm u8p8[19]	538
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	21709
t_AsstFWPstepNstepThresh_Cnt_u16[0]	199
t_AsstFWPstepNstepThresh_Cnt_u16[1]	515
t_AsstFWVehSpd_Kph_u9p7[0]	10240
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	10368 10496
t_AsstFWVehSpd_Kph_u9p7[3]	10624
t_AsstFWVehSpd_Kph_u9p7[4]	10752
t_AsstFWVehSpd_Kph_u9p7[5]	10880
t_AsstFWVehSpd_Kph_u9p7[6]	11008
t_AsstFWVehSpd_Kph_u9p7[7]	11136
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.42999983
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.70000005
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	165.100006
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFirewal$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2 AsstFWUprBoundX HwNm s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2 AsstFWUprBoundX HwNm s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2 AsstFWUprBoundX HwNm s4p11[7][1]	-2048
t2 AsstFWUprBoundX HwNm s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	6144



Name	Input Value	
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096	
	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]		
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-26624	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-24576	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240	
· · · · · · · · · · · · · · · · · · ·	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]		
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]		
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240 -8192	
	-8192	
A GOOD IN INCLUDED A SANTAGE OF	-8192 -6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192 -6144 -4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-8192 -6144 -4096 -2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5] 2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-8192 -6144 -4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-8192 -6144 -4096 -2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5] 2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-8192 -6144 -4096 -2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5] 2_AsstFWUprBoundY_MtrNm_s4p11[5][6] 2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-8192 -6144 -4096 -2048 0	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5] 2_AsstFWUprBoundY_MtrNm_s4p11[5][6] 2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-8192 -6144 -4096 -2048 0 2048 4096 6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5] 2_AsstFWUprBoundY_MtrNm_s4p11[5][6] 2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-8192 -6144 -4096 -2048 0 2048 4096 6144 8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5] 2_AsstFWUprBoundY_MtrNm_s4p11[5][6] 2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192 -6144 -4096 -2048 0 2048 4096 6144 8192 -6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5] 2_AsstFWUprBoundY_MtrNm_s4p11[5][6] 2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192 -6144 -4096 -2048 0 2048 4096 6144 8192 -6144 -4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5] 2_AsstFWUprBoundY_MtrNm_s4p11[5][6] 2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192 -6144 -4096 -2048 0 2048 4096 6144 8192 -6144 -4096 -2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5] 2_AsstFWUprBoundY_MtrNm_s4p11[5][6] 2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192 -6144 -4096 -2048 0 2048 4096 6144 8192 -6144 -4096 -2048 0	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5] 2_AsstFWUprBoundY_MtrNm_s4p11[5][6] 2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192 -6144 -4096 -2048 0 2048 4096 6144 8192 -6144 -4096 -2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5] 2_AsstFWUprBoundY_MtrNm_s4p11[5][6] 2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192 -6144 -4096 -2048 0 2048 4096 6144 8192 -6144 -4096 -2048 0	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5] 2_AsstFWUprBoundY_MtrNm_s4p11[5][6] 2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-8192 -6144 -4096 -2048 0 2048 4096 6144 8192 -6144 -4096 -2048 0 2048 4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5] 2_AsstFWUprBoundY_MtrNm_s4p11[5][6] 2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 2_AsstFWUprBoundY_MtrNm_s4p11[6][5] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-8192 -6144 -4096 -2048 0 2048 4096 6144 8192 -6144 -4096 -2048 0 2048 4096 6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5] 2_AsstFWUprBoundY_MtrNm_s4p11[5][6] 2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-8192 -6144 -4096 -2048 0 2048 4096 6144 8192 -6144 -4096 -2048 0 2048 4096 6144 8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5] 2_AsstFWUprBoundY_MtrNm_s4p11[5][6] 2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 2_AsstFWUprBoundY_MtrNm_s4p11[6][5] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-8192 -6144 -4096 -2048 0 2048 4096 6144 8192 -6144 -4096 -2048 0 2048 4096 6144 8192 10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5] 2_AsstFWUprBoundY_MtrNm_s4p11[5][6] 2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-8192 -6144 -4096 -2048 0 2048 4096 6144 8192 -6144 -4096 -2048 0 2048 4096 6144 8192 10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5] 2_AsstFWUprBoundY_MtrNm_s4p11[5][6] 2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 2_AsstFWUprBoundY_MtrNm_s4p11[6][5] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-8192 -6144 -4096 -2048 0 2048 4096 6144 8192 -6144 -4096 -2048 0 2048 4096 6144 8192 10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5] 2_AsstFWUprBoundY_MtrNm_s4p11[5][6] 2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-8192 -6144 -4096 -2048 0 2048 4096 6144 8192 -6144 -4096 -2048 0 2048 4096 6144 8192 10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5] 2_AsstFWUprBoundY_MtrNm_s4p11[5][6] 2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 2_AsstFWUprBoundY_MtrNm_s4p11[5][9] 2_AsstFWUprBoundY_MtrNm_s4p11[5][10] 2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	-8192 -6144 -4096 -2048 0 2048 4096 6144 8192 -6144 -4096 -2048 0 2048 4096 6144 8192 10248 10248 10240 12288 14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5] 2_AsstFWUprBoundY_MtrNm_s4p11[5][6] 2_AsstFWUprBoundY_MtrNm_s4p11[5][7] 2_AsstFWUprBoundY_MtrNm_s4p11[5][8] 2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	-8192 -6144 -4096 -2048 0 2048 4096 6144 8192 -6144 -4096 -2048 0 2048 4096 6144 8192 10240 12288 14336 -2048	



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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	77
t_AsstFWDefltAssistX_HwNm_u8p8[1]	102
t_AsstFWDefltAssistX_HwNm_u8p8[2]	128
t_AsstFWDefltAssistX_HwNm_u8p8[3]	154
t_AsstFWDefltAssistX_HwNm_u8p8[4]	179
t_AsstFWDefltAssistX_HwNm_u8p8[5]	205
t_AsstFWDefltAssistX_HwNm_u8p8[6]	230
t_AsstFWDefltAssistX_HwNm_u8p8[7]	256
t_AsstFWDefltAssistX_HwNm_u8p8[8]	282
t_AsstFWDefltAssistX_HwNm_u8p8[9]	307
t_AsstFWDefltAssistX_HwNm_u8p8[10]	333
t_AsstFWDefltAssistX_HwNm_u8p8[11]	358
t_AsstFWDefltAssistX_HwNm_u8p8[12]	384
t_AsstFWDefltAssistX_HwNm_u8p8[13]	410
t_AsstFWDefltAssistX_HwNm_u8p8[14]	435
t_AsstFWDefltAssistX_HwNm_u8p8[15]	461
t_AsstFWDefltAssistX_HwNm_u8p8[16]	486
t_AsstFWDefltAssistX_HwNm_u8p8[17]	512
t_AsstFWDefltAssistX_HwNm_u8p8[18]	538
t_AsstFWDefltAssistX_HwNm_u8p8[19]	563
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	18022
t_AsstFWDefitAssistY_MtrNm_s4p11[1]	18227
,	
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	21914
t_AsstFWPstepNstepThresh_Cnt_u16[0]	200
t AsstFWPstepNstepThresh Cnt u16[1]	519
t_AsstFWVehSpd_Kph_u9p7[0]	13184
t_AsstFWVehSpd_Kph_u9p7[1]	13312
t_AsstFWVehSpd_Kph_u9p7[2]	13440
t_AsstFWVehSpd_Kph_u9p7[3]	13568
t_AsstFWVehSpd_kpri_u9p7[3] t_AsstFWVehSpd_kph_u9p7[4]	13696
t_AsstFWVehSpd_Kph_u9p7[5]	13824
t_AsstFWVehSpd_Kph_u9p7[6]	13952
t_AsstFWVehSpd_Kph_u9p7[7]	14080
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.55999994
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2.5999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f3	2 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f3	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_C	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall Per1 HighFregAssist MtrNm f32	
• • • • • • • • • • • • • • • • • • • •	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f3; tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f3; tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.63199997	2.63199997 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	519	519 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.68479991	1.68480003 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.5	3.5 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4	4 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•

T ✓				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.80 (Repeat Count = 1)	· ·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall ActiveKSV M str.K Uls f32	0.019999996
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8610
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-5.9000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.029999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	2
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall LwrBoundKSV M str.K Uls f32	0.60000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.170000002
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.5
k_AsstFWInpLimitHFA_MtrNm_f32	3
k_AsstFWInpLimitHysComp_MtrNm_f32	6.80000019
k_AsstFWNstep_Cnt_u16	2440
k_AsstFWPstep_Cnt_u16	1599
k RestoreThresh MtrNm f32	2.25
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	2048
	2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096 6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096 6144 8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096 6144 8192 10240 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096 6144 8192 10240 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096 6144 8192 10240 -2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096 6144 8192 10240 -2048 0 2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	4096 6144 8192 10240 -2048 0 2048 4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	4096 6144 8192 10240 -2048 0 2048 4096 6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096 6144 8192 10240 -2048 0 2048 4096 6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096 6144 8192 10240 -2048 0 2048 4096 6144 8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096 6144 8192 10240 -2048 0 2048 4096 6144 8192 10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096 6144 8192 10240 -2048 0 2048 4096 6144 8192 10240 12288 14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096 6144 8192 10240 -2048 0 2048 4096 6144 8192 10240 12288 14336 16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096 6144 8192 10240 -2048 0 2048 4096 6144 8192 10240 12288 14336 16384 18432 0



Ame  _AsstFWUprBoundY_MtrNm_s4p11[7][4]  _AsstFWUprBoundY_MtrNm_s4p11[7][5]  _AsstFWUprBoundY_MtrNm_s4p11[7][6]  _AsstFWUprBoundY_MtrNm_s4p11[7][7]  _AsstFWUprBoundY_MtrNm_s4p11[7][8]  _AsstFWUprBoundY_MtrNm_s4p11[7][9]  _AsstFWUprBoundY_MtrNm_s4p11[7][10]  AsstFWUprBoundY_MtrNm_s4p11[7][10]  AsstFWUprBoundY_MtrNm_s4p11[7][10]  AsstFWUpfBoundY_MtrNm_s4p8[0]	Input Value 8192 10240 12288 14336
_AsstFWUprBoundY_MtrNm_s4p11[7][4] _AsstFWUprBoundY_MtrNm_s4p11[7][5] _AsstFWUprBoundY_MtrNm_s4p11[7][6] _AsstFWUprBoundY_MtrNm_s4p11[7][7] _AsstFWUprBoundY_MtrNm_s4p11[7][8] _AsstFWUprBoundY_MtrNm_s4p11[7][9] _AsstFWUprBoundY_MtrNm_s4p11[7][9] _AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192 10240 12288 14336
_AsstFWUprBoundY_MtrNm_s4p11[7][5] _AsstFWUprBoundY_MtrNm_s4p11[7][6] _AsstFWUprBoundY_MtrNm_s4p11[7][7] _AsstFWUprBoundY_MtrNm_s4p11[7][8] _AsstFWUprBoundY_MtrNm_s4p11[7][9] _AsstFWUprBoundY_MtrNm_s4p11[7][10] _AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240 12288 14336
_AsstFWUprBoundY_MtrNm_s4p11[7][6] _AsstFWUprBoundY_MtrNm_s4p11[7][7] _AsstFWUprBoundY_MtrNm_s4p11[7][8] _AsstFWUprBoundY_MtrNm_s4p11[7][9] _AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288 14336
_AsstFWUprBoundY_MtrNm_s4p11[7][7] _AsstFWUprBoundY_MtrNm_s4p11[7][8] _AsstFWUprBoundY_MtrNm_s4p11[7][9] _AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
_AsstFWUprBoundY_MtrNm_s4p11[7][8] _AsstFWUprBoundY_MtrNm_s4p11[7][9] _AsstFWUprBoundY_MtrNm_s4p11[7][10]	
_AsstFWUprBoundY_MtrNm_s4p11[7][9] _AsstFWUprBoundY_MtrNm_s4p11[7][10]	16904
_AsstFWUprBoundY_MtrNm_s4p11[7][10]	16384
	18432
AsstFWDefltAssistX_HwNm_u8p8[0]	20480
	102
AsstFWDefltAssistX_HwNm_u8p8[1]	128
AsstFWDefltAssistX_HwNm_u8p8[2]	154
AsstFWDefltAssistX_HwNm_u8p8[3]	179
AsstFWDefltAssistX_HwNm_u8p8[4]	205
AsstFWDefltAssistX_HwNm_u8p8[5]	230
AsstFWDefltAssistX_HwNm_u8p8[6]	256
AsstFWDefltAssistX_HwNm_u8p8[7]	282
AsstFWDefltAssistX_HwNm_u8p8[8]	307
	333
AsstFWDefltAssistX_HwNm_u8p8[9]	
AsstFWDefltAssistX_HwNm_u8p8[10]	358
AsstFWDefltAssistX_HwNm_u8p8[11]	384
AsstFWDefltAssistX_HwNm_u8p8[12]	410
AsstFWDefltAssistX_HwNm_u8p8[13]	435
AsstFWDefltAssistX_HwNm_u8p8[14]	461
AsstFWDefltAssistX_HwNm_u8p8[15]	486
AsstFWDefltAssistX_HwNm_u8p8[16]	512
AsstFWDefltAssistX_HwNm_u8p8[17]	538
AsstFWDefitAssistX_HwNm_u8p8[18]	563
AsstFWDefitAssistX_HwNm_u8p8[19]	589
, , ,	
AsstFWDefltAssistY_MtrNm_s4p11[0]	18227
AsstFWDefltAssistY_MtrNm_s4p11[1]	18432
AsstFWDefltAssistY_MtrNm_s4p11[2]	18637
AsstFWDefltAssistY_MtrNm_s4p11[3]	18842
AsstFWDefltAssistY_MtrNm_s4p11[4]	19046
AsstFWDefltAssistY_MtrNm_s4p11[5]	19251
AsstFWDefltAssistY_MtrNm_s4p11[6]	19456
AsstFWDefltAssistY_MtrNm_s4p11[7]	19661
AsstFWDefltAssistY_MtrNm_s4p11[8]	19866
AsstFWDefltAssistY_MtrNm_s4p11[9]	20070
AsstFWDefltAssistY_MtrNm_s4p11[10]	20275
AsstFWDefltAssistY_MtrNm_s4p11[11]	20480
AsstFWDefltAssistY_MtrNm_s4p11[12]	20685
AsstFWDefltAssistY_MtrNm_s4p11[13]	20890
AsstFWDefltAssistY_MtrNm_s4p11[14]	21094
AsstFWDefltAssistY_MtrNm_s4p11[15]	21299
AsstFWDefltAssistY_MtrNm_s4p11[16]	21504
AsstFWDefltAssistY_MtrNm_s4p11[17]	21709
AsstFWDefltAssistY_MtrNm_s4p11[18]	21914
AsstFWDefltAssistY_MtrNm_s4p11[19]	22118
AsstFWPstepNstepThresh_Cnt_u16[0]	201
AsstFWPstepNstepThresh_Cnt_u16[1]	523
AsstFWVehSpd_Kph_u9p7[0]	16128
AsstFWVehSpd_Kph_u9p7[1]	16256
AsstFWVehSpd_Kph_u9p7[2]	16384
AsstFWVehSpd_Kph_u9p7[3]	16512
AsstFWVehSpd_Kph_u9p7[4]	16640
AsstFWVehSpd_Kph_u9p7[5]	16768
AsstFWVehSpd_Kph_u9p7[6]	16896
AsstFWVehSpd_Kph_u9p7[7]	17024
t_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.69000006
t_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
t_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4.5999999
• •	4.5999999
t_AssistFirewall_Per1_HwTorque_HwNm_f32.value	
t_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
t_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
t_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	187.300003
t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
_ ,	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
Rte Inst Ap AssistFirewall.AssistFirewall Per1 HighFregAssist MtrNm f32	
t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tot AssistFirewall Per1 HwTorque HwNm f32
t_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.07800007	1.07799995 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	523	523 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.35900009	1.35899997 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.79999971	2.79999995 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5	5 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.81 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	1.10000002
AssistFirewall ActiveKSV M str.K Uls f32	0.100000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.029999993
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	3.29999995
k_AsstFWInpLimitHysComp_MtrNm_f32	3.9000001
k_AsstFWNstep_Cnt_u16	3690
k_AsstFWPstep_Cnt_u16	2706
k_RestoreThresh_MtrNm_f32	2.25999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2 AsstFWUprBoundX HwNm s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	4096
	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	
t2 AcctEM/I IntRoundV MirNim c4n44[0][5]	9102
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	8192 10240



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384	
	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]		
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288	
	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]		
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336	
t2 AsstFWUprBoundY MtrNm s4p11[2][5]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480	
	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]		
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096	
t2 AsstFWUprBoundY MtrNm s4p11[5][3]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	14336	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	128
t_AsstFWDefltAssistX_HwNm_u8p8[1]	154
t_AsstFWDefltAssistX_HwNm_u8p8[2]	179
t_AsstFWDefltAssistX_HwNm_u8p8[3]	205
t_AsstFWDefltAssistX_HwNm_u8p8[4]	230
t_AsstFWDefltAssistX_HwNm_u8p8[5]	256
t_AsstFWDefltAssistX_HwNm_u8p8[6]	282
t_AsstFWDefltAssistX_HwNm_u8p8[7]	307
t_AsstFWDefltAssistX_HwNm_u8p8[8]	333
	358
t_AsstFWDefltAssistX_HwNm_u8p8[9]	
t_AsstFWDefltAssistX_HwNm_u8p8[10]	384
t_AsstFWDefltAssistX_HwNm_u8p8[11]	410
t_AsstFWDefltAssistX_HwNm_u8p8[12]	435
t_AsstFWDefltAssistX_HwNm_u8p8[13]	461
t_AsstFWDefltAssistX_HwNm_u8p8[14]	486
t_AsstFWDefltAssistX_HwNm_u8p8[15]	512
t_AsstFWDefltAssistX_HwNm_u8p8[16]	538
t_AsstFWDefltAssistX_HwNm_u8p8[17]	563
t_AsstFWDefitAssistX_HwNm_u8p8[18]	589
t_AsstFWDefltAssistX_HwNm_u8p8[19]	614
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	22323
t_AsstFWPstepNstepThresh_Cnt_u16[0]	202
t_AsstFWPstepNstepThresh_Cnt_u16[1]	527
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
t_AsstFWVehSpd_Kph_u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	123.099998
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f3.	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f	
•	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_(	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f3	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
	foo that Anniat Firewall Dank United and Commandate foo
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_t	f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_t tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	·



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.99000001	0.99000001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0	0 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.19999981	8.19999981 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.30499983	4.30499983 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-1	-1 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.15699983	3.15700006 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.99000001	0.99000001 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.19999981	8.19999981 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x00	0x00	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	✓

T			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.82 (Repeat Count = 1)	·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-8.80000019
AssistFirewall ActiveKSV M str.K Uls f32	0.20000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	65535
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0599999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.8999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.090000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.039999991
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.20000005
k_AsstFWInpLimitHFA_MtrNm_f32	4.4000001
k_AsstFWInpLimitHysComp_MtrNm_f32	4.0999999
k_AsstFWNstep_Cnt_u16	3813
k_AsstFWPstep_Cnt_u16	2829
k_RestoreThresh_MtrNm_f32	2.26999998
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	14336



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-12288
2 AsstFWUprBoundY MtrNm s4p11[2][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-8192
	-619Z -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336
	· · · · · ·
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-12288 -10240



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	154
t_AsstFWDefltAssistX_HwNm_u8p8[1]	179
t_AsstFWDefltAssistX_HwNm_u8p8[2]	205
t_AsstFWDefltAssistX_HwNm_u8p8[3]	230
t_AsstFWDefltAssistX_HwNm_u8p8[4]	256
t_AsstFWDefltAssistX_HwNm_u8p8[5]	282
t_AsstFWDefltAssistX_HwNm_u8p8[6]	307
t_AsstFWDefltAssistX_HwNm_u8p8[7]	333
t_AsstFWDefltAssistX_HwNm_u8p8[8]	358
t_AsstFWDefltAssistX_HwNm_u8p8[9]	384
t_AsstFWDefltAssistX_HwNm_u8p8[10]	410
t_AsstFWDefltAssistX_HwNm_u8p8[11]	435
t_AsstFWDefltAssistX_HwNm_u8p8[12]	461
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	486 512
t_AsstFWDefitAssistX_HwNm_u8p8[14] t_AsstFWDefitAssistX_HwNm_u8p8[15]	512 538
t_AsstFWDefitAssistX_HwNm_u8p8[16]	563
t_AsstFWDefitAssistX_HwNm_u8p8[17]	589
t_AsstFWDefltAssistX_HwNm_u8p8[18]	614
t_AsstFWDefitAssistX_HwNm_u8p8[19]	640
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	22528
t_AsstFWPstepNstepThresh_Cnt_u16[0]	203
t_AsstFWPstepNstepThresh_Cnt_u16[1]	531
t_AsstFWVehSpd_Kph_u9p7[0]	22016
t_AsstFWVehSpd_Kph_u9p7[1]	22144
t_AsstFWVehSpd_Kph_u9p7[2]	22272 22400
t_AsstFWVehSpd_Kph_u9p7[3] t AsstFWVehSpd_Kph_u9p7[4]	22528
t_AsstFWVehSpd_Kph_u9p7[5]	22656
t_AsstFWVehSpd_Kph_u9p7[6]	22784
t_AsstFWVehSpd_Kph_u9p7[7]	22912
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	234.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-7.03999996	-7.03999996 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	531	531 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.42399979	5.42399979 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.55000019	7.55000019 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.01599979	4.01599979 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	-
Status_Cnt_T_enum	0x01	0x01	~

Τ				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.83 (Repeat Count = 1)	v
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall ActiveKSV M str.K Uls f32	0.300000012
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1000
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	6.099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.070000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.600000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.109999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4
k_AsstFWInpLimitHFA_MtrNm_f32	1.3999998
k_AsstFWInpLimitHysComp_MtrNm_f32	4.0999999
k_AsstFWNstep_Cnt_u16	2812
k_AsstFWPstep_Cnt_u16	1968
k_RestoreThresh_MtrNm_f32	2.27999997
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
:2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
:2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
:2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	8192
	10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192
12_1001 VVOPIDOUTO1_IVILITATII_34P11[1][3]	-0102



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	179
t_AsstFWDefltAssistX_HwNm_u8p8[1]	205
t_AsstFWDefltAssistX_HwNm_u8p8[2]	230
t_AsstFWDefltAssistX_HwNm_u8p8[3]	256
t_AsstFWDefltAssistX_HwNm_u8p8[4]	282
t_AsstFWDefltAssistX_HwNm_u8p8[5]	307
t_AsstFWDefltAssistX_HwNm_u8p8[6]	333
t_AsstFWDefltAssistX_HwNm_u8p8[7]	358
t_AsstFWDefltAssistX_HwNm_u8p8[8]	384
t_AsstFWDefltAssistX_HwNm_u8p8[9]	410
t_AsstFWDefltAssistX_HwNm_u8p8[10]	435
t_AsstFWDefltAssistX_HwNm_u8p8[11]	461
t_AsstFWDefltAssistX_HwNm_u8p8[12]	486
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	512 538
t_AsstFWDefitAssistX_HwNm_u8p8[14] t_AsstFWDefitAssistX_HwNm_u8p8[15]	563
t_AsstFWDefltAssistX_HwNm_u8p8[16]	589
t_AsstFWDefltAssistX_HwNm_u8p8[17]	614
t_AsstFWDefltAssistX_HwNm_u8p8[18]	640
t_AsstFWDefltAssistX_HwNm_u8p8[19]	666
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	22733
t_AsstFWPstepNstepThresh_Cnt_u16[0]	204
t_AsstFWPstepNstepThresh_Cnt_u16[1]	535
t_AsstFWVehSpd_Kph_u9p7[0]	24960
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	25088 25216
t_AsstFWVehSpd_Kph_u9p7[3]	25344
t AsstFWVehSpd Kph u9p7[4]	25472
t_AsstFWVehSpd_Kph_u9p7[5]	25600
t_AsstFWVehSpd_Kph_u9p7[6]	25728
t_AsstFWVehSpd_Kph_u9p7[7]	25856
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	77.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFi$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.76999981	0.769999981 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0	0 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.33099985	6.33099985 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.39999619	0.400000006 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8.32999992	8.32999992 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.769999981	0.769999981 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x00	0x00	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T ✓				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.84 (Repeat Count = 1)	🕶
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall ActiveKSV M str.K Uls f32	0.0599999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	200
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	6.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.119999997
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	1.5
k_AsstFWInpLimitHysComp_MtrNm_f32	4.30000019
k_AsstFWNstep_Cnt_u16	2688
k_AsstFWPstep_Cnt_u16	2091
k RestoreThresh MtrNm f32	2.28999996
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
t2 AsstFWUprBoundX HwNm s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	18432
	11-14-



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384	
	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]		
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	20480	
	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048	
	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]		
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	26624	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240	
	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	205
t_AsstFWDefltAssistX_HwNm_u8p8[1]	230
t_AsstFWDefltAssistX_HwNm_u8p8[2]	256
t_AsstFWDefltAssistX_HwNm_u8p8[3]	282
t_AsstFWDefltAssistX_HwNm_u8p8[4]	307
t_AsstFWDefltAssistX_HwNm_u8p8[5]	333
t_AsstFWDefltAssistX_HwNm_u8p8[6]	358
t_AsstFWDefltAssistX_HwNm_u8p8[7]	384
t_AsstFWDefltAssistX_HwNm_u8p8[8]	410
	435
t_AsstFWDefltAssistX_HwNm_u8p8[9]	
t_AsstFWDefltAssistX_HwNm_u8p8[10]	461
t_AsstFWDefltAssistX_HwNm_u8p8[11]	486
t_AsstFWDefltAssistX_HwNm_u8p8[12]	512
t_AsstFWDefltAssistX_HwNm_u8p8[13]	538
t_AsstFWDefltAssistX_HwNm_u8p8[14]	563
t_AsstFWDefltAssistX_HwNm_u8p8[15]	589
t_AsstFWDefltAssistX_HwNm_u8p8[16]	614
t_AsstFWDefltAssistX_HwNm_u8p8[17]	640
t_AsstFWDefitAssistX_HwNm_u8p8[18]	666
t AsstFWDefitAssistX HwNm u8p8[19]	691
, , ,	
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	20890
1 11	
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	22733
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	22938
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t_AsstFWPstepNstepThresh_Cnt_u16[0]	0
t_AsstFWPstepNstepThresh_Cnt_u16[1]	0
t_AsstFWVehSpd_Kph_u9p7[0]	27904
t_AsstFWVehSpd_Kph_u9p7[1]	28032
t_AsstFWVehSpd_Kph_u9p7[2]	28160
t_AsstFWVehSpd_Kph_u9p7[3]	28288
t_AsstFWVehSpd_Kph_u9p7[4]	28416
t_AsstFWVehSpd_Kph_u9p7[5]	28544
t_AsstFWVehSpd_Kph_u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7]	28800
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	88.1999969
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_	_f32 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNn	•
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tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNn	



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.91400003	2.91400003 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0	0 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.71199989	1.71200001 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.199999809	0.200000003 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.0480001	2.0480001 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.85 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.79999995
AssistFirewall ActiveKSV M str.K Uls f32	0.10000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	344
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	6.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.129999995
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.1999981
k_AsstFWInpLimitHFA_MtrNm_f32	1.70000005
k_AsstFWInpLimitHysComp_MtrNm_f32	4.5
k_AsstFWNstep_Cnt_u16	2564
k_AsstFWPstep_Cnt_u16	2214
k_RestoreThresh_MtrNm_f32	3.30999994
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0



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lame	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
2 AsstFWUprBoundX HwNm s4p11[2][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][3] 2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
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ASSESSED TO THE COURT OF THE PROPERTY OF THE P	0
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][7] 2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048 4096
PAsstFWUprBoundX_HwNm_s4p11[7][7] PAsstFWUprBoundX_HwNm_s4p11[7][8] PAsstFWUprBoundX_HwNm_s4p11[7][9]	2048 4096 6144
2_AsstFWUprBoundX_HwNm_s4p11[7][7] 2_AsstFWUprBoundX_HwNm_s4p11[7][8] 2_AsstFWUprBoundX_HwNm_s4p11[7][9] 2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048 4096 6144 8192
2_AsstFWUprBoundX_HwNm_s4p11[7][7] 2_AsstFWUprBoundX_HwNm_s4p11[7][8] 2_AsstFWUprBoundX_HwNm_s4p11[7][9] 2_AsstFWUprBoundX_HwNm_s4p11[7][10] 2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048 4096 6144 8192 6144
2_AsstFWUprBoundX_HwNm_s4p11[7][7] 2_AsstFWUprBoundX_HwNm_s4p11[7][8] 2_AsstFWUprBoundX_HwNm_s4p11[7][9] 2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048 4096 6144 8192
2_AsstFWUprBoundX_HwNm_s4p11[7][7] 2_AsstFWUprBoundX_HwNm_s4p11[7][8] 2_AsstFWUprBoundX_HwNm_s4p11[7][9] 2_AsstFWUprBoundX_HwNm_s4p11[7][10] 2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048 4096 6144 8192 6144
2_AsstFWUprBoundX_HwNm_s4p11[7][7] 2_AsstFWUprBoundX_HwNm_s4p11[7][8] 2_AsstFWUprBoundX_HwNm_s4p11[7][9] 2_AsstFWUprBoundX_HwNm_s4p11[7][10] 2_AsstFWUprBoundY_MtrNm_s4p11[0][0] 2_AsstFWUprBoundY_MtrNm_s4p11[0][0] 2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048 4096 6144 8192 6144 8192
2_AsstFWUprBoundX_HwNm_s4p11[7][7] 2_AsstFWUprBoundX_HwNm_s4p11[7][8] 2_AsstFWUprBoundX_HwNm_s4p11[7][9] 2_AsstFWUprBoundX_HwNm_s4p11[7][10] 2_AsstFWUprBoundY_MtrNm_s4p11[0][0] 2_AsstFWUprBoundY_MtrNm_s4p11[0][1] 2_AsstFWUprBoundY_MtrNm_s4p11[0][1] 2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048 4096 6144 8192 6144 8192 10240
2_AsstFWUprBoundX_HwNm_s4p11[7][7] 2_AsstFWUprBoundX_HwNm_s4p11[7][8] 2_AsstFWUprBoundX_HwNm_s4p11[7][9] 2_AsstFWUprBoundX_HwNm_s4p11[7][10] 2_AsstFWUprBoundY_MtrNm_s4p11[0][0] 2_AsstFWUprBoundY_MtrNm_s4p11[0][1] 2_AsstFWUprBoundY_MtrNm_s4p11[0][2] 2_AsstFWUprBoundY_MtrNm_s4p11[0][2] 2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048 4096 6144 8192 6144 8192 10240 12288
2_AsstFWUprBoundX_HwNm_s4p11[7][7] 2_AsstFWUprBoundX_HwNm_s4p11[7][8] 2_AsstFWUprBoundX_HwNm_s4p11[7][9] 2_AsstFWUprBoundX_HwNm_s4p11[7][10] 2_AsstFWUprBoundY_MtrNm_s4p11[0][0] 2_AsstFWUprBoundY_MtrNm_s4p11[0][1] 2_AsstFWUprBoundY_MtrNm_s4p11[0][2] 2_AsstFWUprBoundY_MtrNm_s4p11[0][3] 2_AsstFWUprBoundY_MtrNm_s4p11[0][3] 2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048 4096 6144 8192 6144 8192 10240 12288 14336



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5] t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-20480 -18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6] t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	6144
t2 AsstFWUprBoundY MtrNm s4p11[5][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-4096
	1 ***



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096
	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefltAssistX_HwNm_u8p8[0]	230
t_AsstFWDefltAssistX_HwNm_u8p8[1]	256
t_AsstFWDefltAssistX_HwNm_u8p8[2]	282
t_AsstFWDefltAssistX_HwNm_u8p8[3]	307
t_AsstFWDefltAssistX_HwNm_u8p8[4]	333
t_AsstFWDefltAssistX_HwNm_u8p8[5]	358
· · · · · · · · · · · · · · · · · · ·	384
t_AsstFWDefltAssistX_HwNm_u8p8[6]	
t_AsstFWDefltAssistX_HwNm_u8p8[7]	410
t_AsstFWDefltAssistX_HwNm_u8p8[8]	435
t_AsstFWDefltAssistX_HwNm_u8p8[9]	461
t_AsstFWDefltAssistX_HwNm_u8p8[10]	486
t_AsstFWDefltAssistX_HwNm_u8p8[11]	512
t_AsstFWDefltAssistX_HwNm_u8p8[12]	538
t_AsstFWDefltAssistX_HwNm_u8p8[13]	563
t_AsstFWDefltAssistX_HwNm_u8p8[14]	589
t AsstFWDefitAssistX HwNm u8p8[15]	614
t_AsstFWDefltAssistX_HwNm_u8p8[16]	640
t_AsstFWDefltAssistX_HwNm_u8p8[17]	666
t_AsstFWDefltAssistX_HwNm_u8p8[18]	691
t_AsstFWDefltAssistX_HwNm_u8p8[19]	717
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	19866
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t_AsstFWDefltAssistY_MtrNm_s4p11[4]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	21299
t AsstFWDefltAssistY MtrNm s4p11[11]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	22733
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	22938
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	23142
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t_AsstFWPstepNstepThresh_Cnt_u16[0]	5000
t_AsstFWPstepNstepThresh_Cnt_u16[1]	5000
t_AsstFWVehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1]	30976
t_AsstFWVehSpd_Kph_u9p7[2]	31104
t_AsstFWVehSpd_Kph_u9p7[3]	31232
t_AsstFWVehSpd_Kph_u9p7[4]	31360
t_AsstFWVehSpd_Kph_u9p7[5]	31488
t_Asstrwvenspu_kpn_uspr[5] t_AsstFWVehSpd_kph_uspr[6]	
_	31616
t_AsstFWVehSpd_Kph_u9p7[7]	31744
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.6500001
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	99.3000031
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
•	tot AssistEirawall Bort CombinedAssist MtrNm f22
•	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_It	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
togt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_It tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_It tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.61999989	2.61999989 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	2558	2558 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.29799938	3.2980001 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.10500002	4.10500002 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0	0 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.12699986	3.12700009 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.29799938	3.2980001 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	✓

Τ					
Actual Function	Count	Expected Function	Count	Result	
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~	
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•	
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~	
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~	
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~	

Test Step 2.86 (Repeat Count = 1) ✓		
Name	Input Value	
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002	
AssistFirewall ActiveKSV M str.K Uls f32	0.20000003	
AssistFirewall ActiveRawAcc Cnt M u16	2234	
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	
AssistFirewall_CombAsstSV_MtrNm_M_f32	6.4000001	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.0999999	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.059999987	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.8999998	
AssistFirewall LwrBoundKSV M str.SV Uls f32	7	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.60000024	
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.099999	
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.140000001	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.30000019	
k_AsstFWInpLimitHFA_MtrNm_f32	1.8999998	
k_AsstFWInpLimitHysComp_MtrNm_f32	4.69999981	
k_AsstFWNstep_Cnt_u16	2440	
k_AsstFWPstep_Cnt_u16	2337	
k_RestoreThresh_MtrNm_f32	3.31999993	
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-18432	



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
12_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	20480
	22528



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	28672	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144	
	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]		
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0	
	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-28672	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	18432	
t2 AsstFWUprBoundY MtrNm s4p11[5][8]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096	
	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2040	



Description		
2 ASSINIVAÇIRASIONY Mintron_spiritYIIS         009           2 ASSINIVAÇIRASIONE, Mintron_spiritYIIS         009           2 ASSINIVAÇIRASIONE, Mintron_spiritYIIS         0144           2 ASSINIVAÇIRASIONE, Mintron_spiritYIIS         0120           2 ASSINIVAÇIRASIONE, Mintron_spiritYIIS         020           2 ASSINIVAÇIRASIONE, Mintron_spiritYIIS         020           2 ASSINIVAÇIRASIONE, Mintron_spiritYIIS         020           2 ASSINIVAÇIRASIONE, Mintron_spiritYIIS         020           2 ASSINIVAÇIRASIONE, Mintron_spiritYII         021           2 ASSINIVAÇIRASIONE, Mintron_spiritYII         021           2 ASSINIVAÇIRASIONE, Mintron_spiritYII         021 <t< th=""><th>Name</th><th>Input Value</th></t<>	Name	Input Value
	t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	
P. ASSENT/PURPORATOR   AMPINE, 1911 17 18    1912    10.200   10	t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
12.Acet   1.00	t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
20 AOSEMUNDATION Milms Last PITITIO         10248           AL ASSEM Vibritation Milms Last PITITIO         268           AL ASSEM Vibritation Milms Last PITITIO         262           AL ASSEM Vibritation Milms Last PITITION         307           AL ASSEM Vibritation Milms Last Pitition         303           AL ASSEM Vibritation Milms Last Pitition         304           AL ASSEM Vibritation Milms Last Pitition         404           AL ASSEM Vibritation Milms Last Pitition         405           AL ASSEM Vibritation Milms Last Pitition         405           AL ASSEM Vibritation Milms Last Pitition         406           AL ASSEM Vibritation Milms Last Pitition         406           AL ASSEM Vibritation Milms Last Pitition         502           AL ASSEM Vibritation Milms Last Pitition         503           AL ASSEM Vibritation Milms Last Pitition         504	t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
	t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
Death   Deat	t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
	t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
Laser World-Assett, Harbon, 1990 2    333   Laser World-Assett, Harbon, 1990 2    358   Laser World-Assett, Harbon, 1990 2    358   Laser World-Assett, Harbon, 1990 2    410   425   Laser World-Assett, Harbon, 1990 2    410   425   Laser World-Assett, Harbon, 1990 2    461   461   462   463   464	t_AsstFWDefltAssistX_HwNm_u8p8[0]	256
Asset World-Asset   Hohm . spingled   388	t_AsstFWDefltAssistX_HwNm_u8p8[1]	282
Acet Publishasian   Nahmu ugiqqi   38	t_AsstFWDefltAssistX_HwNm_u8p8[2]	307
DASSITY/PORTHASHISKY_HANN_up080 5    ASSITY/PORTHASHISKY_HANN_up080 7    ASSITY/PORTHASHISKY_HANN_up		
LastFVDelhAssist, Newhou, 1998		
LassTW0PdResid.NewNru.gog9		
Lasel PWolfMasel Linkhon, upgel 10		
LastRVPM/Intackin/Lwhom_uspill		
LasePNDPINAcidatix NebMm ubg8111   588   LasePNDPINAcidatix NebMm ubg8112   583   LasePNDPINAcidatix NebMm ubg8113   589   LasePNDPINAcidatix NebMm ubg8113   589   1. AsePNDPINAcidatix NebMm ubg8113   680   1. AsePNDPINAcidatix NebMm ubg8114   684		
LassFWDeRTAcsist NewFun (1981)   558     LassFWDeRTAcsist NewFun (1981)   569     LassFWDeRTAcsist NewFun (1981)   569     LassFWDeRTAcsist NewFun (1981)   569     LassFWDeRTAcsist NewFun (1981)   569     LassFWDeRTAcsist NewFun (1981)   560     LassFWDeRTAcsist NewFun (1981)   717   566     LassFWDeRTAcsist NewFun (1981)   717   567     LassFWDeRTAcsist NewFun (1981)   717   717     LassFWDeRTAcsist NewFun (1981)   717   717   717     LassFWDeRTAcsist NewFun (1981)   717		
Laser NPORTAGENET, Merkin		
LeastFWDeffAcasitX HoNem_u808119  589   LeastFWDeffAcasitX HoNem_u808119  580   LeastFWDeffAcasitX HoNem_u808119  580   LeastFWDeffAcasitX HoNem_u808119  717   LeastFWDeffAcasitX HoNem_u808119  717   LeastFWDeffAcasitX HoNem_u808119  717   LeastFWDeffAcasitX HoNem_u808119  718   LeastFWDeffAcasitX HoNem_u808119  718   LeastFWDeffAcasitX HoNem_u808119  719   LeastFWDeffAcasitX HoNem_u808119  719   LeastFWDeffAcasitX HoNem_u808119  719   LeastFWDeffAcasitX HoNem_u808119  719   LeastFWDeffAcasitX HoNem_u809119  719   LeastFWDeffAcasitX MoNem_u809119  719   Leas		
LassFWDeffAcsisk Hehm_u6q8150   640		
LassFWDeftAcsistX, HeNm_usQq119   666	· · ·	
LassFWDeltAssistX, Hehm. usp8[17]		
LaseFWDethAssistX_Helm_usp8[17]	· · ·	
LassFWDeftAssistY_MnNm_sdp110  1945    LassFWDeftAssistY_MnNm_sdp110  1945    LassFWDeftAssistY_MnNm_sdp110  1966    LassFWDeftAssistY_MnNm_sdp110  20070    LassFWDeftAssistY_MnNm_sdp110  20075    LassFWDeftAssistY_MnNm_sdp110  20070    LassFWDeftAssistY_MnNm_sdp110  20070    LassFWDeftAssistY_MnNm_sdp110  20080    LassFWDeftAssistY_MnNm_sdp110  20080    LassFWDeftAssistY_MnNm_sdp110  20080    LassFWDeftAssistY_MnNm_sdp110  21090    LassFWDeftAssistY_MnNm_sdp110  22090    LassFWDeftAssistY_MnNm_sdp110  23090    LassFWDeftAssistFwdaftAssFWDeftAssist_MnNm_sdp110  23090    LassFWDeftAssistFwdaftAssis		
LassEV/DelfAssistX_MinNm_sdp11[0]   19456		
LassFWDetRAssierY_Minns_sep11(0)   19456		
LassFWDelfAssistY_MthMm_sdp11[1]   19861   AssFWDelfAssistY_MthMm_sdp11[3]   20070   LassFWDelfAssistY_MthMm_sdp11[4]   20275   LassFWDelfAssistY_MthMm_sdp11[5]   20480   LassFWDelfAssistY_MthMm_sdp11[6]   20685   LassFWDelfAssistY_MthMm_sdp11[7]   20890   LassFWDelfAssistY_MthMm_sdp11[8]   21994   LassFWDelfAssistY_MthMm_sdp11[8]   21994   LassFWDelfAssistY_MthMm_sdp11[8]   21994   LassFWDelfAssistY_MthMm_sdp11[9]   21994   LassFWDelfAssistY_MthMm_sdp11[10]   21709   LassFWDelfAssistY_MthMm_sdp11[11]   21709   LassFWDelfAssistY_MthMm_sdp11[12]   21914   LassFWDelfAssistY_MthMm_sdp11[13]   2218   LassFWDelfAssistY_MthMm_sdp11[14]   22333   LassFWDelfAssistY_MthMm_sdp11[15]   22528   LassFWDelfAssistY_MthMm_sdp11[16]   22733   LassFWDelfAssistY_MthMm_sdp11[16]   22733   LassFWDelfAssistY_MthMm_sdp11[16]   22733   LassFWDelfAssistY_MthMm_sdp11[16]   22733   LassFWDelfAssistY_MthMm_sdp11[16]   22734   LassFWDelfAssistY_MthMm_sdp11[16]   23347   LassFWDelfAssistY_MthMm_sdp11[16]   23347   LassFWDelfAssistY_MthMm_sdp11[16]   23442   LassFWDelfAssistY_MthMm_sdp11[16]   23442   LassFWDelfAssistY_MthMm_sdp11[16]   23442   LassFWDelfAssistY_MthMm_sdp11[16]   23442   LassFWDelfAssistY_MthMm_sdp11[16]   244444   LassFWDelfAssistY_MthMm_sdp11[16]   2444444   LassFWDelfAs		
L ASSIFWOEITAASSIRY Minthm_sep11[3] 20070  L ASSIFWOEITAASSIRY Minthm_sep11[6] 20080  L ASSIFWOEITAASSIRY Minthm_sep11[6] 20080  L ASSIFWOEITAASSIRY Minthm_sep11[6] 20080  L ASSIFWOEITAASSIRY Minthm_sep11[7] 20090  L ASSIFWOEITAASSIRY Minthm_sep11[7] 20090  L ASSIFWOEITAASSIRY Minthm_sep11[8] 21094  L ASSIFWOEITAASSIRY Minthm_sep11[8] 21299  L ASSIFWOEITAASSIRY Minthm_sep11[8] 21299  L ASSIFWOEITAASSIRY Minthm_sep11[8] 21290  L ASSIFWOEITAASSIRY Minthm_sep11[8] 21200  L ASSIFWOEITAASSIRY Minthm_sep11[8] 21200  L ASSIFWOEITAASSIRY Minthm_sep11[8] 21218  L ASSIFWOEITAASSIRY Minthm_sep11[8] 21218  L ASSIFWOEITAASSIRY Minthm_sep11[8] 22233  L ASSIFWOEITAASSIRY Minthm_sep11[8] 22233  L ASSIFWOEITAASSIRY Minthm_sep11[8] 22233  L ASSIFWOEITAASSIRY Minthm_sep11[8] 22233  L ASSIFWOEITAASSIRY Minthm_sep11[8] 22342  L ASSIFWOEITAASSIRY Minthm_sep11[8] 22342  L ASSIFWOEITAASSIRY Minthm_sep11[8] 22342  L ASSIFWOEITAASSIRY Minthm_sep11[8] 22342  L ASSIFWOEITAASSIRY Minthm_sep11[8] 23347  L ASSIFWOEITAASSIRY Minthm_sep11[8] 23348  L ASSIFWOEITAASSIRY Minthm_sep11[8] 233488  L ASSIFWOEITAASSIRY Minthm_sep11[8] 233488  L ASSIFWOEITAASSIRY Min		
LassEWDelfAssistY, Mirkm., s4p11[4]         20070           LassEWDelfAssistY, Mirkm., s4p11[6]         20080           LassEWDelfAssistY, Mirkm., s4p11[6]         20085           LassEWDelfAssistY, Mirkm., s4p11[6]         20085           LassEWDelfAssistY, Mirkm., s4p11[8]         21094           LassEWDelfAssistY, Mirkm., s4p11[9]         21289           LassEWDelfAssistY, Mirkm., s4p11[10]         21504           LassEWDelfAssistY, Mirkm., s4p11[10]         21944           LassEWDelfAssistY, Mirkm., s4p11[13]         2118           LassEWDelfAssistY, Mirkm., s4p11[13]         2218           LassEWDelfAssistY, Mirkm., s4p11[16]         22323           LassEWDelfAssistY, Mirkm., s4p11[16]         22333           LassEWDelfAssistY, Mirkm., s4p11[16]         22333           LassEWDelfAssistY, Mirkm., s4p11[16]         22333           LassEWDelfAssistY, Mirkm., s4p11[16]         23342           LassEWDelfAssistY, Mirkm., s4p11[16]         23342           LassEWDelfAssistY, Mirkm., s4p11[16]         23342           LassEWDelfAssistY, Mirkm., s4p11[16]         23442           LassEWDelfAssistY, Mirkm., s4p11[16]         23442           LassEWDelfAssistY, Mirkm., s4p11[16]         3347           LassEWDelfAssistY, Mirkm., s4p11[16]         3442           LassEWDelfAssistY		19866
LASSIFWDeftNasiStY_MtrNm_s4p116    20685     LASSIFWDeftNasiStY_MtrNm_s4p117    20890     LASSIFWDeftNasiStY_MtrNm_s4p118    21094     LASSIFWDeftNasiStY_MtrNm_s4p118    21099     LASSIFWDeftNasiStY_MtrNm_s4p119    21594     LASSIFWDeftNasiStY_MtrNm_s4p119    21594     LASSIFWDeftNasiStY_Mtrnm_s4p1110    21504     LASSIFWDeftNasiStY_Mtrnm_s4p1110    21709     LASSIFWDeftNasiStY_Mtrnm_s4p1113    2118     LASSIFWDeftNasiStY_Mtrnm_s4p1113    2218     LASSIFWDeftNasiStY_Mtrnm_s4p1116    2233     LASSIFWDeftNasiStY_Mtrnm_s4p1116    2233     LASSIFWDeftNasiStY_Mtrnm_s4p1116    2233     LASSIFWDeftNasiStY_Mtrnm_s4p1116    2233     LASSIFWDeftNasiStY_Mtrnm_s4p1116    2233     LASSIFWDeftNasiStY_Mtrnm_s4p1116    2334     LASSIFWDeftNasiStY_Mtrnm_s4p1116    2344     LASSIFWDeftNasiStY_Mtrnm_s4p116    2344     LASSIFWDeftNasiStY_Mtrnm_s4p116    2344     LASSIFWDeftNasiStY_Mtrnm_s4p116    2344     LASSIFWDeftNasiStY_Mtrnm_s4p116    2344     LASSIFWDeftNasiStY_Mtrnm_s4p116    2344     LASSIFWDeftNasiStY_Mtrnm_s4p116    2344     LASSIFWDeftNasiStY_Mtrn		20070
LastFWDeftAssitY_MtrNm_s4p116    20880     LastFWDeftAssitY_MtrNm_s4p118    21094     LastFWDeftAssitY_MtrNm_s4p118    21094     LastFWDeftAssitY_MtrNm_s4p118    21295     LastFWDeftAssitY_MtrNm_s4p118    21504     LastFWDeftAssitY_MtrNm_s4p118    21799     LastFWDeftAssitY_MtrNm_s4p118    21798     LastFWDeftAssitY_MtrNm_s4p118    21798     LastFWDeftAssitY_MtrNm_s4p118    2218     LastFWDeftAssitY_MtrNm_s4p118    2223     LastFWDeftAssitY_MtrNm_s4p118    2233     LastFWDeftAssitY_MtrNm_s4p118    2233     LastFWDeftAssitY_MtrNm_s4p118    2233     LastFWDeftAssitY_MtrNm_s4p118    2233     LastFWDeftAssitY_MtrNm_s4p118    2233     LastFWDeftAssitY_MtrNm_s4p118    2342     LastFWDeftAssitY_MtrNm_s4p118    2344     LastFWDeftAssitY_MtrNm_s4p118    2347     LastFWDeftAssitY_MtrNm_s4p118    2347     LastFWDeftAssitY_MtrNm_s4p118    2348     LastFWDeftAssitY_MtrNm_s4p118    2349     LastFWDeftAssitY_MtrNm_s4p118    3392     LastFWDeftAssitY_MtrNm_s4p118    3392     LastFWDeftAssitY_MtrNm_s4p118    3494     LastFWDeftAssitY_MtrNm_s4p18    3494     LastFWDeftAssitY_MtrNm_s4p18    3494     LastFWDeftAssitY_MtrNm	t_AsstFWDefltAssistY_MtrNm_s4p11[4]	20275
LASSIFWDettNassistY_Minms_stp118  2199   LASSIFWDettNassistY_Minms_stp119  2199   LASSIFWDettNassistY_Minms_stp119  2199   LASSIFWDettNassistY_Minms_stp1119  21709   LASSIFWDettNassistY_Minms_stp1119  21709   LASSIFWDettNassistY_Minms_stp1119  21709   LASSIFWDettNassistY_Minms_stp11119  21914   LASSIFWDettNassistY_Minms_stp11119  22933   LASSIFWDettNassistY_Minms_stp11119  22933   LASSIFWDettNassistY_Minms_stp11119  22933   LASSIFWDettNassistY_Minms_stp11119  22938   LASSIFWDettNassistY_Minms_stp11119  22938   LASSIFWDettNassistY_Minms_stp11119  22938   LASSIFWDettNassistY_Minms_stp1119  23937   LASSIFWDettNassistY_Minms_stp1119  33920   LASSIFWDettNassistTp180, Dupp70  33920   LASSIFWDettNassistTp180, Dupp70  34048   LASSIFWDettNassistTp180, Dupp70  34048   LASSIFWDettNassistTp180, Dupp70  34048   LASSIFWDettNassistTp180, Dupp70  34049   LASSIFWDettNassistTp180	t_AsstFWDefltAssistY_MtrNm_s4p11[5]	20480
LASSIFWOEINASSISY_MINN_s4p11[9]   2199	t_AsstFWDefltAssistY_MtrNm_s4p11[6]	20685
LASSIFWDeftRASSISY_Minkm_s4p11[10]   21504     LASSIFWDeftRASSISY_Minkm_s4p11[11]   21709     LASSIFWDeftRASSISY_Minkm_s4p11[12]   21914     LASSIFWDeftRASSISY_Minkm_s4p11[13]   22118     LASSIFWDeftRASSISY_Minkm_s4p11[13]   22233     LASSIFWDeftRASSISY_Minkm_s4p11[14]   22323     LASSIFWDeftRASSISY_Minkm_s4p11[16]   22528     LASSIFWDeftRASSISY_Minkm_s4p11[17]   22338     LASSIFWDeftRASSISY_Minkm_s4p11[17]   22338     LASSIFWDeftRASSISY_Minkm_s4p11[17]   22338     LASSIFWDeftRASSISY_Minkm_s4p11[17]   22338     LASSIFWDeftRASSISY_Minkm_s4p11[18]   23142     LASSIFWDeftRASSISY_Minkm_s4p11[19]   23347     LASSIFWDeftRASSISY_Minkm_s4p11[19]   23442     LASSIFWDeftRASSISY_Minkm_s4p11[19]   23442     LASSIFWDeftRASSISY_Minkm_s4p11[19]   23442     LASSIFWDeftRASSISY_Minkm_s4p11[19]   33792     LASSIFWDeftRASSISY_Minkm_s4p11[19]   33792     LASSIFWDeftRASSISY_Minkm_s4p11[19]   33792     LASSIFWDeftRASSISY_Minkm_s4p11[19]   34468     LASSIFWDeftRASSISY_Minkm_s4p11[19]   34468     LASSIFWDeftRASSIST_Minkm_s4p11[19]   34560     LASSIFWDeftRASSIST_Mink	t_AsstFWDefltAssistY_MtrNm_s4p11[7]	20890
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tgt_Rte_Inst_Ap_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lett_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lett_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_AsstFirewall_Per1_AsstFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lett_tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lett_tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_Rte_Inst_Ap_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgt tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	110.099998
tgt_Rte_Inst_Ap_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igc tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32	$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32$	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum	$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_legendering the property of th$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
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tgt_kte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32 tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.879999995	0.879999995 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	547	547 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.87799978	4.87799978 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-0.200000286	-0.200000003 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.20599985	4.20599985 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.879999995	0.879999995 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Τ				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.87 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.099999
AssistFirewall ActiveKSV M str.K Uls f32	0.30000012
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4554
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	6.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0700000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.150000006
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.4000001
k AsstFWInpLimitHFA MtrNm f32	2.05999994
k_AsstFWInpLimitHysComp_MtrNm_f32	4.9000001
k_AsstFWNstep_Cnt_u16	2316
k_AsstFWPstep_Cnt_u16	0
k RestoreThresh MtrNm f32	3.32999992
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2 AsstFWUprBoundX HwNm s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2 AsstFWUprBoundX HwNm s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384
== :::::::::::::::::::::::::::::::::::	1.550.



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3] t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	2048
t2_Asst WoprBoundX_HwNm_s4p11[3][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240 12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][9] t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2 AsstFWUprBoundX HwNm s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	4.4000
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-12288 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-12288 -10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-12288 -10240



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-14336
t2_AsstrWUprBoundY_MtrNm_s4p11[1][9]	-12288
	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
t2_Asst WopiBoundY_MtrNm_s4p11[6][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	0



Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
	10240
2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
:_AsstFWDefltAssistX_HwNm_u8p8[0]	282
:_AsstFWDefltAssistX_HwNm_u8p8[1]	307
:_AsstFWDefltAssistX_HwNm_u8p8[2]	333
:_AsstFWDefltAssistX_HwNm_u8p8[3]	358
:_AsstFWDefltAssistX_HwNm_u8p8[4]	384
:_AsstFWDefltAssistX_HwNm_u8p8[5]	410
:_AsstFWDefltAssistX_HwNm_u8p8[6]	435
:_AsstFWDefltAssistX_HwNm_u8p8[7]	461
:_AsstFWDefltAssistX_HwNm_u8p8[8]	486
:_AsstFWDefltAssistX_HwNm_u8p8[9]	512
:_AsstFWDefltAssistX_HwNm_u8p8[10]	538
:_AsstFWDefltAssistX_HwNm_u8p8[11]	563
:_AsstFWDefltAssistX_HwNm_u8p8[12]	589
:_AsstFWDefltAssistX_HwNm_u8p8[13]	614
:_AsstFWDefltAssistX_HwNm_u8p8[14]	640
:_AsstFWDefltAssistX_HwNm_u8p8[15]	666
: AsstFWDefltAssistX HwNm u8p8[16]	691
:_AsstFWDefltAssistX_HwNm_u8p8[17]	717
:_AsstFWDefltAssistX_HwNm_u8p8[18]	742
:_AsstFWDefitAssistX_HwNm_u8p8[19]	768
:_AsstFWDefitAssistY_MtrNm_s4p11[0]	19661
:_AsstFWDefitAssistY_MtrNm_s4p11[1]	19866
1 11	
:_AsstFWDefltAssistY_MtrNm_s4p11[2]	20070
:_AsstFWDefltAssistY_MtrNm_s4p11[3]	20275
:_AsstFWDefltAssistY_MtrNm_s4p11[4]	20480
:_AsstFWDefltAssistY_MtrNm_s4p11[5]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	20890
:_AsstFWDefltAssistY_MtrNm_s4p11[7]	21094
:_AsstFWDefltAssistY_MtrNm_s4p11[8]	21299
:_AsstFWDefltAssistY_MtrNm_s4p11[9]	21504
:_AsstFWDefltAssistY_MtrNm_s4p11[10]	21709
:_AsstFWDefltAssistY_MtrNm_s4p11[11]	21914
:_AsstFWDefltAssistY_MtrNm_s4p11[12]	22118
:_AsstFWDefltAssistY_MtrNm_s4p11[13]	22323
:_AsstFWDefltAssistY_MtrNm_s4p11[14]	22528
:_AsstFWDefltAssistY_MtrNm_s4p11[15]	22733
:_AsstFWDefltAssistY_MtrNm_s4p11[16]	22938
:_AsstFWDefltAssistY_MtrNm_s4p11[17]	23142
:_AsstFWDefltAssistY_MtrNm_s4p11[18]	23347
:_AsstFWDefltAssistY_MtrNm_s4p11[19]	23552
:_AsstFWPstepNstepThresh_Cnt_u16[0]	208
:_AsstFWPstepNstepThresh_Cnt_u16[1]	551
:_AsstFWVehSpd_Kph_u9p7[0]	36736
:_AsstFWVehSpd_Kph_u9p7[1]	36864
_AsstFWVehSpd_Kph_u9p7[1] :_AsstFWVehSpd_Kph_u9p7[2]	36992
_AsstFWVehSpd_Kph_u9p7[2] :_AsstFWVehSpd_Kph_u9p7[3]	37120
_AsstFWVehSpd_kph_u9p7[3] : AsstFWVehSpd_kph_u9p7[4]	
_ , _ , _ ,	37248
:_AsstFWVehSpd_Kph_u9p7[5]	37376
:_AsstFWVehSpd_Kph_u9p7[6]	37504
:_AsstFWVehSpd_Kph_u9p7[7]	37632
gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.90999985
gt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
gt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
gt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-6
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	121.199997
	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
· · · · · · · · · · · · · · · · · · ·	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.16999984	2.17000008 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	551	551 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.77799988	5.77799988 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.19999981	6.19999981 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.3349998	3.33500004 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.88 (Repeat Count = 1)	v v v v v v v v v v v v v v v v v v v
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.79999995
AssistFirewall ActiveKSV M str.K Uls f32	0.0599999987
AssistFirewall ActiveRawAcc Cnt M u16	3322
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	6.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.159999996
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.79999995
k_AsstFWInpLimitHFA_MtrNm_f32	2.29999995
k_AsstFWInpLimitHysComp_MtrNm_f32	5.0999999
k_AsstFWNstep_Cnt_u16	2192
k_AsstFWPstep_Cnt_u16	5000
k_RestoreThresh_MtrNm_f32	3.33999991
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336
	·



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_Asst WopiBoundX_HwNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0
	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3] t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstrWUprBoundX_HwNm_s4p11[7][4]	2048
12_Asst WopiBoundX_HwNm_s4p11[7][4]	4096
:2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-2048



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-28672	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-30720	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-28672	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-22528	
2 AsstFWUprBoundY MtrNm s4p11[2][5]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192	
	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192	
	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]		
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-14336	
t2 AsstFWUprBoundY MtrNm s4p11[4][6]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	26624	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	28672	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096	
= -1 -1	L 111	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	307
t_AsstFWDefltAssistX_HwNm_u8p8[1]	333
t_AsstFWDefltAssistX_HwNm_u8p8[2]	358
t_AsstFWDefltAssistX_HwNm_u8p8[3]	384
t_AsstFWDefltAssistX_HwNm_u8p8[4]	410
t_AsstFWDefltAssistX_HwNm_u8p8[5]	435
t_AsstFWDefltAssistX_HwNm_u8p8[6]	461
t_AsstFWDefltAssistX_HwNm_u8p8[7]	486
t_AsstFWDefitAssistX_HwNm_u8p8[8]	512
	538
t_AsstFWDefltAssistX_HwNm_u8p8[9]	
t_AsstFWDefltAssistX_HwNm_u8p8[10]	563
t_AsstFWDefltAssistX_HwNm_u8p8[11]	589
t_AsstFWDefltAssistX_HwNm_u8p8[12]	614
t_AsstFWDefltAssistX_HwNm_u8p8[13]	640
t_AsstFWDefltAssistX_HwNm_u8p8[14]	666
t_AsstFWDefltAssistX_HwNm_u8p8[15]	691
t_AsstFWDefltAssistX_HwNm_u8p8[16]	717
t_AsstFWDefltAssistX_HwNm_u8p8[17]	742
t_AsstFWDefitAssistX_HwNm_u8p8[18]	768
t_AsstFWDefitAssistX_HwNm_u8p8[19]	794
, , , , , , , , , , , , , , , , , , ,	
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	21709
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	22733
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22938
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	23142
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	23347
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	23552
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	23757
t_AsstFWPstepNstepThresh_Cnt_u16[0]	209
t_AsstrWPstepNstepThresh_Cnt_u16[1]	555
t_AsstFWVehSpd_Kph_u9p7[0]	39680
t_AsstFWVehSpd_Kph_u9p7[1]	39808
t_AsstFWVehSpd_Kph_u9p7[2]	39936
t_AsstFWVehSpd_Kph_u9p7[3]	40064
t_AsstFWVehSpd_Kph_u9p7[4]	40192
t_AsstFWVehSpd_Kph_u9p7[5]	40320
t_AsstFWVehSpd_Kph_u9p7[6]	40448
t_AsstFWVehSpd_Kph_u9p7[7]	40576
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.03999996
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2.0999999
·	2.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	132.300003
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_k	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.63199997	2.63199997 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	555	555 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.55200005	1.55200005 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.5	6.5 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.28399992	4.28399992 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.89 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall ActiveKSV M str.K Uls f32	0.019999996
AssistFirewall_ActiveRawAcc_Cnt_M_u16	222
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	6.6999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.029999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	2
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.60000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.170000002
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.9000001
k_AsstFWInpLimitHFA_MtrNm_f32	3.2999995
k_AsstFWInpLimitHysComp_MtrNm_f32	5.30000019
k_AsstFWNstep_Cnt_u16	2000
k AsstFWPstep Cnt u16	2500
k RestoreThresh MtrNm f32	3.3499999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2 AsstFWUprBoundX HwNm s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240
	-10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096
40 ApptEMUlarDoundV Muhler - 4: 44503553	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-2048 0



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144 4000
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2046 0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4] t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144 4006
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144
a	Vr



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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	333
t_AsstFWDefltAssistX_HwNm_u8p8[1]	358
t_AsstFWDefltAssistX_HwNm_u8p8[2]	384
t_AsstFWDefltAssistX_HwNm_u8p8[3]	410
t_AsstFWDefltAssistX_HwNm_u8p8[4]	435
t_AsstFWDefltAssistX_HwNm_u8p8[5]	461
t_AsstFWDefltAssistX_HwNm_u8p8[6]	486
t_AsstFWDefltAssistX_HwNm_u8p8[7]	512
t_AsstFWDefltAssistX_HwNm_u8p8[8]	538
t_AsstFWDefltAssistX_HwNm_u8p8[9]	563
t_AsstFWDefltAssistX_HwNm_u8p8[10]	589
t_AsstFWDefltAssistX_HwNm_u8p8[11]	614
t_AsstFWDefltAssistX_HwNm_u8p8[12]	640
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	666 691
t_AsstFWDefitAssistX_HwNm_u8p8[14] t_AsstFWDefitAssistX_HwNm_u8p8[15]	717
t_AsstFWDefitAssistX_HwNm_u8p8[16]	742
t_AsstFWDefitAssistX_HwNm_u8p8[17]	768
t_AsstFWDefltAssistX_HwNm_u8p8[18]	794
t_AsstFWDefltAssistX_HwNm_u8p8[19]	819
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	22733
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	22938
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	23142
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	23347
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	23552
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	23757
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	23962
t_AsstFWPstepNstepThresh_Cnt_u16[0]	210
t_AsstFWPstepNstepThresh_Cnt_u16[1]	559 42624
t_AsstFWVehSpd_Kph_u9p7[0]	
t_AsstFWVehSpd_Kph_u9p7[1]	42752 42880
t_AsstFWVehSpd_Kph_u9p7[2] t_AsstFWVehSpd_Kph_u9p7[3]	43008
t_AsstFWVehSpd_kph_u9p7[4]	43136
t_AsstFWVehSpd_Kph_u9p7[5]	43264
t_AsstFWVehSpd_Kph_u9p7[6]	43392
t_AsstFWVehSpd_Kph_u9p7[7]	43520
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.17000008
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	143.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFi$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.07800007	1.07799995 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	559	559 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.37100005	1.37100005 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.4000001	6.4000001 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.34000003	1.34000003 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T ·				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.90 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.099999
AssistFirewall ActiveKSV M str.K Uls f32	0.10000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	344
AssistFirewall AsstReducedPerfSV Cnt M Iqc	0
AssistFirewall CombAsstSV MtrNm M f32	6.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.090000036
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4
k_AsstFWInpLimitHFA_MtrNm_f32	4.30000019
k_AsstFWInpLimitHysComp_MtrNm_f32	2
k_AsstFWNstep_Cnt_u16	0
k_AsstFWPstep_Cnt_u16	200
k RestoreThresh MtrNm f32	3.3599999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	4096



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192	
	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]		
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-10240	
	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]		
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-26624	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-24576	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-18432	
2 AsstFWUprBoundY MtrNm s4p11[2][5]	-16384	
	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]		
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336	
	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]		
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144	
	8192	
2 AsstEWUprBoundY MtrNm s4n11[6][8]	U10 <u>L</u>	
	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	12288 2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	12288	
12_AsstFWUprBoundY_MtrNm_s4p11[6][8] 12_AsstFWUprBoundY_MtrNm_s4p11[6][9] 12_AsstFWUprBoundY_MtrNm_s4p11[6][10] 12_AsstFWUprBoundY_MtrNm_s4p11[7][0] 12_AsstFWUprBoundY_MtrNm_s4p11[7][1] 12_AsstFWUprBoundY_MtrNm_s4p11[7][2]	12288 2048	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	22528
t_AsstFWDefltAssistX_HwNm_u8p8[0]	358
t_AsstFWDefltAssistX_HwNm_u8p8[1]	384
t_AsstFWDefltAssistX_HwNm_u8p8[2]	410
t_AsstFWDefltAssistX_HwNm_u8p8[3]	435
t_AsstFWDefltAssistX_HwNm_u8p8[4]	461
t_AsstFWDefltAssistX_HwNm_u8p8[5]	486
t_AsstFWDefltAssistX_HwNm_u8p8[6]	512
t_AsstFWDefltAssistX_HwNm_u8p8[7]	538
t_AsstFWDefltAssistX_HwNm_u8p8[8]	563 589
t_AsstFWDefltAssistX_HwNm_u8p8[9] t_AsstFWDefltAssistX_HwNm_u8p8[10]	614
t_AsstFWDefitAssistX_HwNm_u8p8[11]	640
t AsstFWDefitAssistX HwNm u8p8[12]	666
t_AsstFWDefltAssistX_HwNm_u8p8[13]	691
t AsstFWDefitAssistX HwNm u8p8[14]	717
t_AsstFWDefltAssistX_HwNm_u8p8[15]	742
t_AsstFWDefltAssistX_HwNm_u8p8[16]	768
t_AsstFWDefltAssistX_HwNm_u8p8[17]	794
t_AsstFWDefltAssistX_HwNm_u8p8[18]	819
t_AsstFWDefltAssistX_HwNm_u8p8[19]	845
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	22733
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	22938
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	23142
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	23347
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	23552
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	23757
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	23962
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	24166
t_AsstFWPstepNstepThresh_Cnt_u16[0] t_AsstFWPstepNstepThresh_Cnt_u16[1]	211 563
t_AsstFWVehSpd_Kph_u9p7[0]	45568
t_AsstFWVehSpd_Kph_u9p7[1]	45696
t_AsstFWVehSpd_Kph_u9p7[2]	45824
t_AsstFWVehSpd_Kph_u9p7[3]	45952
t AsstFWVehSpd Kph u9p7[4]	46080
t_AsstFWVehSpd_Kph_u9p7[5]	46208
t_AsstFWVehSpd_Kph_u9p7[6]	46336
t_AsstFWVehSpd_Kph_u9p7[7]	46464
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.30000019
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.39999998
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	154.100006
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_left$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.78999996	2.78999996 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	544	544 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.26499987	4.26499987 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5	5 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.08999991	2.08999991 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.91 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	2.7999995
AssistFirewall ActiveKSV M str.K Uls f32	0.20000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	2212
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall CombAsstSV MtrNm M f32	6.9000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0599999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.8999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.100000001
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	5.30000019
k_AsstFWInpLimitHysComp_MtrNm_f32	1
k_AsstFWNstep_Cnt_u16	5000
k_AsstFWPstep_Cnt_u16	44
k_RestoreThresh_MtrNm_f32	3.36999989
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
	-2040
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2 AsstFWUprBoundX HwNm s4p11[6][3]	2048
	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
· · · · ·	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	4096



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0] t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	10240



	(14.11.10.10
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
t2_Asst WopiBoundY_MtrNm_s4p11[7][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576
t_AsstFWDefltAssistX_HwNm_u8p8[0]	384
t_AsstFWDefltAssistX_HwNm_u8p8[1]	410
t_AsstFWDefltAssistX_HwNm_u8p8[2]	435
t_AsstFWDefltAssistX_HwNm_u8p8[3]	461
t_AsstFWDefltAssistX_HwNm_u8p8[4]	486
t AsstFWDefltAssistX HwNm u8p8[5]	512
t_AsstFWDefltAssistX_HwNm_u8p8[6]	538
t_AsstFWDefltAssistX_HwNm_u8p8[7]	563
t_AsstFWDefltAssistX_HwNm_u8p8[8]	589
	614
t_AsstFWDefltAssistX_HwNm_u8p8[9]	
t_AsstFWDefltAssistX_HwNm_u8p8[10]	640
t_AsstFWDefltAssistX_HwNm_u8p8[11]	666
t_AsstFWDefltAssistX_HwNm_u8p8[12]	691
t_AsstFWDefltAssistX_HwNm_u8p8[13]	717
t_AsstFWDefltAssistX_HwNm_u8p8[14]	742
t_AsstFWDefltAssistX_HwNm_u8p8[15]	768
t_AsstFWDefltAssistX_HwNm_u8p8[16]	794
t AsstFWDefltAssistX HwNm u8p8[17]	819
t_AsstFWDefitAssistX_HwNm_u8p8[18]	845
	870
t_AsstFWDefltAssistX_HwNm_u8p8[19]	
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	-184
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	-164
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	-143
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	-123
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	-102
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	-82
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	-61
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	-41
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	-20
	0
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	20
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	41
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	61
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	82
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	102
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	123
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	143
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	164
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	184
t_AsstFWPstepNstepThresh_Cnt_u16[0]	212
t_AsstFWPstepNstepThresh_Cnt_u16[1]	567
t_AsstFWVehSpd_Kph_u9p7[0]	1408
t_AsstFWVehSpd_Kph_u9p7[1]	1536
t_AsstFWVehSpd_Kph_u9p7[2]	1664
t_AsstFWVehSpd_Kph_u9p7[3]	1792
t_AsstFWVehSpd_Kph_u9p7[4]	1920
t_AsstFWVehSpd_Kph_u9p7[5]	2048
t_AsstFWVehSpd_Kph_u9p7[6]	2176
t_AsstFWVehSpd_Kph_u9p7[7]	2304
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.42999983
•	
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.70000005
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	165.300003
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
•	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	
	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
• • •	,
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	,
• • • • • • • • • • • • • • • • • • • •	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.24000001	2.24000001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	567	567 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-0.100097656	-0.100097656 ± 4.88E-04	<b>~</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.20200014	5.20200014 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2	2 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3	3 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-0.100097656	-0.100097656 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>~</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.1000002
AssistFirewall_ActiveKSV_M_str.K_UIs_f32	0.30000012
	334
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall CombAsstSV MtrNm M f32	7
	6.099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	0.0700000003
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.600000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.109999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
<_AsstFWInpLimitBaseAsst_MtrNm_f32	4.19999981
k_AsstFWInpLimitHFA_MtrNm_f32	6.30000019
<_AsstFWInpLimitHysComp_MtrNm_f32	1
<_AsstFWNstep_Cnt_u16	2500
k_AsstFWPstep_Cnt_u16	21
<pre>&lt;_RestoreThresh_MtrNm_f32</pre>	3.38000011
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9] t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	4096 -2048
	-2046
t2_AsstFWUprBoundX_HwNm_s4p11[6][1] t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2 AsstFWUprBoundX HwNm s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
=	
t2 AsstFWUprBoundY MtrNm s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	4096 6144



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288	
t2_Asst WoprBoundY_MtrNm_s4p11[0][10]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-6144	
	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]		
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432	
	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]		
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288	
	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]		
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096	
	1111	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	
t_AsstFWDefltAssistX_HwNm_u8p8[0]	410
t_AsstFWDefltAssistX_HwNm_u8p8[1]	435
t_AsstFWDefltAssistX_HwNm_u8p8[2]	461
t_AsstFWDefltAssistX_HwNm_u8p8[3]	486
t_AsstFWDefltAssistX_HwNm_u8p8[4]	512
t_AsstFWDefltAssistX_HwNm_u8p8[5]	538
t_AsstFWDefltAssistX_HwNm_u8p8[6]	563
t_AsstFWDefltAssistX_HwNm_u8p8[7]	589
t_AsstFWDefltAssistX_HwNm_u8p8[8]	614
t_AsstFWDefltAssistX_HwNm_u8p8[9]	640
t_AsstFWDefltAssistX_HwNm_u8p8[10]	666
t_AsstFWDefltAssistX_HwNm_u8p8[11]	691
t_AsstFWDefltAssistX_HwNm_u8p8[12]	717
t_AsstFWDefltAssistX_HwNm_u8p8[13]	742
t_AsstFWDefltAssistX_HwNm_u8p8[14]	768
t_AsstFWDefltAssistX_HwNm_u8p8[15]	794
t_AsstFWDefltAssistX_HwNm_u8p8[16]	819
t_AsstFWDefltAssistX_HwNm_u8p8[17]	845
t_AsstFWDefltAssistX_HwNm_u8p8[18]	870
t_AsstFWDefltAssistX_HwNm_u8p8[19]	896
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	-143
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	-82
	-20
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	41
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	102
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	164
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	225
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	287
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	348
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	410
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	471
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	532
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	594
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	655
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	717
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	778
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	840
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	901
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	963
t_AsstFWPstepNstepThresh_Cnt_u16[0]	213
t_AsstFWPstepNstepThresh_Cnt_u16[1]	571
t_AsstFWVehSpd_Kph_u9p7[0]	4352
t_AsstFWVehSpd_Kph_u9p7[1]	4480
t_AsstFWVehSpd_Kph_u9p7[2]	4608
t_AsstFWVehSpd_Kph_u9p7[3]	4736
t AsstFWVehSpd Kph u9p7[4]	4864
t_AsstFWVehSpd_Kph_u9p7[5]	4992
t_AsstFWVehSpd_Kph_u9p7[6]	5120
t_AsstFWVehSpd_Kph_u9p7[7]	5248
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.55999994
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2.5999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176.399994
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt	_le_tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
_	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1 HighFreqAssist MtrNm f32	tgt_Assisti ilewaii_Fei1_filgili feqAssist_WithVili_132
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_Assist ilewali_Feli_Filghi FeqAssist_Mithin_l52  tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.07000005	1.07000005 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	355	355 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.81680965	5.81681013 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.21899986	6.21899986 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.79999971	2.79999995 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.21999979	4.21999979 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	5.81680965	5.81681013 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~

Τ				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.93 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.79999995
AssistFirewall ActiveKSV M str.K Uls f32	0.10000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8118
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.129999995
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.5
k_AsstFWInpLimitHFA_MtrNm_f32	8.80000019
k_AsstFWInpLimitHysComp_MtrNm_f32	6.38000011
k_AsstFWNstep_Cnt_u16	2192
k_AsstFWPstep_Cnt_u16	2091
k_RestoreThresh_MtrNm_f32	3.3900001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288
12_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
2 AsstFWUprBoundX HwNm s4p11[6][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
:2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	6144
	8192
	0.194
:2_AsstFWUprBoundY_MtrNm_s4p11[0][5] :2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	10240



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-2048	
	0	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]		
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-12288	
2 AsstFWUprBoundY MtrNm s4p11[2][5]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-8192	
	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]		
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192	
	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-14336	
	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]		
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	2048	
2 AsstFWUprBoundY MtrNm s4p11[4][9]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048	
:2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048	
	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	435
t_AsstFWDefltAssistX_HwNm_u8p8[1]	461
t_AsstFWDefltAssistX_HwNm_u8p8[2]	486
t AsstFWDefltAssistX HwNm u8p8[3]	512
t_AsstFWDefltAssistX_HwNm_u8p8[4]	538
t_AsstFWDefltAssistX_HwNm_u8p8[5]	563
t_AsstFWDefltAssistX_HwNm_u8p8[6]	589
t_AsstFWDefltAssistX_HwNm_u8p8[7]	614
t_AsstFWDefltAssistX_HwNm_u8p8[8]	640
t_AsstFWDefltAssistX_HwNm_u8p8[9]	666
t_AsstFWDefltAssistX_HwNm_u8p8[10]	691
t_AsstFWDefltAssistX_HwNm_u8p8[11]	717
t_AsstFWDefltAssistX_HwNm_u8p8[12]	742
t_AsstFWDefltAssistX_HwNm_u8p8[13]	768
t_AsstFWDefltAssistX_HwNm_u8p8[14]	794
t_AsstFWDefltAssistX_HwNm_u8p8[15]	819
t_AsstFWDefltAssistX_HwNm_u8p8[16]	845
t_AsstFWDefltAssistX_HwNm_u8p8[17]	870
t_AsstFWDefltAssistX_HwNm_u8p8[18]	896
t_AsstFWDefltAssistX_HwNm_u8p8[19]	922
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2458
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2662
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2867
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3277
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	3482
t_AsstFWDefitAssistY_MtrNm_s4p11[6]	3686
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	3891
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4301
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	4506
	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[15] t_AsstFWDefltAssistY_MtrNm_s4p11[16]	5530 5734
t_AsstFWDefltAssistY_MtrNm_s4p11[17] t_AsstFWDefltAssistY_MtrNm_s4p11[18]	5939
	6144
t_AsstFWDefthAssistY_MtrNm_s4p11[19]	6349
t_AsstFWPstepNstepThresh_Cnt_u16[0]	214
t_AsstFWPstepNstepThresh_Cnt_u16[1]	575
t_AsstFWVehSpd_Kph_u9p7[0]	7296
t_AsstFWVehSpd_Kph_u9p7[1]	7424
t_AsstFWVehSpd_Kph_u9p7[2]	7552
t_AsstFWVehSpd_Kph_u9p7[3]	7680
t_AsstFWVehSpd_Kph_u9p7[4]	780 2867



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.51999998	2.51999998 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	575	575 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.10009766	3.10009766 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.26999998	4.26999998 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.5	3.5 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.03999996	2.03999996 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.10009766	3.10009766 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Name	
AssistFirewall_ActiveKSV_M_str.K_Uls_132 0.090000036 AssistFirewall_ActiveRawAcc_Cnt_M_u16 109 AssistFirewall_CombAssisV_MtrNm_M_132 -1.10000002 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_132 2.2000005 AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_132 2.000005 AssistFirewall_HiFreqKSV_M_str.CPF_Str.K_Uls_132 1.89999982 AssistFirewall_HiFreqKSV_M_str.CF_Uls_132 1.8999998 AssistFirewall_LwBoundKSV_M_str.SV_Uls_132 1.8999998 AssistFirewall_LwBoundKSV_M_str.K_Uls_132 1.8999998 AssistFirewall_LyrBoundKSV_M_str.SV_Uls_132 1.0000003 AssistFirewall_UprBoundKSV_M_str.SV_Uls_132 1.10000002 AssistFirewall_UprBoundKSV_M_str.SV_Uls_132 1.10000002 AssistFirewall_UprBoundKSV_M_str.SV_Uls_132 1.10000002 AssistFirewall_UprBoundKSV_M_str.X_Uls_132 1.10000002 AssistFirewall_UprBoundKSV_M_str.X_Uls_132 1.10000002 AssistFirewall_UprBoundKSV_M_str.X_Uls_132 1.10000002 AssistFirewall_UprBoundKSV_M_str.X_Uls_132 1.10000002 AssistFirewall_UprBoundKSV_M_str.X_Uls_132 1.10000002 AssistFirewall_UprBoundKSV_M_str.X_Uls_132 1.100000000000000000000000000000000000	
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	
AssistFirewall_AssitReducedPerfSV_Cnt_M_lgc 1 AssistFirewall_CombAssisV_MtrNm_M_f32 2.20000005 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32 2.20000005 AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32 2.20000005 AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32 0.0799999982 AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32 1.89999998 AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32 5.099999 AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32 0.070000003 AssistFirewall_PDCountStatus_Cnt_M_lgc 1 AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 1.0000002 AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 1.0000002 AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 1.0000002 AssistFirewall_UprBoundKSV_M_str.K_Uls_f32 1.0000002 AssistFirewall_UprBoundKSV_M_str.K_Uls_f32 1.0000002 AssistFirewall_UprBoundKSV_M_str.K_Uls_f32 1.0000002 AssistFirewall_UprBoundKSV_M_str.K_Uls_f32 1.0000002 AssistFirewall_UprBoundKSV_M_str.K_Uls_f32 1.0000002 AssistFirewall_UprBoundK_MtrNm_f32 1.0000000 AssistFirewall_UprBoundK_MtrNm_f32 1.000000000000000000000000000000000000	
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	
AssistFirewall_CombAsstSV_MtrNm_M_f32 -1.10000002 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32 -2.0000005 AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32 -0.0799999982 AssistFirewall_LwrBoundKSV_M_str.CF_Uls_f32 -1.89999998 AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32 -0.070000003 AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32 -0.070000003 AssistFirewall_UprBoundKSV_M_str.K_Uls_f32 -1.10000002 AssistFirewall_UprBoundK_MtrNm_f32 -2.5  K_AsstFWInpLimitHFA_MtrNm_f32 -2.5  K_AsstFWInpLimitHFA_MtrNm_f32 -2.5  K_AsstFWInpLimitHFysComp_MtrNm_f32 -3.78999996  K_AsstFWUprBoundK_HwNm_s4p110[0] -1.2000  AssistFWUprBoundX_HwNm_s4p110[0] -1.2288  12_AsstFWUprBoundX_HwNm_s4p110[1] -1.0240  12_AsstFWUprBoundX_HwNm_s4p110[1] -1.0240  12_AsstFWUprBoundX_HwNm_s4p110[1] -4.0966  12_AsstFWUprBoundX_HwNm_s4p110[1] -4.0966  12_AsstFWUprBoundX_HwNm_s4p110[15] -2.048	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	
AssistFirewall_PNCountStatus_Cnt_M_lgc	
AssistFirewall_PNCountStatus_Cnt_M_lgc	
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 AssistFirewall_UprBoundKSV_M_str.K_Uls_f32 Rte_Inst_Ap_AssistFirewall k_AsstFWInpLimitBaseAsst_MtrNm_f32 k_AsstFWInpLimitHFA_MtrNm_f32 k_AsstFWInpLimitHysComp_MtrNm_f32 k_AsstFWInpLimitHysComp_MtrNm_f32 k_AsstFWInpLimitHysComp_MtrNm_f32 k_AsstFWInpLimitHysComp_MtrNm_f32 k_AsstFWStep_Cnt_u16 k_AsstFWPstep_Cnt_u16 k_RestoreThresh_MtrNm_f32 1.8999998 t2_AsstFWUprBoundX_HwNm_s4p11[0][0] -12288 t2_AsstFWUprBoundX_HwNm_s4p11[0][1] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[0][2] t2_AsstFWUprBoundX_HwNm_s4p11[0][3] t2_AsstFWUprBoundX_HwNm_s4p11[0][4] t2_AsstFWUprBoundX_HwNm_s4p11[0][4] t2_AsstFWUprBoundX_HwNm_s4p11[0][5] -2048	
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	
Rte_Inst_Ap_AssistFirewall       tgt_Rte_Inst_Ap_AssistFirewall         k_AsstFWInpLimitBaseAsst_MtrNm_f32       4         k_AsstFWInpLimitHFA_MtrNm_f32       2.5         k_AsstFWInpLimitHysComp_MtrNm_f32       3.78999996         k_AsstFWNstep_Cnt_u16       3928         k_AsstFWPstep_Cnt_u16       1107         k_RestoreThresh_MtrNm_f32       1.89999998         t2_AsstFWUprBoundX_HwNm_s4p11[0][0]       -12288         t2_AsstFWUprBoundX_HwNm_s4p11[0][1]       -10240         t2_AsstFWUprBoundX_HwNm_s4p11[0][2]       -8192         t2_AsstFWUprBoundX_HwNm_s4p11[0][3]       -6144         t2_AsstFWUprBoundX_HwNm_s4p11[0][4]       -4096         t2_AsstFWUprBoundX_HwNm_s4p11[0][5]       -2048	
k_AsstFWInpLimitHFA_MtrNm_f32       2.5         k_AsstFWInpLimitHysComp_ltrNm_f32       3.78999996         k_AsstFWNstep_Cnt_u16       3928         k_AsstFWPstep_Cnt_u16       1107         k_RestoreThresh_MtrNm_f32       1.89999998         t2_AsstFWUprBoundX_HwNm_s4p11[0][0]       -12288         t2_AsstFWUprBoundX_HwNm_s4p11[0][1]       -10240         t2_AsstFWUprBoundX_HwNm_s4p11[0][2]       -8192         t2_AsstFWUprBoundX_HwNm_s4p11[0][3]       -6144         t2_AsstFWUprBoundX_HwNm_s4p11[0][4]       -4096         t2_AsstFWUprBoundX_HwNm_s4p11[0][5]       -2048	
k_AsstFWInpLimitHFA_MtrNm_f32       2.5         k_AsstFWInpLimitHysComp_MtrNm_f32       3.78999996         k_AsstFWNstep_Cnt_u16       3928         k_AsstFWPstep_Cnt_u16       1107         k_RestoreThresh_MtrNm_f32       1.89999998         t2_AsstFWUprBoundX_HwNm_s4p11[0][0]       -12288         t2_AsstFWUprBoundX_HwNm_s4p11[0][1]       -10240         t2_AsstFWUprBoundX_HwNm_s4p11[0][2]       -8192         t2_AsstFWUprBoundX_HwNm_s4p11[0][3]       -6144         t2_AsstFWUprBoundX_HwNm_s4p11[0][4]       -4096         t2_AsstFWUprBoundX_HwNm_s4p11[0][5]       -2048	
k_AsstFWInpLimitHysComp_MtrNm_f32       3.78999996         k_AsstFWNstep_Cnt_u16       3928         k_AsstFWPstep_Cnt_u16       1107         k_RestoreThresh_MtrNm_f32       1.89999998         t2_AsstFWUprBoundX_HwNm_s4p11[0][0]       -12288         t2_AsstFWUprBoundX_HwNm_s4p11[0][1]       -10240         t2_AsstFWUprBoundX_HwNm_s4p11[0][2]       -8192         t2_AsstFWUprBoundX_HwNm_s4p11[0][3]       -6144         t2_AsstFWUprBoundX_HwNm_s4p11[0][4]       -4096         t2_AsstFWUprBoundX_HwNm_s4p11[0][5]       -2048	
k_AsstFWNstep_Cnt_u16       3928         k_AsstFWPstep_Cnt_u16       1107         k_RestoreThresh_MtrNm_f32       1.89999998         t2_AsstFWUprBoundX_HwNm_s4p11[0][0]       -12288         t2_AsstFWUprBoundX_HwNm_s4p11[0][1]       -10240         t2_AsstFWUprBoundX_HwNm_s4p11[0][2]       -8192         t2_AsstFWUprBoundX_HwNm_s4p11[0][3]       -6144         t2_AsstFWUprBoundX_HwNm_s4p11[0][4]       -4096         t2_AsstFWUprBoundX_HwNm_s4p11[0][5]       -2048	
k_AsstFWPstep_Cnt_u16       1107         k_RestoreThresh_MtrNm_f32       1.89999998         t2_AsstFWUprBoundX_HwNm_s4p11[0][0]       -12288         t2_AsstFWUprBoundX_HwNm_s4p11[0][1]       -10240         t2_AsstFWUprBoundX_HwNm_s4p11[0][2]       -8192         t2_AsstFWUprBoundX_HwNm_s4p11[0][3]       -6144         t2_AsstFWUprBoundX_HwNm_s4p11[0][4]       -4096         t2_AsstFWUprBoundX_HwNm_s4p11[0][5]       -2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][0] -12288 t2_AsstFWUprBoundX_HwNm_s4p11[0][1] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[0][2] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[0][3] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[0][4] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[0][5] -2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][1] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[0][2] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[0][3] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[0][4] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[0][5] -2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][1] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[0][2] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[0][3] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[0][4] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[0][5] -2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][3] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[0][4] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[0][5] -2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][4] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[0][5] -2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][5] -2048	
7 - 7 - 7 - 7 - 7 - 7 - 7 - 7 - 7 - 7 -	
t2_AsstFWUprBoundX_HwNm_s4p11[0][6] 0	
t2_AsstFWUprBoundX_HwNm_s4p11[0][7] 2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][8] 4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][9] 6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][10] 8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][0] -10240	
t2_AsstFWUprBoundX_HwNm_s4p11[1][1] -8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][2] -6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][3] -4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][4] -2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5] 0	
t2_AsstFWUprBoundX_HwNm_s4p11[1][6] 2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7] 4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][8] 6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][9] 8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][10] 10240	
t2_AsstFWUprBoundX_HwNm_s4p11[2][0] -2048	



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	14336



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-16384	
:2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-14336	
	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]		
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	2048	
	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240	
, , , , , , , , , , , , , , , , , , , ,	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]		
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	461
t_AsstFWDefltAssistX_HwNm_u8p8[1]	486
t_AsstFWDefltAssistX_HwNm_u8p8[2]	512
t_AsstFWDefltAssistX_HwNm_u8p8[3]	538
t_AsstFWDefltAssistX_HwNm_u8p8[4]	563
t_AsstFWDefltAssistX_HwNm_u8p8[5]	589
t_AsstFWDefltAssistX_HwNm_u8p8[6]	614
t_AsstFWDefltAssistX_HwNm_u8p8[7]	640
· • • • • • • • • • • • • • • • • • • •	666
t_AsstFWDefltAssistX_HwNm_u8p8[8]	
t_AsstFWDefltAssistX_HwNm_u8p8[9]	691
t_AsstFWDefltAssistX_HwNm_u8p8[10]	717
t_AsstFWDefltAssistX_HwNm_u8p8[11]	742
t_AsstFWDefltAssistX_HwNm_u8p8[12]	768
t_AsstFWDefltAssistX_HwNm_u8p8[13]	794
t_AsstFWDefltAssistX_HwNm_u8p8[14]	819
t_AsstFWDefltAssistX_HwNm_u8p8[15]	845
t_AsstFWDefltAssistX_HwNm_u8p8[16]	870
t AsstFWDefltAssistX HwNm u8p8[17]	896
t_AsstFWDefitAssistX_HwNm_u8p8[18]	922
	947
t_AsstFWDefltAssistX_HwNm_u8p8[19]	
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2662
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2867
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6554
	215
t_AsstFWPstepNstepThresh_Cnt_u16[0]	
t_AsstFWPstepNstepThresh_Cnt_u16[1]	579
t_AsstFWVehSpd_Kph_u9p7[0]	10240
t_AsstFWVehSpd_Kph_u9p7[1]	10368
t_AsstFWVehSpd_Kph_u9p7[2]	10496
t_AsstFWVehSpd_Kph_u9p7[3]	10624
t_AsstFWVehSpd_Kph_u9p7[4]	10752
t_AsstFWVehSpd_Kph_u9p7[5]	10880
t_AsstFWVehSpd_Kph_u9p7[6]	11008
t_AsstFWVehSpd_Kph_u9p7[7]	11136
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	9
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90.1999969
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_	
•	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_t	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
	_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm	_ioz tgi_rosisti irewaii_r ci i_riyateresiseetiip_iviti viii_toz
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enur	



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.82099986	2.8210001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	579	579 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.20019531	3.20019531 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.63199997	2.63199997 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.74300003	4.74300003 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.18900001	1.18900001 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.20019531	3.20019531 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.95 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall ActiveKSV M str.K Uls f32	0.090000036
AssistFirewall_ActiveRawAcc_Cnt_M_u16	109
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.8999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.070000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0099999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4
k_AsstFWInpLimitHFA_MtrNm_f32	2.5
k_AsstFWInpLimitHysComp_MtrNm_f32	3.78999996
k_AsstFWNstep_Cnt_u16	3928
k_AsstFWPstep_Cnt_u16	1107
k_RestoreThresh_MtrNm_f32	1.89999998
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-10240
t2 AsstFWUprBoundX HwNm s4p11[4][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7] t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9] t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
	10240 -16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2] t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	12288
10 A (FIAM) D (V. A.	4.4220
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	14336



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048	
	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]		
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0	
	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]		
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048	
	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]		
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	14336	
. = . : = : 1 : 1 : 1 : 1 : 1		



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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	486
t_AsstFWDefltAssistX_HwNm_u8p8[1]	512
t_AsstFWDefltAssistX_HwNm_u8p8[2]	538
t_AsstFWDefltAssistX_HwNm_u8p8[3]	563
t_AsstFWDefltAssistX_HwNm_u8p8[4]	589
t_AsstFWDefltAssistX_HwNm_u8p8[5]	614
t_AsstFWDefltAssistX_HwNm_u8p8[6]	640
t_AsstFWDefltAssistX_HwNm_u8p8[7]	666
t_AsstFWDefltAssistX_HwNm_u8p8[8]	691
t_AsstFWDefltAssistX_HwNm_u8p8[9]	717
t_AsstFWDefltAssistX_HwNm_u8p8[10]	742
t_AsstFWDefltAssistX_HwNm_u8p8[11]	768 794
t_AsstFWDefltAssistX_HwNm_u8p8[12]	
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	819 845
t_AsstFWDefitAssistX_HwNm_u8p8[14] t_AsstFWDefitAssistX_HwNm_u8p8[15]	845 870
t_AsstFWDefltAssistX_HwNm_u8p8[16]	896
t_AsstFWDefitAssistX_HwNm_u8p8[17]	922
t_AsstFWDefltAssistX_HwNm_u8p8[18]	947
t_AsstFWDefltAssistX_HwNm_u8p8[19]	973
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2867
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6758
t_AsstFWPstepNstepThresh_Cnt_u16[0]	216
t_AsstFWPstepNstepThresh_Cnt_u16[1]	583
t_AsstFWVehSpd_Kph_u9p7[0]	13184
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	13312 13440
t_AsstFWVehSpd_Kph_u9p7[3]	13568
t AsstFWVehSpd Kph u9p7[4]	13696
t_AsstFWVehSpd_Kph_u9p7[5]	13824
t_AsstFWVehSpd_Kph_u9p7[6]	13952
t_AsstFWVehSpd_Kph_u9p7[7]	14080
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	9
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90.3000031
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFi$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.82099986	2.8210001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	583	583 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.29980469	3.29980469 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.63199997	2.63199997 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.67299986	4.67299986 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.199	1.199 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.29980469	3.29980469 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•

Τ			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.96 (Repeat Count = 1)	· ·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.30000019
AssistFirewall ActiveKSV M str.K Uls f32	0.40000006
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.079999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11199999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.119999997
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.219999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.80000019
k_AsstFWInpLimitHFA_MtrNm_f32	6.40999985
k_AsstFWInpLimitHysComp_MtrNm_f32	6.71000004
k_AsstFWNstep_Cnt_u16	4052
k_AsstFWPstep_Cnt_u16	2460
k_RestoreThresh_MtrNm_f32	4.42999983
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192 
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3] t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192 10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][9] t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2 AsstFWUprBoundX HwNm s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	6144
12_AsstFWUprBoundY_MtrNm_s4p11[0][0] 12_AsstFWUprBoundY_MtrNm_s4p11[0][1] 12_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144 8192
12_AsstFWUprBoundY_MtrNm_s4p11[0][0] 12_AsstFWUprBoundY_MtrNm_s4p11[0][1] 12_AsstFWUprBoundY_MtrNm_s4p11[0][2] 12_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144 8192 10240
12_AsstFWUprBoundY_MtrNm_s4p11[0][0] 12_AsstFWUprBoundY_MtrNm_s4p11[0][1] 12_AsstFWUprBoundY_MtrNm_s4p11[0][2] 12_AsstFWUprBoundY_MtrNm_s4p11[0][3] 12_AsstFWUprBoundY_MtrNm_s4p11[0][4]	6144 8192 10240 12288
12_AsstFWUprBoundY_MtrNm_s4p11[0][0] 12_AsstFWUprBoundY_MtrNm_s4p11[0][1] 12_AsstFWUprBoundY_MtrNm_s4p11[0][2] 12_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144 8192 10240



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144	
2 AsstFWUprBoundY MtrNm s4p11[2][5]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048	
	-2040	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]		
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	14336	
	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	28672	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192	
	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]		
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192	
t2 AsstFWUprBoundY MtrNm s4p11[4][9]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096	
:2_AsstrWUprBoundY_MtrNm_s4p11[6][10]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240	



	l
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	512
t_AsstFWDefltAssistX_HwNm_u8p8[1]	538
t_AsstFWDefltAssistX_HwNm_u8p8[2]	563
t_AsstFWDefltAssistX_HwNm_u8p8[3]	589
t_AsstFWDefltAssistX_HwNm_u8p8[4]	614
t_AsstFWDefltAssistX_HwNm_u8p8[5]	640
t_AsstFWDefltAssistX_HwNm_u8p8[6]	666
t_AsstFWDefltAssistX_HwNm_u8p8[7]	691
t_AsstFWDefltAssistX_HwNm_u8p8[8]	717
t_AsstFWDefltAssistX_HwNm_u8p8[9]	742
t_AsstFWDefltAssistX_HwNm_u8p8[10]	768
t_AsstFWDefltAssistX_HwNm_u8p8[11]	794
t_AsstFWDefltAssistX_HwNm_u8p8[12]	819
t_AsstFWDefltAssistX_HwNm_u8p8[13]	845
t_AsstFWDefltAssistX_HwNm_u8p8[14]	870
t_AsstFWDefltAssistX_HwNm_u8p8[15]	896
t_AsstFWDefltAssistX_HwNm_u8p8[16]	922
t_AsstFWDefltAssistX_HwNm_u8p8[17]	947
t_AsstFWDefltAssistX_HwNm_u8p8[18]	973
t_AsstFWDefltAssistX_HwNm_u8p8[19]	998
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4301
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4915
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	5120
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	5325
	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6963
t_AsstFWPstepNstepThresh_Cnt_u16[0]	217
t_AsstFWPstepNstepThresh_Cnt_u16[1]	587
t_AsstFWVehSpd_Kph_u9p7[0]	16128
t_AsstFWVehSpd_Kph_u9p7[1]	16256
t_AsstFWVehSpd_Kph_u9p7[2]	16384
t_AsstFWVehSpd_Kph_u9p7[3]	16512
t_AsstFWVehSpd_Kph_u9p7[4]	16640
t_AsstFWVehSpd_Kph_u9p7[5]	16768
t_AsstFWVehSpd_Kph_u9p7[6]	16896
t_AsstFWVehSpd_Kph_u9p7[7]	17024
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.19999981
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.5999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.4000001
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.5999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	_
	tgt_AssistFirewall_Per1_Defeat_AsstTbl Service Cnt lqc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_Asst WoprBoundX_HwNm_s4p11[2][6]	-2048
	-2040
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_Asst WoprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2 AsstFWUprBoundX HwNm s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	
	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	6144
E_7.000. Tropibound1_intiffin_04p11[o][r]	0.11



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-6144	
	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]		
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384	
	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0	
	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	12288	
:2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	26624	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	28672	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	538
t_AsstFWDefltAssistX_HwNm_u8p8[1]	563
t_AsstFWDefltAssistX_HwNm_u8p8[2]	589
t_AsstFWDefltAssistX_HwNm_u8p8[3]	614
t_AsstFWDefltAssistX_HwNm_u8p8[4]	640
t_AsstFWDefltAssistX_HwNm_u8p8[5]	666
t_AsstFWDefltAssistX_HwNm_u8p8[6]	691
t_AsstFWDefltAssistX_HwNm_u8p8[7]	717
t_AsstFWDefltAssistX_HwNm_u8p8[8]	742
t_AsstFWDefltAssistX_HwNm_u8p8[9]	768
t_AsstFWDefltAssistX_HwNm_u8p8[10]	794
t_AsstFWDefltAssistX_HwNm_u8p8[11]	819
t_AsstFWDefltAssistX_HwNm_u8p8[12]	845
t_AsstFWDefltAssistX_HwNm_u8p8[13]	870
t_AsstFWDefltAssistX_HwNm_u8p8[14]	896
t_AsstFWDefltAssistX_HwNm_u8p8[15]	922
t_AsstFWDefltAssistX_HwNm_u8p8[16]	947
t_AsstFWDefltAssistX_HwNm_u8p8[17]	973
t_AsstFWDefltAssistX_HwNm_u8p8[18]	998
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1024
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7168
t_AsstFWPstepNstepThresh_Cnt_u16[0] t AsstFWPstepNstepThresh Cnt u16[1]	218
	591
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3] t AsstFWVehSpd Kph u9p7[4]	19456
	19584
t_AsstFWVehSpd_Kph_u9p7[5] t_AsstFWVehSpd_Kph_u9p7[6]	19712 19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.30000019
tgt_AssistFirewall_Per1_BaseAssistCmd_intrinm_132.value  tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgc.value	-5.30000019
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.69999981
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.5 -5.5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.69999981
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	187.100006
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32
J	0



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-2.70000005	-2.70000005 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	591	591 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.5	-3.5 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-6.28999996	-6.28999996 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-4.63300037	-4.6329999 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.5369997	-5.53700018 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-3.5	-3.5 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

- Τ				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.98 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.5
AssistFirewall ActiveKSV M str.K Uls f32	0.60000024
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8733
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall CombAsstSV MtrNm M f32	1.1000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.100000001
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11399996
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.80000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.140000001
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.19999981
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.239999995
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5
k_AsstFWInpLimitHFA_MtrNm_f32	6.42999983
k_AsstFWInpLimitHysComp_MtrNm_f32	6.92999983
k_AsstFWNstep_Cnt_u16	3053
k_AsstFWPstep_Cnt_u16	2706
k RestoreThresh MtrNm f32	4.44999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
	8192



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4] t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6] t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[o][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144
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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	563
t_AsstFWDefltAssistX_HwNm_u8p8[1]	589
t_AsstFWDefltAssistX_HwNm_u8p8[2]	614
t_AsstFWDefltAssistX_HwNm_u8p8[3]	640
t_AsstFWDefltAssistX_HwNm_u8p8[4]	666
t_AsstFWDefltAssistX_HwNm_u8p8[5]	691
t_AsstFWDefltAssistX_HwNm_u8p8[6]	717
t_AsstFWDefltAssistX_HwNm_u8p8[7]	742
t_AsstFWDefltAssistX_HwNm_u8p8[8]	768
t_AsstFWDefltAssistX_HwNm_u8p8[9]	794
t_AsstFWDefltAssistX_HwNm_u8p8[10]	819
t_AsstFWDefltAssistX_HwNm_u8p8[11]	845 870
t_AsstFWDefltAssistX_HwNm_u8p8[12]	
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	896 922
t_AsstFWDefitAssistX_HwNm_u8p8[14] t AsstFWDefitAssistX HwNm_u8p8[15]	947
t_AsstFWDefltAssistX_HwNm_u8p8[16]	973
t_AsstFWDefltAssistX_HwNm_u8p8[17]	998
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1050
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7168
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	7373
t_AsstFWPstepNstepThresh_Cnt_u16[0]	219
t_AsstFWPstepNstepThresh_Cnt_u16[1]	595
t_AsstFWVehSpd_Kph_u9p7[0]	22016
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	22144 22272
t_AsstFWVehSpd_Kph_u9p7[3]	22400
t_AsstFWVehSpd_Kph_u9p7[4]	22528
t_AsstFWVehSpd_Kph_u9p7[5]	22656
t_AsstFWVehSpd_Kph_u9p7[6]	22784
t_AsstFWVehSpd_Kph_u9p7[7]	22912
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.4000001
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.67000008
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.5999999
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.67000008
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	198.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_legendering the property of th$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-2.19999981	-2.20000005 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	595	595 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.60009766	-3.60009766 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-4.05000019	-4.05000019 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.04405499	5.04405451 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.39199972	-5.3920002 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-3.60009766	-3.60009766 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.99 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.5
AssistFirewall ActiveKSV M str.K Uls f32	0.0120000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8856
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.109999999
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11500001
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.9000001
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.150000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.25
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.099999
k_AsstFWInpLimitHFA_MtrNm_f32	6.44000006
k_AsstFWInpLimitHysComp_MtrNm_f32	7.03999996
k_AsstFWNstep_Cnt_u16	2053
k_AsstFWPstep_Cnt_u16	2829
k_RestoreThresh_MtrNm_f32	4.46000004
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-30720
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-16384



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
42 ApptEM/LipsDovind// Mtshire adad4[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	
12_AsstFWUprBoundY_MtrNm_s4p11[7][1]  12_AsstFWUprBoundY_MtrNm_s4p11[7][2]  12_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144 -4096



Name	Input Value
Name t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2046 0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefltAssistX_HwNm_u8p8[0]	589
t_AsstFWDefltAssistX_HwNm_u8p8[1]	614
t_AsstFWDefltAssistX_HwNm_u8p8[2]	640 666
t_AsstFWDefltAssistX_HwNm_u8p8[3] t_AsstFWDefltAssistX_HwNm_u8p8[4]	691
t_AsstFWDefltAssistX_HwNm_u8p8[5]	717
t_AsstFWDefltAssistX_HwNm_u8p8[6]	742
t_AsstFWDefltAssistX_HwNm_u8p8[7]	768
t_AsstFWDefltAssistX_HwNm_u8p8[8]	794
t_AsstFWDefltAssistX_HwNm_u8p8[9]	819
t_AsstFWDefltAssistX_HwNm_u8p8[10]	845
t_AsstFWDefltAssistX_HwNm_u8p8[11]	870
t_AsstFWDefltAssistX_HwNm_u8p8[12]	896
t_AsstFWDefltAssistX_HwNm_u8p8[13]	922
t_AsstFWDefltAssistX_HwNm_u8p8[14]	947
t_AsstFWDefltAssistX_HwNm_u8p8[15]	973
t_AsstFWDefltAssistX_HwNm_u8p8[16] t_AsstFWDefltAssistX_HwNm_u8p8[17]	998 1024
t_AsstFWDefitAssistX_HwNm_u8p8[18]	1050
t_AsstFWDefitAssistX_HwNm_u8p8[19]	1075
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[11] t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5939 6144
t_AsstFWDefitAssistY_MtrNm_s4p11[13]	6349
t_AsstFWDefitAssistY_MtrNm_s4p11[14]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7578
t_AsstFWPstepNstepThresh_Cnt_u16[0]	220
t_AsstFWPstepNstepThresh_Cnt_u16[1]	599
t_AsstFWVehSpd_Kph_u9p7[0]	24960
t_AsstFWVehSpd_Kph_u9p7[1]	25088
t_AsstFWVehSpd_Kph_u9p7[2]	25216
t_AsstFWVehSpd_Kph_u9p7[3] t_AsstFWVehSpd_Kph_u9p7[4]	25344 25472
t_AsstFWVehSpd_Kph_u9p7[5]	25472 25600
t_AsstFWVehSpd_Kph_u9p7[6]	25728
t_AsstFWVehSpd_Kph_u9p7[7]	25856
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.5
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.11000013
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7.32999992
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	209.399994
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tot AggictEirowall Bort Defect Aggt The Carrier Cat Inc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lett_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.43400002	5.43400002 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	599	599 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.70019531	3.70019531 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.24259996	-5.24259996 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.48147964	5.48147964 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.82499981	5.82499981 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.70019531	3.70019531 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•

Τ			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.100 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	5.5999999
AssistFirewall ActiveKSV M str.K UIs f32	0.0130000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8979
AssistFirewall AsstReducedPerfSV Cnt M Igc	0
AssistFirewall CombAsstSV MtrNm M f32	7.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.119999997
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11600006
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall LwrBoundKSV M str.K Uls f32	0.159999996
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.19999981
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.25999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.19999981
k AsstFWInpLimitHFA MtrNm f32	6.44999981
k_AsstFWInpLimitHysComp_MtrNm_f32	7.1500001
k_AsstFWNstep_Cnt_u16	1053
k_AsstFWPstep_Cnt_u16	2952
k RestoreThresh MtrNm f32	4.46999979
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2 AsstFWUprBoundX HwNm s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192



	( =# := 10=10
Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_Asst WopiBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_Asst WoprBoundX_HwNm_s4p11[5][1]	-10240
t2_Asst WopiBoundX_HwNm_s4p11[5][1]	-8192
	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3] t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_Asst WopiBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
tz_AsstFWUprBoundX_HwNm_s4p11[7][6] t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-22528
42 A a a 4 F W   In a D a con al W   M 4 a b long a 2 a 4 a 4 a 6 0 1 ( 4 )	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	
t2_AsstrWUprBoundY_MtrNm_s4p11[0][5]	-18432
	-18432 -16384



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-10240
	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
2 AsstFWUprBoundY MtrNm s4p11[2][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240
	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-8192
2 AsstFWUprBoundY MtrNm s4p11[5][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
, , , , , , , , , , , , , , , , , , , ,	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
, 10511 **Opt-Doutid tiviti (4111_34p t [[0][0]	
A AcotEM/Lipr Pound V MtrNim c 4 = 44 (C)[O]	
	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	14336 -8192



Input Value
0
2048
4096
6144
8192
10240
12288
614
640
666
691
717
742
768
794
819
845
870
896
922
947
973
998
1024
1050
1075
1101
3891
4096
4301
4506
4710
4915
5120
5325
5530
5734
5939
6144
6349
6554
6758
6963
7168
7373
7578
7782
221
603
27904
28032
28160
28288
28416
28544
28672
28800
-5.5999999
0
-5.19999981
7.21999979
7.44000006
0
220.5
220.5 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32  tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32  tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32  t_lt_tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 t_t_t_t_tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 t_lt_lt_sassistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 t_t_t_t_tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.52719975	5.52720022 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	603	603 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.79980469	3.79980469 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.31799984	-5.31799984 ± 4.88E-04	<b>~</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.67999983	5.67999983 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.14799976	6.14799976 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.79980469	3.79980469 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Τ			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.101 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.6999981
AssistFirewall ActiveKSV M str.K Uls f32	0.0140000004
AssistFirewall_ActiveRawAcc_Cnt_M_u16	9102
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.69999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.129999995
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11699998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.170000002
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.30000019
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.270000011
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.30000019
k_AsstFWInpLimitHFA_MtrNm_f32	6.46000004
k_AsstFWInpLimitHysComp_MtrNm_f32	7.26000023
k_AsstFWNstep_Cnt_u16	53
k_AsstFWPstep_Cnt_u16	3075
k_RestoreThresh_MtrNm_f32	4.48000002
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
	18432
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_Asst WorlboundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
	4096
:2_AsstFWUprBoundX_HwNm_s4p11[5][7] :2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
12_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
:2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-14336



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
.c_noou vvopiduuiu1_iviii1iuini_54p11[4][10]	24JI U



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	640
t_AsstFWDefltAssistX_HwNm_u8p8[1]	666
t_AsstFWDefltAssistX_HwNm_u8p8[2]	691
t_AsstFWDefltAssistX_HwNm_u8p8[3]	717
t_AsstFWDefltAssistX_HwNm_u8p8[4]	742
t_AsstFWDefltAssistX_HwNm_u8p8[5]	768
t_AsstFWDefltAssistX_HwNm_u8p8[6]	794
t_AsstFWDefltAssistX_HwNm_u8p8[7]	819
t_AsstFWDefltAssistX_HwNm_u8p8[8]	845
t_AsstFWDefltAssistX_HwNm_u8p8[9]	870
t_AsstFWDefltAssistX_HwNm_u8p8[10]	896
t_AsstFWDefltAssistX_HwNm_u8p8[11]	922
t_AsstFWDefltAssistX_HwNm_u8p8[12]	947
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	973 998
t_AsstFWDefitAssistX_HwNm_u8p8[14] t_AsstFWDefitAssistX_HwNm_u8p8[15]	1024
t AsstFWDefitAssistX HwNm u8p8[16]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1126
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7987
t_AsstFWPstepNstepThresh_Cnt_u16[0]	222
t_AsstFWPstepNstepThresh_Cnt_u16[1]	607
t_AsstFWVehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	30976 31104
t_AsstFWVehSpd_Kph_u9p7[3]	31232
t_AsstFWVehSpd_Kph_u9p7[4]	31360
t_AsstFWVehSpd_Kph_u9p7[5]	31488
t_AsstFWVehSpd_Kph_u9p7[6]	31616
t_AsstFWVehSpd_Kph_u9p7[7]	31744
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.69999981
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.88999987
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.32999992
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7.55000019
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	231.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFi$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.62019968	5.62020016 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	607	607 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.89990234	3.89990234 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-3.86439991	-3.86439991 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.98903036	6.98903036 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.78900003	3.78900003 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	•
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.89990234	3.89990234 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Τ			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.102 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	5.80000019
AssistFirewall ActiveKSV M str.K UIs f32	0.0149999997
AssistFirewall_ActiveRawAcc_Cnt_M_u16	9225
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	7.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.140000001
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11800003
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.1999981
AssistFirewall LwrBoundKSV M str.K Uls f32	0.180000007
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.4000001
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.280000001
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.4000001
k_AsstFWInpLimitHFA_MtrNm_f32	6.46999979
k_AsstFWInpLimitHysComp_MtrNm_f32	7.36999989
k_AsstFWNstep_Cnt_u16	123
k_AsstFWPstep_Cnt_u16	3198
k RestoreThresh MtrNm f32	4.48999977
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	0
	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-24576 -22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-18432
LA MASIC VICIDIDADIDAT INTENIO SADTITUTAL	-16384
	4.4000
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-14336 -12288



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6] t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6] t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	26624
t2 AsstFWUprBoundY MtrNm s4p11[5][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096
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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	0
t_AsstFWDefltAssistX_HwNm_u8p8[1]	0
t_AsstFWDefltAssistX_HwNm_u8p8[2]	0
t_AsstFWDefltAssistX_HwNm_u8p8[3]	0
t_AsstFWDefltAssistX_HwNm_u8p8[4]	0
t_AsstFWDefltAssistX_HwNm_u8p8[5]	0
t_AsstFWDefltAssistX_HwNm_u8p8[6]	0
t_AsstFWDefltAssistX_HwNm_u8p8[7]	0
t_AsstFWDefltAssistX_HwNm_u8p8[8]	0
t_AsstFWDefltAssistX_HwNm_u8p8[9]	0
t_AsstFWDefltAssistX_HwNm_u8p8[10]	0
t_AsstFWDefltAssistX_HwNm_u8p8[11]	0
t_AsstFWDefltAssistX_HwNm_u8p8[12]	0
t_AsstFWDefltAssistX_HwNm_u8p8[13]	0
t_AsstFWDefltAssistX_HwNm_u8p8[14]	0
t_AsstFWDefltAssistX_HwNm_u8p8[15]	0
t_AsstFWDefltAssistX_HwNm_u8p8[16]	0
t_AsstFWDefltAssistX_HwNm_u8p8[17]	0
t_AsstFWDefltAssistX_HwNm_u8p8[18]	0
t_AsstFWDefltAssistX_HwNm_u8p8[19]	0
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	8192
t_AsstFWPstepNstepThresh_Cnt_u16[0]	223
t_AsstFWPstepNstepThresh_Cnt_u16[1]	611
t_AsstFWVehSpd_Kph_u9p7[0]	33792
t_AsstFWVehSpd_Kph_u9p7[1]	33920
t_AsstFWVehSpd_Kph_u9p7[2]	34048
t_AsstFWVehSpd_Kph_u9p7[3]	34176
t_AsstFWVehSpd_Kph_u9p7[4]	34304
t_AsstFWVehSpd_Kph_u9p7[5]	34432
t_AsstFWVehSpd_Kph_u9p7[6]	34560
t_AsstFWVehSpd_Kph_u9p7[7]	34688
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.67000008
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7.65999985
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	222.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lq	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.7130003	5.71299982 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	611	611 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	4	4 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-2.29439998	-2.29439998 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.34399986	6.34399986 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.04800034	4.04799986 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4	4 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.103 (Repeat Count = 1)	and the second s
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.9000001
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0160000008
AssistFirewall_ActiveRawAcc_Cnt_M_u16	9348
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.150000006
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11899996
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.30000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.189999998
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.289999992
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.5
k_AsstFWInpLimitHFA_MtrNm_f32	6.48000002
k_AsstFWInpLimitHysComp_MtrNm_f32	7.48000002
k_AsstFWNstep_Cnt_u16	234
k_AsstFWPstep_Cnt_u16	3321
k_RestoreThresh_MtrNm_f32	5.51000023
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096
t2_Asst WoprboundX_1WNIII_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144
	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_1WNIII_s4p11[6][2]	
t2_AsstFWUprBoundX_HWNm_s4p11[6][3] t2 AsstFWUprBoundX HwNm s4p11[6][4]	6144
_	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-22528
	-20480
tz Asstevuprboungy Mitriam s4b11101111	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	I-1043Z
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-18432 -16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-16384 -14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-16384



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1] t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144
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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[1]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[2]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[3]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[4]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[5]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[6]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[7]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[8]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[9]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[10]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[11]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[12]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	2560 2560
t_AsstFWDefitAssistX_HwNm_u8p8[14] t_AsstFWDefitAssistX_HwNm_u8p8[15]	2560
t_AsstFWDefitAssistX_HwNm_u8p8[16]	2560
t_AsstFWDefitAssistX_HwNm_u8p8[17]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[18]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[19]	2560
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	8397
t_AsstFWPstepNstepThresh_Cnt_u16[0]	224
t_AsstFWPstepNstepThresh_Cnt_u16[1]	615
t_AsstFWVehSpd_Kph_u9p7[0]	36736
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	36864 36992
t_AsstFWVehSpd_Kph_u9p7[3]	37120
t AsstFWVehSpd Kph u9p7[4]	37248
t_AsstFWVehSpd_Kph_u9p7[5]	37376
t_AsstFWVehSpd_Kph_u9p7[6]	37504
t_AsstFWVehSpd_Kph_u9p7[7]	37632
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.78000021
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.11000013
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.55000019
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.31999969
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	253.100006
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFi$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.80560017	5.80560017 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	615	615 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	2.20019531	2.20019531 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.33899975	7.33900023 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.19300032	7.19299984 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.32499981	4.32499981 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	2.20019531	2.20019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>~</b>
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Τ						
Actual Function	Count	Expected Function	Count	Result		
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~		
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•		
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~		
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>		
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~		

Test Step 2.104 (Repeat Count = 1)		
Name	Input Value	
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6	
AssistFirewall ActiveKSV M str.K Uls f32	0.0170000009	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	9471	
AssistFirewall AsstReducedPerfSV Cnt M lgc	0	
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.5	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.30000019	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.159999996	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12	
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.4000001	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.200000003	
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.5	
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.300000012	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.5999999	
k_AsstFWInpLimitHFA_MtrNm_f32	6.48999977	
k_AsstFWInpLimitHysComp_MtrNm_f32	7.59000015	
k_AsstFWNstep_Cnt_u16	345	
k_AsstFWPstep_Cnt_u16	3444	
k RestoreThresh MtrNm f32	5.51999998	
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288	
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096	
t2 AsstFWUprBoundX HwNm s4p11[0][9]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432	
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384	
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336	
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288	
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5] t2_AsstFWUprBoundX_HwNm_s4p11[1][6] t2_AsstFWUprBoundX_HwNm_s4p11[1][7] t2_AsstFWUprBoundX_HwNm_s4p11[1][8] t2_AsstFWUprBoundX_HwNm_s4p11[1][9] t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	-6144 -4096 -2048 0 2048	



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-12288
t2 AsstFWUprBoundX HwNm s4p11[4][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	2048
	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336 -12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-14336
	-12288
t2 AsstFWUprBoundY MtrNm s4p11[0][4]	, ·
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-10240 -8192



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	10240	
	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]		
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240	
	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	8192	
12_1.0011 VYOPIDOUNUT_IVILITYIII_34PTT[/][3]	0192	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	22528
t_AsstFWDefltAssistX_HwNm_u8p8[0]	717
t_AsstFWDefltAssistX_HwNm_u8p8[1]	742
t_AsstFWDefltAssistX_HwNm_u8p8[2]	768
t_AsstFWDefltAssistX_HwNm_u8p8[3]	794
t_AsstFWDefltAssistX_HwNm_u8p8[4]	819
t_AsstFWDefltAssistX_HwNm_u8p8[5]	845
t_AsstFWDefltAssistX_HwNm_u8p8[6]	870
t_AsstFWDefltAssistX_HwNm_u8p8[7]	896
t_AsstFWDefltAssistX_HwNm_u8p8[8]	922
t_AsstFWDefltAssistX_HwNm_u8p8[9]	947
t_AsstFWDefltAssistX_HwNm_u8p8[10]	973
t_AsstFWDefltAssistX_HwNm_u8p8[11]	998
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	1050 1075
t_AsstFWDefitAssistX_HwNm_u8p8[14] t AsstFWDefitAssistX HwNm_u8p8[15]	1101
t_AsstFWDefitAssistX_HwNm_u8p8[16]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1203
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	8602
t_AsstFWPstepNstepThresh_Cnt_u16[0]	225
t_AsstFWPstepNstepThresh_Cnt_u16[1]	619
t_AsstFWVehSpd_Kph_u9p7[0]	39680
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	39808 39936
t_AsstFWVehSpd_Kph_u9p7[3]	40064
t_AsstFWVehSpd_Kph_u9p7[4]	40192
t_AsstFWVehSpd_Kph_u9p7[5]	40320
t_AsstFWVehSpd_Kph_u9p7[6]	40448
t_AsstFWVehSpd_Kph_u9p7[7]	40576
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.88999987
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.21999979
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.65999985
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.43000031
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	12.3999996
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFi$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.89799976	5.89799976 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	619	619 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.20019531	4.20019531 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.60080051	7.60080004 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.11999989	7.11999989 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-3.8499999	-3.8499999 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4.20019531	4.20019531 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.105 (Repeat Count = 1)	V
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.099999
AssistFirewall ActiveKSV M str.K Uls f32	0.0179999992
AssistFirewall_ActiveRawAcc_Cnt_M_u16	9594
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	7.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.170000002
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12100005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.20999993
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.5999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.310000002
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.69999981
k_AsstFWInpLimitHFA_MtrNm_f32	6.5
k_AsstFWInpLimitHysComp_MtrNm_f32	7.69999981
k_AsstFWNstep_Cnt_u16	456
k_AsstFWPstep_Cnt_u16	3567
k_RestoreThresh_MtrNm_f32	5.53000021
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-18432



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-6144
	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2 AsstFWUprBoundX HwNm s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	
	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-4096
LZ_ASSIL WOOPIDOUNGT_WILLIAMIT_S4PTT[U][/]	-4050



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	4096



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576
t_AsstFWDefltAssistX_HwNm_u8p8[0]	742
t_AsstFWDefltAssistX_HwNm_u8p8[1]	768
t_AsstFWDefltAssistX_HwNm_u8p8[2]	794
t_AsstFWDefltAssistX_HwNm_u8p8[3]	819
t_AsstFWDefltAssistX_HwNm_u8p8[4]	845
t_AsstFWDefltAssistX_HwNm_u8p8[5]	870
t_AsstFWDefltAssistX_HwNm_u8p8[6]	896
t_AsstFWDefltAssistX_HwNm_u8p8[7]	922
t_AsstFWDefltAssistX_HwNm_u8p8[8]	947
t_AsstFWDefltAssistX_HwNm_u8p8[9]	973
t_AsstFWDefltAssistX_HwNm_u8p8[10]	998
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1229
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	-205
t_AsstFWPstepNstepThresh_Cnt_u16[0] t AsstFWPstepNstepThresh Cnt u16[1]	226
	623
t_AsstFWVehSpd_Kph_u9p7[0]	42624
t_AsstFWVehSpd_Kph_u9p7[1]	42752 42880
t_AsstFWVehSpd_Kph_u9p7[2] t_AsstFWVehSpd_Kph_u9p7[3]	42880
t_AsstFWVenSpd_kpn_usp7[3] t_AsstFWVehSpd_kph_usp7[4]	43008
_ , _ , _ , . ;	43264
t_AsstFWVehSpd_Kph_u9p7[5] t_AsstFWVehSpd_Kph_u9p7[6]	43392
	43520 43520
t_AsstFWVehSpd_Kph_u9p7[7] tqt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	43320
tgt_AssistFirewall_Per1_BaseAssistCmd_intrinm_132.value  tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_Deteat_Assist_MtrNm_f32.value  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.32999992
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_r32.value  tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.76999998
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.099999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	19.5
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_Assist_MithNff_i32	
tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_beleat_AssistOi_service_Crit_inst_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_intintin_is2  tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32
0	0



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.99020004	5.99020004 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	623	623 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-0.100097656	-0.100097656 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.68900013	5.68900013 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.0250001	7.0250001 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-3.5539999	-3.5539999 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-0.100097656	-0.100097656 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Input Value	
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	
AssistFirewall_ActiveKSV_M_str.K_Uls_f32       0.0189999994         AssistFirewall_ActiveRawAcc_Cnt_M_u16       9717         AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc       1         AssistFirewall_CombAsstSV_MtrNm_M_f32       7.69999981         AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32       5.5         AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32       0.180000007         AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32       1.12199998         AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32       6.5999999         AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32       0.219999999         AssistFirewall_PNCountStatus_Cnt_M_lgc       1         AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32       -5.69999981         AssistFirewall_UprBoundKSV_M_str.K_Uls_f32       0.319999993         Rte_Inst_Ap_AssistFirewall       tgt_Rte_Inst_Ap_AssistFirewall         k_AsstFWInpLimitBaseAsst_MtrNm_f32       5.80000019	
AssistFirewall_ActiveRawAcc_Cnt_M_u16       9717         AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc       1         AssistFirewall_CombAsstSV_MtrNm_M_f32       7.69999981         AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32       5.5         AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32       0.180000007         AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32       1.12199998         AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32       6.5999999         AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32       0.219999999         AssistFirewall_PNCountStatus_Cnt_M_lgc       1         AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32       -5.69999981         AssistFirewall_UprBoundKSV_M_str.K_Uls_f32       0.319999993         Rte_Inst_Ap_AssistFirewall       tg_Rte_Inst_Ap_AssistFirewall         k_AsstFWInpLimitBaseAsst_MtrNm_f32       5.80000019	
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc       1         AssistFirewall_CombAsstSV_MtrNm_M_f32       7.69999981         AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32       5.5         AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32       0.180000007         AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32       1.12199998         AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32       6.5999999         AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32       0.219999999         AssistFirewall_PNCountStatus_Cnt_M_lgc       1         AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32       -5.6999981         AssistFirewall_UprBoundKSV_M_str.K_Uls_f32       0.319999993         Rte_Inst_Ap_AssistFirewall       tg_Rte_Inst_Ap_AssistFirewall         k_AsstFWInpLimitBaseAsst_MtrNm_f32       5.80000019	
AssistFirewall_CombAsstSV_MtrNm_M_f32       7.69999981         AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32       5.5         AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32       0.180000007         AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32       1.12199998         AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32       6.5999999         AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32       0.219999999         AssistFirewall_PNCountStatus_Cnt_M_lgc       1         AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32       -5.6999981         AssistFirewall_UprBoundKSV_M_str.K_Uls_f32       0.319999993         Rte_Inst_Ap_AssistFirewall       tg_Rte_Inst_Ap_AssistFirewall         k_AsstFWInpLimitBaseAsst_MtrNm_f32       5.80000019	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32       0.180000007         AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32       1.12199998         AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32       6.5999999         AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32       0.219999999         AssistFirewall_PNCountStatus_Cnt_M_lgc       1         AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32       -5.6999981         AssistFirewall_UprBoundKSV_M_str.K_Uls_f32       0.319999993         Rte_Inst_Ap_AssistFirewall       tgt_Rte_Inst_Ap_AssistFirewall         k_AsstFWInpLimitBaseAsst_MtrNm_f32       5.80000019	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32       0.180000007         AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32       1.12199998         AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32       6.5999999         AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32       0.219999999         AssistFirewall_PNCountStatus_Cnt_M_lgc       1         AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32       -5.6999981         AssistFirewall_UprBoundKSV_M_str.K_Uls_f32       0.319999993         Rte_Inst_Ap_AssistFirewall       tgt_Rte_Inst_Ap_AssistFirewall         k_AsstFWInpLimitBaseAsst_MtrNm_f32       5.80000019	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32       1.12199998         AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32       6.599999         AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32       0.219999999         AssistFirewall_PNCountStatus_Cnt_M_lgc       1         AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32       -5.6999981         AssistFirewall_UprBoundKSV_M_str.K_Uls_f32       0.319999993         Rte_Inst_Ap_AssistFirewall       tgt_Rte_Inst_Ap_AssistFirewall         k_AsstFWInpLimitBaseAsst_MtrNm_f32       5.80000019	
AssistFirewall_LwrBoundKSV_M_str.Ky_Uls_f32       6.5999999         AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32       0.219999999         AssistFirewall_PNCountStatus_Cnt_M_lgc       1         AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32       -5.6999981         AssistFirewall_UprBoundKSV_M_str.K_Uls_f32       0.319999993         Rte_Inst_Ap_AssistFirewall       tgt_Rte_Inst_Ap_AssistFirewall         k_AsstFWInpLimitBaseAsst_MtrNm_f32       5.80000019	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32       0.219999999         AssistFirewall_PNCountStatus_Cnt_M_lgc       1         AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32       -5.6999981         AssistFirewall_UprBoundKSV_M_str.K_Uls_f32       0.319999993         Rte_Inst_Ap_AssistFirewall       tgt_Rte_Inst_Ap_AssistFirewall         k_AsstFWInpLimitBaseAsst_MtrNm_f32       5.80000019	
AssistFirewall_PNCountStatus_Cnt_M_lgc       1         AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32       -5.69999981         AssistFirewall_UprBoundKSV_M_str.K_Uls_f32       0.319999993         Rte_Inst_Ap_AssistFirewall       tgt_Rte_Inst_Ap_AssistFirewall         k_AsstFWInpLimitBaseAsst_MtrNm_f32       5.80000019	
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 -5.69999981  AssistFirewall_UprBoundKSV_M_str.K_Uls_f32 0.319999993  Rte_Inst_Ap_AssistFirewall tgt_Rte_Inst_Ap_AssistFirewall  k_AsstFWInpLimitBaseAsst_MtrNm_f32 5.80000019	
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32  Rte_Inst_Ap_AssistFirewall  k_AsstFWInpLimitBaseAsst_MtrNm_f32  0.319999993  tgt_Rte_Inst_Ap_AssistFirewall  5.80000019	
Rte_Inst_Ap_AssistFirewall tgt_Rte_Inst_Ap_AssistFirewall	
·	
k AsstFWInpLimitHFA MtrNm f32 6.51000023	
k_AsstFWInpLimitHysComp_MtrNm_f32 7.80999994	
k_AsstFWNstep_Cnt_u16 567	
k_AsstFWPstep_Cnt_u16 3690	
k RestoreThresh MtrNm f32 5.53999996	
12_AsstFWUprBoundX_HwNm_s4p11[0][0] -8192	
12_AsstFWUprBoundX_HwNm_s4p11[0][1] -6144	
12_AsstFWUprBoundX_HwNm_s4p11[0][2] -4096	
12_AsstFWUprBoundX_HwNm_s4p11[0][3] -2048	
12_AsstFWUprBoundX_HwNm_s4p11[0][4] 0	
12_AsstFWUprBoundX_HwNm_s4p11[0][5] 2048	
12_AsstFWUprBoundX_HwNm_s4p11[0][6] 4096	
12_AsstFWUprBoundX_HwNm_s4p11[0][7] 6144	
12_AsstFWUprBoundX_HwNm_s4p11[0][8] 8192	
12 AsstFWUprBoundX HwNm s4p11[0][9] 10240	
12_AsstFWUprBoundX_HwNm_s4p11[0][10] 12288	
12_AsstFWUprBoundX_HwNm_s4p11[1][0] -14336	
12_AsstFWUprBoundX_HwNm_s4p11[1][1] -12288	
12_AsstFWUprBoundX_HwNm_s4p11[1][2] -10240	
12_AsstFWUprBoundX_HwNm_s4p11[1][3] -8192	
12_AsstFWUprBoundX_HwNm_s4p11[1][4] -6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5] -4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][6] -2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7] 0	
12_AsstFWUprBoundX_HwNm_s4p11[1][8] 2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][9] 4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][10] 6144	
12_AsstFWUprBoundX_HwNm_s4p11[2][0] -16384	



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
12_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
:2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240
:2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-8192
	-6192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-16384	
t2_AsstrWUprBoundY_MtrNm_s4p11[1][1]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	28672	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432	
	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-2048	
t2 AsstFWUprBoundY MtrNm s4p11[4][6]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	0	



	(
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	768
t_AsstFWDefltAssistX_HwNm_u8p8[1]	794
t_AsstFWDefltAssistX_HwNm_u8p8[2]	819
t_AsstFWDefltAssistX_HwNm_u8p8[3]	845
t_AsstFWDefltAssistX_HwNm_u8p8[4]	870
t_AsstFWDefltAssistX_HwNm_u8p8[5]	896
t_AsstFWDefltAssistX_HwNm_u8p8[6]	922
t_AsstFWDefltAssistX_HwNm_u8p8[7]	947
t_AsstFWDefltAssistX_HwNm_u8p8[8]	973
t_AsstFWDefltAssistX_HwNm_u8p8[9]	998
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	1101
t_AsstFWDefitAssistX_HwNm_u8p8[14] t_AsstFWDefitAssistX_HwNm_u8p8[15]	1152
t_AsstFWDefitAssistX_HwNm_u8p8[16]	1178
t_AsstFWDefitAssistX_HwNm_u8p8[17]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1254
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	32767
t_AsstFWPstepNstepThresh_Cnt_u16[0]	227
t_AsstFWPstepNstepThresh_Cnt_u16[1]	627
t_AsstFWVehSpd_Kph_u9p7[0]	45568
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	45696 45824
t_AsstFWVehSpd_Kph_u9p7[3]	45952
t AsstFWVehSpd Kph u9p7[4]	46980
t_AsstFWVehSpd_Kph_u9p7[5]	46208
t_AsstFWVehSpd_Kph_u9p7[6]	46336
t_AsstFWVehSpd_Kph_u9p7[7]	46464
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7.11000013
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.44000006
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.88000011
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.19999981
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	26.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AsstTbl\_Service\_Cnt\_Inst\_AsstTbl\_Service\_Cnt\_Inst\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.08220005	6.08220005 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	627	627 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.78980017	5.78980017 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.90799999	6.90799999 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-3.23599982	-3.23600006 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Τ				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.107 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.30000019
AssistFirewall ActiveKSV M str.K Uls f32	0.019999996
AssistFirewall_ActiveRawAcc_Cnt_M_u16	9840
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.18999998
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12300003
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.69999981
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.230000004
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.330000013
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.9000001
k_AsstFWInpLimitHFA_MtrNm_f32	6.51999998
k_AsstFWInpLimitHysComp_MtrNm_f32	7.92000008
k_AsstFWNstep_Cnt_u16	678
k_AsstFWPstep_Cnt_u16	3813
k_RestoreThresh_MtrNm_f32	5.55000019
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
12_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2 AsstFWUprBoundX HwNm s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
12_AsstFWUprBoundX_HwNm_s4p11[6][10]	
	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-12288
:2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-2048



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048	
	0	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]		
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144	
	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-2048	
	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]		
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0	
	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096	



		( 44 4 10 10 10
22. ASSEN'QUIPROSANCH Michina   Septimina	me Ir	Input Value
2.AssFVUD-BoundY, Minhthm   1991   1796   1926   1926   2.AssFVUD-BoundY, Minhthm   1991   1797   1228   1928   2.AssFVUD-BoundY, Minhthm   1991   1797   1228   1928   2.AssFVUD-BoundY, Minhthm   1991   1797   1838   1991   1.AssFVUD-BoundY, Minhthm   1991   1797   1838   1991   1.AssFVUD-BoundY, Minhthm   1991   1991   1.AssFVUD-BoundY, Hown   1996   1992   1.AssFVUD-BoundY, Hown   1996   1.AssFVUD-Bou		•
2. AssIPV/UPGBOURD, Minhtset   17  [76]   10240   2. AssIPV/UPGBOURD, Minhtset   17  [76]   14330   12. AssIPV/UPGBOURD, Minhtset   17  [76]   14330   14. AssIPV/UPGBOURD, Minhtset   17  [76]   14330   14. AssIPV/UPGBOURD, Minhtset   17  [76]   16. AssIPV/UPGBOURD, Minhtset   17  [76]   16. AssIPV/UPGBOURD, Minhtset   17  [76]   16. AssIPV/UPGBOURD, Minhtset   17  [76]   17  [		
2. AsaFWQbiBound*, Minhtm*, 4611/178    1538    2. AsaFWQbiBound*, Minhtm*, 4611/178    1638    2. AsaFWQbiBound*, Minhtm*, 4611/178    189    174    1		
2. Assel Pulpile Bound's Minkins 4511   TEB    14386         2. Assel Pulpile Bound's Minkins 4511   TEB    1832		
2. ABSPW/DEROADNI, Michan, abs 117[10]   1938[2]   1 ABSP   2. ABSPW/DEROADNI, Michan, abs 117[10]   1938[2]   1 ABSP   2. ABSPW/DEROADNI, Michan, abs 17[10]   1948[2]   1959	, = = , , , , ,	
12. ASSET PUBLISHANDER   1947   1942		
Least PVODHAssist J. Harbit 1989  1   Least PVODHAssist J. Mark 1989  1   Least	, = = , , , , ,	
LassTW0MRAssistX_Hwhm usp81		
LassFVDelfiAssist Newhr up9813   86   LassFVDelfiAssist Newhr up9814   86   LassFVDelfiAssist Newhr up9814   86   LassFVDelfiAssist Newhr up9819   947   LassFVDelfiAssist Newhr up9819   947   LassFVDelfiAssist Newhr up9819   947   LassFVDelfiAssist Newhr up9819   948   LassFVDelfiAssist Newhr up9819   1024   LassFVDelfiAssist Newhr up9819   1024   LassFVDelfiAssist Newhr up9819   1025   LassFVDelfiAssist Newhr up9819   1026   LassFVDelfiAssist Newhr up9819   1026   LassFVDelfiAssist Newhr up9819   1027   LassFVDelfiAssist Newhr up9819   1026   LassFVDelfiAss	sstFWDefltAssistX_HwNm_u8p8[0] 7	794
LastFW0MAssix   Nehm up98 3   870	sstFWDefltAssistX_HwNm_u8p8[1] 8	319
LassiPVDelfiAssistX_Hwhm_usp8[0]   922     LassiPVDelfiAssistX_Hwhm_usp8[0]   947     LassiPVDelfiAssistX_Hwhm_usp8[0]   947     LassiPVDelfiAssistX_Hwhm_usp8[0]   948     LassiPVDelfiAssistX_Hwhm_usp8[0]   908     LassiPVDelfiAssistX_Hwhm_usp8[0]   1024     LassiPVDelfiAssistX_Hwhm_usp8[0]   1026     LassiPVDelfiAssistX_Hwhm_usp8[0]   1026     LassiPVDelfiAssistX_Hwhm_usp8[0]   1026     LassiPVDelfiAssistX_Hwhm_usp8[1]   1076     LassiPVDelfiAssistX_Hwhm_usp8[1]   1076     LassiPVDelfiAssistX_Hwhm_usp8[1]   1126     LassiPVDelfiAssistX_Hwhm_usp8[1]   1126     LassiPVDelfiAssistX_Hwhm_usp8[1]   1126     LassiPVDelfiAssistX_Hwhm_usp8[1]   1126     LassiPVDelfiAssistX_Hwhm_usp8[1]   1230     LassiPVDelfiAssistX_Mintm_asp1[1]   2867     LassiPVDelfiAssistX_Mintm_asp1[1]   2867     LassiPVDelfiAssistX_Mintm_asp1[1]   2867     LassiPVDelfiAssistX_Mintm_asp1[1]   2867     LassiPVDelfiAssistX_Mintm_asp1[1]   3068     LassiPVDelfiAssistX_Mintm_asp1[1]   4096     La	sstFWDefltAssistX_HwNm_u8p8[2] 8	345
LassPWDelfiAssistX, HeVm, u8p8[5]   922     LassPWDelfiAssistX, HeVm, u8p8[7]   937     LassPWDelfiAssistX, HeVm, u8p8[7]   938     LassPWDelfiAssistX, HeVm, u8p8[7]   938     LassPWDelfiAssistX, HeVm, u8p8[7]   1055     LassPWDelfiAssistX, HeVm, u8p8[1]   1055     LassPWDelfiAssistX, HeVm, u8p8[1]   1055     LassPWDelfiAssistX, HeVm, u8p8[1]   1075     LassPWDelfiAssistX, HeVm, u8p8[1]   1075     LassPWDelfiAssistX, HeVm, u8p8[1]   1101     LassPWDelfiAssistX, HeVm, u8p8[1]   1152     LassPWDelfiAssistX, HeVm, u8p8[1]   1152     LassPWDelfiAssistX, HeVm, u8p8[1]   1152     LassPWDelfiAssistX, HeVm, u8p8[1]   1290     LassPWDelfiAssistY, MeVm, u8p1[1]   2488     LassPWDelfiAssistY, MeVm, u8p1[1]   2489     LassPWDelfiAssistY, MeVm, u8p1[1]   2489     LassPWDelfiAssistY, MeVm, u8p1[1]   3072     LassPWDelfiAssistY, MeVm, u8p1[1]   3482     LassPWDelfiAssistY, MeVm, u8p1[1]   3482     LassPWDelfiAssistY, MeVm, u8p1[1]   398     LassPWDelfiAssistY, MeVm, u8p1[1]   398     LassPWDelfiAssistY, MeVm, u8p1[1]   4090     LassPWDelfiAssistY, MeVm,	sstFWDefltAssistX_HwNm_u8p8[3] 8	370
LassFWDeffAssistX, HeNn, uspRifs  947	sstFWDefltAssistX_HwNm_u8p8[4] 8	396
LassFWDelfiAssistX_HeVm_u8p8[7]	sstFWDefltAssistX HwNm u8p8[5] 9	322
LassFWDelfiAssistX_HeVm_u8p8[7]		
LasaFW0PfAsaistX, HeVm., u8p8(8)   98	, , ,	
LassFW0elfAssistX, HeNn, u8p8[9]   1024	1 1	
LassiFWDelftAssistX, HwNm_u8p8[10]	, , ,	
LassiPWDelflassistX, HwNm.up8g113		
LastFWDelfLassiaX, Hwhm_u8p8[12]		
LASSIFWDelflAssistX_Hwhm_u8p8[13]	sstFWDefltAssistX_HwNm_u8p8[11]	1075
LASSIFWDeltAssieXL.HwNm.uBp8[16] 1703  LASSIFWDeltAssieXL.HwNm.uBp8[16] 1703  LASSIFWDeltAssieXL.HwNm.uBp8[17] 1229  LASSIFWDeltAssieXL.HwNm.uBp8[17] 1229  LASSIFWDeltAssieXL.HwNm.uBp8[18] 1254  LASSIFWDeltAssieXL.HwNm.uBp8[18] 1264  LASSIFWDeltAssieXL.HwNm.uBp8[18] 1264  LASSIFWDeltAssieXL.HwNm.uBp8[18] 1260  LASSIFWDeltAssieXL.HwNm.uBp8[18] 1260  LASSIFWDeltAssieXL.HwNm.uBp8[18] 1260  LASSIFWDeltAssieXL.HwNm.uBp8[18] 1260  LASSIFWDeltAssieXV.MrNm.uBp11[1] 2662  LASSIFWDeltAssieXV.MrNm.uBp11[3] 3072  LASSIFWDeltAssieXV.MrNm.uBp11[4] 3277  LASSIFWDeltAssieXV.MrNm.uBp11[6] 3482  LASSIFWDeltAssieXV.MrNm.uBp11[6] 3482  LASSIFWDeltAssieXV.MrNm.uBp11[7] 3891  LASSIFWDeltAssieXV.MrNm.uBp11[8] 4096  LASSIFWDeltAssieXV.MrNm.uBp11[8] 4096  LASSIFWDeltAssieXV.MrNm.uBp11[19] 4301  LASSIFWDeltAssieXV.MrNm.uBp11[19] 4301  LASSIFWDeltAssieXV.MrNm.uBp11[19] 4915  LASSIFWDeltAssieXV.MrNm.uBp11[19] 4915  LASSIFWDeltAssieXV.MrNm.uBp11[19] 4915  LASSIFWDeltAssieXV.MrNm.uBp11[19] 5520  LASSIFWDeltAssieXV.MrNm.uBp11[19] 5530  LASSIFWDeltAssieXV.MrNm.u	sstFWDefltAssistX_HwNm_u8p8[12]	1101
LASSIFWDelftAssistX, HwNm_u8p8[15]	sstFWDefltAssistX_HwNm_u8p8[13]	1126
LassiFWDelftAssiatX, HwNm_u6p8[17]	sstFWDefltAssistX_HwNm_u8p8[14]	1152
LassiFWDelftAssiatX, HwNm_u6p8[17]	sstFWDefltAssistX_HwNm_u8p8[15]	1178
LassiFWDelftAssistX_HwNm_u8p8[17]   1259   1254   1254   1254   1254   1254   1254   1254   1256		
LassiFWDelftAssistX_HwNm_u8p8[18]   1280		
LassiFWDefitAssistY_Mrhm_s4p110    2458		
LASSIFWORTHASSISTY_MITNIM_selpt112  2662   LASSIFWORTHASSISTY_MITNIM_selpt112  2667   LASSIFWORTHASSISTY_MITNIM_selpt113  3972   LASSIFWORTHASSISTY_MITNIM_selpt116  3672   LASSIFWORTHASSISTY_MITNIM_selpt116  3686   LASSIFWORTHASSISTY_MITNIM_selpt116  3686   LASSIFWORTHASSISTY_MITNIM_selpt116  3686   LASSIFWORTHASSISTY_MITNIM_selpt116  3686   LASSIFWORTHASSISTY_MITNIM_selpt116  3686   LASSIFWORTHASSISTY_MITNIM_selpt116  4996   LASSIFWORTHASSISTY_MITNIM_selpt116  5996   LASSIFWORTHASSISTY_MITNIM_selpt116  5996   LASSIFWORTHASSISTY_MITNIM_selpt116  5996   LASSIFWORTHASSISTY_MITNIM_selpt116  5999   LASSIFWORTHASSISTY_MITNIM_SELPT16  59999   LASSIFWORTHASSISTY_MITNIM_SELPT16  599999   LASSIFWORTHASSISTY_MITNIM_SELPT16  5999999   LASSIFFWORTHASSISTY_MITNIM_SELPT16  5999999   LASSIFFWORTHASSISTY_MITNIM_SELPT16  5999999   LASSIFFWORTHASSISTY_MITNIM_SELPT16  59999999   LASSIFFWORTHASSISTY_MITNIM_SELPT16  59999999   LASSIFFWORTHASSISTY_MITNIM_SELPT16  59999999   LA		
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t_AsstFWVehSpd_Kph_u9p7[6] 2176  t_AsstFWVehSpd_Kph_u9p7[7] 2304  tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value 7.21999979  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value 0  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value 7.55000019  tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value 7.98999977  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value 5.30000019  tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value 1  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value 33.0999985  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgt tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgt tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HighFre	sstFWVehSpd_Kph_u9p7[4] 1	1920
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tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value  7.21999979  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value  7.55000019  tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value  7.98999977  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value  7.98999977  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value  7.53000019  tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value  1 33.0999985  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_AsstFirewallActive_Uls_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_leter.  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_leter.  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_leter.  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_leter.  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_leter.  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_leter.  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	sstFWVehSpd_Kph_u9p7[6] 2	2176
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value  7.21999979  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value  7.55000019  tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value  7.98999977  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value  7.98999977  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value  7.53000019  tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value  1 33.0999985  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_AsstFirewallActive_Uls_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_leter.  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_leter.  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_leter.  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_leter.  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_leter.  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_leter.  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	sstFWVehSpd_Kph_u9p7[7] 2	2304
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value  7.55000019  7.98999977  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value  7.53000019  tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value  1 33.0999985  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgt  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgt  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgt  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgt  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	, = , = , 1.3	
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value  7.55000019  7.98999977  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value  7.5000019  7.98999977  -5.30000019  1  1  33.099985  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value  1  33.099985  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_letgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AssistDirevall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_letgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value  7.98999977  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value  5.30000019  tgt_AssistFirewall_Per1_WEC_Counter_Cnt_enum.value  1 33.099985  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_itgt_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_Defeat_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_itgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_itgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value  -5.30000019  tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value  33.0999985  tgt_AssistFirewall_Per1_AsstFirewall_Per1_AsstFirewallActive_Uls_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value  1 33.099985  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	·	
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value  33.0999985  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall.Per1_Defeat_AsstTbl_Service_Cnt_lt  tgt_Rte_Inst_Ap_AssistFirewall.AssistFi		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32  tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32  tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32  tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32  tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lettgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lettgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32  tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32  tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	gt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgctgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tx	gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgctgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm f32	gt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
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tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32		•



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.17400026	6.17399979 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	9162	9162 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.10009766	3.10009766 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.88879967	5.88880014 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.38899994	5.38899994 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.72699976	7.72700024 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.10009766	3.10009766 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x00	0x00	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T .				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.108 (Repeat Count = 1)	v v v v v v v v v v v v v v v v v v v
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.4000001
AssistFirewall_ActiveKSV_M_str.K_UIs_f32	0.020999997
AssistFirewall_ActiveRawAcc_Cnt_M_u16	9963
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.69999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.20000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12399995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.80000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.239999995
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.19999981
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.34000004
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6
k_AsstFWInpLimitHFA_MtrNm_f32	6.53000021
k_AsstFWInpLimitHysComp_MtrNm_f32	8.02999973
k_AsstFWNstep_Cnt_u16	789
k_AsstFWPstep_Cnt_u16	3936
k_RestoreThresh_MtrNm_f32	5.55999994
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2 AsstFWUprBoundX HwNm s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144
	7777
	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096 -2048
	-4096 -2048 0



		(
Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-12288	
	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]		
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-12288	
	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]		
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096	
	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144	
	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]		
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048	
t2_Asst WoprBoundY_MtrNm_s4p11[6][1]	4096	
	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]		
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528	
t2_AsstrWUprBoundY_MtrNm_s4p11[7][0]	0	
	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144	



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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	819
t_AsstFWDefltAssistX_HwNm_u8p8[1]	845
t_AsstFWDefltAssistX_HwNm_u8p8[2]	870
t_AsstFWDefltAssistX_HwNm_u8p8[3]	896
t_AsstFWDefltAssistX_HwNm_u8p8[4]	922
t_AsstFWDefltAssistX_HwNm_u8p8[5]	947
t_AsstFWDefltAssistX_HwNm_u8p8[6]	973
t_AsstFWDefltAssistX_HwNm_u8p8[7]	998
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	1152 1178
t_AsstFWDefitAssistX_HwNm_u8p8[14] t_AsstFWDefitAssistX_HwNm_u8p8[15]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1229
t_AsstFWDefitAssistX_HwNm_u8p8[17]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1280
t AsstFWDefltAssistX HwNm u8p8[19]	1306
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	23962
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	24166
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	24371
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	24781
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	24986
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	25190
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	25395
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	25600
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	25805
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	26010
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	26214
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	26419
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	26829
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	27034
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	27238
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	27443
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	27648
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	27853
t_AsstFWPstepNstepThresh_Cnt_u16[0]	229
t_AsstFWPstepNstepThresh_Cnt_u16[1]	635
t_AsstFWVehSpd_Kph_u9p7[0]	4352 4480
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	4608
t_AsstFWVehSpd_Kph_u9p7[3]	4736
t AsstFWVehSpd Kph u9p7[4]	4864
t_AsstFWVehSpd_Kph_u9p7[5]	4992
t_AsstFWVehSpd_Kph_u9p7[6]	5120
t_AsstFWVehSpd_Kph_u9p7[7]	5248
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7.32999992
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.65999985
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8.10000038
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.31999969
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	40.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFi$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.2656002	6.2656002 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	9174	9174 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	8.67199993	8.67199993 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.97487545	4.97487497 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8.42559338	8.42559338 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>~</b>

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.109 (Repeat Count = 1)	·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.5
AssistFirewall ActiveKSV M str.K Uls f32	0.0219999999
AssistFirewall_ActiveRawAcc_Cnt_M_u16	10086
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.20999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.125
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.9000001
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.25
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.30000019
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.349999994
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	6.53999996
k_AsstFWInpLimitHysComp_MtrNm_f32	8.14000034
k_AsstFWNstep_Cnt_u16	900
k_AsstFWPstep_Cnt_u16	4059
k_RestoreThresh_MtrNm_f32	5.55999994
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstrWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
, , , , , , , , , , , , , , , , , , , ,	
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_Asst WopiBoundX_HwNm_s4p11[4][10] t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2 AsstFWUprBoundX HwNm s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstrWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2046
	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	
12_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	2048
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Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192	
	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]		
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-2048	
:2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	0	
	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]		
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-30720	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-28672	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-22528	
12_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240	
t2 AsstFWUprBoundY MtrNm s4p11[4][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]		
	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096	
t2 AsstFWUprBoundY MtrNm s4p11[5][6]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192	
t2 AsstFWUprBoundY MtrNm s4p11[5][8]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	6144	
	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	0132	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	22528
t_AsstFWDefltAssistX_HwNm_u8p8[0]	845
t_AsstFWDefltAssistX_HwNm_u8p8[1]	870
t_AsstFWDefltAssistX_HwNm_u8p8[2]	896
t_AsstFWDefltAssistX_HwNm_u8p8[3]	922
t_AsstFWDefltAssistX_HwNm_u8p8[4]	947
t_AsstFWDefltAssistX_HwNm_u8p8[5]	973
t_AsstFWDefltAssistX_HwNm_u8p8[6]	998
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1024
t_AsstFWDefitAssistX_HwNm_u8p8[8]	1050
	1075
t_AsstFWDefltAssistX_HwNm_u8p8[9]	
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1280
t_AsstFWDefitAssistX_HwNm_u8p8[18]	1306
	1331
t_AsstFWDefltAssistX_HwNm_u8p8[19]	
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	-203
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	-201
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	-199
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	-197
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	-195
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	-193
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	-190
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	-188
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	-186
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	-184
t_AsstFWDefitAssistY_MtrNm_s4p11[11]	-182
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	-180
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	-178
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	-176
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	-174
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	-172
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	-170
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	-168
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	-166
t_AsstFWPstepNstepThresh_Cnt_u16[0]	230
t AsstFWPstepNstepThresh Cnt u16[1]	639
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t_AsstFWVehSpd_Kph_u9p7[0]	7296
t_AsstFWVehSpd_Kph_u9p7[1]	7424
t_AsstFWVehSpd_Kph_u9p7[2]	7552
t_AsstFWVehSpd_Kph_u9p7[3]	7680
t_AsstFWVehSpd_Kph_u9p7[4]	7808
t_AsstFWVehSpd_Kph_u9p7[5]	7936
t_AsstFWVehSpd_Kph_u9p7[6]	8064
t_AsstFWVehSpd_Kph_u9p7[7]	8192
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7.44000006
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.76999998
·	8.21000004
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.43000031
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	47.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lg	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.35699987	6.35699987 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	639	639 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-0.0810546875	-0.0810546875 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	8.94580078	8.94579983 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.42500019	6.42500019 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.21848631	6.21848631 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-0.0810546875	-0.0810546875 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•

T .				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.110 (Repeat Count = 1)	van de la company de la co
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.5999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.023
AssistFirewall_ActiveRawAcc_Cnt_M_u16	10209
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.900001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.219999999
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12600005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.25999999
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.400001
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.360000014
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6.19999981
k_AsstFWInpLimitHFA_MtrNm_f32	6.55000019
k_AsstFWInpLimitHysComp_MtrNm_f32	8.25
k_AsstFWNstep_Cnt_u16	1011
k_AsstFWPstep_Cnt_u16	4182
k_RestoreThresh_MtrNm_f32	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2 AsstFWUprBoundX HwNm s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2 AsstFWUprBoundX HwNm s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_frwnin_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240 8102
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	
t2_AsstFWUprBoundX_HwNm_s4p11[6][7] t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8] t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10] t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	
	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	6144



News	Invest Value
Name	Input Value 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8] t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-18432 -16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	10240



	(
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576
t_AsstFWDefltAssistX_HwNm_u8p8[0]	870
t_AsstFWDefltAssistX_HwNm_u8p8[1]	896
t_AsstFWDefltAssistX_HwNm_u8p8[2]	922
t_AsstFWDefltAssistX_HwNm_u8p8[3]	947
t_AsstFWDefltAssistX_HwNm_u8p8[4]	973
t_AsstFWDefltAssistX_HwNm_u8p8[5]	998
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	1203 1229
t_AsstFWDefitAssistX_HwNm_u8p8[14] t_AsstFWDefitAssistX_HwNm_u8p8[15]	1254
t_AsstFWDefitAssistX_HwNm_u8p8[16]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1357
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2458
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2662
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2867
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6144
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	6349
t_AsstFWPstepNstepThresh_Cnt_u16[0]	231
t_AsstFWPstepNstepThresh_Cnt_u16[1]	643
t_AsstFWVehSpd_Kph_u9p7[0]	10240 10368
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	10496
t_AsstFWVehSpd_Kph_u9p7[3]	10624
t AsstFWVehSpd Kph u9p7[4]	10752
t_AsstFWVehSpd_Kph_u9p7[5]	10880
t_AsstFWVehSpd_Kph_u9p7[6]	11008
t_AsstFWVehSpd_Kph_u9p7[7]	11136
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7.55000019
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.88000011
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8.31999969
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.53999996
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	54.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFi$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.44819975	6.44820023 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	643	643 ± 1	<b>~</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.10009766	3.10009766 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	9.22200012	9.22200012 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.22000027	6.21999979 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>~</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.29113674	6.29113674 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.10009766	3.10009766 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>~</b>
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.111 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.6999981
AssistFirewall ActiveKSV M str.K Uls f32	0.0240000002
AssistFirewall_ActiveRawAcc_Cnt_M_u16	10332
AssistFirewall AsstReducedPerfSV Cnt M Iqc	1
AssistFirewall CombAsstSV MtrNm M f32	-7.69999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.230000004
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12699997
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.270000011
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.370000005
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6.30000019
k_AsstFWInpLimitHFA_MtrNm_f32	6.55999994
k_AsstFWInpLimitHysComp_MtrNm_f32	8.35999966
k_AsstFWNstep_Cnt_u16	1122
k_AsstFWPstep_Cnt_u16	4305
k_RestoreThresh_MtrNm_f32	8.80000019
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_Asst WopiBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10] t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	
	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstrWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
12_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144	
	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]		
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288	
t2_Asst WoprBoundY_MtrNm_s4p11[2][10]	-26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-12288	
	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192	
	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]		
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-28672	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-26624	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-24576	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	8192	
	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	12288	



2. Asarr Wijsche Sach Villens - schiff [17] 2. Asarr Wijsche Sach Villens - schiff [17] 3. Asarr Wijsche Sach Villens - schiff [17] 4. Asarr Wijsche Sach Villens - schiff [17] 4. Asarr Wijsche Sach Villens - schiff [17] 5. Asarr Wijsche Sach Villens - schiff [17] 6. Asarr Winsche Sach	Name	Input Value
	t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	
PLANSPLY  FRANCE   STATISTICS	t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	16384
2. Aces*PUNPERSONNER**   254171919   2075   2. Aces*PUNPERSONNER**   254171919   2025   2. Aces*PUNPERSONNER**   25417191   2025   2. Aces*PUNPERSON	t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	18432
2 AGENT PURITIONS (MATH)   154117101   20224	t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	20480
2 AGENT/VORHICAGENT, Harbon, Uspill)	t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	22528
Death Victor Assauck, Protein, Jugid 19   926	t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	24576
LaserWorkindossiX Hebm uppilg  977   AsserWorkindossiX Hebm uppilg  977   AsserWorkindossiX Hebm uppilg  978   AsserWorkindossiX Hebm uppilg  979   AsserWorkindossiX Hebm uppilg  979   AsserWorkindossiX Hebm uppilg  1000   Chassi WorkindossiX H	t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	26624
Lapst PVOORMoonED, Hohms, 20052]   975	t_AsstFWDefltAssistX_HwNm_u8p8[0]	896
Laser Worldwasser, Namou, applied   998	t_AsstFWDefltAssistX_HwNm_u8p8[1]	922
Classif Novellikasiski, Hwhsu (1998)   1024   1005   1005   1 Aces PW-Collikasiski, Hwhsu (1998)   1006   1 Aces PW-Collikasiski, Hwhsu (1998)   1006   10	t_AsstFWDefltAssistX_HwNm_u8p8[2]	947
Laser Workfasser, Newhor Legist   100		973
Lasar Worlshasari, Hwhm, upptig    1900		
LASSIT/WORTAGESIC   New Judge   101	· · · ·	
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LASET VOMARASSIX How to 1968 (1)		
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LaseFWDefiAssistX, HeVm. up98150   1306	· · ·	
LassFWDeftAcsistX, Hebnius sp8[19]   1306		
LassFWDelfacesitX, Herbin_usp8[17]   1331     LassFWDelfacesitX, Herbin_usp8[18]   1367     LassFWDelfacesitX, Herbin_usp8[19]   132     LassFWDelfacesitX, Herbin_usp8[19]   132     LassFWDelfacesitX, Mintro, scp11[1]   2867     LassFWDelfacesitX, Mintro, scp11[1]   3072     LassFWDelfacesitX, Mintro, scp11[3]   3072     LassFWDelfacesitX, Mintro, scp11[4]   3482     LassFWDelfacesitX, Mintro, scp11[6]   3886     LassFWDelfacesitX, Mintro, scp11[6]   3891     LassFWDelfacesitX, Mintro, scp11[6]   3991     LassFWDelfacesitX, Mintro, scp11[6]   4096     LassFWDelfacesitX, Mintro, scp11[6]   500     LassFW		
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LASSIFWDeftAssistY_Mrkm_s4p11(6)   3891	t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3482
LASSIFWDettNassistY_MinNm_s4p11 8	t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3686
LASSIFWDeftAssistY_Minns_sqh11 8	t_AsstFWDefltAssistY_MtrNm_s4p11[6]	3891
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t. AsstFWDefftAssistY_MtrNm_s4p11[18]         6349           t. AsstFWDeftBAssistY_MtrNm_s4p11[19]         6554           t. AsstFWPstepNstepThresh_Cnt_u16[0]         232           t. AsstFWPstepNstepThresh_Cnt_u16[1]         647           t. AsstFWVehSpd_Kph_u9p7[0]         13184           t. AsstFWbefpd_Kph_u9p7[1]         13312           t. AsstFWehSpd_Kph_u9p7[2]         13440           t. AsstFWehSpd_Kph_u9p7[3]         13568           t. AsstFWehSpd_Kph_u9p7[5]         13896           t. AsstFWehSpd_Kph_u9p7[6]         13852           t. AsstFWehSpd_Kph_u9p7[7]         14080           tt_AsstFirewall_Per1_BaseAssistCmd_MtrNm_f32_value         7.6599985           tgt_AssistFirewall_Per1_Befeat_AsstTbL_Service_Cnt_lgc_value         0           tgt_AssistFirewall_Per1_HybfreqAssist_MtrNm_f32_value         8.43000031           tgt_AssistFirewall_Per1_HybreresisComp_MtrNm_f32_value         8.64999962           tgt_AssistFirewall_Per1_HybreresisComp_MtrNm_f32_value         61.099985           tgt_AssistFirewall_Per1_WEC_Counter_Cnt_enum_value         2           tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum_value         2           tgt_Re_Inst_Ap_AssistFirewall_AssistFirewall_Per1_AsstFirewallAssistFirewall_Per1_BaseAssistCmd_MtrNm_f32         1gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32           tgt_Re_Inst_Ap_AssistFirewall_Assist		
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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.53919983	6.53919983 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	647	647 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.20019531	3.20019531 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	9.50060081	9.50059986 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.83901548	5.83901548 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.31500006	7.31500006 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.20019531	3.20019531 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>~</b>

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.112 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.80000019
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0250000004
AssistFirewall_ActiveRawAcc_Cnt_M_u16	10455
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.239999995
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12800002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.19999981
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.280000001
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.5999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.379999995
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6.400001
k_AsstFWInpLimitHFA_MtrNm_f32	6.57000017
k_AsstFWInpLimitHysComp_MtrNm_f32	8.47000027
k_AsstFWNstep_Cnt_u16	1233
k_AsstFWPstep_Cnt_u16	4428
k_RestoreThresh_MtrNm_f32	4.400001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-4096



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2 AsstFWUprBoundX HwNm s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	
	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	12288
	1.2200



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432
t2 AsstFWUprBoundY MtrNm s4p11[1][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	U



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	922
t_AsstFWDefltAssistX_HwNm_u8p8[1]	947
t_AsstFWDefltAssistX_HwNm_u8p8[2]	973
t_AsstFWDefltAssistX_HwNm_u8p8[3]	998
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	1254 1280
t_AsstFWDefitAssistX_HwNm_u8p8[14] t_AsstFWDefitAssistX_HwNm_u8p8[15]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1382
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1408
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2867
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6554
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	6758
t_AsstFWPstepNstepThresh_Cnt_u16[0]	233
t_AsstFWPstepNstepThresh_Cnt_u16[1]	651
t_AsstFWVehSpd_Kph_u9p7[0]	16128
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	16256 16384
t_AsstFWVehSpd_Kph_u9p7[3]	16512
t_AsstFWVehSpd_kph_u9p7[4]	16640
t_AsstFWVehSpd_Kph_u9p7[5]	16768
t_AsstFWVehSpd_Kph_u9p7[6]	16896
t_AsstFWVehSpd_Kph_u9p7[7]	17024
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7.76999998
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	8.10000038
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8.53999996
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.76000023
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	68.3000031
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFi$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.63000011	6.63000011 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	651	651 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.29980469	3.29980469 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	9.7816	9.7816 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.46399975	5.46400023 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8.13199997	8.13199997 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.29980469	3.29980469 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Τ				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.113 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.30000019
AssistFirewall ActiveKSV M str.K Uls f32	0.40000006
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11199999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.119999997
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.219999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.80000019
k_AsstFWInpLimitHFA_MtrNm_f32	6.40999985
k_AsstFWInpLimitHysComp_MtrNm_f32	6.71000004
k_AsstFWNstep_Cnt_u16	4052
k_AsstFWPstep_Cnt_u16	2460
k_RestoreThresh_MtrNm_f32	4.42999983
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2 AsstFWUprBoundX HwNm s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
	4096
t2 AsstFWUprBoundY MtrNm s4n11[0][2]	1000
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0
, , , , , , , , , , , , , , , , , , , ,	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
, , , , , , , , , , , , , , , , , , , ,	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240



Nama	Innut Value
Name t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	Input Value -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[/][4] t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	947
t_AsstFWDefltAssistX_HwNm_u8p8[1]	973
t_AsstFWDefltAssistX_HwNm_u8p8[2]	998
t_AsstFWDefltAssistX_HwNm_u8p8[3]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1382
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1408
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1434
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3072
t_AsstFWDefitAssistY_MtrNm_s4p11[1]	3277 3482
t_AsstFWDefltAssistY_MtrNm_s4p11[2] t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3686
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	3891
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6963
t_AsstFWPstepNstepThresh_Cnt_u16[0]	234
t_AsstFWPstepNstepThresh_Cnt_u16[1]	655
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
t_AsstFWVehSpd_Kph_u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.19999981
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	1 5 5000000
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.599999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.4000001 -5.5999999
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	-5.5999999 1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176.100006
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_AssirtIrewallActive_ois_132	tgt_AssistFirewall_Per1_AssistCmd_MtrNm_f32
tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	1
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32
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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.30000019	-5.30000019 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487	8487 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-16	-16 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-6.06399965	-6.06400013 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019	-5.30000019 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999	5.0999999 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-16	-16 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x00	0x00	•
NTC_Cnt_T_enum	0xC6	0xC6	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~

Τ				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	<b>✓</b>

Test Step 2.114 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.4000001
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.5
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8610
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	0
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.090000036
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11300004
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.4000001
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.129999995
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.230000004
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.9000001
k_AsstFWInpLimitHFA_MtrNm_f32	6.42000008
k_AsstFWInpLimitHysComp_MtrNm_f32	6.82000017
k_AsstFWNstep_Cnt_u16	4053
k_AsstFWPstep_Cnt_u16	2583
k_RestoreThresh_MtrNm_f32	4.44000006
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2 AsstFWUprBoundX HwNm s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-0144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	12288
	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	
t2 AcetEM/I IntRoundV MtrNm c4c44[0][7]	1639/
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7] t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384 18432



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096
	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480
	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-14336
	-14336 -12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240
	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240
	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
12 ASSII WODIDOUIIUT WIITINII SADTITTIIAT	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096



Name	Input Value		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144		
t_AsstFWDefltAssistX_HwNm_u8p8[0]	819		
t_AsstFWDefltAssistX_HwNm_u8p8[1]	845		
t_AsstFWDefltAssistX_HwNm_u8p8[2]	870		
t_AsstFWDefltAssistX_HwNm_u8p8[3]	896		
t_AsstFWDefltAssistX_HwNm_u8p8[4]	922		
t_AsstFWDefltAssistX_HwNm_u8p8[5]	947		
t AsstFWDefltAssistX HwNm u8p8[6]	973		
t_AsstFWDefltAssistX_HwNm_u8p8[7]	998		
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1024		
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1050		
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1075		
t_AsstFWDefitAssistX_HwNm_u8p8[11]	1101		
	1126		
t_AsstFWDefltAssistX_HwNm_u8p8[12] t AsstFWDefltAssistX HwNm u8p8[13]			
, ,	1152		
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1178		
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1203		
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1229		
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1254		
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1280		
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1306		
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3277		
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3482		
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3686		
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3891		
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096		
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4301		
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4506		
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4710		
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4915		
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5120		
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5325		
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5530		
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5734		
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5939		
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6144		
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6349		
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6554		
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6758		
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6963		
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7168		
t_AsstFWPstepNstepThresh_Cnt_u16[0]	235		
t_AsstFWPstepNstepThresh_Cnt_u16[1]	659		
t_AsstFWVehSpd_Kph_u9p7[0]	22016		
t_AsstFWVehSpd_Kph_u9p7[1]	22144		
t_AsstFWVehSpd_Kph_u9p7[2]	22272		
t_AsstFWVehSpd_Kph_u9p7[3]	22400		
t_AsstFWVehSpd_Kph_u9p7[4]	22528		
t_AsstFWVehSpd_Kph_u9p7[5]	22656		
t_AsstFWVehSpd_Kph_u9p7[6]	22784		
t_AsstFWVehSpd_Kph_u9p7[7]	22912		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.30000019		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.69999981		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.5		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.69999981		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	187.199997		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32			
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cn			
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32		
•		2	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	, , ,	<u>.</u>	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32		
Name	Actual Value Exped	cted Value	Resu



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveRawAcc_Cnt_M_u16	659	659 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.5	-3.5 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-6.28999996	-6.28999996 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.0880003	-5.08799982 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.19199991	-5.19199991 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-3.5	-3.5 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	<b>~</b>
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.115 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.5
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.600000024
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8733
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.100000001
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11399996
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.80000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.140000001
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.19999981
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.239999995
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5
k AsstFWInpLimitHFA MtrNm f32	6.42999983
k_AsstFWInpLimitHysComp_MtrNm_f32	6.92999983
k_AsstFWNstep_Cnt_u16	3053
k_AsstFWPstep_Cnt_u16	2706
k_RestoreThresh_MtrNm_f32	4.44999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240 -8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3] t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240 12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8] t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192 0
t2_AsstFWUprBoundX_HwNm_s4p11[6][0] t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144 -4006
t2_AsstFWUprBoundX_HwNm_s4p11[7][4] t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5] t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	20480



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240
	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-8192
	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	6144
t2 AsstFWUprBoundY MtrNm s4p11[5][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
12_/1001. 14 Opt Doung (_tall(18111_04p) [[/][4]	-1000



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] t_AsstFWDefitAssistX_HwNm_u8p8[0]	8192 870
t_AsstFWDefltAssistX_HwNm_u8p8[1]	896
t_AsstFWDefltAssistX_HwNm_u8p8[2]	922
t_AsstFWDefltAssistX_HwNm_u8p8[3]	947
t_AsstFWDefltAssistX_HwNm_u8p8[4]	973
t_AsstFWDefltAssistX_HwNm_u8p8[5]	998
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1229 1254
t_AsstFWDefltAssistX_HwNm_u8p8[15] t_AsstFWDefltAssistX_HwNm_u8p8[16]	1280
t_AsstFWDefitAssistX_HwNm_u8p8[17]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1357
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5734
t_AsstFWDefttAssistY_MtrNm_s4p11[12] t_AsstFWDefttAssistY_MtrNm_s4p11[13]	5939 6144
t_AsstFWDefitAssistY_MtrNm_s4p11[14]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7373
t_AsstFWPstepNstepThresh_Cnt_u16[0]	236
t_AsstFWPstepNstepThresh_Cnt_u16[1]	663
t_AsstFWVehSpd_Kph_u9p7[0]	24960
t_AsstFWVehSpd_Kph_u9p7[1]	25088
t_AsstFWVehSpd_Kph_u9p7[2]	25216
t_AsstFWVehSpd_Kph_u9p7[3]	25344
t_AsstFWVehSpd_Kph_u9p7[4]	25472
t_AsstFWVehSpd_Kph_u9p7[5]	25600
t_AsstFWVehSpd_Kph_u9p7[6]	25728
t_AsstFWVehSpd_Kph_u9p7[7] tqt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	25856 -5.4000001
tgt_AssistFirewall_Per1_BaseAssistCmd_witrium_132.value tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	-5.4000001 0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.67000008
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.5999999
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.67000008
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	198.300003
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32$	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32$	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFi$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-2.19999981	-2.20000005 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	663	663 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.60009766	-3.60009766 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-4.05000019	-4.05000019 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.6983614	4.6983614 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.44813251	-5.44813299 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-3.60009766	-3.60009766 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.116 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.5
AssistFirewall ActiveKSV M str.K Uls f32	0.0120000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8856
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.109999999
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11500001
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.900001
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.150000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.25
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	6.44000006
k_AsstFWInpLimitHysComp_MtrNm_f32	7.03999996
k_AsstFWNstep_Cnt_u16	2053
k_AsstFWPstep_Cnt_u16	2829
k_RestoreThresh_MtrNm_f32	4.46000004
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_Asst WopiboundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
	6144
IZ ASSLEWUDIBOUNGT MILININ S40 HOURDI	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240 12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240 12288



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0] t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-4096



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefltAssistX_HwNm_u8p8[0]	896
t_AsstFWDefltAssistX_HwNm_u8p8[1]	922
t_AsstFWDefltAssistX_HwNm_u8p8[2]	947
t_AsstFWDefltAssistX_HwNm_u8p8[3]	973
t_AsstFWDefltAssistX_HwNm_u8p8[4]	998
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	1229 1254
t_AsstFWDefitAssistX_HwNm_u8p8[14] t_AsstFWDefitAssistX_HwNm_u8p8[15]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1306
t_AsstFWDefitAssistX_HwNm_u8p8[17]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1382
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7578
t_AsstFWPstepNstepThresh_Cnt_u16[0]	237
t_AsstFWPstepNstepThresh_Cnt_u16[1]	667 27904
t_AsstFWVehSpd_Kph_u9p7[0]	
t_AsstFWVehSpd_Kph_u9p7[1]	28032 28160
t_AsstFWVehSpd_Kph_u9p7[2] t_AsstFWVehSpd_Kph_u9p7[3]	28288
t_AsstFWVehSpd_kph_u9p7[4]	28416
t_AsstFWVehSpd_Kph_u9p7[5]	28544
t_AsstFWVehSpd_Kph_u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7]	28800
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.5
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.11000013
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7.32999992
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	209.300003
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.43400002	5.43400002 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	667	667 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.70019531	3.70019531 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.24259996	-5.24259996 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.56500006	4.56500006 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.82499981	7.82499981 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.70019531	3.70019531 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Τ			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Name	est Step 2.117 (Repeat Count = 1)	
AssistFirewall_ActiveKSV_M_str, X_UIs_I32		Input Value
AssistFirewall ActiveKSV M_str. K_Uls_/32 AssistFirewall_ActiveRawAcc_Cnt_M_u16 AssistFirewall_AssistAeucedPfSV_Cnt_M_lge 0 AssistFirewall_AssistAeucedPfSV_Cnt_M_lge AssistFirewall_HireqKSV_M_str.LPF_Str.K_Uls_/32 AssistFirewall_HireqKSV_M_str.LPF_Str.K_Uls_/32 AssistFirewall_HireqKSV_M_str.LPF_Str.K_Uls_/32 AssistFirewall_LWBoundKSV_M_str.CF_Uls_/32 AssistFirewall_LwBoundKSV_M_str.CF_Uls_/32 AssistFirewall_LwBoundKSV_M_str.CF_Uls_/32 AssistFirewall_UwBoundKSV_M_str.CF_Uls_/32 AssistFirewall_UwBoundKSV_M_str.CF_Uls_/32 AssistFirewall_UwBoundKSV_M_str.CF_Uls_/32 AssistFirewall_UpBoundKSV_M_str.CF_Uls_/32 AssistFirewall_UpBoundKSV_M_str.CF_Uls_/32 AssistFirewall_UpBoundKSV_M_str.K_Uls_/32 AssistFirewall_UpBoundKSV_M_str.K_Uls_/32 AssistFirewall_UpBoundKSV_M_str.K_Uls_/32 AssistFirewall_UpBoundKSV_M_str.K_Uls_/32 AssistFirewall_UpBoundKSV_M_str.K_Uls_/32 AssistFirewall_UpBoundKSV_M_str.K_Uls_/32 AssistFirewall_UpBoundKSV_M_str.K_Uls_/32 AssistFirewall_UpBoundKSV_M_str.K_Uls_/32 AssistFirewall_UpBoundX_HwM_str/32 AssistFirewall_UpBoundX_HwM_str/32 AssistFirewall_UpBoundX_HwM_str/32 AssistFirewall_UpBoundX_HwM_str/32 AssistFirewall_UpBoundX_HwM_str/32 AssistFirewall_UpBoundX_HwM_str/34011[0][0] AssistFirewall_UpBoundX_HwM_str/34011[0][		·
AssistFirewall_AssiReducedPerfSV_CRI_M_1g0 0 AssistFirewall_AssiReducedPerfSV_CRI_M_1g0 0 AssistFirewall_AssiReducedPerfSV_CRI_M_1g2 7.19999981 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_132 -5.599999 AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_132 0.11999997 AssistFirewall_HiFreqKSV_M_str.CF_Uls_132 1.11600006 AssistFirewall_LwrBoundKSV_M_str.K_Uls_132 6 AssistFirewall_LwrBoundKSV_M_str.K_Uls_132 1.1060006 AssistFirewall_LwrBoundKSV_M_str.K_Uls_132 1.1060006 AssistFirewall_LwrBoundKSV_M_str.K_Uls_132 1.1060006 AssistFirewall_UprBoundKSV_M_str.K_Uls_132 1.1060006 AssistFirewall_UprBoundKSV_M_str.K_Uls_132 1.1060006 AssistFirewall_UprBoundKSV_M_str.K_Uls_132 1.1060006 AssistFirewall_UprBoundKSV_M_str.K_Uls_132 1.1060000000000000000000000000000000000		
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc         0           AssistFirewall_CombAsstSV_Mtrhm_M_J32         7.19999981           AssistFirewall_HiFreqKSV_M_str_LPF_Str_K_Uls_J32         -5.5999999           AssistFirewall_HiFreqKSV_M_str_LPF_Str_K_Uls_J32         0.119999997           AssistFirewall_HiFreqKSV_M_str_CF_Uls_J62         1.11600006           AssistFirewall_LwrBoundKSV_M_str_SV_Uls_J32         0.159999996           AssistFirewall_WrBoundKSV_M_str_SV_Uls_J32         0.159999991           AssistFirewall_UprBoundKSV_M_str_SV_Uls_J32         6.19999981           AssistFirewall_UprBoundKSV_M_str_SV_Uls_J32         0.25999999           Rte_Inst_Ap_AssistFirewall         tg_Re_Inst_Ap_AssistFirewall           k_AsstFWInpLimitHsA_mtrMm_f32         6.14999981           k_AsstFWInpLimitHsA_mtrMm_f32         6.44999981           k_AsstFWInpLimitHsA_mtrMm_f32         6.4999998           k_AsstFWInpLimitHsA_mtrMm_f32         4.46999998           k_AsstFWInpLimitHs_MtrMm_f32         4.46999979           k_AsstFWInpEoundX_HwNm_s4p11[0][0]         4.46999979           k_AsstFWUpRboundX_HwNm_s4p11[0][1]         4.096           k_AsstFWUpRboundX_HwNm_s4p11[0][1]         4.096           k_AsstFWUpRboundX_HwNm_s4p11[0][1]         4.096           k_AsstFWUpRboundX_HwNm_s4p11[0][6]         6144           k_Asst		8979
AssistFirewall_HiFreqKSV_M_str.UP_Str.SV_UIs_f32		
AssistFirewall_HiFreqKSV_M_str.CP_Us_f32 1.1160006 AssistFirewall_LHiFreqKSV_M_str.CP_Us_f32 1.1160006 AssistFirewall_LwrBoundKSV_M_str.XV_Uls_f32 6.15999996 AssistFirewall_PNCountStatus_Cnt_M_lgc 1.61999981 AssistFirewall_UprBoundKSV_M_str.K_Uls_f32 6.1999981 AssistFirewall_UprBoundKSV_M_str.K_Uls_f32 6.1999981 AssistFirewall_UprBoundKSV_M_str.K_Uls_f32 0.25999999 Rte_Inst_Ap_AssistFirewall typfBoundKSV_M_str.K_Uls_f32 0.25999999 Rte_Inst_Ap_AssistFirewall typfBoundKSV_M_str.K_Uls_f32 0.25999999 AssistFirewall_Ap_AssistFirewall typfBoundKSV_M_str.K_Uls_f32 0.25999999 Rte_Inst_Ap_AssistFirewall typfBoundKSV_M_str.K_Uls_f32 0.25999999 AssistFirewall_Ap_AssistFirewall typfBoundKSV_M_str.K_Uls_f32 0.25999999 AssistFiver_Ap_AssistFirewall typfBoundK_M_str.M_f32 0.44999981 AssistFiver_Ap_AssistFirewall typfBoundK_M_str.M_f32 0.44999981 AssistFiver_Ap_AssistFirewall 0.53 AssistFiver_A		
AssistFirewall_HiFreqKSV_M_str.CP_Us_f32 1.1160006 AssistFirewall_LHiFreqKSV_M_str.CP_Us_f32 1.1160006 AssistFirewall_LwrBoundKSV_M_str.XV_Uls_f32 6.15999996 AssistFirewall_PNCountStatus_Cnt_M_lgc 1.61999981 AssistFirewall_UprBoundKSV_M_str.K_Uls_f32 6.1999981 AssistFirewall_UprBoundKSV_M_str.K_Uls_f32 6.1999981 AssistFirewall_UprBoundKSV_M_str.K_Uls_f32 0.25999999 Rte_Inst_Ap_AssistFirewall typfBoundKSV_M_str.K_Uls_f32 0.25999999 Rte_Inst_Ap_AssistFirewall typfBoundKSV_M_str.K_Uls_f32 0.25999999 AssistFirewall_Ap_AssistFirewall typfBoundKSV_M_str.K_Uls_f32 0.25999999 Rte_Inst_Ap_AssistFirewall typfBoundKSV_M_str.K_Uls_f32 0.25999999 AssistFirewall_Ap_AssistFirewall typfBoundKSV_M_str.K_Uls_f32 0.25999999 AssistFiver_Ap_AssistFirewall typfBoundK_M_str.M_f32 0.44999981 AssistFiver_Ap_AssistFirewall typfBoundK_M_str.M_f32 0.44999981 AssistFiver_Ap_AssistFirewall 0.53 AssistFiver_A		-5.5999999
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32         1.11600006           AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32         6           AssistFirewall_PNCountStatus_Cnt_M_lgc         1           AssistFirewall_UprBoundKSV_M_str.K_Uls_f32         6.19999981           AssistFirewall_UprBoundKSV_M_str.K_Uls_f32         6.19999981           AssistFirewall_UprBoundKSV_M_str.K_Uls_f32         0.25999999           Rte_Inst_Ap_AssistFirewall         tg_Rte_Inst_Ap_AssistFirewall           k_AssifWinpLimitBaseAsst_MtrNm_f32         5.1999981           k_AssifWinpLimitHFA_MtrNm_f32         6.44999981           k_AssifWinpLimitHysComp_MtrNm_f32         7.1500001           k_AssifWinpSe_Cnt_u16         2952           k_AssifWupSep_Cnt_u16         2952           k_RestoreThresh_MtrNm_f32         4.46999979           2_AssifWupBoundX_HwNm_s4p11[0][1]         -6144           2_AssifWupBoundX_HwNm_s4p11[0][2]         -2048           2_AssifWupBoundX_HwNm_s4p11[0][3]         0           2_AssifWupBoundX_HwNm_s4p11[0][4]         2048           2_AssifWupBoundX_HwNm_s4p11[0][6]         6144           2_AssifWupBoundX_HwNm_s4p11[0][6]         6144           2_AssifWupBoundX_HwNm_s4p11[0][6]         6144           2_AssifWupBoundX_HwNm_s4p11[0][6]         6144           2_AssifWupBoundX_HwN	·	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32         0.159999996           AssistFirewall_PNCountStatus_Cnt_M_gc         1           AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32         6.1999981           AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32         0.25999999           Re_Inst_Ap_AssistFirewall         tgt_Ret_Inst_Ap_AssistFirewall           k_AssifWinpLimitBaseAsst_MtrNm_f32         5.19999981           k_AssifWinpLimitHy-MtrNm_f32         6.44999981           k_AssifWinpLimitHy-MtrNm_f32         7.1500001           k_AssifWinpLimitHy-Comp_MtrNm_f32         7.1500001           k_AssifWinpLimitHy-Comp_MtrNm_f32         4.6999979           k_AssifWinpLimitHy-Scomp_MtrNm_f32         4.6999979           k_RestoreThresh_MtrNm_f32         4.6999979           k_RestoreThresh_MtrNm_s4p11[0][0]         -6144           12_AssifWuprBoundX_HwNm_s4p11[0][1]         4096           12_AssifWuprBoundX_HwNm_s4p11[0][2]         2048           12_AssifWuprBoundX_HwNm_s4p11[0][3]         0           12_AssifWuprBoundX_HwNm_s4p11[0][6]         4096           12_AssifWuprBoundX_HwNm_s4p11[0][6]         4096           12_AssifWuprBoundX_HwNm_s4p11[0][6]         4096           12_AssifWuprBoundX_HwNm_s4p11[0][7]         8192           12_AssifWuprBoundX_HwNm_s4p11[0][9]         10240	·	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32         0.159999996           AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32         6.1999981           AssistFirewall_UprBoundKSV_M_str.K_Uls_f32         0.25999999           Rte_Inst_Ap_AssistFirewall         tgt_Rte_Inst_Ap_AssistFirewall           k_AssiFWinpLimitBaseAsst_MtrNm_f32         5.19999981           k_AssiFWinpLimitHFA_MtrNm_f32         6.44999981           k_AssiFWinpLimitHFA_MtrNm_f32         7.1500001           k_AssiFWstep_Cnt_u16         1053           k_AssiFWpstep_Cnt_u16         2952           k_RestoreThresh_MtrNm_f32         4.46999979           12_AssiFWUprBoundX_HwNm_s4p11[0][0]         6144           12_AssiFWUprBoundX_HwNm_s4p11[0][1]         4096           12_AssiFWUprBoundX_HwNm_s4p11[0][2]         2048           12_AssiFWUprBoundX_HwNm_s4p11[0][3]         0           12_AssiFWUprBoundX_HwNm_s4p11[0][4]         2048           12_AssiFWUprBoundX_HwNm_s4p11[0][6]         6144           12_AssiFWUprBoundX_HwNm_s4p11[0][6]         6144           12_AssiFWUprBoundX_HwNm_s4p11[0][6]         6144           12_AssiFWUprBoundX_HwNm_s4p11[0][6]         6144           12_AssiFWUprBoundX_HwNm_s4p11[0][6]         6144           12_AssiFWUprBoundX_HwNm_s4p11[0][6]         6144           12_AssiFWUprBoundX_HwNm_		
AssistFirewall_PNCountStatus_Cnt_M_lgc 1 AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 6.19999981 AssistFirewall_UprBoundKSV_M_str.K_Uls_f32 0.25999999 Rte_Inst_Ap_AssistFirewall tgt_Rte_Inst_Ap_AssistFirewall k_AssifWnpLimitBaseAsst_MtrNm_f32 5.1999981 k_AssifWnpLimitHFA_MtrNm_f32 6.4499981 k_AssifWnpLimitHFA_MtrNm_f32 7.1500001 k_AssifWnstep_Cnt_uf6 1053 k_AssifWnstep_Cnt_uf6 2952 k_RestoreThresh_MtrNm_f32 4.46999979 12_AssifWuprBoundX_HwNm_s4p11[0][0] 6144 12_AssifWuprBoundX_HwNm_s4p11[0][1] 4096 12_AssifWuprBoundX_HwNm_s4p11[0][2] 2048 12_AssifWUprBoundX_HwNm_s4p11[0][3] 0 12_AssifWUprBoundX_HwNm_s4p11[0][4] 2048 12_AssifWUprBoundX_HwNm_s4p11[0][4] 2048 12_AssifWUprBoundX_HwNm_s4p11[0][6] 6144 12_AssifWUprBoundX_HwNm_s4p11[0][6] 6144 12_AssifFWUprBoundX_HwNm_s4p11[0][6] 614		
AssistFirewall_UprBoundKSV_M_str.KV_Uls_f32		1
AssistFirewall_UprBoundKSV_M_str.K_Uls_132       0.25999999         Rte_Inst_Ap_AssistFirewall       tgt_Rte_Inst_Ap_AssistFirewall         k_AsstFWInpLimitBaseAsst_MtrNm_132       5.19999981         k_AsstFWInpLimitHysComp_MtrNm_132       6.4499981         k_AsstFWInpLimitHysComp_MtrNm_132       7.1500001         k_AsstFWPstep_Cnt_u16       2952         k_AsstFWpstep_Cnt_u16       2952         k_RestoreThresh_MtrNm_132       4.46999979         t2_AsstFWUprBoundX_HwNm_s4p11[0][0]       -6144         t2_AsstFWUprBoundX_HwNm_s4p11[0][1]       4096         t2_AsstFWUprBoundX_HwNm_s4p11[0][2]       2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][4]       2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][6]       4096         t2_AsstFWUprBoundX_HwNm_s4p11[0][6]       6144         t2_AsstFWUprBoundX_HwNm_s4p11[0][7]       8192         t2_AsstFWUprBoundX_HwNm_s4p11[0][8]       10240         t2_AsstFWUprBoundX_HwNm_s4p11[0][9]       12288         t2_AsstFWUprBoundX_HwNm_s4p11[0][10]       14336         t2_AsstFWUprBoundX_HwNm_s4p11[0][10]       14336         t2_AsstFWUprBoundX_HwNm_s4p11[0][10]       14336         t2_AsstFWUprBoundX_HwNm_s4p11[0][10]       14336	·	6.19999981
Rte_Inst_Ap_AssistFirewall         tgt_Rte_Inst_Ap_AssistFirewall           k_AsstFWInpLimitBaseAsst_MtrNm_f32         5.1999981           k_AsstFWInpLimitHFA_MtrNm_f32         6.4499981           k_AsstFWNstep_Cnt_u16         1053           k_AsstFWPstep_Cnt_u16         2952           k_RestoreThresh_MtrNm_f32         4.46999979           t_PastFWUprBoundX_HwNm_s4p11[0][0]         -6144           t_PastFWUprBoundX_HwNm_s4p11[0][1]         4096           t_PastFWUprBoundX_HwNm_s4p11[0][2]         -2048           t_PastFWUprBoundX_HwNm_s4p11[0][3]         0           t_PastFWUprBoundX_HwNm_s4p11[0][6]         4096           t_PastFWUprBoundX_HwNm_s4p11[0][6]         4096           t_PastFWUprBoundX_HwNm_s4p11[0][6]         4096           t_PastFWUprBoundX_HwNm_s4p11[0][6]         4096           t_PastFWUprBoundX_HwNm_s4p11[0][6]         4096           t_PastFWUprBoundX_HwNm_s4p11[0][6]         4096           t_PastFWUprBoundX_HwNm_s4p11[0][6]         6144           t_PastFWUprBoundX_HwNm_s4p11[0][7]         8192           t_PastFWUprBoundX_HwNm_s4p11[0][8]         10240           t_PastFWUprBoundX_HwNm_s4p11[0][9]         12288           t_PastFWUprBoundX_HwNm_s4p11[0][10]         14336           t_PastFWUprBoundX_HwNm_s4p11[0][10]         4096	·	0.25999999
k_AsstFWInpLimitHFA_MtrNm_f32       6.44999981         k_AsstFWInpLimitHysComp_MtrNm_f32       7.1500001         k_AsstFWNstep_Cnt_u16       1053         k_AsstFWPstep_Cnt_u16       2952         k_RestoreThresh_MtrNm_f32       4.46999979         t2_AsstFWUprBoundX_HwNm_s4p11[0][0]       -6144         t2_AsstFWUprBoundX_HwNm_s4p11[0][1]       -4096         t2_AsstFWUprBoundX_HwNm_s4p11[0][2]       -2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][4]       2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][5]       4096         t2_AsstFWUprBoundX_HwNm_s4p11[0][6]       4096         t2_AsstFWUprBoundX_HwNm_s4p11[0][6]       6144         t2_AsstFWUprBoundX_HwNm_s4p11[0][6]       6144         t2_AsstFWUprBoundX_HwNm_s4p11[0][7]       8192         t2_AsstFWUprBoundX_HwNm_s4p11[0][8]       10240         t2_AsstFWUprBoundX_HwNm_s4p11[0][9]       12288         t2_AsstFWUprBoundX_HwNm_s4p11[0][10]       14336         t2_AsstFWUprBoundX_HwNm_s4p11[0][10]       14336         t2_AsstFWUprBoundX_HwNm_s4p11[0][10]       -2048	·	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitHysComp_MtrNm_f32       7.1500001         k_AsstFWNstep_Cnt_u16       1053         k_AsstFWPstep_Cnt_u16       2952         k_RestoreThresh_MtrNm_f32       4.46999979         t2_AsstFWUprBoundX_HwNm_s4p11[0][0]       -6144         t2_AsstFWUprBoundX_HwNm_s4p11[0][1]       -4096         t2_AsstFWUprBoundX_HwNm_s4p11[0][2]       -2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][4]       2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][5]       4096         t2_AsstFWUprBoundX_HwNm_s4p11[0][6]       6144         t2_AsstFWUprBoundX_HwNm_s4p11[0][7]       8192         t2_AsstFWUprBoundX_HwNm_s4p11[0][8]       10240         t2_AsstFWUprBoundX_HwNm_s4p11[0][9]       12288         t2_AsstFWUprBoundX_HwNm_s4p11[0][10]       14336         t2_AsstFWUprBoundX_HwNm_s4p11[0][10]       14336         t2_AsstFWUprBoundX_HwNm_s4p11[0][10]       -2048	AsstFWInpLimitBaseAsst_MtrNm_f32	5.19999981
k_AsstFWNstep_Cnt_u16       1053         k_AsstFWPstep_Cnt_u16       2952         k_RestoreThresh_MtrNm_f32       4.46999979         t2_AsstFWUprBoundX_HwNm_s4p11[0][0]       -6144         t2_AsstFWUprBoundX_HwNm_s4p11[0][1]       -4096         t2_AsstFWUprBoundX_HwNm_s4p11[0][2]       -2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][3]       0         t2_AsstFWUprBoundX_HwNm_s4p11[0][4]       2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][5]       4096         t2_AsstFWUprBoundX_HwNm_s4p11[0][6]       6144         t2_AsstFWUprBoundX_HwNm_s4p11[0][7]       8192         t2_AsstFWUprBoundX_HwNm_s4p11[0][8]       10240         t2_AsstFWUprBoundX_HwNm_s4p11[0][9]       12288         t2_AsstFWUprBoundX_HwNm_s4p11[0][10]       14336         t2_AsstFWUprBoundX_HwNm_s4p11[1][0]       -2048	AsstFWInpLimitHFA_MtrNm_f32	6.44999981
k_AsstFWNstep_Cnt_u16       1053         k_AsstFWPstep_Cnt_u16       2952         k_RestoreThresh_MtrNm_f32       4.46999979         t2_AsstFWUprBoundX_HwNm_s4p11[0][0]       -6144         t2_AsstFWUprBoundX_HwNm_s4p11[0][1]       -4096         t2_AsstFWUprBoundX_HwNm_s4p11[0][2]       -2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][3]       0         t2_AsstFWUprBoundX_HwNm_s4p11[0][4]       2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][5]       4096         t2_AsstFWUprBoundX_HwNm_s4p11[0][6]       6144         t2_AsstFWUprBoundX_HwNm_s4p11[0][7]       8192         t2_AsstFWUprBoundX_HwNm_s4p11[0][8]       10240         t2_AsstFWUprBoundX_HwNm_s4p11[0][9]       12288         t2_AsstFWUprBoundX_HwNm_s4p11[0][10]       14336         t2_AsstFWUprBoundX_HwNm_s4p11[1][0]       -2048	AsstFWInpLimitHysComp MtrNm f32	7.1500001
k_AsstFWPstep_Cnt_u16       2952         k_RestoreThresh_MtrNm_f32       4.46999979         t2_AsstFWUprBoundX_HwNm_s4p11[0][0]       -6144         t2_AsstFWUprBoundX_HwNm_s4p11[0][1]       -4096         t2_AsstFWUprBoundX_HwNm_s4p11[0][2]       -2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][3]       0         t2_AsstFWUprBoundX_HwNm_s4p11[0][4]       2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][5]       4096         t2_AsstFWUprBoundX_HwNm_s4p11[0][6]       6144         t2_AsstFWUprBoundX_HwNm_s4p11[0][7]       8192         t2_AsstFWUprBoundX_HwNm_s4p11[0][8]       10240         t2_AsstFWUprBoundX_HwNm_s4p11[0][9]       12288         t2_AsstFWUprBoundX_HwNm_s4p11[0][10]       14336         t2_AsstFWUprBoundX_HwNm_s4p11[1][0]       -2048		1053
k_RestoreThresh_MtrNm_f32       4.46999979         t2_AsstFWUprBoundX_HwNm_s4p11[0][0]       -6144         t2_AsstFWUprBoundX_HwNm_s4p11[0][1]       -4096         t2_AsstFWUprBoundX_HwNm_s4p11[0][2]       -2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][3]       0         t2_AsstFWUprBoundX_HwNm_s4p11[0][4]       2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][5]       4096         t2_AsstFWUprBoundX_HwNm_s4p11[0][6]       6144         t2_AsstFWUprBoundX_HwNm_s4p11[0][7]       8192         t2_AsstFWUprBoundX_HwNm_s4p11[0][8]       10240         t2_AsstFWUprBoundX_HwNm_s4p11[0][9]       12288         t2_AsstFWUprBoundX_HwNm_s4p11[0][10]       14336         t2_AsstFWUprBoundX_HwNm_s4p11[1][0]       -2048	·	2952
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]       -4096         t2_AsstFWUprBoundX_HwNm_s4p11[0][2]       -2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][3]       0         t2_AsstFWUprBoundX_HwNm_s4p11[0][4]       2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][5]       4096         t2_AsstFWUprBoundX_HwNm_s4p11[0][6]       6144         t2_AsstFWUprBoundX_HwNm_s4p11[0][7]       8192         t2_AsstFWUprBoundX_HwNm_s4p11[0][8]       10240         t2_AsstFWUprBoundX_HwNm_s4p11[0][9]       12288         t2_AsstFWUprBoundX_HwNm_s4p11[0][10]       14336         t2_AsstFWUprBoundX_HwNm_s4p11[1][0]       -2048	·	4.46999979
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]       -4096         t2_AsstFWUprBoundX_HwNm_s4p11[0][2]       -2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][3]       0         t2_AsstFWUprBoundX_HwNm_s4p11[0][4]       2048         t2_AsstFWUprBoundX_HwNm_s4p11[0][5]       4096         t2_AsstFWUprBoundX_HwNm_s4p11[0][6]       6144         t2_AsstFWUprBoundX_HwNm_s4p11[0][7]       8192         t2_AsstFWUprBoundX_HwNm_s4p11[0][8]       10240         t2_AsstFWUprBoundX_HwNm_s4p11[0][9]       12288         t2_AsstFWUprBoundX_HwNm_s4p11[0][10]       14336         t2_AsstFWUprBoundX_HwNm_s4p11[1][0]       -2048	AsstFWUprBoundX HwNm s4p11[0][0]	-6144
12_AsstFWUprBoundX_HwNm_s4p11[0][2]       -2048         12_AsstFWUprBoundX_HwNm_s4p11[0][3]       0         12_AsstFWUprBoundX_HwNm_s4p11[0][4]       2048         12_AsstFWUprBoundX_HwNm_s4p11[0][5]       4096         12_AsstFWUprBoundX_HwNm_s4p11[0][6]       6144         12_AsstFWUprBoundX_HwNm_s4p11[0][7]       8192         12_AsstFWUprBoundX_HwNm_s4p11[0][8]       10240         12_AsstFWUprBoundX_HwNm_s4p11[0][9]       12288         12_AsstFWUprBoundX_HwNm_s4p11[0][10]       14336         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       -2048		-4096
12 AsstFWUprBoundX_HwNm_s4p11[0][4]       2048         12 AsstFWUprBoundX_HwNm_s4p11[0][5]       4096         12 AsstFWUprBoundX_HwNm_s4p11[0][6]       6144         12 AsstFWUprBoundX_HwNm_s4p11[0][7]       8192         12 AsstFWUprBoundX_HwNm_s4p11[0][8]       10240         12 AsstFWUprBoundX_HwNm_s4p11[0][9]       12288         12 AsstFWUprBoundX_HwNm_s4p11[0][10]       14336         12 AsstFWUprBoundX_HwNm_s4p11[1][0]       -2048		-2048
12_AsstFWUprBoundX_HwNm_s4p11[0][5]       4096         12_AsstFWUprBoundX_HwNm_s4p11[0][6]       6144         12_AsstFWUprBoundX_HwNm_s4p11[0][7]       8192         12_AsstFWUprBoundX_HwNm_s4p11[0][8]       10240         12_AsstFWUprBoundX_HwNm_s4p11[0][9]       12288         12_AsstFWUprBoundX_HwNm_s4p11[0][10]       14336         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       -2048	_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
12 AsstFWUprBoundX_HwNm_s4p11[0][6]       6144         12 AsstFWUprBoundX_HwNm_s4p11[0][7]       8192         12 AsstFWUprBoundX_HwNm_s4p11[0][8]       10240         12 AsstFWUprBoundX_HwNm_s4p11[0][9]       12288         12 AsstFWUprBoundX_HwNm_s4p11[0][10]       14336         12 AsstFWUprBoundX_HwNm_s4p11[1][0]       -2048	_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
12_AsstFWUprBoundX_HwNm_s4p11[0][7]       8192         12_AsstFWUprBoundX_HwNm_s4p11[0][8]       10240         12_AsstFWUprBoundX_HwNm_s4p11[0][9]       12288         12_AsstFWUprBoundX_HwNm_s4p11[0][10]       14336         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       -2048		4096
12_AsstFWUprBoundX_HwNm_s4p11[0][8]     10240       12_AsstFWUprBoundX_HwNm_s4p11[0][9]     12288       12_AsstFWUprBoundX_HwNm_s4p11[0][10]     14336       12_AsstFWUprBoundX_HwNm_s4p11[1][0]     -2048	_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
12_AsstFWUprBoundX_HwNm_s4p11[0][8]     10240       12_AsstFWUprBoundX_HwNm_s4p11[0][9]     12288       12_AsstFWUprBoundX_HwNm_s4p11[0][10]     14336       12_AsstFWUprBoundX_HwNm_s4p11[1][0]     -2048		8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]		10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0] -2048	AsstFWUprBoundX HwNm s4p11[0][9]	12288
	_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
42. ApatEM In Page 24 V. Livilia adot45(4)(4)	_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
IZ_ASSIF W UPI DOUNDA_ MWNM_S4P T1 [1    1    1    1    1    1    1	_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
12_AsstFWUprBoundX_HwNm_s4p11[1][2] 2048	_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
12_AsstFWUprBoundX_HwNm_s4p11[1][3] 4096		4096
12_AsstFWUprBoundX_HwNm_s4p11[1][4] 6144		6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5] 8192		8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6] 10240		10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7] 12288	_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
12_AsstFWUprBoundX_HwNm_s4p11[1][8] 14336		14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9] 16384	_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10] 18432	_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0] 0	_AsstFWUprBoundX_HwNm_s4p11[2][0]	0



Name	Input Value	
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192	
t2_Asst WopiBoundX_HwNm_s4p11[2][4]		
	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384	
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432	
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480	
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384	
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432	
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480	
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0	
	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]		
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384	
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336	
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288	
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240	
, , , , , , , , , , , , , , , , , , , ,		
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096	
12_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	8192	
:2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	22528	



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	28672	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144	
	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]		
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048	
	0	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]		
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048	
	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]		
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-28672	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048	
:2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2040	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]		
	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048	
= -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1		



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	922
t_AsstFWDefltAssistX_HwNm_u8p8[1]	947
t_AsstFWDefltAssistX_HwNm_u8p8[2]	973
t_AsstFWDefltAssistX_HwNm_u8p8[3]	998
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[9] t_AsstFWDefltAssistX_HwNm_u8p8[10]	1152 1178
	1203
t_AsstFWDefltAssistX_HwNm_u8p8[11] t_AsstFWDefltAssistX_HwNm_u8p8[12]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1280
t AsstFWDefitAssistX HwNm u8p8[15]	1306
t AsstFWDefltAssistX HwNm u8p8[16]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1382
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1408
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[17] t AsstFWDefltAssistY_MtrNm_s4p11[18]	7578
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	7782 7987
t_AsstFWPstepNstepThresh_Cnt_u16[0]	238
t AsstFWPstepNstepThresh Cnt u16[1]	671
t_AsstFWVehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1]	30976
t_AsstFWVehSpd_Kph_u9p7[2]	31104
t_AsstFWVehSpd_Kph_u9p7[3]	31232
t_AsstFWVehSpd_Kph_u9p7[4]	31360
t_AsstFWVehSpd_Kph_u9p7[5]	31488
t_AsstFWVehSpd_Kph_u9p7[6]	31616
t_AsstFWVehSpd_Kph_u9p7[7]	31744
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.5999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.19999981
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.21999979
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7.44000006
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	220.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_le	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.52719975	5.52720022 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	671	671 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	•
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.89990234	3.89990234 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.31799984	-5.31799984 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.4000001	4.4000001 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8.22799969	8.22799969 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.89990234	3.89990234 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	•
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T ·				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.118 (Repeat Count = 1)	van de la companya d
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-8.80000019
AssistFirewall ActiveKSV M str.K Uls f32	0.00125584798
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-52.7999992
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00125584798
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00062859
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-8.80000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00125584798
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-16
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00125584798
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	0
k_AsstFWInpLimitHFA_MtrNm_f32	0
k_AsstFWInpLimitHysComp_MtrNm_f32	0
k_AsstFWNstep_Cnt_u16	0
k_AsstFWPstep_Cnt_u16	0
k_RestoreThresh_MtrNm_f32	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-20480



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-20480
	-20480
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-32768



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-32768
	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-32768
	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-32768
	1 11
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-32768
:2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	
E 7.000 TT ODIDOUINT INITIALITY OF THE INITIALITY	
	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-32768
2_AsstFWUprBoundY_MtrNm_s4p11[6][0] 2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-32768 -32768
i2_AsstFWUprBoundY_MtrNm_s4p11[6][0] i2_AsstFWUprBoundY_MtrNm_s4p11[6][1] i2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-32768 -32768 -32768
i2_AsstFWUprBoundY_MtrNm_s4p11[6][0] i2_AsstFWUprBoundY_MtrNm_s4p11[6][1] i2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-32768 -32768
i2_AsstFWUprBoundY_MtrNm_s4p11[6][0] i2_AsstFWUprBoundY_MtrNm_s4p11[6][1] i2_AsstFWUprBoundY_MtrNm_s4p11[6][2] i2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-32768 -32768 -32768
i2_AsstFWUprBoundY_MtrNm_s4p11[6][0] i2_AsstFWUprBoundY_MtrNm_s4p11[6][1] i2_AsstFWUprBoundY_MtrNm_s4p11[6][2] i2_AsstFWUprBoundY_MtrNm_s4p11[6][3] i2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-32768 -32768 -32768 -32768
i2_AsstFWUprBoundY_MtrNm_s4p11[6][0] i2_AsstFWUprBoundY_MtrNm_s4p11[6][1] i2_AsstFWUprBoundY_MtrNm_s4p11[6][2] i2_AsstFWUprBoundY_MtrNm_s4p11[6][3] i2_AsstFWUprBoundY_MtrNm_s4p11[6][4] i2_AsstFWUprBoundY_MtrNm_s4p11[6][4] i2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-32768 -32768 -32768 -32768 -32768 -32768
12_AsstFWUprBoundY_MtrNm_s4p11[6][0] 12_AsstFWUprBoundY_MtrNm_s4p11[6][1] 12_AsstFWUprBoundY_MtrNm_s4p11[6][2] 12_AsstFWUprBoundY_MtrNm_s4p11[6][3] 12_AsstFWUprBoundY_MtrNm_s4p11[6][4] 12_AsstFWUprBoundY_MtrNm_s4p11[6][5] 12_AsstFWUprBoundY_MtrNm_s4p11[6][5] 12_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768
12_AsstFWUprBoundY_MtrNm_s4p11[6][0] 12_AsstFWUprBoundY_MtrNm_s4p11[6][1] 12_AsstFWUprBoundY_MtrNm_s4p11[6][2] 12_AsstFWUprBoundY_MtrNm_s4p11[6][3] 12_AsstFWUprBoundY_MtrNm_s4p11[6][4] 12_AsstFWUprBoundY_MtrNm_s4p11[6][5] 12_AsstFWUprBoundY_MtrNm_s4p11[6][6] 12_AsstFWUprBoundY_MtrNm_s4p11[6][6] 12_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768
12_AsstFWUprBoundY_MtrNm_s4p11[6][0] 12_AsstFWUprBoundY_MtrNm_s4p11[6][1] 12_AsstFWUprBoundY_MtrNm_s4p11[6][2] 12_AsstFWUprBoundY_MtrNm_s4p11[6][3] 12_AsstFWUprBoundY_MtrNm_s4p11[6][4] 12_AsstFWUprBoundY_MtrNm_s4p11[6][5] 12_AsstFWUprBoundY_MtrNm_s4p11[6][6] 12_AsstFWUprBoundY_MtrNm_s4p11[6][6] 12_AsstFWUprBoundY_MtrNm_s4p11[6][7] 12_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768
12_AsstFWUprBoundY_MtrNm_s4p11[6][0] 12_AsstFWUprBoundY_MtrNm_s4p11[6][1] 12_AsstFWUprBoundY_MtrNm_s4p11[6][2] 12_AsstFWUprBoundY_MtrNm_s4p11[6][3] 12_AsstFWUprBoundY_MtrNm_s4p11[6][4] 12_AsstFWUprBoundY_MtrNm_s4p11[6][5] 12_AsstFWUprBoundY_MtrNm_s4p11[6][6] 12_AsstFWUprBoundY_MtrNm_s4p11[6][7] 12_AsstFWUprBoundY_MtrNm_s4p11[6][7] 12_AsstFWUprBoundY_MtrNm_s4p11[6][8] 12_AsstFWUprBoundY_MtrNm_s4p11[6][8]	-32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	-32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	-32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	-32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768
12_AsstFWUprBoundY_MtrNm_s4p11[6][0] 12_AsstFWUprBoundY_MtrNm_s4p11[6][1] 12_AsstFWUprBoundY_MtrNm_s4p11[6][2] 12_AsstFWUprBoundY_MtrNm_s4p11[6][3] 12_AsstFWUprBoundY_MtrNm_s4p11[6][4] 12_AsstFWUprBoundY_MtrNm_s4p11[6][5] 12_AsstFWUprBoundY_MtrNm_s4p11[6][6] 12_AsstFWUprBoundY_MtrNm_s4p11[6][7] 12_AsstFWUprBoundY_MtrNm_s4p11[6][8] 12_AsstFWUprBoundY_MtrNm_s4p11[6][9] 12_AsstFWUprBoundY_MtrNm_s4p11[6][9] 12_AsstFWUprBoundY_MtrNm_s4p11[6][10] 12_AsstFWUprBoundY_MtrNm_s4p11[7][0] 12_AsstFWUprBoundY_MtrNm_s4p11[7][0] 12_AsstFWUprBoundY_MtrNm_s4p11[7][1] 12_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768 -32768



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tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
t_lt tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
Lij tgt_Assisti ilewaii_Feli_Deleat_Asstibi_Selvice_Crit_igc
tgt_Assist inewal_Fe1_beleat_assist_MtrNm_f32
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-8.78894901	-8.78894901 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0	0 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	•
AssistFirewall_CombAsstSV_MtrNm_M_f32	0.100097656	0.100097656 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-52.7336922	-52.7336922 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-8.76885509	-8.76885509 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-16	-16 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	0.100097656	0.100097656 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	•
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•

T ·				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.119 (Repeat Count = 1)	and the second of the second o
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8.80000019
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.715390444
AssistFirewall_ActiveRawAcc_Cnt_M_u16	65535
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	52.7999992
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.715390444
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	2.09537959
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8.80000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.715390444
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	15.9995003
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.715390444
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	8.80000019
k_AsstFWInpLimitHFA_MtrNm_f32	8.80000019
k_AsstFWInpLimitHysComp_MtrNm_f32	8.80000019
k_AsstFWNstep_Cnt_u16	5000
k_AsstFWPstep_Cnt_u16	5000
k_RestoreThresh_MtrNm_f32	8.80000019
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
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t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	20480
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t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	20480



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	20480
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	20480
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	20480
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	20480
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2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	20480
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	20480
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	20480
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t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	20480
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	20480
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t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	20480
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t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	20480
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t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	20480
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2_AsstFWUprBoundX_HwNm_s4p11[7][4]	20480
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t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	32767
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t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	32767



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	32767
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t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	32767
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t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	32767
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t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	32767 32767



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	32767
t_AsstFWDefltAssistX_HwNm_u8p8[0]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[1]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[2]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[3]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[4]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[5]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[6]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[7]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[8]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[9]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[10]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[11]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[12]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	2560 2560
t_AsstFWDefitAssistX_HwNm_u8p8[14] t AsstFWDefitAssistX HwNm_u8p8[15]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[16]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[17]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[18]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[19]	2560
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	32767
t_AsstFWPstepNstepThresh_Cnt_u16[0]	5000
t_AsstFWPstepNstepThresh_Cnt_u16[1]	5000
t_AsstFWVehSpd_Kph_u9p7[0]	65408
t_AsstFWVehSpd_Kph_u9p7[1]	65408 65408
t_AsstFWVehSpd_Kph_u9p7[2] t_AsstFWVehSpd_Kph_u9p7[3]	65408
t_AsstFWVehSpd_Kph_u9p7[4]	65408
t_AsstFWVehSpd_Kph_u9p7[5]	65408
t_AsstFWVehSpd_Kph_u9p7[6]	65408
t_AsstFWVehSpd_Kph_u9p7[7]	65408
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	8.80000019
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	1
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	8.80000019
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	10
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.80000019
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	255
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFirewal$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8.80000019	8.80000019 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	65535	65535 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	26.4000015	26.3999996 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	33.9136925	33.9136925 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8.80000019	8.80000019 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	15.9995003	15.9995003 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	26.4000015	26.3999996 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	<b>✓</b>

Τ			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~



Test Case 3: Path test



#### Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)
CPU Cycles:

TC3.1 6628.00 Cycles
TC3.2 6629.00 Cycles
TC3.3 6629.00 Cycles
TC3.4 6629.00 Cycles
TC3.5 6629.00 Cycles
TC3.6 6629.00 Cycles
TC3.7 6629.00 Cycles
TC3.8 6629.00 Cycles
TC3.9 6629.00 Cycles
TC3.10 6629.00 Cycles
TC3.11 6629.00 Cycles
TC3.11 6629.00 Cycles
TC3.12 6629.00 Cycles
TC3.13 6629.00 Cycles
TC3.14 6629.00 Cycles
TC3.15 6629.00 Cycles
TC3.16 6629.00 Cycles
TC3.17 6629.00 Cycles



#### **Description** Vector Description

```
TS3.1"((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HysteresisComp_MtrNm_T_f32)<=(-k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=True &&
     ((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((BaseAssistCmd_MtrNm_T_f32)<=(-k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32)>=( UprBoundFilt_MtrNm_T_f32))=True && DefltAsst_MtrNm_T_f32 =
   Productionino(et) =False && ((LowFreqInput_mitNmT___132)=( )prBoundarii_mitNmT___132)]=True && DelftAsstLookup_MtrNm_T_f32 * ((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32) = DelftAsstLookup_MtrNm_T_f32) | ((LowFreqInput_MtrNm_T_f32) | ((LowFreqInput_MtrNm_T_f32) | ((LowFreqInput_MtrNm_T_f32) = DelftAsstLookup_MtrNm_T_f32) | (LowFreqInput_MtrNm_T_f32) | (LowFreqInput_MtrNm_T_f32) | (LowFreqInput_MtrNm_T_f32) | ((AssistFirewall_ActiveRawAcc_Cnt_M_u16) = ((AssistFWPstepNstep_Cnt_T_str.Threshold) - ((AssistFirewall_ActiveRawAcc_Cnt_M_u16) = ((AssistF
(TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=True && (AsstFWActive_Uls_T_f32>1)=True"
TS3.2"((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=True && ((BaseAssistCmd_MtrNm_T_f32))=True && ((HighFreqAssist_MtrNm_T_f32))=(E_AsstFWInpLimitHFA_MtrNm_f32))=True && ((BaseAssistCmd_MtrNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32))=True && ((AssistFirewall_ActiveRawAcc_Cnt_M_u16)<((AsstFWPstepNstep_Cnt_T_str.Threshold)-(AsstFWPstepNstep_Cnt_T_str.Pstep)))=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16)=((AsstFWPstepNstepThresh_Cnt_u16[1])
=True && (((Abs_f32_m(SumInput_MtrNm_T_f32)-AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>1)=True && (AssistFirewall_CombAsstSV_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=True && ((HighFreqAssist_MtrNm_T_f32))=(k_AsstFWInpLimitHFA_MtrNm_f32))=True && ((BaseAssistCmd_MtrNm_T_f32)=True && ((HighFreqAssist_MtrNm_T_f32))=(k_AsstFWInpLimitHFA_MtrNm_f32))=True && ((BaseAssistCmd_MtrNm_T_f32)=True && ((HighFreqAssist_MtrNm_T_f32))=(k_AsstFWInpLimitHFA_MtrNm_f32))=True && ((BaseAssistCmd_MtrNm_T_f32)=True && ((HighFreqAssist_MtrNm_T_f32))=(k_AsstFWInpLimitHFA_MtrNm_f32))=True && ((BaseAssistCmd_MtrNm_T_f32)=True && ((BaseAssistCmd_MtrNm_T_f32
         (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=True &&
   ((High-freqAssist_MtrNm_ I_32)>= (K_AsstF-WinpLimitHrA_MtrNm_132))= ITue && ((BaseAssistCmd_MtrNm_ I_32)>= ITue && ((BaseAssistCmd_MtrNm_ I_32)>= ITue && ((DefeatAsstTblSvc_Cnt_T_gc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode))=True && ((LowFreqInput_MtrNm_T_f32)>= (UprBoundFilt_MtrNm_T_f32))=True &&DefitAsst_MtrNm_T_f32 = DefitAsstLookup_MtrNm_T_f32 * ((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=True && ((AssistFirewall_ActiveRawAcc_Cnt_M_u16) < ((AsstFWPstepNstep_Cnt_T_str.Threshold) - (AsstFWPstepNstep_Cnt_T_str.Pstep)))=True && ((AssistFirewall_ActiveRawAcc_Cnt_M_u16) < (AsstFWPstepNstepThresh_Cnt_u16[1]) = True && (((Abs_f32_m(SumInput_MtrNm_T_f32 - AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=true && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=True && (AssistFirewall_CndAsstSV_MtrNm_M_f32>8.8)=True && (Assi
     (RastFwicking Library Find of the SastFwing Library Li
     k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HighFreqAssist_MtrNm_T_f32))=(k_AsstFWInpLimitHFA_MtrNm_f32))=True && ((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((BaseAssistCmd_MtrNm_T_f32))=False && ((DefeatAsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum !=
k_AsstFWInpLimitBaseAsst_MtrNm_[32))=False && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32)=(UprBoundFilt_MtrNm_T_f32))=True && DefltAsst_Dokup_MtrNm_T_f32 ((Idoat32)Sign_f32_m(HwTorque_HwNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32) || (LowFreqInput_MtrNm_T_f32) || (LowFreqInput_MtrNm_T_f32) || (LowFreqInput_MtrNm_T_f32) || (LowFreqInput_MtrNm_T_f32) || (LowFreqInput_MtrNm_T_f32) \ \ \] UprBoundFilt_MtrNm_T_f32) |=True && ((AssistFirewall_ActiveRawAcc_Cnt_M_u16) < ((AsstFWPstepNstep_Cnt_T_str.Threshold) < (AsstFWPstepNstep_Cnt_T_str.Pstep)))=False && ((AssistFirewall_ActiveRawAcc_Cnt_M_u16) < (LowFreyIngut_MtrNm_M_f32) < LowFreyIngut_MtrNm_M_f32 < LowFreyIngut_MtrNm_M_f32) < LowFreyIngut_MtrNm_M_f32 < LowFreyIngut_MtrNm_f32 < LowFreyIng
 &&((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=True && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((HysteresisComp_MtrNm_T_f32)>=(-k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HysteresisComp_MtrNm_T_f32))=False && ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_T_f32))=False && ((HighFreqAssist_MtrNm_f32))=False && ((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32)>=( UprBoundFilt_MtrNm_T_f32))=True && DefitAsst_Okup_MtrNm_T_f32 * ((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32) <
 DetitAsstLookup_mtrnn__1_32 * ([noat32]sign_t32_m(hw1orque_hwnm_1_t32]) = True && ( (LowFreqinput_mtrnm_1_t32 * ((AssistFirewall_ActiveRawAcc_Cnt_M_u16) * ((AsstFWPstepNstep_Cnt_T_str.Threshold) * ((AsstFWPstepNstep_Cnt_u16[1] * ((AsstFWPstep_Cnt_u16[1] * ((AsstFWPstep_Cnt_u16[1] * ((AsstFWPstep_Cnt_u16[1] * ((AsstFWPstep_Cnt_u16[1] * ((AsstFWPstep_Cnt
       (Asstructive_Uls_T_f32<=0)=False"
TS3.6"((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=True &&
     ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=False && ((HighFreqAssist_MtrNm_T2))=False && ((HighFreqAssist_MtrNm_T32))=False && ((HighFreqAssist_MtrNm_T32))=False && ((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((DefeatAsstTblSvc_Cnt_T_lgc!=
     D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32)>=( UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=true && DefltAsst_MtrNm_T_f32 = DefltAsstLookup_MtrNm_T_f32 *
     UprBoundFilt_WitrNm_I_132)=true && DefitAsst_MtrNm_I_132 = DefitAsstLookup_MtrNm_I_132 \(((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32 < LwrBoundFilt_MtrNm_T_f32) || \((LowFreqInput_MtrNm_T_f32 > UprBoundFilt_MtrNm_T_f32) = True && ((AssistFirewall_ActiveRawAcc_Cnt_M_u16) < ((AsstFWPstepNstep_Cnt_T_str.Threshold) < ((AsstFWPstepNstep_Cnt_T_str.Pstep))) = True && ((AssistFirewall_ActiveRawAcc_Cnt_M_u16) < (AsstFWPstepNstepThresh_Cnt_u16[1]) = True && (((Abs_f32_m(SumInput_MtrNm_T_f32 - AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || \((TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc)) = True && (AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_CombAsstSV_MtrNm_M_f32) && (AssistFirew
         (AsstFWActive_Uls_T_f32>1)=True"
     TS3.7"(HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HysteresisComp_MtrNm_T_f32)<=(-k_AsstFWInpLimitHysComp_MtrNm_f32))=False ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=False && ((HighFreqAssist_MtrNm_T_f32)<=(-k_AsstFWInpLimitHFA_MtrNm_f32))=False
   ((High-freqAssist_MtrNm_I__132)<=(-k_Asstr-WinpLimitHFA_MtrNm_I32))=False  
&&((BaseAssistCmd_MtrNm_T_f32)>=(k_Asstr-WinpLimitHFA_MtrNm_I32))=True  
&& ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC)  
&& (MECCounter_Cnt_T_enum != ProductionMode))  
=False  
&& ((LowFreqInput_MtrNm_T_f32)>=( UprBoundFilt_MtrNm_T_f32))=False  
&& ((LowFreqInput_MtrNm_T_f32))=true  
&& DefltAsst_MtrNm_T_f32  
= DefltAsstLookup_MtrNm_T_f32  
* ((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=False  
&& ((LowFreqInput_MtrNm_T_f32 < LwrBoundFilt_MtrNm_T_f32) || (LowFreqInput_MtrNm_T_f32 > UprBoundFilt_MtrNm_T_f32) )=True
```



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&&((AssistFirewall_ActiveRawAcc_Cnt_M_u16)<((AsstFWPstepNstep_Cnt_T_str.Threshold)-(AsstFWPstepNstep_Cnt_T_str.Pstep)))=False &&
         (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[1])=False && (AssistFirewall_CombAsstSV_MtrNm_M_f32<=-8.8)=True&& (((Abs_f32_m(SumInput_MtrNm_T_f32 - AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) ||
       (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=True && (AsstFWActive_Uls_T_f32>1)=True"
 (AsstFWActive_Uls_T_f32>1)=True"
TS3.8"""((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HysteresisComp_MtrNm_T_f32)<=(-k_AsstFWInpLimitHysComp_MtrNm_T_f32))=False && ((HighFreqAssist_MtrNm_T_f32))=False && ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=False && ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=False && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32)>=( UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32)>=( UprBoundFilt_MtrNm_T_f32)=( UprBoundFilt_MtrNm_T_f32)=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32)=False && ((LowFreqInput_MtrNm_T_f32))=
     LwrBoundFilt_MtrNm_T_f32) ||

(LowFreqInput_MtrNm_T_f32 > UprBoundFilt_MtrNm_T_f32) )=FALSE

&&((AssistFirewall_ActiveRawAcc_Cnt_M_u16)>((AsstFWPstepNstep_Cnt_T_str.Nstep)=True && (AssistFirewall_ActiveRawAcc_Cnt_M_u16)
     &&((AssistFirewall_ActiveRawAcc_cnt_m_u1o)>((AsstFwPstepNstep_cnt_1_str.Nstep)=1fue && (AssistFirewall_ActiveRawAcc_cnt_m_u16)> = t_AsstFWPstepNstepThresh_Cnt_u16[0])=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32<=-8.8)=True&& (((Abs_f32_m(SumInput_MtrNm_T_f32 - AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32<=-8.8)=False && (AssistFirewall_CT_f32>1)=True*"
 "TS3.9"((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=True && ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=True && ((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((BaseAssistCmd_MtrNm_T_f32)<=(-k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((DefeatAsstTblSvc_Cnt_T_lgc!= D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32)>=( UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32)>=( UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32) = UprBoundFilt_MtrNm_T_f32) = UprBoundFilt_MtrNm_T_f32 = UprBoundFilt_MtrNm_T_f32) = UprBoundFilt_MtrNm_T_f32 = UprBoundFilt_MtrNm_T_f32) = True && ((AssistFirewall_ActiveRawAcc_Cnt_M_u16) > (AssistFirewall_ActiveRawAcc_Cnt_M_u16) > (AssistFirewall_ActiveRawAc
     &&(((Assistr-irewall_ActiveRawAcc_Cnt_M_u16)<((Assit-WPstepnstep_Cnt_1_str.Pstep)))=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16)>= t_AsstFWPstepnStep_Cnt_u16[1])=True && (AssistFirewall_CombAsstSV_MtrNm_u16])=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32<=-8.8)=True&& (((Abs_f32_m(SumInput_MtrNm_T_f32 - AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=True && (AssistFirewall_Comp_MtrNm_T_f32)=False && ((HysteresisComp_MtrNm_T_f32)>=(-
   UprBoundFilt_MtrNm_T_f32)=True && DeftHasst_MtrNm_T_f32 = DeftHasstLookup_MtrNm_T_f32 * ((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32 < LwrBoundFilt_MtrNm_T_f32) || ((LowFreqInput_MtrNm_T_f32 > UprBoundFilt_MtrNm_T_f32))=True && (((AssistFirewall_ActiveRawAcc_Cnt_M_u16)<(((AsstFWPstepNstep_Cnt_T_str.Threshold)-(AsstFWPstepNstep_Cnt_T_str.Pstep)))=True && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 > t_AsstFWPstepNstepThresh_Cnt_u16[1])=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 > t_AsstFWPstepNstepThresh_Cnt_u16[0])=True && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 > t_AsstFWPstepNstepThresh_Cnt_u16[0])=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32<) > k_RestoreThresh_MtrNm_T_f32 & AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_132) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32<-8.8)=False && (Assi
         (AsstFWActive_Uls_T_f32>1)=True
 (AsstFWActive_Uls_T_f32>1)=True"
TS3.11"((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=True &&
((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=True &&
((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=False && ((DefeatAsstTblSvc_Cnt_T_lgc !=
D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False &&
((LowFreqInput_MtrNm_T_f32)>=(LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32)=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrN
         >= t_AsstFWPstepNstepThresh_Cnt_u16[1] )=False && ( AssistFirewall_ActiveRawAcc_Cnt_M_u16 >
   Jerus Lassif Writerhaster Intestical Intertion (Assist Pirewall Active RawAcc_Cnt_M_u16 > t_Assif Writerhaster Direction (Assist Pirewall_Active RawAcc_Cnt_M_u16 > t_Assif Writerhaster Direction (Intertion (Assist Pirewall_Combass V_MtrNm_M_f32 <= -8.8) = True & (((Abs_f32_m(SumInput_MtrNm_T_f32 - Assist Pirewall_Combass V_MtrNm_M_f32) > k_Restore Thresh_MtrNm_f32) & (Assist Pirewall_Asst Reduced PerfSV_Cnt_M_lgc == TRUE)) || (TRUE == Assist Pirewall_PNCount Status_Cnt_M_lgc)) = True & (Assist Pirewall_Combass V_MtrNm_M_f32 <= -8.8) = False & (Assist Watrive_Uls_T_f32 <+ 0.8) = False & (Assist Watrive_Uls_T_f32 <= 0.9) = False & (Assist Watrive_Uls_T_f32 <= 0.9) = False & (Assist Watrive_Uls_T_f32 <= 0.9) = False & (Watrive_Uls_T_f32 <= 0.9)
   (Asstr-Wactive_Dis_1_is2*)=False && (Asstr-Wactive_Dis_1_is2*)=False && ((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_T_f32))=False && ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=True &&((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=True &&((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((LowFreqInput_MtrNm_T_f32)>=(LyrBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32)>=(LyrBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32)>=(LyrBoundFilt_MtrNm_T_f32)=False && ((LowFreqInput_MtrNm_T_f32)>=(LyrBoundFilt_MtrNm_T_f32)=False && ((LowFreqInput_MtrNm_T_f32)>=(LyrBoundFilt_MtrNm_T_f32)=False && ((LowFreqInput_MtrNm_T_f32)>=(LyrBoundFilt_MtrNm_T_f32)=False && ((LowFreqInput_MtrNm_T_f32)>=(LyrBoundFilt_MtrNm_T_f32)=False && ((LowFreqInput_MtrNm_T_f32)=False && ((LowFreqInput_MtrNm_T_f32)=Fa
     UprBoundFilt_MtrNm_T_f32))=True && DefitAsst_MtrNm_T_f32 = DefitAsstLookup_MtrNm_T_f32 * ((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32 < LwrBoundFilt_MtrNm_T_f32) || (LowFreqInput_MtrNm_T_f32 > UprBoundFilt_MtrNm_T_f32) )=False
(LowFreqInput_MtrNm_T_32 > UprBoundFilt_MtrNm_T_32))=False && ((AssistFirewall_ActiveRawAcc_Cnt_M_u16)<((AsstFWPstepNstep_Cnt_T_str.Threshold)-(AsstFWPstepNstep_Cnt_T_str.Pstep)))=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstep_Cnt_T_str.Threshold)-(AsstFWPstepNstep_Cnt_T_str.Pstep)))=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[1])=True && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[0])=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32<=-8.8)=True&& (((Ass_{32}_m(SumInput_MtrNm_T_f32 - AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32<=-8.8)=False && ((HighFreqAssist_MtrNm_T_f32))=False && ((HighFreqAssist_MtrNm_T_f32))=False && ((HighFreqAssist_MtrNm_T_f32))=False && ((Interface))=False && ((DefeatAsstTblSvc_Cnt_T_lgc!=D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum!= ProductionMode))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32)=-(-UprBoundFilt_MtrNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32) <=(-UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((L
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&&(AssisFirewall, ActiveRawAcc, Cott. M. u16)<(AssiFiVPstepNstep. Cnt. T. str. Threshold)-(AssiFiVPstepNstep. Cnt. T. str. Patep))=True && (AssisFirewall ActiveRawAcc, Cnt. M. u16)</td>
 >1. AssiFiVPstepNstepTresh. Cnt. u16(0) = True && (AssisFirewall CombAssiSV MtrNn. M. 132.2 = 8.8)=True&& ((Abs. 132 \_m(Suminput\_MtrNn. T. 132 - AssisFirewall CombAssiSV MtrNn. M. 132.2 ) & RestoreThresh. MtrNm. 132.9 & (AssisFirewall CombAssiSV MtrNn. M. 132.2 ) & RestoreThresh. MtrNm. 132.9 & (AssisFirewall CombAssiSV MtrNn. M. 132.2 - 8.8)=False && (AssisFirewall CombAssiSV MtrNn. M. 132.2 + 8.8)=False && (AssisFirewall CombAssiSV MtrNn. M. 132.2)=False && (AssisFirewall CombAssiSV MtrNn. MtrNn. 132.2)=False && (HighFireqAssist MtrNn. T. 132)=c(-k. AssiFWinpLimitHyScomp. MtrNn. T. 132)=c(-k. AssiFWinpLimitHyA. MtrNn. T. 132)=False && ((BaseAssistCmd\_MtrNn. T. 132)=c(-k. AssiFWinpLimitHyA. MtrNn. T. 132)=False && ((BaseAssistCmd\_MtrNn. T. 132)=c(-k. AssiFWinpLimitHyA. MtrNn. T. 132)=c(-k. AssiFWinpLimitHyA. MtrNn. T. 132)=c(-k. AssiFWinpLimitHyA. MtrNn. T. 132)=False && ((BaseAssistCmd\_MtrNn. T. 132)=False && ((BaseAssistCmd\_MtrNn. T. 132)=False && ((BaseAssistCmd\_MtrNn. T. 132)=False && ((BaseAssistComp\_MtrNn. T. 132)=False && (HighFireqAssist\_MtrNn. T. 132)=c(-k. AssiFWinpLimitHyA. MtrNn. T. 132)=False && (HighFireqAssist\_MtrNn. T. 132)=False && (HighFireqAssist\_MtrNn. T. 132)=c(-k. AssiFWinpLimitHyA. MtrNn. T. 132)=False && ((BaseAssistCodm\_MtrNn. T. 132)=False && ((BaseAssistCodm\_MtrNn. T. 132)=False && ((HighFireqAssist\_MtrNn. T. 132)=False && ((HighFireqAssist\_MtrNn. T. 132)=False && ((HighFireqAssist\_MtrNn. T. 132)=False && ((HighFireqAssist\_MtrNn. T. 132)=False && ((HighFireqAssist\_M

(LowFreqInput\_MtrNm\_T\_f32 > UprBoundFilt\_MtrNm\_T\_f32) )=True &&((AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16)<((AsstFWPstepNstep\_Cnt\_T\_str.Threshold)-(AsstFWPstepNstep\_Cnt\_T\_str.Pstep)))=True && (AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16 > t\_AsstFWPstepNstepThresh\_Cnt\_u16[1] )=False && (AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16 > t\_AsstFWPstepNstepNstepThresh\_Cnt\_u16[0] )=True &&(AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32<-8.8)=True&& ((Abs\_f32\_m(SumInput\_MtrNm\_T\_f32 - AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32) > k\_RestoreThresh\_MtrNm\_f32) && (AssistFirewall\_AsstReducedPerfSV\_Cnt\_M\_lgc == TRUE)) || (TRUE == AssistFirewall\_PNCountStatus\_Cnt\_M\_lgc))=True && (AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32<-8.8)=True && (AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32<-8.8)=True && (AsstFWActive\_Uls\_T\_f32>1)=False && (AsstFWActive\_Uls\_T\_f32<-0)=True "

Test Step 3.1 (Repeat Count = 1)	✓
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.090000036
AssistFirewall_ActiveRawAcc_Cnt_M_u16	109
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.89999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0700000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0099999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4
k_AsstFWInpLimitHFA_MtrNm_f32	2.5
k_AsstFWInpLimitHysComp_MtrNm_f32	3.78999996
k_AsstFWNstep_Cnt_u16	3928
k_AsstFWPstep_Cnt_u16	1107
k_RestoreThresh_MtrNm_f32	1.89999998
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-16384
=	
t2 AsstFWUprBoundY MtrNm s4p11[5][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-14336 -12288



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	26
t_AsstFWDefltAssistX_HwNm_u8p8[1]	51
t_AsstFWDefltAssistX_HwNm_u8p8[2]	77
t_AsstFWDefltAssistX_HwNm_u8p8[3]	102
t_AsstFWDefltAssistX_HwNm_u8p8[4]	128
t_AsstFWDefltAssistX_HwNm_u8p8[5]	154
t_AsstFWDefltAssistX_HwNm_u8p8[6]	179
t_AsstFWDefltAssistX_HwNm_u8p8[7]	205
t_AsstFWDefltAssistX_HwNm_u8p8[8]	230
t_AsstFWDefltAssistX_HwNm_u8p8[9]	256
t_AsstFWDefltAssistX_HwNm_u8p8[10]	282
t_AsstFWDefltAssistX_HwNm_u8p8[11]	307
t_AsstFWDefltAssistX_HwNm_u8p8[12]	333
	358
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	384
	410
t_AsstFWDefltAssistX_HwNm_u8p8[15]	
t_AsstFWDefltAssistX_HwNm_u8p8[16]	435
t_AsstFWDefltAssistX_HwNm_u8p8[17]	461
t_AsstFWDefltAssistX_HwNm_u8p8[18]	486
t_AsstFWDefltAssistX_HwNm_u8p8[19]	512
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-204
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	0
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	26624
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	28672
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	30720
	0
t_AsstFWPstepNstepThresh_Cnt_u16[0]	
t_AsstFWPstepNstepThresh_Cnt_u16[1]	0
t_AsstFWVehSpd_Kph_u9p7[0]	1408
t_AsstFWVehSpd_Kph_u9p7[1]	1536
t_AsstFWVehSpd_Kph_u9p7[2]	1664
t_AsstFWVehSpd_Kph_u9p7[3]	1792
t_AsstFWVehSpd_Kph_u9p7[4]	1920
t_AsstFWVehSpd_Kph_u9p7[5]	2048
t_AsstFWVehSpd_Kph_u9p7[6]	2176
t_AsstFWVehSpd_Kph_u9p7[7]	2304
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-8.80000019



Name	Input Value		
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt lgc.value			
tgt AssistFirewall Per1 HighFreqAssist MtrNm f32.value	5		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	9		
tgt AssistFirewall Per1 HysteresisComp MtrNm f32.value	1.10000002		
tgt AssistFirewall Per1 MEC Counter Cnt enum.value	0		
tgt AssistFirewall Per1 VehicleSpeed Kph f32.value	90		
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 AsstFirewallActive UIs f32	tgt AssistFirewall Per1 AsstFirewallActive U	Jls f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_Mtr	 :Nm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_Mt	rNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_le	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Ser	vice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mtrl	Nm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f	32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_Mt	rNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_	enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_	<u>f</u> 32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.82099986	2.8210001 ± 4.88E-04	~
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32 AssistFirewall_ActiveRawAcc_Cnt_M_u16	2.82099986 0	2.8210001 ± 4.88E-04 0 ± 1	<b>✓</b>
			<b>V</b>
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0	0 ± 1	\ \ \ \ \ \ \ \
AssistFirewall_ActiveRawAcc_Cnt_M_u16 AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0 ± 1 1	· · · · · · · · · · · · · · · · · · ·
AssistFirewall_ActiveRawAcc_Cnt_M_u16 AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall_CombAsstSV_MtrNm_M_f32	0 1 8.80000019	0 ± 1 1 8.80000019 ± 4.88E-04	*****
AssistFirewall_ActiveRawAcc_Cnt_M_u16 AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall_CombAsstSV_MtrNm_M_f32 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	0 1 8.80000019 1.9920001	0 ± 1 1 8.80000019 ± 4.88E-04 1.99199998 ± 4.88E-04	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
AssistFirewall_ActiveRawAcc_Cnt_M_u16 AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall_CombAsstSV_MtrNm_M_f32 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32 AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0 1 8.80000019 1.9920001 5.2329998	0 ± 1 1 8.80000019 ± 4.88E-04 1.99199998 ± 4.88E-04 5.2329998 ± 4.88E-04	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
AssistFirewall_ActiveRawAcc_Cnt_M_u16 AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall_CombAsstSV_MtrNm_M_132 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32 AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32 AssistFirewall_PNCountStatus_Cnt_M_lgc	0 1 8.80000019 1.9920001 5.2329998	0 ± 1 1 8.80000019 ± 4.88E-04 1.99199998 ± 4.88E-04 5.2329998 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16 AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall_CombAsstSV_MtrNm_M_f32 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32 AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32 AssistFirewall_PNCountStatus_Cnt_M_lgc AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	0 1 8.80000019 1.9920001 5.2329998 1 1.11900008	0 ± 1 1 8.80000019 ± 4.88E-04 1.99199998 ± 4.88E-04 5.2329998 ± 4.88E-04 1 1.11899996 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16 AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall_CombAsstSV_MtrNm_M_f32 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32 AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32 AssistFirewall_PNCountStatus_Cnt_M_lgc AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0 1 8.80000019 1.9920001 5.2329998 1 1.11900008	0 ± 1 1 8.80000019 ± 4.88E-04 1.99199998 ± 4.88E-04 5.2329998 ± 4.88E-04 1 1.11899996 ± 4.88E-04 1 ± 3.05E-05	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16 AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall_CombAsstSV_MtrNm_M_f32 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32 AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32 AssistFirewall_PNCountStatus_Cnt_M_lgc AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	0 1 8.80000019 1.9920001 5.2329998 1 1.11900008 1 8.80000019	0 ± 1 1 8.80000019 ± 4.88E-04 1.99199998 ± 4.88E-04 5.2329998 ± 4.88E-04 1 1.11899996 ± 4.88E-04 1 ± 3.05E-05 8.80000019 ± 9.77E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16 AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall_CombAsstSV_MtrNm_M_f32 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32 AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32 AssistFirewall_PNCountStatus_Cnt_M_lgc AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value NTC_Cnt_T_enum	0 1 8.80000019 1.9920001 5.2329998 1 1.11900008 1 8.80000019 0xC6	0 ± 1 1 8.80000019 ± 4.88E-04 1.99199998 ± 4.88E-04 5.2329998 ± 4.88E-04 1 1.11899996 ± 4.88E-04 1 ± 3.05E-05 8.80000019 ± 9.77E-04 0xC6	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16 AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall_CombAsstSV_MtrNm_M_f32 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32 AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32 AssistFirewall_PNCountStatus_Cnt_M_lgc AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value NTC_Cnt_T_enum Param_Cnt_T_u08	0 1 8.80000019 1.9920001 5.2329998 1 1.11900008 1 8.80000019 0xC6 0x01	0 ± 1 1 8.80000019 ± 4.88E-04 1.99199998 ± 4.88E-04 5.2329998 ± 4.88E-04 1 1.11899996 ± 4.88E-04 1 ± 3.05E-05 8.80000019 ± 9.77E-04 0xC6 0x01	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16 AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall_CombAsstSV_MtrNm_M_f32 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32 AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32 AssistFirewall_PNCountStatus_Cnt_M_lgc AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value NTC_Cnt_T_enum Param_Cnt_T_u08 Status_Cnt_T_enum	0 1 8.80000019 1.9920001 5.2329998 1 1.11900008 1 8.80000019 0xC6 0x01	0 ± 1 1 8.80000019 ± 4.88E-04 1.99199998 ± 4.88E-04 5.2329998 ± 4.88E-04 1 1.11899996 ± 4.88E-04 1 ± 3.05E-05 8.80000019 ± 9.77E-04 0xC6 0x01 0x01	~

$oldsymbol{ au}$			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	-

Test Step 3.2 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.039999991
AssistFirewall_ActiveRawAcc_Cnt_M_u16	6500
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.14999998
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.029999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.39999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0199999996
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0049999989
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3
k_AsstFWInpLimitHFA_MtrNm_f32	1.5
k_AsstFWInpLimitHysComp_MtrNm_f32	1.10000002
k_AsstFWNstep_Cnt_u16	4548
k_AsstFWPstep_Cnt_u16	492
k_RestoreThresh_MtrNm_f32	1.39999998
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2 AsstFWUprBoundX HwNm s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240 -8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
12_A5511*WUPIDUUHUA_FIWINII_S4P11[0][9]	
t2 AcctEM/I InrRoundY Husbin canadatication	20490
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][10] t2_AsstFWUprBoundX_HwNm_s4p11[7][0] t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	20480 -12288 -10240



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
	2048
12_AsstFWUprBoundX_HwNm_s4p11[7][7]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-12288
	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	26624
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	28672
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
رد_AsstFWUprBoundY_MtrNm_s4p11[4][4] الاستخدام الاستخدام الإنجام ا	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-24576
	-22528
2 AsstFWUprBoundY MtrNm s4n11[5][1]	
	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-18432
i2_AsstFWUprBoundY_MtrNm_s4p11[5][2] i2_AsstFWUprBoundY_MtrNm_s4p11[5][3] i2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-18432 -16384
i2_AsstFWUprBoundY_MtrNm_s4p11[5][2] i2_AsstFWUprBoundY_MtrNm_s4p11[5][3] i2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-18432
i2_AsstFWUprBoundY_MtrNm_s4p11[5][2] i2_AsstFWUprBoundY_MtrNm_s4p11[5][3] i2_AsstFWUprBoundY_MtrNm_s4p11[5][4] i2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-18432 -16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] t2_AsstFWUprBoundY_MtrNm_s4p11[5][3] t2_AsstFWUprBoundY_MtrNm_s4p11[5][4] t2_AsstFWUprBoundY_MtrNm_s4p11[5][5] t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-18432 -16384 -14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1] t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] t2_AsstFWUprBoundY_MtrNm_s4p11[5][3] t2_AsstFWUprBoundY_MtrNm_s4p11[5][4] t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-18432 -16384 -14336 -12288



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	102
t_AsstFWDefltAssistX_HwNm_u8p8[1]	128
t_AsstFWDefltAssistX_HwNm_u8p8[2]	154
t_AsstFWDefltAssistX_HwNm_u8p8[3]	179
t_AsstFWDefltAssistX_HwNm_u8p8[4]	205
t_AsstFWDefltAssistX_HwNm_u8p8[5]	230 256
t_AsstFWDefltAssistX_HwNm_u8p8[6] t_AsstFWDefltAssistX_HwNm_u8p8[7]	282
t_AsstFWDefltAssistX_HwNm_u8p8[8]	307
t_AsstFWDefltAssistX_HwNm_u8p8[9]	333
t_AsstFWDefltAssistX_HwNm_u8p8[10]	358
t_AsstFWDefltAssistX_HwNm_u8p8[11]	384
t_AsstFWDefltAssistX_HwNm_u8p8[12]	410
t_AsstFWDefltAssistX_HwNm_u8p8[13]	435
t_AsstFWDefltAssistX_HwNm_u8p8[14]	461
t_AsstFWDefltAssistX_HwNm_u8p8[15]	486
t_AsstFWDefltAssistX_HwNm_u8p8[16]	512
t_AsstFWDefltAssistX_HwNm_u8p8[17]	538
t_AsstFWDefltAssistX_HwNm_u8p8[18]	563
t_AsstFWDefltAssistX_HwNm_u8p8[19]	589
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6] t_AsstFWDefltAssistY_MtrNm_s4p11[7]	6144 12288
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	20480
t_AsstFWPstepNstepThresh_Cnt_u16[0]	125
t_AsstFWPstepNstepThresh_Cnt_u16[1]	219
t_AsstFWVehSpd_Kph_u9p7[0]	10240
t_AsstFWVehSpd_Kph_u9p7[1]	10368
t_AsstFWVehSpd_Kph_u9p7[2]	10496
t_AsstFWVehSpd_Kph_u9p7[3]	10624
t_AsstFWVehSpd_Kph_u9p7[4]	10752
	1000
t_AsstFWVehSpd_Kph_u9p7[5] t_AsstFWVehSpd_Kph_u9p7[6]	10880 11008



Name	Input Value		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4.0999999		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	40		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	_Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_N	ltrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_N	/trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	le tgt_AssistFirewall_Per1_Defeat_AsstTbl_Se	ervice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mi	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm	_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_N	/ltrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt	t_enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph	n_f32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.76000023	5.76000023 ± 4.88E-04	<b>✓</b>
AssistFirewall_ActiveRawAcc_Cnt_M_u16	219	219 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	-
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.01800013	5.01800013 ± 4.88E-04	-
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8.03999996	8.03999996 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.97000003	3.97000003 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	-
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>→</b>
NTC_Cnt_T_enum	0xC9	0xC9	-
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T -				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	-

Test Step 3.3 (Repeat Count = 1)	·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1000
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.16999996
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.60000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0399999991
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00700000022
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1
k_AsstFWInpLimitHFA_MtrNm_f32	1.89999998
k_AsstFWInpLimitHysComp_MtrNm_f32	2.5
k_AsstFWNstep_Cnt_u16	4300
k_AsstFWPstep_Cnt_u16	738
k_RestoreThresh_MtrNm_f32	1.60000002
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048



Name	Input Value	
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240	
t2_Asst WorlboundX_HwNm_s4p11[0][10]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432	
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384	
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336	
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288	
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048	
	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]		
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432	
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336	
	-12288	
12_AsstFWUprBoundX_HwNm_s4p11[6][2]		
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144	



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	Ō
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0] t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336 -12288
	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2] t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048
t2 AsstFWUprBoundY MtrNm s4p11[3][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-6144



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	154
t_AsstFWDefltAssistX_HwNm_u8p8[1]	179
t_AsstFWDefitAssistX_HwNm_u8p8[2]	205
t_AsstFWDefltAssistX_HwNm_u8p8[3]	230
t_AsstFWDefltAssistX_HwNm_u8p8[4]	256
t_AsstFWDefltAssistX_HwNm_u8p8[5]	282
t_AsstFWDefltAssistX_HwNm_u8p8[6]	307
t_AsstFWDefltAssistX_HwNm_u8p8[7]	333
t_AsstFWDefltAssistX_HwNm_u8p8[8]	358
t_AsstFWDefltAssistX_HwNm_u8p8[9]	384
t_AsstFWDefltAssistX_HwNm_u8p8[10]	410
t_AsstFWDefltAssistX_HwNm_u8p8[11]	435
t_AsstFWDefltAssistX_HwNm_u8p8[12]	461
t_AsstFWDefltAssistX_HwNm_u8p8[13]	486
t_AsstFWDefltAssistX_HwNm_u8p8[14]	512
t_AsstFWDefltAssistX_HwNm_u8p8[15]	538
t_AsstFWDefltAssistX_HwNm_u8p8[16]	563
t_AsstFWDefltAssistX_HwNm_u8p8[17]	589
t_AsstFWDefltAssistX_HwNm_u8p8[18]	614
t_AsstFWDefltAssistX_HwNm_u8p8[19]	640
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	10240
t AsstFWDefltAssistY MtrNm s4p11[5]	10240
t_AsstFWDefitAssistY_MtrNm_s4p11[6]	10240
	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720
t_AsstFWPstepNstepThresh_Cnt_u16[0]	127
t_AsstFWPstepNstepThresh_Cnt_u16[1]	227
t_AsstFWVehSpd_Kph_u9p7[0]	16128
t_AsstFWVehSpd_Kph_u9p7[1]	16256
t_AsstFWVehSpd_Kph_u9p7[2]	16384
t_AsstFWVehSpd_Kph_u9p7[3]	16512
t_AsstFWVehSpd_Kph_u9p7[4]	16640
t_AsstFWVehSpd_Kph_u9p7[5]	16768
t_AsstFWVehSpd_Kph_u9p7[6]	16896
	10000



Name	Input Value		
t_AsstFWVehSpd_Kph_u9p7[7]	17024		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-8.80000019		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	6		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	60		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	_Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_M	trNm_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32$	tgt_AssistFirewall_Per1_CombinedAssist_M	ltrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	_l( tgt_AssistFirewall_Per1_Defeat_AsstTbl_Se	ervice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mt	rNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_	_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_N	ftrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt	_enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph	_f32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7.51999998	7.51999998 ± 4.88E-04	-
AssistFirewall_ActiveRawAcc_Cnt_M_u16	227	227 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	-
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.73000002	6.73000002 ± 4.88E-04	-
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.51200008	2.51200008 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	-
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.95800018	5.95800018 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	-
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	-
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	-
NTC_Cnt_T_enum	0xC9	0xC9	-
Param_Cnt_T_u08	0x01	0x01	-
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T .				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	-
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 3.4 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0199999996
AssistFirewall_ActiveRawAcc_Cnt_M_u16	200
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.13
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0099999998
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.20000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00899999961
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00300000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.20000005
k_AsstFWInpLimitHFA_MtrNm_f32	1.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	3
k_AsstFWNstep_Cnt_u16	4796
k_AsstFWPstep_Cnt_u16	246
k_RestoreThresh_MtrNm_f32	1.20000005
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
, , , , , , , , , , , , , , , , , , , ,	
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
12_10011 VVOP1D0U11U/_1 (WINITI_0+P11[/][/]	-10004



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
	-6144
12_AsstFWUprBoundX_HwNm_s4p11[7][5]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-20480
	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
12_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	4096
	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-22528
t2_Asst WopiBoundY_MtrNm_s4p11[5][4]	-20480
	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-14336



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4] t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	51
t_AsstFWDefltAssistX_HwNm_u8p8[1]	77
t_AsstFWDefltAssistX_HwNm_u8p8[2]	102
t_AsstFWDefltAssistX_HwNm_u8p8[3]	128
t_AsstFWDefltAssistX_HwNm_u8p8[4]	154
t_AsstFWDefltAssistX_HwNm_u8p8[5]	179
t_AsstFWDefltAssistX_HwNm_u8p8[6]	205
t_AsstFWDefltAssistX_HwNm_u8p8[7]	230
t_AsstFWDefltAssistX_HwNm_u8p8[8]	256
t_AsstFWDefltAssistX_HwNm_u8p8[9]	282
t_AsstFWDefltAssistX_HwNm_u8p8[10]	307
t_AsstFWDefltAssistX_HwNm_u8p8[11]	333
t_AsstFWDefltAssistX_HwNm_u8p8[12]	358
t_AsstFWDefltAssistX_HwNm_u8p8[13]	384
t_AsstFWDefltAssistX_HwNm_u8p8[14]	410
t_AsstFWDefltAssistX_HwNm_u8p8[15]	435
t_AsstFWDefltAssistX_HwNm_u8p8[16]	461
t_AsstFWDefltAssistX_HwNm_u8p8[17]	486
t_AsstFWDefltAssistX_HwNm_u8p8[18]	512
t_AsstFWDefltAssistX_HwNm_u8p8[19]	538
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	0
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192 8192
t_AsstFWDefltAssistY_MtrNm_s4p11[8] t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	12288
t_AsstFWDefitAssistY_MtrNm_s4p11[10] t_AsstFWDefitAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefitAssistY_MtrNm_s4p11[11] t_AsstFWDefitAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefitAssistY_MtrNm_s4p11[12]	18432
t_AsstFWDefitAssistY_MtrNm_s4p11[13]	20480
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720
t_AsstFWPstepNstepThresh_Cnt_u16[0]	123
t_AsstFWPstepNstepThresh_Cnt_u16[1]	211
t_AsstFWVehSpd_Kph_u9p7[0]	4352
t_AsstFWVehSpd_Kph_u9p7[1]	4480
t_AsstFWVehSpd_Kph_u9p7[2]	4608
t_AsstFWVehSpd_Kph_u9p7[3]	4736
t_AsstFWVehSpd_Kph_u9p7[4]	4864



Name	Input Value		
t_AsstFWVehSpd_Kph_u9p7[6]	5120		
t_AsstFWVehSpd_Kph_u9p7[7]	5248		
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	8.80000019		
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	0		
tgt AssistFirewall Per1 HighFregAssist MtrNm f32.value	2.20000005		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	2		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	20		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_I	Jls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_Mti	rNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_Mt	rNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_k	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Ser	vice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mtr	Nm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_t	32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_Mi	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_	enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_	<u>f</u> 32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.92000008	3.92000008 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	211	211 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.02399993	3.02399993 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.01800013	6.01800013 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.98199999	1.98199999 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	<b>✓</b>

Test Step 3.5 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.30000019
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.40000006
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11199999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.119999997
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.219999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.80000019
k_AsstFWInpLimitHFA_MtrNm_f32	6.40999985
k_AsstFWInpLimitHysComp_MtrNm_f32	6.71000004
k_AsstFWNstep_Cnt_u16	4052
k_AsstFWPstep_Cnt_u16	2460
k_RestoreThresh_MtrNm_f32	4.42999983
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192



Name	Input Value	
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048	
	0	
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]		
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384	
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288	
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096	
t2 AsstFWUprBoundX HwNm s4p11[2][5]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384	
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336	
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288	
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144	
	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]		
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048	
	0	
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]		
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336	
=	1.1555	



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096
	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
LE_/ 1001 VY OPI DOUNG I _IVILITYIII_54P I T[O][O]	0144



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288	
t_AsstFWDefltAssistX_HwNm_u8p8[0]	333	
t AsstFWDefltAssistX HwNm u8p8[1]	358	
t_AsstFWDefltAssistX_HwNm_u8p8[2]	384	
t_AsstFWDefitAssistX_HwNm_u8p8[3]	410	
t_AsstFWDefltAssistX_HwNm_u8p8[4]	435	
t_AsstFWDefltAssistX_HwNm_u8p8[5]	461	
t_AsstFWDefltAssistX_HwNm_u8p8[6]	486	
t_AsstFWDefltAssistX_HwNm_u8p8[7]	512	
t_AsstFWDefltAssistX_HwNm_u8p8[8]	538	
t_AsstFWDefltAssistX_HwNm_u8p8[9]	563	
t_AsstFWDefltAssistX_HwNm_u8p8[10]	589	
t_AsstFWDefltAssistX_HwNm_u8p8[11]	614	
t_AsstFWDefltAssistX_HwNm_u8p8[12]	640	
t_AsstFWDefltAssistX_HwNm_u8p8[13]	666	
t_AsstFWDefltAssistX_HwNm_u8p8[14]	691	
t_AsstFWDefltAssistX_HwNm_u8p8[15]	717	
t_AsstFWDefltAssistX_HwNm_u8p8[16]	742	
t_AsstFWDefltAssistX_HwNm_u8p8[17]	768	
t_AsstFWDefltAssistX_HwNm_u8p8[18]	794	
t_AsstFWDefltAssistX_HwNm_u8p8[19]	819	
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-204	
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	0	
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2048	
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096	
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	4096	
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	6144	
t_AsstFWDefitAssistY_MtrNm_s4p11[6]	6144	
t_AsstFWDefitAssistY_MtrNm_s4p11[6]	8192	
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8192	
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240	
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288	
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336	
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384	
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432	
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480	
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528	
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576	
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624	
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672	
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720	
t_AsstFWPstepNstepThresh_Cnt_u16[0]	134	
t_AsstFWPstepNstepThresh_Cnt_u16[1]	255	
t_AsstFWVehSpd_Kph_u9p7[0]	36736	
t_AsstFWVehSpd_Kph_u9p7[1]	36864	
t_AsstFWVehSpd_Kph_u9p7[2]	36992	
t_AsstFWVehSpd_Kph_u9p7[3]	37120	
t_AsstFWVehSpd_Kph_u9p7[4]	37248	
	0.210	



Name	Input Value		
t_AsstFWVehSpd_Kph_u9p7[5]	37376		
t_AsstFWVehSpd_Kph_u9p7[6]	37504		
t_AsstFWVehSpd_Kph_u9p7[7]	37632		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.19999981		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	1		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.5999999		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.4000001		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.5999999		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	_Uls_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32$	tgt_AssistFirewall_Per1_BaseAssistCmd_M	trNm_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32$	tgt_AssistFirewall_Per1_CombinedAssist_N	ltrNm_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Service\_Cn$	_lt_tgt_AssistFirewall_Per1_Defeat_AsstTbl_Se	ervice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mt	rNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_	_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_N	ftrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt	_enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph	_f32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.30000019	-5.30000019 ± 4.88E-04	<b>~</b>
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487	8487 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-16	-16 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-6.06399965	-6.06399965 ± 4.88E-04	<b>~</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019	-5.30000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>~</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999	5.0999999 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	<b>~</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-16	-16 ± 9.77E-04	<b>~</b>
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC6	0xC6	•
Param_Cnt_T_u08	0x01	0x01	-
Status_Cnt_T_enum	0x00	0x00	<b>✓</b>

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 3.6 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	2.20000005
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0799999982
AssistFirewall_ActiveRawAcc_Cnt_M_u16	106
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.19000006
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0700000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00899999961
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3
k_AsstFWInpLimitHFA_MtrNm_f32	1.29999995
k_AsstFWInpLimitHysComp_MtrNm_f32	3.29999995
k_AsstFWNstep_Cnt_u16	4052
k_AsstFWPstep_Cnt_u16	984
k_RestoreThresh_MtrNm_f32	1.79999995
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144
	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-14336
	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096
	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-16384
:2_Asst WopiBoundY_MtrNm_s4p11[4][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192
	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048
	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	205
t_AsstFWDefltAssistX_HwNm_u8p8[1]	230
t_AsstFWDefltAssistX_HwNm_u8p8[2]	256
t_AsstFWDefltAssistX_HwNm_u8p8[3]	282
t_AsstFWDefltAssistX_HwNm_u8p8[4]	307
t_AsstFWDefltAssistX_HwNm_u8p8[5]	333
t_AsstFWDefltAssistX_HwNm_u8p8[6]	358
t_AsstFWDefltAssistX_HwNm_u8p8[7]	384
t_AsstFWDefltAssistX_HwNm_u8p8[8]	410
t_AsstFWDefltAssistX_HwNm_u8p8[9]	435
t_AsstFWDefltAssistX_HwNm_u8p8[10]	461
t_AsstFWDefltAssistX_HwNm_u8p8[11]	486
t_AsstFWDefltAssistX_HwNm_u8p8[12]	512 538
t_AsstFWDefltAssistX_HwNm_u8p8[13]	563
t_AsstFWDefltAssistX_HwNm_u8p8[14] t AsstFWDefltAssistX HwNm u8p8[15]	589
t_AsstFWDefltAssistX_HwNm_u8p8[16]	614
t_AsstFWDefitAssistX_HwNm_u8p8[17]	640
t_AsstFWDefItAssistX_HwNm_u8p8[18]	666
t_AsstFWDefltAssistX_HwNm_u8p8[19]	691
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-204
t AsstFWDefltAssistY MtrNm s4p11[1]	0
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720
t_AsstFWPstepNstepThresh_Cnt_u16[0]	129
t_AsstFWPstepNstepThresh_Cnt_u16[1]	235
t_AsstFWVehSpd_Kph_u9p7[0]	22016
t_AsstFWVehSpd_Kph_u9p7[1]	22144
t_AsstFWVehSpd_Kph_u9p7[2]	22272 22400
t_AsstFWVehSpd_Kph_u9p7[3]	22400
t_AsstFWVehSpd_Kph_u9p7[4]	22528



Name	Input Value		
t_AsstFWVehSpd_Kph_u9p7[6]	22784		
t_AsstFWVehSpd_Kph_u9p7[7]	22912		
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	3		
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	0		
tgt AssistFirewall Per1 HighFregAssist MtrNm f32.value	0		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8		
tot AssistFirewall Per1 HysteresisComp MtrNm f32.value	8		
tgt AssistFirewall Per1 MEC Counter Cnt enum.value	1		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	80		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_I	lle f22	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_Mtr		
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 CombinedAssist MtrNm f32	tgt_AssistFirewall_Fer1_baseAssistCifid_iviti tgt_AssistFirewall_Per1_CombinedAssist_Mt		
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 Defeat AsstTbl Service Cnt In		=	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mtrl		
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 HwTorque HwNm f32			
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_mwTorque_mwnm_i32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f tqt AssistFirewall Per1 HysteresisComp Mt		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_	=	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.02400017	2.02399993 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	235	235 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.46399999	1.46399999 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.33400011	4.33400011 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.9460001	7.9460001 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	<b>~</b>
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>✓</b>

Test Step 3.7 (Repeat Count = 1)	
	Innut Value
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0060000005
AssistFirewall_ActiveRawAcc_Cnt_M_u16	115
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.29999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0599999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.090000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.029999993
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.4000001
k_AsstFWInpLimitHFA_MtrNm_f32	2.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	4.76999998
k_AsstFWNstep_Cnt_u16	3680
k_AsstFWPstep_Cnt_u16	1353
k_RestoreThresh_MtrNm_f32	2.0999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_Asst WopiBoundX_HwNm_s4p11[1][7]	8192
, , , , , , , , , , , , , , , , , , , ,	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_Asst WoprBoundX_HwNm_s4p11[4][0]	-12288
12_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
:2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048



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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144
:2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192
:2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-14336
	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
2 AsstFWUprBoundY MtrNm s4p11[3][9]	
	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0
Z_A33ti Wopi Bound I _With Mil_34p I T[3][3]	



Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192	
	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]		
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192	
t_AsstFWDefltAssistX_HwNm_u8p8[0]	282	
t_AsstFWDefltAssistX_HwNm_u8p8[1]	307	
t_AsstFWDefltAssistX_HwNm_u8p8[2]	333	
t_AsstFWDefltAssistX_HwNm_u8p8[3]	358	
t_AsstFWDefltAssistX_HwNm_u8p8[4]	384	
t_AsstFWDefltAssistX_HwNm_u8p8[5]	410	
t_AsstFWDefltAssistX_HwNm_u8p8[6]	435	
t_AsstFWDefltAssistX_HwNm_u8p8[7]	461	
t_AsstFWDefltAssistX_HwNm_u8p8[8]	486	
t_AsstFWDefltAssistX_HwNm_u8p8[9]	512	
t_AsstFWDefltAssistX_HwNm_u8p8[10]	538	
t_AsstFWDefltAssistX_HwNm_u8p8[11]	563	
t_AsstFWDefltAssistX_HwNm_u8p8[12]	589	
t_AsstFWDefltAssistX_HwNm_u8p8[13]	614	
t_AsstFWDefltAssistX_HwNm_u8p8[14]	640	
t_AsstFWDefltAssistX_HwNm_u8p8[15]	666	
t_AsstFWDefltAssistX_HwNm_u8p8[16]	691	
t_AsstFWDefltAssistX_HwNm_u8p8[17]	717	
t_AsstFWDefltAssistX_HwNm_u8p8[18]	742	
t_AsstFWDefltAssistX_HwNm_u8p8[19]	768	
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4096	
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4096	
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4096	
t AsstFWDefltAssistY MtrNm s4p11[3]	4096	
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096	
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144	
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144	
t AsstFWDefltAssistY MtrNm s4p11[7]	12288	
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	12288	
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	12288	
·	12288	
t_AsstFWDefltAssistY_MtrNm_s4p11[10]		
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	12288	
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12288	
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	16384	
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	16384	
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16384	
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	20480	
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	20480	
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	20480	
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	20480	
t_AsstFWPstepNstepThresh_Cnt_u16[0]	132	
t_AsstFWPstepNstepThresh_Cnt_u16[1]	247	
t_AsstFWVehSpd_Kph_u9p7[0]	30848	
t_AsstFWVehSpd_Kph_u9p7[1]	30976	
t_AsstFWVehSpd_Kph_u9p7[2]	31104	
t_AsstFWVehSpd_Kph_u9p7[3]	31232	
t_AsstFWVehSpd_Kph_u9p7[4]	31360	
	01000	



Name Input Value



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
	-8192
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
:2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6192
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
:2_AsstFWUprBoundX_HwNm_s4p11[4][9] :2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
:2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144



Name	Input Value	
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048	
12_AsstFWUprBoundX_HwNm_s4p11[7][2]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048	
	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]		
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240	
t2_AsstrWUprBoundY_MtrNm_s4p11[3][7]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-24576	
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	16384	



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	282
t_AsstFWDefltAssistX_HwNm_u8p8[1]	307
t_AsstFWDefltAssistX_HwNm_u8p8[2]	333
t_AsstFWDefltAssistX_HwNm_u8p8[3]	358
t_AsstFWDefltAssistX_HwNm_u8p8[4]	384
t_AsstFWDefltAssistX_HwNm_u8p8[5]	410
t_AsstFWDefltAssistX_HwNm_u8p8[6]	435
t_AsstFWDefltAssistX_HwNm_u8p8[7]	461
t_AsstFWDefltAssistX_HwNm_u8p8[8]	486
t_AsstFWDefltAssistX_HwNm_u8p8[9]	512
t_AsstFWDefltAssistX_HwNm_u8p8[10]	538
t_AsstFWDefltAssistX_HwNm_u8p8[11]	563
t_AsstFWDefltAssistX_HwNm_u8p8[12]	589
t_AsstFWDefltAssistX_HwNm_u8p8[13]	614
t_AsstFWDefltAssistX_HwNm_u8p8[14]	640
t_AsstFWDefltAssistX_HwNm_u8p8[15]	666
t_AsstFWDefltAssistX_HwNm_u8p8[16]	691
t_AsstFWDefltAssistX_HwNm_u8p8[17]	717
t_AsstFWDefltAssistX_HwNm_u8p8[18]	742
t_AsstFWDefltAssistX_HwNm_u8p8[19]	768
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	6144
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t_AsstFWDefltAssistY_MtrNm_s4p11[3]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	30720
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720
t_AsstFWPstepNstepThresh_Cnt_u16[0]	170
t_AsstFWPstepNstepThresh_Cnt_u16[1]	399
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456



t_AsstFWVehSpd_Kph_u9p7[4] 19584  t_AsstFWVehSpd_Kph_u9p7[5] 19840  t_AsstFWVehSpd_Kph_u9p7[6] 19840  t_AsstFWVehSpd_Kph_u9p7[7] 19968  tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value 4.09999999  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Ont_lgc.value 0  tgt_AssistFirewall_Per1_HiphFreqAssist_MtrNm_f32.value 1.10000002  tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value 9-9  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value 1.10000002  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Ont_lgc.value 9-9  tgt_AssistFirewall_Per1_MysteresisComp_MtrNm_f32.value 1.10000002  tgt_AssistFirewall_Per1_MysteresisComp_MtrNm_f32.value 0  tgt_AssistFirewall_Per1_MysteresisComp_MtrNm_f32.value 1.10000002  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value 0  tgt_AssistFirewall_Per1_SastFirewall_AssistFirewall_Per1_AsstFirewall_Per1_AsstFirewall_Per1_AsstFirewall_Per1_AsstFirewall_Per1_AssistFirewall_Per1_AssistFirewall_Per1_AssistFirewall_Per1_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgt tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgt tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgt tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgt tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgt tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgt tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgt tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Mec_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Mec_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall_Per1_VehicleSpeed_Kph_f32		I			_
L AssiFWehSpd, Kph_u9p7[5] 19712  L AssiFWehSpd, Kph_u9p7[7] 1998  1gt, AssiFirewall, Perl_BaseAssistCmd_MtnNm_i32_value 4.0999999  tgt, AssistFirewall, Perl_BaseAssistCmd_MtnNm_i32_value 0.10000002  tgt, AssistFirewall, Perl_HysteresisComp_MtnNm_i32_value 1.10000002  tgt, Rel. Inst, Ap. AssistFirewall, AssistFirewall, Perl_AssistFirewall, Perl_AssistFirewall, Perl_AssistFirewall, Perl_BaseAssistFirewall, Perl_AssistFirewall, Perl_AssistFirewall, Perl_Defeat, AssistFirewall, Perl_BaseAssistFirewall, Perl_Defeat, AssistFirewall, Perl_Defeat, Perl	Name	Input Value			
LAssiFWehSpd_Kph_u9p7f0	t_AsstFWVehSpd_Kph_u9p7[4]	19584			
LAssiFFiveAll_Perl_BaseAssisCmd_MtrNm_f32.value	t_AsstFWVehSpd_Kph_u9p7[5]	•			
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32_value	t_AsstFWVehSpd_Kph_u9p7[6]	19840			
tgl_AssistFirewall_Perl_Defeat_AsstTbl_Service_Cnt_Igc.value tgl_AssistFirewall_Perl_HighFreqAssist_MirNm_f32_value  tgl_AssistFirewall_Perl_HybreregisComp_MirNm_f32_value  tgl_AssistFirewall_Perl_HybreregisComp_MirNm_f32_value  tgl_AssistFirewall_Perl_HybreregisComp_MirNm_f32_value  tgl_AssistFirewall_Perl_HybreregisComp_MirNm_f32_value  tgl_AssistFirewall_Perl_HybreregisComp_MirNm_f32_value  tgl_Rel_Inst_Ap_AssistFirewall_AssistFirewall_Perl_BaseAssistCmd_MirNm_f32  tgl_Rel_Inst_Ap_AssistFirewall_AssistFirewall_Perl_BaseAssistCmd_MirNm_f32  tgl_Rel_Inst_Ap_AssistFirewall_AssistFirewall_Perl_Defeat_AssTD_Service_Cnt_Igc  tgl_Rel_Inst_Ap_AssistFirewall_AssistFirewall_Perl_HybreregisComp_MirNm_f32  tgl_Rel_Inst_Ap_AssistFirewall_AssistFirewall_Perl_HybreregisComp_MirNm_f32  tgl_Rel_Inst_Ap_AssistFirewall_AssistFirewall_Perl_HybreregisComp_MirNm_f32  tgl_Rel_Inst_Ap_AssistFirewall_AssistFirewall_Perl_HybreregisComp_MirNm_f32  tgl_Rel_Inst_Ap_AssistFirewall_ResistFirewall_Perl_HybreregisComp_MirNm_f32  tgl_Rel_Inst_Ap_AssistFirewall_AssistFirewall_Perl_HybreregisComp_MirNm_f32  tgl_Rel_Inst_Ap_AssistFirewall_AssistFirewall_Perl_HybreregisComp_MirNm_f32  tgl_Rel_Inst_Ap_AssistFirewall_ResistFirewall_Perl_HybreregisComp_MirNm_f32  tgl_AssistFirewall_Perl_HybreregisComp_MirNm_f32  tgl_AssistFirewall_Perl_HybreregisComp_MirNm_f32  tgl_AssistFirewall_Perl_HybreregisComp_MirNm_f32  tgl_AssistFirewall_Perl_MEC_Counter_Ont_enum  tgl_Rel_Inst_Ap_AssistFirewall_Perl_Perl_Perl_Rel_Counter_Ont_enum  tgl_Rel_Inst_Ap_AssistFirewall_Perl_Perl_Perl_Perl_Perl_Perl_Perl_Pe	t_AsstFWVehSpd_Kph_u9p7[7]	19968			
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32_value	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.0999999			
tgt_AssistFirewall_Per1_HystresisComp_Mrthm_f32.value  tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value  77  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_AsstFirewallAssistFirewall_Per1_AsstFirewall_Per1_AsstFirewallAssistFirewall_Per1_AsstFirewall_Per1_AsstFirewallAssistFirewall_Per1_AsstFirewallAssistFirewall_Per1_AsstFirewall_Per1_AsstFirewallAssistFirewall_Per1_Defeat_AssistTirewall_Per1_Defeat_AssistFirewall_Per1_HysteresisComp_MtnNm_f32  tgt_Rei_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtnNm_f32  tgt_AssistFirewall_Per1_HysteresisComp_MtnNm_f32  tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum  tgt_Rei_Inst_Ap_AssistFirewall_Per1_Per1_Per1_Per1_Per1_Per1_Per1_Per1	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0			
tgt_AssistFirewall_Per1_HysteresisComp_ltrtNm_f32.value  tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Je  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Je  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Hybrace_HwNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Hybrace_HwNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Hybrace_HwNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Hybrace_HwNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Hybrace_HwNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Hybrace_Scomp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Hybrace_Scomp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Hybrace_Scomp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Hybrace_Scomp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Hybrace_Scomp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Hybrace_Scomp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Hybrace_Scomp_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_VehicleSpeed_Kph_f32  Name  Actual Value  AssistFirewall_ActiveRow_Acc_Cnt_M_uf6  AssistFirewall_ActiveRow_Acc_Cnt_M_uf6  AssistFirewall_ActiveRow_Acc_Cnt_M_uf6  AssistFirewall_ActiveRow_Acc_Cnt_M_uf6  AssistFirewall_HifreqKSV_M_str.SV_Uls_f32  4	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002			
tgt_AssistFirewall_Per1_WEC_Counter_Cnt_enum.value  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32_value  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_AsstFirewallActive_Uls_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ls  tgt_AssistFirewall_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ls  tgt_AssistFirewall_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HwTorque_HwNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HwTorque_HwNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HwTorque_HwNm_f32  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_MetreciscComp_MtrNm_f32  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_AssistFirewall_Per1_Untorque_HwNm_f32  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32  Name  Actual Value  Expected Value  Res  AssistFirewall_AssistReducedPerfSV_Cnt_M_lgc  0 0 0  AssistFirewall_AssistPirewall_AssistPirewall_Per1_AssistPirewall_Per1_AssistPirewall_Per1_AssistPirewall_Per1_AssistPirewall_Per1_AssistPirewall_Per1_AssistPirewall_Per1_Per1_Per1_Per1_Per1_Per1_Per1_Per1	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-9			
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_132.value 77  tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_BaseAssistCmd_MtrNm_132 tgt_Rte_Inst_Ap_AssistFirewall_Per1_BaseAssistCmd_MtrNm_132 tgt_Rte_Inst_Ap_AssistFirewall_Per1_BaseAssistCmd_MtrNm_132 tgt_AssistFirewall_Per1_BaseAssistFirewall_Per1_CombinedAssist_MtrNm_132 tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AssitTb_Service_Cnt_Igt_Igt_AssistFirewall_Per1_Defeat_AssitTb_Service_Cnt_Igt_Igt_AssistFirewall_Per1_Defeat_AssitTb_Service_Cnt_Igt_Igt_AssistFirewall_Per1_HybreqAssist_MtrNm_132 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HybreqAssist_MtrNm_132 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HybreqAssist_MtrNm_132 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HybreqAssist_MtrNm_132 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HybreqAssist_MtrNm_132 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HybreqAssist_MtrNm_132 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HybreqAssist_MtrNm_132 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HybreqAssist_MtrNm_132 tgt_AssistFirewall_Per1_HybreqAssist_MtrNm_132 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_VehicleSpeed_Kph_132 tgt_AssistFirewall_Per1_VehicleSpeed_Kph_132 tgt_Ass	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002			
tgt.Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defact_AsstTbl_Service_Cnt_lg tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defact_AsstTbl_Service_Cnt_lg tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_MtbC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall_Per1_MtbC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall_Per1_VehicleSpeed_Kph_f32  Mame  Actual Value  AssistFirewall_ActiveKSV_M_str.SV_Uls_f32  AssistFirewall_ActiveKSV_M_str.SV_Uls_f32  AssistFirewall_ActiveRawAcc_Cnt_M_uf6  AssistFirewall_AssistAeducedPerfSV_Cnt_M_lgc  AssistFirewall_LiFreqKSV_M_str.SV_Uls_f32  AssistFirewall_HiFreqKSV_M_str.SV_Uls_f32  AssistFirewall_LiFreqKSV_M_str.SV_Uls_f32  AssistFirewall_LiFreqKSV_M_str.SV_Uls_f32  AssistFirewall_LiPrequondKSV_M_str.SV_Uls_f32  AssistFirewall_LiPrequondKSV_M_str.SV_Uls_f32  AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32  AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32  AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32  AssistFirewall_Per1_CombinedAssist_MtrNm_f32  tgt_AssistFirewall_Per1_AsstFirewallAesist_MtrNm_f32  AssistFirewall_Per1_CombinedAssist_MtrNm_f32  AssistFirewall_Per1_CombinedAssist_MtrNm_f32  AssistFirewall_Per1_CombinedAssist_MtrNm_f32  AssistFirewall_Per1_CombinedAssist_MtrNm_f32  AssistFirewall_Per1_Defact_AssttDiscord_Tip_fact_Assist_MtrNm_f32  AssistFirewall_Per1_AsstFirewall_Per1_AsstFirewall_Per1_AsstFirewall_Per1_AsstFirewall_Per1_AsstFirewall_Per1_AsstFirewall_Per1_AsstFirewall_Per1_	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0			
tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_letter_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_letter_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall_Per1_VehicleSpeed_Kpf_f32  Name  Actual Value  Expected Value  RestablistFirewall_AssistFirewall_Per1_VehicleSpeed_Kpf_f32  AssistFirewall_AssistFirewall_Per1_VehicleSpeed_Kpf_f32  AssistFirewall_AssistFirewall_Per1_VehicleSpeed_Kpf_f32  AssistFirewall_AssistFirewall_Per1_VehicleSpeed_Kpf_f32  AssistFirewall_AssistFirewall_Per1_WisteresisComp_MtrNm_f32  4 Actual Value  Expected Value  RestablistFirewall_Per1_VehicleSpeed_Kpf_f32  AssistFirewall_AssistFirewall_Per1_VehicleSpeed_Kpf_f32  AssistFirewall_CombAsstSV_MtrNm_M_f32  4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	77			
tgt_Rte_Inst_Ap_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ls tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Ref1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall_Per1_VehicleSpeed_Kph_f32  Name  Actual Value  Actual Value  AssistFirewall_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall_Per1_VehicleSpeed_Kph_f32  Name  Actual Value  AssistFirewall_AssistReducedPerfSv_Cnt_M_gc  AssistFirewall_AssixtReducedPerfSv_Cnt_M_gc  0  0  48sistFirewall_AssixtReducedPerfSv_Cnt_M_gc  4	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_I	Jls_f32		
tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AssiTbl_Service_Cnt_lg tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall_Per1_VehicleSpeed_Kph_f32  Name  Actual Value  Expected Value  Res  AssistFirewall_ActiveKSV_M_str.SV_Uls_f32  1.98000002 1.98000002 ± 4.88E-04  AssistFirewall_AssistFir	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_Mt	rNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HighFreqAssist_MtrNm_132  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_132  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_132  tgt_Rte_Inst_Ap_AssistFirewall_Per1_HysteresisComp_MtrNm_132  tgt_Rte_Inst_Ap_AssistFirewall_Per1_MEC_Counter_Cnt_enum  tgt_Rte_Inst_Ap_AssistFirewall_Per1_MEC_Counter_Cnt_enum  tgt_Rte_Inst_Ap_AssistFirewall_Per1_MEC_Counter_Cnt_enum  tgt_Rte_Inst_Ap_AssistFirewall_Per1_VehicleSpeed_Kph_132  Name  Actual Value  Expected Value  Res  AssistFirewall_ActiveKSV_M_str.SV_UIs_132  AssistFirewall_ActiveRawAcc_Cnt_M_u16  AssistFirewall_ActiveRawAcc_Cnt_M_u16  AssistFirewall_AssistReducedPerfSV_Cnt_M_lgc  0  0  AssistFirewall_HiFreqKSV_M_str.SV_UIs_132  4 ± 4.88E-04  AssistFirewall_HiFreqKSV_M_str.SV_UIs_132  AssistFirewall_LwBoundfKSV_M_str.SV_UIs_132  AssistFirewall_UprBoundKSV_M_str.SV_UIs_132  AssistFirewall_Per1_AsstFirewallActive_UIs_132.value  4 ± 9.77E-04  NTC_Cnt_T_enum  OxC6  OxC6  OxC6  OxC6  OxC6	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_Mt	rNm_f32		
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tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_MEC_Counter_Cnt_enum         tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum           tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_VehicleSpeed_Kph_f32         tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32           Name         Actual Value         Expected Value         Res           AssistFirewall_ActiveRsv_M_str.SV_Uls_f32         1.98000002         1.98000002 ± 4.88E-04         1.98000002 ± 4.88E-04           AssistFirewall_AssitReducedPerfSV_Cnt_M_uf6         246         246 ± 1         0         0           AssistFirewall_CombAsstSV_MtrNm_M_f32         4         4 ± 4.88E-04         4         4.88E-04           AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32         1.15799999         1.15799999 ± 4.88E-04         1.15799999 ± 4.88E-04         0	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_t	32		
tgt_Rte_Inst_Ap_AssistFirewall_Per1_VehicleSpeed_Kph_f32         tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32           Name         Actual Value         Expected Value         Res           AssistFirewall_ActiveKSV_M_str.SV_Uls_f32         1.98000002         1.98000002 ± 4.88E-04           AssistFirewall_ActiveRawAcc_Cnt_M_u16         246         246 ± 1           AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc         0         0           AssistFirewall_CombAsstSV_MtrNm_M_f32         4         4 ± 4.88E-04           AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32         1.15799999         1.15799999 ± 4.88E-04           AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32         -6.19999981         -6.19999981 ± 4.88E-04           AssistFirewall_PROuntStatus_Cnt_M_lgc         0         0         0           AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32         7.90100002         7.90100002 ± 4.88E-04           tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value         1         1 ± 3.05E-05           tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value         4         4 ± 9.77E-04           NTC_Cnt_T_enum         0xC6         0xC6           Param_Cnt_T_u08         0x01         0x01	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_M	trNm_f32		
Name         Actual Value         Expected Value         Res           AssistFirewall_ActiveKSV_M_str.SV_UIs_f32         1,98000002         1,98000002 ± 4.88E-04           AssistFirewall_ActiveRawAcc_Cnt_M_u16         246         246 ± 1           AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc         0         0           AssistFirewall_CombAsstSV_MtrNm_M_f32         4         4 ± 4.88E-04           AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_UIs_f32         1.15799999         1.15799999 ± 4.88E-04           AssistFirewall_LwrBoundKSV_M_str.SV_UIs_f32         -6.19999981         -6.19999981 ± 4.88E-04           AssistFirewall_PNCountStatus_Cnt_M_lgc         0         0           AssistFirewall_UprBoundKSV_M_str.SV_UIs_f32         7.90100002         7.90100002 ± 4.88E-04           tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32.value         1         1 ± 3.05E-05           tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value         4         4 ± 9.77E-04           NTC_Cnt_T_enum         0xC6         0xC6           Param_Cnt_T_u08         0x01         0x01	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_	enum		
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32  AssistFirewall_ActiveRawAcc_Cnt_M_u16  AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc  O  AssistFirewall_CombAsstSV_MtrNm_M_f32  AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_UIs_f32  AssistFirewall_LwrBoundKSV_M_str.SV_UIs_f32  AssistFirewall_PNCountStatus_Cnt_M_lgc  O  AssistFirewall_UprBoundKSV_M_str.SV_UIs_f32  AssistFirewall_UprBoundKSV_M_str.SV_UIs_f32  AssistFirewall_UprBoundKSV_M_str.SV_UIs_f32  AssistFirewall_UprBoundKSV_M_str.SV_UIs_f32  AssistFirewall_UprBoundKSV_M_str.SV_UIs_f32  AssistFirewall_UprBoundKSV_M_str.SV_UIs_f32  AssistFirewall_UprBoundKSV_M_str.SV_UIs_f32  AssistFirewall_UprBoundKSV_M_str.SV_UIs_f32  AssistFirewall_Per1_AsstFirewallActive_UIs_f32.value  AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value  AssistFirewall_Per1_Combi	tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_	_f32		
AssistFirewall_ActiveRawAcc_Cnt_M_u16       246       246 ± 1         AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc       0       0         AssistFirewall_CombAsstSV_MtrNm_M_f32       4       4 ± 4.88E-04         AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32       1.15799999       1.15799999 ± 4.88E-04         AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32       -6.19999981       -6.19999981 ± 4.88E-04         AssistFirewall_PNCountStatus_Cnt_M_lgc       0       0         AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32       7.90100002       7.90100002 ± 4.88E-04         tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value       1       1 ± 3.05E-05         tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value       4       4 ± 9.77E-04         NTC_Cnt_T_enum       0xC6       0xC6         Param_Cnt_T_u08       0x01       0x01	Name	Actual Value	Expected Value	Re	esult
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc       0       0         AssistFirewall_CombAsstSV_MtrNm_M_f32       4       4 ± 4.88E-04         AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32       1.15799999       1.15799999 ± 4.88E-04         AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32       -6.19999981       -6.19999981 ± 4.88E-04         AssistFirewall_PNCountStatus_Cnt_M_lgc       0       0         AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32       7.90100002       7.90100002 ± 4.88E-04         tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value       1       1 ± 3.05E-05         tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value       4       4 ± 9.77E-04         NTC_Cnt_T_enum       0xC6       0xC6         Param_Cnt_T_u08       0x01       0x01	AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.98000002	1.98000002 ± 4.88E-04		~
AssistFirewall_CombAsstSV_MtrNm_M_f32       4       4 ± 4.88E-04         AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32       1.15799999       1.15799999 ± 4.88E-04         AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32       -6.19999981       -6.19999981 ± 4.88E-04         AssistFirewall_PNCountStatus_Cnt_M_lgc       0       0         AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32       7.90100002       7.90100002 ± 4.88E-04         tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value       1       1 ± 3.05E-05         tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value       4       4 ± 9.77E-04         NTC_Cnt_T_enum       0xC6       0xC6         Param_Cnt_T_u08       0x01       0x01	AssistFirewall_ActiveRawAcc_Cnt_M_u16	246	246 ± 1		<b>~</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32       1.15799999       1.15799999 ± 4.88E-04         AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32       -6.19999981       -6.19999981 ± 4.88E-04         AssistFirewall_PNCountStatus_Cnt_M_lgc       0       0         AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32       7.90100002       7.90100002 ± 4.88E-04         tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value       1       1 ± 3.05E-05         tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value       4       4 ± 9.77E-04         NTC_Cnt_T_enum       0xC6       0xC6         Param_Cnt_T_u08       0x01       0x01	AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0		•
AssistFirewall_LwrBoundKSV_M_str.SV_UIs_f32       -6.19999981       -6.19999981 ± 4.88E-04         AssistFirewall_PNCountStatus_Cnt_M_lgc       0       0         AssistFirewall_UprBoundKSV_M_str.SV_UIs_f32       7.90100002       7.90100002 ± 4.88E-04         tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32.value       1       1 ± 3.05E-05         tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value       4       4 ± 9.77E-04         NTC_Cnt_T_enum       0xC6       0xC6         Param_Cnt_T_u08       0x01       0x01	AssistFirewall_CombAsstSV_MtrNm_M_f32	4	4 ± 4.88E-04		~
AssistFirewall_PNCountStatus_Cnt_M_lgc       0       0         AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32       7.90100002       7.90100002 ± 4.88E-04         tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value       1       1 ± 3.05E-05         tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value       4       4 ± 9.77E-04         NTC_Cnt_T_enum       0xC6       0xC6         Param_Cnt_T_u08       0x01       0x01	AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.15799999	1.15799999 ± 4.88E-04		<b>~</b>
AssistFirewall_UprBoundKSV_M_str.SV_UIs_f32       7.90100002       7.90100002 ± 4.88E-04         tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32.value       1       1 ± 3.05E-05         tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value       4       4 ± 9.77E-04         NTC_Cnt_T_enum       0xC6       0xC6         Param_Cnt_T_u08       0x01       0x01	AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-6.19999981	-6.19999981 ± 4.88E-04		<b>~</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value       1       1 ± 3.05E-05         tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value       4       4 ± 9.77E-04         NTC_Cnt_T_enum       0xC6       0xC6         Param_Cnt_T_u08       0x01       0x01	AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0		<b>~</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value       4       4 ± 9.77E-04         NTC_Cnt_T_enum       0xC6       0xC6         Param_Cnt_T_u08       0x01       0x01	AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.90100002	7.90100002 ± 4.88E-04		<b>~</b>
NTC_Cnt_T_enum         0xC6         0xC6           Param_Cnt_T_u08         0x01         0x01	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05		~
Param_Cnt_T_u08	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4	4 ± 9.77E-04		<b>~</b>
	NTC_Cnt_T_enum	0xC6	0xC6		~
Status_Cnt_T_enum 0x00 0x00	Param_Cnt_T_u08	0x01	0x01		~
	Status_Cnt_T_enum	0x00	0x00		~
NTC_Cnt_T_enum 0xC9 0xC9	NTC_Cnt_T_enum	0xC9	0xC9		~
Param_Cnt_T_u08	Param_Cnt_T_u08	0x01	0x01		~
Status_Cnt_T_enum         0x00         0x00	Status_Cnt_T_enum	0x00	0x00		~

Τ				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 3.9 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.050000007
AssistFirewall_ActiveRawAcc_Cnt_M_u16	800
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.15999997
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.039999991
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.5
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.029999993
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00600000005
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2
k_AsstFWInpLimitHFA_MtrNm_f32	1.70000005
k_AsstFWInpLimitHysComp_MtrNm_f32	2.0999999
k_AsstFWNstep_Cnt_u16	4424
k_AsstFWPstep_Cnt_u16	615
k_RestoreThresh_MtrNm_f32	1.5
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	-6144
	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
1 - 1 - 1 - 1	-22528
t2 AsstFWUprBoundY MtrNm s4p11[5][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0] t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-20480



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2 AsstFWUprBoundY MtrNm s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
	128
t_AsstFWDefltAssistX_HwNm_u8p8[0]	154
t_AsstFWDefltAssistX_HwNm_u8p8[1]	
t_AsstFWDefltAssistX_HwNm_u8p8[2]	179
t_AsstFWDefltAssistX_HwNm_u8p8[3]	205
t_AsstFWDefltAssistX_HwNm_u8p8[4]	230
t_AsstFWDefltAssistX_HwNm_u8p8[5]	256
t_AsstFWDefltAssistX_HwNm_u8p8[6]	282
t_AsstFWDefltAssistX_HwNm_u8p8[7]	307
t_AsstFWDefltAssistX_HwNm_u8p8[8]	333
t_AsstFWDefltAssistX_HwNm_u8p8[9]	358
t_AsstFWDefltAssistX_HwNm_u8p8[10]	384
t_AsstFWDefltAssistX_HwNm_u8p8[11]	410
t_AsstFWDefltAssistX_HwNm_u8p8[12]	435
t_AsstFWDefltAssistX_HwNm_u8p8[13]	461
t_AsstFWDefltAssistX_HwNm_u8p8[14]	486
t_AsstFWDefltAssistX_HwNm_u8p8[15]	512
t_AsstFWDefltAssistX_HwNm_u8p8[16]	538
t_AsstFWDefltAssistX_HwNm_u8p8[17]	563
t_AsstFWDefltAssistX_HwNm_u8p8[18]	589
t_AsstFWDefltAssistX_HwNm_u8p8[19]	614
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	6144
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	8192
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	8192
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	8192
	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	28672
t_AsstFWPstepNstepThresh_Cnt_u16[0]	126
t_AsstFWPstepNstepThresh_Cnt_u16[1]	223
t_AsstFWVehSpd_Kph_u9p7[0]	13184
t_AsstFWVehSpd_Kph_u9p7[1]	13312
t_AsstFWVehSpd_Kph_u9p7[2]	13440
	10770



Name	Input Value		
t_AsstFWVehSpd_Kph_u9p7[3]	13568		
t_AsstFWVehSpd_Kph_u9p7[4]	13696		
t_AsstFWVehSpd_Kph_u9p7[5]	13824		
t_AsstFWVehSpd_Kph_u9p7[6]	13952		
t_AsstFWVehSpd_Kph_u9p7[7]	14080		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	50		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive	_Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_N	ltrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_N	/trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Se	ervice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mi	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm	_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_N	/trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt	t_enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph	n_f32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.6500001	6.6500001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	223	223 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.83199978	5.83199978 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.39700007	1.39699996 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.96400023	4.96400023 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	•

Test Step 3.10 (Repeat Count = 1)		~
Name	Input Value	
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.7999995	
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.100000001	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	344	
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	
AssistFirewall_CombAsstSV_MtrNm_M_f32	6.30000019	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.099999	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.7999995	
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5	
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.0999999	
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.129999995	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.19999981	
k_AsstFWInpLimitHFA_MtrNm_f32	1.70000005	
k_AsstFWInpLimitHysComp_MtrNm_f32	4.5	
k_AsstFWNstep_Cnt_u16	2564	
k_AsstFWPstep_Cnt_u16	2214	
k_RestoreThresh_MtrNm_f32	3.3099994	
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240	



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[1][10] 2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0
	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
12_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
2 AsstFWUprBoundX HwNm s4p11[3][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
2 AsstFWUprBoundX HwNm s4p11[4][3]	6144
رح AsstFWUprBoundX_HwNm_s4p11[4][4] 2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_Asst WopiBoundX_HwNm_s4p11[6][4]	2048
	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	



Name	Input Value	
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192	
t2 AsstFWUprBoundX HwNm s4p11[6][9]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288	
12_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	8192	
	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]		
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	24576	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	26624	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048	
:2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2046	
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-30720	
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-28672	
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-26624	
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-24576	
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-20480	
	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]		
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-14336	
	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12200	
	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]		
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9] t2_AsstFWUprBoundY_MtrNm_s4p11[4][10] t2_AsstFWUprBoundY_MtrNm_s4p11[5][0] t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-10240 2048	



	(
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240
t2_AsstrWUprBoundY_MtrNm_s4p11[6][2]	12288
	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefltAssistX_HwNm_u8p8[0]	230
t_AsstFWDefltAssistX_HwNm_u8p8[1]	256
t_AsstFWDefltAssistX_HwNm_u8p8[2]	282
t_AsstFWDefitAssistX_HwNm_u8p8[3]	307
t_AsstFWDefitAssistX_HwNm_u8p8[4]	333
t_AsstFWDefitAssistX_HwNm_u8p8[5]	358
	384
t_AsstFWDefltAssistX_HwNm_u8p8[6] t_AsstFWDefltAssistX_HwNm_u8p8[7]	410
t_AsstFWDefltAssistX_HwNm_u8p8[8]	435
t_AsstFWDefltAssistX_HwNm_u8p8[9]	461
t_AsstFWDefltAssistX_HwNm_u8p8[10]	486
t_AsstFWDefltAssistX_HwNm_u8p8[11]	512
t_AsstFWDefltAssistX_HwNm_u8p8[12]	538
t_AsstFWDefltAssistX_HwNm_u8p8[13]	563
t_AsstFWDefltAssistX_HwNm_u8p8[14]	589
t_AsstFWDefltAssistX_HwNm_u8p8[15]	614
t_AsstFWDefltAssistX_HwNm_u8p8[16]	640
t_AsstFWDefltAssistX_HwNm_u8p8[17]	666
t_AsstFWDefltAssistX_HwNm_u8p8[18]	691
t_AsstFWDefltAssistX_HwNm_u8p8[19]	717
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-204
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	0
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8192
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	14336
t_AsstFWDefitAssistY_MtrNm_s4p11[11]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720
	5000
t_AsstFWPstepNstepThresh_Cnt_u16[0]	5000
	5000
t_AsstFWPstepNstepThresh_Cnt_u16[0] t_AsstFWPstepNstepThresh_Cnt_u16[1] t_AsstFWVehSpd_Kph_u9p7[0]	





Name	Input Value	
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432	
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384	
t2_Asst WoprBoundX_HwNm_s4p11[0][1]	-14336	
12_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288	
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144	
	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]		
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288	
	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]		
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384	
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432	
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480	
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048	
, , , , , , , , , , , , , , , , , , , ,		
12_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432	
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336	
:2_AsstFWUprBoundX_HwNm_s4p11[5][3]		
	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192	
	-6144	
	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096 -2048	
t2_AsstFWUprBoundX_HwNm_s4p11[5][7] t2_AsstFWUprBoundX_HwNm_s4p11[5][8]		
l2_AsstFWUprBoundX_HwNm_s4p11[5][7] l2_AsstFWUprBoundX_HwNm_s4p11[5][8] l2_AsstFWUprBoundX_HwNm_s4p11[5][9]	-2048 0	
i2_AsstFWUprBoundX_HwNm_s4p11[5][7] i2_AsstFWUprBoundX_HwNm_s4p11[5][8] i2_AsstFWUprBoundX_HwNm_s4p11[5][9] i2_AsstFWUprBoundX_HwNm_s4p11[5][10]	-2048 0 2048	
I2_AsstFWUprBoundX_HwNm_s4p11[5][7] I2_AsstFWUprBoundX_HwNm_s4p11[5][8] I2_AsstFWUprBoundX_HwNm_s4p11[5][9] I2_AsstFWUprBoundX_HwNm_s4p11[5][10] I2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048 0 2048 -16384	
I2_AsstFWUprBoundX_HwNm_s4p11[5][7] I2_AsstFWUprBoundX_HwNm_s4p11[5][8] I2_AsstFWUprBoundX_HwNm_s4p11[5][9] I2_AsstFWUprBoundX_HwNm_s4p11[5][10] I2_AsstFWUprBoundX_HwNm_s4p11[6][0] I2_AsstFWUprBoundX_HwNm_s4p11[6][0] I2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048 0 2048 -16384 -14336	
12_AsstFWUprBoundX_HwNm_s4p11[5][7] 12_AsstFWUprBoundX_HwNm_s4p11[5][8] 12_AsstFWUprBoundX_HwNm_s4p11[5][9] 12_AsstFWUprBoundX_HwNm_s4p11[5][10] 12_AsstFWUprBoundX_HwNm_s4p11[6][0] 12_AsstFWUprBoundX_HwNm_s4p11[6][1] 12_AsstFWUprBoundX_HwNm_s4p11[6][1] 12_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048 0 2048 -16384 -14336 -12288	
I2_AsstFWUprBoundX_HwNm_s4p11[5][7] I2_AsstFWUprBoundX_HwNm_s4p11[5][8] I2_AsstFWUprBoundX_HwNm_s4p11[5][9] I2_AsstFWUprBoundX_HwNm_s4p11[5][10] I2_AsstFWUprBoundX_HwNm_s4p11[6][0] I2_AsstFWUprBoundX_HwNm_s4p11[6][1] I2_AsstFWUprBoundX_HwNm_s4p11[6][2] I2_AsstFWUprBoundX_HwNm_s4p11[6][2] I2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048 0 2048 -16384 -14336	
t2_AsstFWUprBoundX_HwNm_s4p11[5][7] t2_AsstFWUprBoundX_HwNm_s4p11[5][8] t2_AsstFWUprBoundX_HwNm_s4p11[5][9] t2_AsstFWUprBoundX_HwNm_s4p11[5][10] t2_AsstFWUprBoundX_HwNm_s4p11[6][0] t2_AsstFWUprBoundX_HwNm_s4p11[6][1] t2_AsstFWUprBoundX_HwNm_s4p11[6][2] t2_AsstFWUprBoundX_HwNm_s4p11[6][2] t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048 0 2048 -16384 -14336 -12288	
t2_AsstFWUprBoundX_HwNm_s4p11[5][6] t2_AsstFWUprBoundX_HwNm_s4p11[5][7] t2_AsstFWUprBoundX_HwNm_s4p11[5][8] t2_AsstFWUprBoundX_HwNm_s4p11[5][9] t2_AsstFWUprBoundX_HwNm_s4p11[5][10] t2_AsstFWUprBoundX_HwNm_s4p11[6][0] t2_AsstFWUprBoundX_HwNm_s4p11[6][1] t2_AsstFWUprBoundX_HwNm_s4p11[6][2] t2_AsstFWUprBoundX_HwNm_s4p11[6][3] t2_AsstFWUprBoundX_HwNm_s4p11[6][3] t2_AsstFWUprBoundX_HwNm_s4p11[6][4] t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048 0 2048 -16384 -14336 -12288 -10240	



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8] t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384
	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10] t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048
	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0] t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
t2 AsstFWUprBoundY MtrNm s4p11[5][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240
t2 AsstFWUprBoundY MtrNm s4p11[7][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	128
t_AsstFWDefltAssistX_HwNm_u8p8[1]	154
t_AsstFWDefltAssistX_HwNm_u8p8[2]	179
t_AsstFWDefltAssistX_HwNm_u8p8[3]	205
t_AsstFWDefltAssistX_HwNm_u8p8[4]	230
t_AsstFWDefltAssistX_HwNm_u8p8[5]	256
t_AsstFWDefltAssistX_HwNm_u8p8[6]	282
t_AsstFWDefltAssistX_HwNm_u8p8[7]	307
t_AsstFWDefltAssistX_HwNm_u8p8[8]	333
t_AsstFWDefltAssistX_HwNm_u8p8[9]	358
t_AsstFWDefltAssistX_HwNm_u8p8[10]	384
t_AsstFWDefltAssistX_HwNm_u8p8[11]	410
t_AsstFWDefltAssistX_HwNm_u8p8[12]	435
t_AsstFWDefltAssistX_HwNm_u8p8[13]	461
t_AsstFWDefltAssistX_HwNm_u8p8[14]	486
t_AsstFWDefltAssistX_HwNm_u8p8[15]	512
t AsstFWDefltAssistX HwNm u8p8[16]	538
	563
t_AsstFWDefltAssistX_HwNm_u8p8[17] t_AsstFWDefltAssistX_HwNm_u8p8[18]	589
t_AsstFWDefitAssistX_HwNm_u8p8[19]	614
t_AsstFWDefitAssistX_Hwnm_u8p8[19]  t_AsstFWDefitAssistY_MtrNm_s4p11[0]	4096
t_AsstFWDefitAssistY_MtrNm_s4p11[0]  t_AsstFWDefitAssistY_MtrNm_s4p11[1]	4096
t_AsstFWDefitAssistY_MtrNm_s4p11[1]  t_AsstFWDefitAssistY_MtrNm_s4p11[2]	4096
t_AsstFWDefitAssistY_MtrNm_s4p11[2]  t_AsstFWDefitAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	20480
t_AsstFWPstepNstepThresh_Cnt_u16[0] t_AsstFWPstepNstepThresh_Cnt_u16[1]	202 527



Name	Input Value		
t_AsstFWVehSpd_Kph_u9p7[1]	19200		
t_AsstFWVehSpd_Kph_u9p7[2]	19328		
t_AsstFWVehSpd_Kph_u9p7[3]	19456		
t_AsstFWVehSpd_Kph_u9p7[4]	19584		
t_AsstFWVehSpd_Kph_u9p7[5]	19712		
t_AsstFWVehSpd_Kph_u9p7[6]	19840		
t_AsstFWVehSpd_Kph_u9p7[7]	19968		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-3		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.0999999		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	123		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_M	trNm_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_legendress and the property of the property of$	_lt tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph	_f32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.99000001	0.99000001 ± 4.88E-04	•
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0	0 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0	•
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.19999981	8.19999981 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.30499983	4.30499983 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-1	-1 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.15699983	3.15700006 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.99000001	0.99000001 ± 3.05E-05	•
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.19999981	8.19999981 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x00	0x00	•
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~

T →				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	•

Test Step 3.12 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0099999978
AssistFirewall_ActiveRawAcc_Cnt_M_u16	112
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00899999961
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00800000038
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00200000009
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	2.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	4.28000021
k_AsstFWNstep_Cnt_u16	3804
k_AsstFWPstep_Cnt_u16	1230



	(1,4,1,0,1,0,1,0,1,0,1,0,1,0,1,0,1,0,1,0,
Name	Input Value
k_RestoreThresh_MtrNm_f32	2
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6] t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2 AsstFWUprBoundX HwNm s4p11[2][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][2] t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-10240 -8192
	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4] t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5] t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7] t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-10240



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	256
t_AsstFWDefltAssistX_HwNm_u8p8[1]	282
t_AsstFWDefltAssistX_HwNm_u8p8[2]	307
t_AsstFWDefltAssistX_HwNm_u8p8[3]	333
t_AsstFWDefltAssistX_HwNm_u8p8[4] t_AsstFWDefltAssistX_HwNm_u8p8[5]	358 384
t_AsstFWDefitAssistX_HwNm_u8p8[6]	410
t_AsstFWDefitAssistX_HwNm_u8p8[7]	435
t_AsstFWDefitAssistX_HwNm_u8p8[8]	461
t_AsstFWDefltAssistX_HwNm_u8p8[9]	486
t_AsstFWDefltAssistX_HwNm_u8p8[10]	512
t_AsstFWDefltAssistX_HwNm_u8p8[11]	538
t_AsstFWDefltAssistX_HwNm_u8p8[12]	563
t_AsstFWDefltAssistX_HwNm_u8p8[13]	589
t_AsstFWDefltAssistX_HwNm_u8p8[14]	614
t_AsstFWDefltAssistX_HwNm_u8p8[15]	640
t_AsstFWDefltAssistX_HwNm_u8p8[16]	666
t_AsstFWDefltAssistX_HwNm_u8p8[17]	691
t_AsstFWDefltAssistX_HwNm_u8p8[18]	717
t_AsstFWDefltAssistX_HwNm_u8p8[19]	742
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	10240
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10240 12288
t_AsstFWDefltAssistY_MtrNm_s4p11[9] t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefitAssistY_MtrNm_s4p11[10]  t_AsstFWDefitAssistY_MtrNm_s4p11[11]	12288
t_AsstFWDefitAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefitAssistY_MtrNm_s4p11[13]	14336
t_AsstFWDefitAssistY_MtrNm_s4p11[14]	14336
t_AsstFWDefitAssistY_MtrNm_s4p11[14]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	18432
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	20480
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	24576
t_AsstFWPstepNstepThresh_Cnt_u16[0]	131
t_AsstFWPstepNstepThresh_Cnt_u16[1]	243



	le cons		
Name	Input Value		
t_AsstFWVehSpd_Kph_u9p7[0]	27904		
t_AsstFWVehSpd_Kph_u9p7[1]	28032		
t_AsstFWVehSpd_Kph_u9p7[2]	28160		
t_AsstFWVehSpd_Kph_u9p7[3]	28288		
t_AsstFWVehSpd_Kph_u9p7[4]	28416		
t_AsstFWVehSpd_Kph_u9p7[5]	28544		
t_AsstFWVehSpd_Kph_u9p7[6]	28672		
t_AsstFWVehSpd_Kph_u9p7[7]	28800		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	10		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	_Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_M	ltrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_le			
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.97000003	2.97000003 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	243	243 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	•
AssistFirewall_CombAsstSV_MtrNm_M_f32	1	1 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.97660005	1.97660005 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0079999	5.0079999 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	0.987999976	0.987999976 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	1	1 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>~</b>
Param_Cnt_T_u08	0x01	0x01	
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
			•

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	-

Test Step 3.13 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00800000038
AssistFirewall_ActiveRawAcc_Cnt_M_u16	121
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00899999961
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.03999996
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00600000005
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.099999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0500000007
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3
k_AsstFWInpLimitHFA_MtrNm_f32	4.5
k_AsstFWInpLimitHysComp_MtrNm_f32	5.75
k_AsstFWNstep_Cnt_u16	3432



Name	Input Value	
k_AsstFWPstep_Cnt_u16	1599	
k_RestoreThresh_MtrNm_f32	2.29999995	
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336	
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288	
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7] t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288	
	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]		
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384	
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288	
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384	
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336	
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288	
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048	
t2_Asst WorlboundX_HwNm_s4p11[3][10]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[6][1] t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048	
	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]		
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048	



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192
	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-4096
LZ_A55II-WOPIDOUNUT_WITHNITI_S4PTT[4][7]	
t2 AcetEWI In Round V M+rNm c4n44[4][9]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8] t2_AsstFWUprBoundY_MtrNm_s4p11[4][9] t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	0 2048



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	333
t_AsstFWDefltAssistX_HwNm_u8p8[1]	358
t_AsstFWDefltAssistX_HwNm_u8p8[2]	384
t_AsstFWDefltAssistX_HwNm_u8p8[3]	410
t_AsstFWDefltAssistX_HwNm_u8p8[4]	435
t_AsstFWDefltAssistX_HwNm_u8p8[5]	461
t_AsstFWDefltAssistX_HwNm_u8p8[6]	486
t_AsstFWDefltAssistX_HwNm_u8p8[7]	512
t_AsstFWDefltAssistX_HwNm_u8p8[8]	538
t_AsstFWDefltAssistX_HwNm_u8p8[9]	563
t_AsstFWDefltAssistX_HwNm_u8p8[10]	589 614
t_AsstFWDefltAssistX_HwNm_u8p8[11]	
t_AsstFWDefltAssistX_HwNm_u8p8[12] t_AsstFWDefltAssistX_HwNm_u8p8[13]	640 666
t AsstFWDefitAssistX HwNm u8p8[14]	691
t AsstFWDefitAssistX HwNm u8p8[15]	717
t_AsstFWDefitAssistX_HwNm_u8p8[16]	742
t_AsstFWDefitAssistX_HwNm_u8p8[17]	768
t_AsstFWDefitAssistX_HwNm_u8p8[18]	794
t_AsstFWDefltAssistX_HwNm_u8p8[19]	819
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720
t_AsstFWPstepNstepThresh_Cnt_u16[0]	134



Nama	Innut Value		
Name	Input Value		
t_AsstFWPstepNstepThresh_Cnt_u16[1]	255		
t_AsstFWVehSpd_Kph_u9p7[0]	36736		
t_AsstFWVehSpd_Kph_u9p7[1]	36864		
t_AsstFWVehSpd_Kph_u9p7[2]	36992		
t_AsstFWVehSpd_Kph_u9p7[3]	37120		
t_AsstFWVehSpd_Kph_u9p7[4]	37248		
t_AsstFWVehSpd_Kph_u9p7[5]	37376		
t_AsstFWVehSpd_Kph_u9p7[6]	37504		
t_AsstFWVehSpd_Kph_u9p7[7]	37632		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	8		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3.0999999		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	0		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.0999999		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	44		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lq	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	32 tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt	_enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.991999984	0.991999984 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	255	255 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	5	5 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.14589977	6.14589977 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.95799994	2.95799994 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.04500008	5.04500008 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.991999984	0.991999984 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	5	5 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	-

T ✓				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	•
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	•

Test Step 3.14 (Repeat Count = 1)		✓.
Name	Input Value	
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.30000019	
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.40000006	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487	
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.19999981	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11199999	
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.119999997	
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999	
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.219999999	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.80000019	
k_AsstFWInpLimitHFA_MtrNm_f32	6.40999985	
k_AsstFWInpLimitHysComp_MtrNm_f32	6.71000004	



Name	Input Value
k_AsstFWNstep_Cnt_u16	4052
k_AsstFWPstep_Cnt_u16	2460
k_RestoreThresh_MtrNm_f32	4.42999983
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10] t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_Asst WorlboundX_HwNm_s4p11[1][1] t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
10. A = 4 F \ A \       = D =	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	
t2_AsstFWUprBoundX_HwNm_s4p11[6][1] t2_AsstFWUprBoundX_HwNm_s4p11[6][2] t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0 2048



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1] t2 AsstFWUprBoundY MtrNm_s4p11[3][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
12_7.0001 VV OPTDOUTED 1_IVILLIVIII_0+P T T[+][ TU]	27010



	( -10-10
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
t2_AsstrWUprBoundY_MtrNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_Asst WopiBoundY_MtrNm_s4p11[7][4]	-6144
	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	947
t_AsstFWDefltAssistX_HwNm_u8p8[1]	947
t_AsstFWDefltAssistX_HwNm_u8p8[2]	998
t_AsstFWDefltAssistX_HwNm_u8p8[3]	998
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1408
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1408
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-204
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	0
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	6144
t_AsstFWDefitAssistY_MtrNm_s4p11[6]	6144
	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
C took Weene toolet Livitings ap 11[10]	
	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576 26624
t_AsstFWDefltAssistY_MtrNm_s4p11[16] t_AsstFWDefltAssistY_MtrNm_s4p11[17] t_AsstFWDefltAssistY_MtrNm_s4p11[18]	



Name	Input Value		
t_AsstFWPstepNstepThresh_Cnt_u16[0]	234		
t_AsstFWPstepNstepThresh_Cnt_u16[1]	655		
t_AsstFWVehSpd_Kph_u9p7[0]	19072		
t_AsstFWVehSpd_Kph_u9p7[1]	19200		
t_AsstFWVehSpd_Kph_u9p7[2]	19328		
t_AsstFWVehSpd_Kph_u9p7[3]	19456		
t_AsstFWVehSpd_Kph_u9p7[4]	19584		
t_AsstFWVehSpd_Kph_u9p7[5]	19712		
t_AsstFWVehSpd_Kph_u9p7[6]	19840		
t_AsstFWVehSpd_Kph_u9p7[7]	19968		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.19999981		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	1		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.5999999		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.4000001		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.5999999		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewall/	Active_Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistC	Cmd_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAs	ssist_MtrNm_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cntervice = 0.0000000000000000000000000000000000$	nt_l( tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc		
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HighFreqAss	sist_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisCo	omp_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counte	er_Cnt_enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpee	d_Kph_f32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-3.18000007	-3.18000007 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	655	655 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019	-8.80000019 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-6.06399965	-6.06400013 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-4.90400028	-4.90399981 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.79002142	2.79002142 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-8.80000019	-8.80000019 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T ✓				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	•
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 3.15 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.30000019
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.40000006
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.079999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11199999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.119999997
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.099999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.219999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.80000019
k_AsstFWInpLimitHFA_MtrNm_f32	6.40999985



12_AsstFWUprBoundX_HwNm_s4p1151][1] Name	-8192 Input Value
k_AsstFWInpLimitHysComp_MtrNm_f32	6.71000004
k_AsstFWNstep_Cnt_u16	4052
k_AsstFWPstep_Cnt_u16	2460
k_RestoreThresh_MtrNm_f32	4.42999983
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	=

 $t2\_AsstFWUprBoundX\_HwNm\_s4p1142][7]$ 



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
	-2046 0
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048
	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
:2_Asst WopiBoundY_MtrNm_s4p11[4][2]	8192
:2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
12_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
t2 AsstFWUprBoundY MtrNm s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	947 973
t_AsstFWDefltAssistX_HwNm_u8p8[1] t_AsstFWDefltAssistX_HwNm_u8p8[2]	998
t_AsstFWDefltAssistX_HwNm_u8p8[3]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[14] t_AsstFWDefltAssistX_HwNm_u8p8[15]	1306 1331
t AsstFWDefitAssistX HwNm u8p8[16]	1357
t_AsstFWDefitAssistX_HwNm_u8p8[17]	1382
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1408
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1434
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-204
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	0
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6] t_AsstFWDefltAssistY_MtrNm_s4p11[7]	6144 8192
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	8192
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672



Name	Input Value		
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720		
t_AsstFWPstepNstepThresh_Cnt_u16[0]	234		
t_AsstFWPstepNstepThresh_Cnt_u16[1]	655		
t_AsstFWVehSpd_Kph_u9p7[0]	19072		
t_AsstFWVehSpd_Kph_u9p7[1]	19200		
t_AsstFWVehSpd_Kph_u9p7[2]	19328		
t_AsstFWVehSpd_Kph_u9p7[3]	19456		
t_AsstFWVehSpd_Kph_u9p7[4]	19584		
t_AsstFWVehSpd_Kph_u9p7[5]	19712		
t_AsstFWVehSpd_Kph_u9p7[6]	19840		
t_AsstFWVehSpd_Kph_u9p7[7]	19968		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.19999981		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	1		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.5999999		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.4000001		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.5999999		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActiv	e_Uls_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32$	tgt_AssistFirewall_Per1_BaseAssistCmd_	MtrNm_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32$	tgt_AssistFirewall_Per1_CombinedAssist_	_MtrNm_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Defeat\_AsstTbl\_Service$	_lttgt_AssistFirewall_Per1_Defeat_AsstTbl_	Service_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_l	MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNi	m_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp	_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_C	nt_enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_K	ph_f32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-3.18000007	-3.18000007 ± 4.88E-04	<b>✓</b>
AssistFirewall_ActiveRawAcc_Cnt_M_u16	655	655 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019	-8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-6.06399965	-6.06400013 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-4.90400028	-4.90399981 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.79002142	2.79002142 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-8.80000019	-8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status Cnt T enum	0x01	0x01	<b>✓</b>

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	<b>~</b>
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 3.16 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0199999996
AssistFirewall_ActiveRawAcc_Cnt_M_u16	130
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.79999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0299999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.07000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00899999961
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0799999982
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.9000001



Name   Assert Windpuls (Windpuls (	
LastPWineCounty   Last   Las	
AsarWinderpoor U16   1988	
NadSW-Paper Ort UT6	
Seesing   Sees	
2. ASSPY/UPB BOUND, THANN_ 1947 10001   -8192   -8194   -819	
2. ASSP/VLyGeloud, Nebrus, 24(1901)	
2 ASSIN/UpiGenord, Nahm, apt 110 2    4096	
2. ABSEPTURE DOUBLE   NAME	
2. ASSEPTUJUSBOUNDX. Holm., pst-110161   0   2. ASSEPTUJUSBOUNDX. Holm., pst-110161   006   2. ASSEPTUJUSBOUNDX. Holm., pst-110161   006   2. ASSEPTUJUSBOUNDX. Holm., pst-110171   144   2. ASSEPTUJUSBOUNDX. Holm., pst-110181   1024   2. ASSEPTUJUSBOUNDX. Holm., pst-110181   0   2. ASSEPTUJUSBOUNDX. Holm., pst-110181	
2. ASSIPYU/piSchurdX. Heb/m. apti 1006   0.006   12. ASSIPYU/piSchurdX. Heb/m. apti 1006   0.006   12. ASSIPYU/piSchurdX. Heb/m. apti 1008   0.1024   1.006	
2. ASSIPVIJUPBOLINEX   Note:	
2. ASSET/WUPSCHOOK   Note: Asset   1001   1024	
12   ASSEPT/Up/BoundX, Hehm., selp 110  19    1228    12   228    12   238    12   248    248	
2_ASSEP_UNDSONCK_HAMPON_SEPTION[10]   12288   12_ASSEP_UNDSONCK_HAMPON_SEPTION[10]   6-1544   12_ASSEP_UNDSONCK_HAMPON_SEPTION[11]   4-0096   12_ASSEP_UNDSONCK_HAMPON_SEPTION[11]   4-0096   12_ASSEP_UNDSONCK_HAMPON_SEPTION[11]   7-0096   12_ASSEP_UNDSONCK_HAMPON_SEPTION[11]   7-0096   12_ASSEP_UNDSONCK_HAMPON_SEPTION[11]   7-0096   12_ASSEP_UNDSONCK_HAMPON_SEPTION[11]   7-0096   12_ASSEP_UNDSONCK_HAMPON_SEPTION[11]   7-0096   1-0096   12_ASSEP_UNDSONCK_HAMPON_SEPTION[11]   7-0096   1-0096	
2. ABSER/PURPSOUNDK, HANNIN, SEP11[19]	
2. ASSEPWUPBORNIX, HANNIN, SEP111  3     2048    2. ASSEPWUPBORNIX, HANNIN, SEP11  1  4    2048    2. ASSEPWUPBORNIX, HANNIN, SEP11  1  6    4056    2. ASSEPWUPBORNIX, HANNIN, SEP11  1  6    4056    2. ASSEPWUPBORNIX, HANNIN, SEP11  1  7    8152    2. ASSEPWUPBORNIX, HANNIN, SEP11  1  9    12288    2. ASSEPWUPBORNIX, HANNIN, SEP11  1  9    12288    2. ASSEPWUPBORNIX, HANNIN, SEP11  1  9    12388    2. ASSEPWUPBORNIX, HANNIN, SEP11  1  9    4056    2. ASSEPWUPBORNIX, HANNIN, SEP11  2  1    4058    2. ASSEPWUPBORNIX, HANNIN, SEP11  2  1    4054    2. ASSEPWUPBORNIX, HANNIN, SEP11  3  1    4058    2. ASSEPWUPBORNIX, HANNIN, SEP11  3  1   4058    2. ASSEPWUPBORNIX, HANNIN, SEP11  3  1   4058    2. ASSEPWUPBORNIX, HANNIN, SEP11  3  1   4058    2. ASSEPWUPBORNIX, HANNIN, SEP11  3  1   4058    2. ASSEPWUPBORNIX, HANNIN, SEP11  3  1   4058    2. ASSEPWUPBORNIX, HANNIN, SEP11  3  1   4058    2. ASSEPWUPBORNIX, HANNIN, SEP11  3  1   4058    2. ASSEPWUPBORNIX, HANNIN, SEP11  3  1   4058    2. ASSEPWUPBORNIX, HANNIN, SEP11  3  1   4058    2. ASSEPWUPBORNIX, HANNIN, SEP11  3  1   4058    2. ASSEPWUPBORNIX, HANNIN, SEP11  3  1   4058    2.	
22_assiPVUpRoundX_HwNn_s4p11[1]61   2048   22_assiPVUpRoundX_HwNn_s4p11[1]61   4056   22_assiPVUpRoundX_HwNn_s4p11[1]61   4056   22_assiPVUpRoundX_HwNn_s4p11[1]61   4056   4056   22_assiPVUpRoundX_HwNn_s4p11[1]71   8192   22_assiPVUpRoundX_HwNn_s4p11[1]61   4056   4	
2. ASSE/WUPDBoundX, HwNm. s4p11[1] 5    6144     2. ASSE/WUPDBoundX, HwNm. s4p11[1] 6    6144     3. ASSE/WUPDBoundX, HwNm. s4p11[1] 7    8192     3. ASSE/WUPDBoundX, HwNm. s4p11[1] 8    10240     3. ASSE/WUPDBoundX, HwNm. s4p11[1] 9    12288     3. ASSE/WUPDBoundX, HwNm. s4p11[1] 9    14336     3. ASSE/WUPDBoundX, HwNm. s4p11[2] 1   -6144     4. ASSE/WUPDBoundX, HwNm. s4p11[2] 1   -699     3. ASSE/WUPDBoundX, HwNm. s4p11[2] 2   -2048     3. ASSE/WUPDBoundX, HwNm. s4p11[2] 3   0     4. ASSE/WUPDBoundX, HwNm. s4p11[2] 3   0     5. ASSE/WUPDBoundX, HwNm. s4p11[2] 4   2048     5. ASSE/WUPDBoundX, HwNm. s4p11[2] 5   696     6. ASSE/WUPDBoundX, HwNm. s4p11[2] 6   6144     7. ASSE/WUPDBoundX, HwNm. s4p11[2] 9   6144     7. ASSE/WUPDBoundX, HwNm. s4p11[2] 9   6144     7. ASSE/WUPDBoundX, HwNm. s4p11[2] 9   1228     7. ASSE/WUPDBoundX, HwNm. s4p11[2] 9   14336     7. ASSE/WUPDBoundX, HwNm. s4p11[3] 0   -10240     7. ASSE/WUPDBoundX, HwNm. s4p11[3] 0   -10240     7. ASSE/WUPDBoundX, HwNm. s4p11[3] 0   -10240     7. ASSE/WUPDBoundX, HwNm. s4p11[3] 1   -8192	
2. AssEWUpFboundX, HwNm_s4p11[1]    10240   122888   12288   122888   12288   122888   122888   122888   122888   122888   122888   122888	
2. ASSETWUPPGOUNDX_HWNm_s4p117[1]91   12386   14336   12. ASSETWUPPGOUNDX_HWNm_s4p117[1]91   14336	
2. ASSIFWUPRBOUNDX_HWNm_s4p11[2  0    -6144   -6966       2. ASSIFWUPRBOUNDX_HWNm_s4p11[2  1]   -4096       2. ASSIFWUPRBOUNDX_HWNm_s4p11[2  3    0   0   0   0   0   0   0   0   0	
2_AssFWUprBoundX_HwnM_s4p11[2] 1   -4096	
12   AssFWUprBoundX   HwNm   s4p11 2  3    2048	
12_ASSIPWUprBoundX_HwNm_s4p11[2][4]   2048	
12_AssIFWUprBoundX_HwhM_s4p11[2][4]   2048   2048   2_AssIFWUprBoundX_HwhM_s4p11[2][6]   4096   40	
12_AssIFWUprBoundX_HwNm_s4p11[2] 5    4096     12_AssIFWUprBoundX_HwNm_s4p11[2] 6    6144     12_AssIFWUprBoundX_HwNm_s4p11[2] 8    10240     12_AssIFWUprBoundX_HwNm_s4p11[2] 8    10240     12_AssIFWUprBoundX_HwNm_s4p11[2] 8    10240     12_AssIFWUprBoundX_HwNm_s4p11[2] 9    12288     12_AssIFWUprBoundX_HwNm_s4p11[3] 0    10240     12_AssIFWUprBoundX_HwNm_s4p11[3] 0    10240     12_AssIFWUprBoundX_HwNm_s4p11[3] 1    8192     12_AssIFWUprBoundX_HwNm_s4p11[3] 1    8192     12_AssIFWUprBoundX_HwNm_s4p11[3] 3    4096     12_AssIFWUprBoundX_HwNm_s4p11[3] 3    4096     12_AssIFWUprBoundX_HwNm_s4p11[3] 6    2048     12_AssIFWUprBoundX_HwNm_s4p11[3] 6    2048     12_AssIFWUprBoundX_HwNm_s4p11[3] 6    2048     12_AssIFWUprBoundX_HwNm_s4p11[3] 9    8192     12_AssIFWUprBoundX_HwNm_s4p11[3] 9    8192     12_AssIFWUprBoundX_HwNm_s4p11[3] 9    2048     12_AssIFWUprBoundX_HwNm_s4p11[3] 9    2048     12_AssIFWUprBoundX_HwNm_s4p11[3] 9    3192     12_AssIFWUprBoundX_HwNm_s4p11[3] 9    3192     12_AssIFWUprBoundX_HwNm_s4p11[3] 9    2048     12_AssIFWUprBoundX_HwNm_s4p11[4] 1    0     12_AssIFWUprBoundX_HwNm_s4p11[4] 1    0     12_AssIFWUprBoundX_HwNm_s4p11[4] 1    0     12_AssIFWUprBoundX_HwNm_s4p11[4] 1    6     12_AssIFWUprBoundX_HwNm_s4p11[6] 2    6     12_AssIFWUprBoundX_HwNm_s4p11[6] 3    6     12_AssIFWUprBoundX_HwNm_s4p11[6] 5	
12_AssFWUprBoundX_HwNm_s4p11[2] 6   2_AssFWUprBoundX_HwNm_s4p11[2] 7   3_192   2_AssFWUprBoundX_HwNm_s4p11[2] 9   2_AssFWUprBoundX_HwNm_s4p11[2] 9   2_AssFWUprBoundX_HwNm_s4p11[2] 9   2_AssFWUprBoundX_HwNm_s4p11[2] 9   2_AssFWUprBoundX_HwNm_s4p11[2] 10   1_AssFWUprBoundX_HwNm_s4p11[3] 10   2_AssFWUprBoundX_HwNm_s4p11[3] 11   3_192   2_AssFWUprBoundX_HwNm_s4p11[3] 11   3_192   2_AssFWUprBoundX_HwNm_s4p11[3] 3   2_AssFWUprBoundX_HwNm_s4p11[3] 4   2_AssFWUprBoundX_HwNm_s4p11[3] 4   2_AssFWUprBoundX_HwNm_s4p11[3] 4   2_AssFWUprBoundX_HwNm_s4p11[3] 6   2_AssFWUprBoundX_HwNm_s4p11[3] 7   4_096   2_AssFWUprBoundX_HwNm_s4p11[3] 7   4_096   2_AssFWUprBoundX_HwNm_s4p11[3] 9   2_AssFWUprBoundX_HwNm_s4p11[3] 9   2_AssFWUprBoundX_HwNm_s4p11[3] 9   2_AssFWUprBoundX_HwNm_s4p11[3] 9   2_AssFWUprBoundX_HwNm_s4p11[3] 9   2_AssFWUprBoundX_HwNm_s4p11[4] 10   2_AssFWUprBoundX_HwNm_s4p11[4] 10   2_AssFWUprBoundX_HwNm_s4p11[4] 11   0_12_AssFWUprBoundX_HwNm_s4p11[4] 11   0_2_AssFWUprBoundX_HwNm_s4p11[4] 11   0_AssFWUprBoundX_HwNm_s4p11[4] 11   0_AssFWUprBoundX_HwNm_s4p11[5] 11   0_AssFWUprBoundX_HwNm_s4p11[5] 11   0_AssFWUprBoundX_HwNm_s4p11[5] 11   0_AssFWUprBoundX_HwNm_s4p11[5] 11   0_AssFWUprBoundX_HwNm_s4p11[5] 11   0_AssFWUprBoundX_HwN	
12_AssiFWUprBoundX_HwNm_s4p112  T    2_AssiFWUprBoundX_HwNm_s4p112  S    10240   12288   10240   12_AssiFWUprBoundX_HwNm_s4p112  S    10240   12_AssiFWUprBoundX_HwNm_s4p112  S    12_AssiFWUprBoundX_HwNm_s4p112  S    12_AssiFWUprBoundX_HwNm_s4p113  S    10240   12_AssiFWUprBoundX_HwNm_s4p113  S    10240   12_AssiFWUprBoundX_HwNm_s4p113  S    12_AssiFWUprBoundX_HwNm_s4p114  S    14_AssiFWUprBoundX_HwNm_s4p114  S    14_AssiFWUprBoundX_HwNm_s4p115  S    14_AssiFWUprBoundX_HwNm_s4p115  S    14_AssiFWUprBoundX_HwNm_s4p115  S    14_AssiFWUprBoundX_HwNm_s4p115  S    14_AssiFWUprBoundX_HwNm_s4p115  S    14_AssiFWUprBoundX_HwNm_s4p115  S	
2. AssiFWUprBoundX_HwNm_s4p11[2][8]   10240   12288   10240   12288   12288   10240   12288	
12_AssiFWUprBoundX_HwNm_s4p11[2][9]	
12   AsstFWUprBoundX   HwNm_s4p11[2] 10    10240   1	
12_AsstFWUprBoundX_HwNm_s4p11[3][0] -10240 12_AsstFWUprBoundX_HwNm_s4p11[3][1] -8192 12_AsstFWUprBoundX_HwNm_s4p11[3][2] -6144 12_AsstFWUprBoundX_HwNm_s4p11[3][3] -4096 12_AsstFWUprBoundX_HwNm_s4p11[3][4] -2048 12_AsstFWUprBoundX_HwNm_s4p11[3][6] -2048 12_AsstFWUprBoundX_HwNm_s4p11[3][6] -2048 12_AsstFWUprBoundX_HwNm_s4p11[3][6] -2048 12_AsstFWUprBoundX_HwNm_s4p11[3][7] -4096 12_AsstFWUprBoundX_HwNm_s4p11[3][8] -6144 12_AsstFWUprBoundX_HwNm_s4p11[3][9] -8192 12_AsstFWUprBoundX_HwNm_s4p11[3][0] -2048 12_AsstFWUprBoundX_HwNm_s4p11[4][0] -2048 12_AsstFWUprBoundX_HwNm_s4p11[4][0] -2048 12_AsstFWUprBoundX_HwNm_s4p11[4][2] -2048 12_AsstFWUprBoundX_HwNm_s4p11[4][2] -2048 12_AsstFWUprBoundX_HwNm_s4p11[4][2] -2048 12_AsstFWUprBoundX_HwNm_s4p11[4][3] -6144 12_AsstFWUprBoundX_HwNm_s4p11[4][3] -6144 12_AsstFWUprBoundX_HwNm_s4p11[4][6] -10240 12_AsstFWUprBoundX_HwNm_s4p11[6][6] -4096 12_AsstFWUprBoundX_HwNm_s4p11[6][6] -4096 12_AsstFWUprBoundX_HwNm_s4p11[6][6] -0086 12_AsstFWUprBoundX_HwNm_s4p11[6][6] -0086 12_AsstFWUprBoundX_HwNm_s4p11[6][6] -0086 12_AsstFWUprBoundX_HwNm_s4p11[6][6] -0086 12_AsstFWUprBoundX_HwNm_s4p11[6][6] -0096 12_AsstFWUprBo	
12_AssiFWUprBoundX_HwNm_s4p11[3][1]       -8192         12_AssiFWUprBoundX_HwNm_s4p11[3][2]       -6144         12_AssiFWUprBoundX_HwNm_s4p11[3][3]       -4096         12_AssiFWUprBoundX_HwNm_s4p11[3][6]       -2048         12_AssiFWUprBoundX_HwNm_s4p11[3][6]       0         12_AssiFWUprBoundX_HwNm_s4p11[3][7]       4096         12_AssiFWUprBoundX_HwNm_s4p11[3][8]       0         12_AssiFWUprBoundX_HwNm_s4p11[3][8]       6144         12_AssiFWUprBoundX_HwNm_s4p11[3][9]       8192         12_AssiFWUprBoundX_HwNm_s4p11[4][0]       10240         12_AssiFWUprBoundX_HwNm_s4p11[4][0]       2048         12_AssiFWUprBoundX_HwNm_s4p11[4][1]       0         12_AssiFWUprBoundX_HwNm_s4p11[4][3]       4096         12_AssiFWUprBoundX_HwNm_s4p11[4][3]       4096         12_AssiFWUprBoundX_HwNm_s4p11[4][3]       4096         12_AssiFWUprBoundX_HwNm_s4p11[4][6]       6144         12_AssiFWUprBoundX_HwNm_s4p11[4][6]       10240         12_AssiFWUprBoundX_HwNm_s4p11[4][6]       10240         12_AssiFWUprBoundX_HwNm_s4p11[4][6]       10240         12_AssiFWUprBoundX_HwNm_s4p11[4][6]       14336         12_AssiFWUprBoundX_HwNm_s4p11[4][6]       14336         12_AssiFWUprBoundX_HwNm_s4p11[6][6]       4096         12_AssiFWUprBoundX_HwNm_s4p11[6][6	
12_AssiFWUprBoundX_HwNm_s4p11[3][1]       -8192         12_AssiFWUprBoundX_HwNm_s4p11[3][2]       -6144         12_AssiFWUprBoundX_HwNm_s4p11[3][3]       -4096         12_AssiFWUprBoundX_HwNm_s4p11[3][6]       -2048         12_AssiFWUprBoundX_HwNm_s4p11[3][6]       0         12_AssiFWUprBoundX_HwNm_s4p11[3][7]       4096         12_AssiFWUprBoundX_HwNm_s4p11[3][8]       0         12_AssiFWUprBoundX_HwNm_s4p11[3][8]       6144         12_AssiFWUprBoundX_HwNm_s4p11[3][9]       8192         12_AssiFWUprBoundX_HwNm_s4p11[4][0]       10240         12_AssiFWUprBoundX_HwNm_s4p11[4][0]       2048         12_AssiFWUprBoundX_HwNm_s4p11[4][1]       0         12_AssiFWUprBoundX_HwNm_s4p11[4][3]       4096         12_AssiFWUprBoundX_HwNm_s4p11[4][3]       4096         12_AssiFWUprBoundX_HwNm_s4p11[4][3]       4096         12_AssiFWUprBoundX_HwNm_s4p11[4][6]       6144         12_AssiFWUprBoundX_HwNm_s4p11[4][6]       10240         12_AssiFWUprBoundX_HwNm_s4p11[4][6]       10240         12_AssiFWUprBoundX_HwNm_s4p11[4][6]       10240         12_AssiFWUprBoundX_HwNm_s4p11[4][6]       14336         12_AssiFWUprBoundX_HwNm_s4p11[4][6]       14336         12_AssiFWUprBoundX_HwNm_s4p11[6][6]       4096         12_AssiFWUprBoundX_HwNm_s4p11[6][6	
12_AsstFWUprBoundX_HwNm_s4p11[3][2]       -6144         12_AsstFWUprBoundX_HwNm_s4p11[3][4]       -2048         12_AsstFWUprBoundX_HwNm_s4p11[3][5]       0         12_AsstFWUprBoundX_HwNm_s4p11[3][6]       2048         12_AsstFWUprBoundX_HwNm_s4p11[3][7]       4096         12_AsstFWUprBoundX_HwNm_s4p11[3][8]       6144         12_AsstFWUprBoundX_HwNm_s4p11[3][9]       8192         12_AsstFWUprBoundX_HwNm_s4p11[3][10]       10240         12_AsstFWUprBoundX_HwNm_s4p11[4][0]       -2048         12_AsstFWUprBoundX_HwNm_s4p11[4][1]       0         12_AsstFWUprBoundX_HwNm_s4p11[4][2]       2048         12_AsstFWUprBoundX_HwNm_s4p11[4][3]       4096         12_AsstFWUprBoundX_HwNm_s4p11[4][4]       6144         12_AsstFWUprBoundX_HwNm_s4p11[4][4]       6144         12_AsstFWUprBoundX_HwNm_s4p11[4][5]       8192         12_AsstFWUprBoundX_HwNm_s4p11[4][6]       10240         12_AsstFWUprBoundX_HwNm_s4p11[4][6]       10240         12_AsstFWUprBoundX_HwNm_s4p11[4][7]       1228         12_AsstFWUprBoundX_HwNm_s4p11[4][6]       14336         12_AsstFWUprBoundX_HwNm_s4p11[4][6]       14336         12_AsstFWUprBoundX_HwNm_s4p11[5][0]       4096         12_AsstFWUprBoundX_HwNm_s4p11[5][0]       4096         12_AsstFWUprBoundX_HwNm_s4p11[5]	
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12_AsstFWUprBoundX_HwNm_s4p11[4][6]       10240         12_AsstFWUprBoundX_HwNm_s4p11[4][7]       12288         12_AsstFWUprBoundX_HwNm_s4p11[4][8]       14336         12_AsstFWUprBoundX_HwNm_s4p11[4][9]       16384         12_AsstFWUprBoundX_HwNm_s4p11[4][10]       18432         12_AsstFWUprBoundX_HwNm_s4p11[5][0]       -4096         12_AsstFWUprBoundX_HwNm_s4p11[5][1]       -2048         12_AsstFWUprBoundX_HwNm_s4p11[5][2]       0         12_AsstFWUprBoundX_HwNm_s4p11[5][3]       2048         12_AsstFWUprBoundX_HwNm_s4p11[5][4]       4096         12_AsstFWUprBoundX_HwNm_s4p11[5][5]       6144	
12_AsstFWUprBoundX_HwNm_s4p11[4][7]	
12_AsstFWUprBoundX_HwNm_s4p11[4][8]       14336         12_AsstFWUprBoundX_HwNm_s4p11[4][9]       16384         12_AsstFWUprBoundX_HwNm_s4p11[4][10]       18432         12_AsstFWUprBoundX_HwNm_s4p11[5][0]       -4096         12_AsstFWUprBoundX_HwNm_s4p11[5][1]       -2048         12_AsstFWUprBoundX_HwNm_s4p11[5][2]       0         12_AsstFWUprBoundX_HwNm_s4p11[5][3]       2048         12_AsstFWUprBoundX_HwNm_s4p11[5][4]       4096         12_AsstFWUprBoundX_HwNm_s4p11[5][5]       6144	
12_AsstFWUprBoundX_HwNm_s4p11[4]]9] 16384 12_AsstFWUprBoundX_HwNm_s4p11[4][10] 18432 12_AsstFWUprBoundX_HwNm_s4p11[5][0] -4096 12_AsstFWUprBoundX_HwNm_s4p11[5][1] -2048 12_AsstFWUprBoundX_HwNm_s4p11[5][2] 0 12_AsstFWUprBoundX_HwNm_s4p11[5][3] 2048 12_AsstFWUprBoundX_HwNm_s4p11[5][4] 4096 12_AsstFWUprBoundX_HwNm_s4p11[5][5] 6144	
12_AsstFWUprBoundX_HwNm_s4p11[4][10]       18432         12_AsstFWUprBoundX_HwNm_s4p11[5][0]       -4096         12_AsstFWUprBoundX_HwNm_s4p11[5][1]       -2048         12_AsstFWUprBoundX_HwNm_s4p11[5][2]       0         12_AsstFWUprBoundX_HwNm_s4p11[5][3]       2048         12_AsstFWUprBoundX_HwNm_s4p11[5][4]       4096         12_AsstFWUprBoundX_HwNm_s4p11[5][5]       6144	
12_AsstFWUprBoundX_HwNm_s4p11[5][0]       -4096         12_AsstFWUprBoundX_HwNm_s4p11[5][1]       -2048         12_AsstFWUprBoundX_HwNm_s4p11[5][2]       0         12_AsstFWUprBoundX_HwNm_s4p11[5][3]       2048         12_AsstFWUprBoundX_HwNm_s4p11[5][4]       4096         12_AsstFWUprBoundX_HwNm_s4p11[5][5]       6144	
12_AsstFWUprBoundX_HwNm_s4p11[5][1]       -2048         12_AsstFWUprBoundX_HwNm_s4p11[5][2]       0         12_AsstFWUprBoundX_HwNm_s4p11[5][3]       2048         12_AsstFWUprBoundX_HwNm_s4p11[5][4]       4096         12_AsstFWUprBoundX_HwNm_s4p11[5][5]       6144	
12_AsstFWUprBoundX_HwNm_s4p11[5][2]       0         12_AsstFWUprBoundX_HwNm_s4p11[5][3]       2048         12_AsstFWUprBoundX_HwNm_s4p11[5][4]       4096         12_AsstFWUprBoundX_HwNm_s4p11[5][5]       6144	
12_AsstFWUprBoundX_HwNm_s4p11[5][3]       2048         12_AsstFWUprBoundX_HwNm_s4p11[5][4]       4096         12_AsstFWUprBoundX_HwNm_s4p11[5][5]       6144	
t2_AsstFWUprBoundX_HwNm_s4p11[5][4] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[5][5] 6144	
12_AsstFWUprBoundX_HwNm_s4p11[5][5] 6144	
tz_Asst+wuprBoundX_HwNm_s4p11[5][6] 8192	
t2_AsstFWUprBoundX_HwNm_s4p11[5][7] 10240	
t2_AsstFWUprBoundX_HwNm_s4p11[5][8] 12288	
t2_AsstFWUprBoundX_HwNm_s4p11[5][9] 14336	
t2_AsstFWUprBoundX_HwNm_s4p11[5][10] 16384	
t2_AsstFWUprBoundX_HwNm_s4p11[6][0] 0	
12_AsstFWUprBoundX_HwNm_s4p11[6][1] 2048	



Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	18432
	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	4096
re	1000



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	22528 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	410
t_AsstFWDefltAssistX_HwNm_u8p8[1]	435
t_AsstFWDefltAssistX_HwNm_u8p8[2]	461 486
t_AsstFWDefltAssistX_HwNm_u8p8[3]	512
t_AsstFWDefltAssistX_HwNm_u8p8[4] t_AsstFWDefltAssistX_HwNm_u8p8[5]	538
t_AsstFWDefltAssistX_HwNm_u8p8[6]	563
t_AsstFWDefitAssistX_HwNm_u8p8[7]	589
t_AsstFWDefltAssistX_HwNm_u8p8[8]	614
t_AsstFWDefltAssistX_HwNm_u8p8[9]	640
t_AsstFWDefltAssistX_HwNm_u8p8[10]	666
t_AsstFWDefltAssistX_HwNm_u8p8[11]	691
t AsstFWDefltAssistX HwNm u8p8[12]	717
t_AsstFWDefltAssistX_HwNm_u8p8[13]	742
t_AsstFWDefltAssistX_HwNm_u8p8[14]	768
t_AsstFWDefltAssistX_HwNm_u8p8[15]	794
t_AsstFWDefltAssistX_HwNm_u8p8[16]	819
t_AsstFWDefltAssistX_HwNm_u8p8[17]	845
t_AsstFWDefltAssistX_HwNm_u8p8[18]	870
t_AsstFWDefltAssistX_HwNm_u8p8[19]	896
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	5324
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	5529
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6348
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	6553
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	7372
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	7577
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	7987 8192
t_AsstFWDefltAssistY_MtrNm_s4p11[15] t_AsstFWDefltAssistY_MtrNm_s4p11[16]	8396
	10000



Name	Input Value		
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	8806		
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	9011		
t_AsstFWPstepNstepThresh_Cnt_u16[0]	137		
t_AsstFWPstepNstepThresh_Cnt_u16[1]	267		
t_AsstFWVehSpd_Kph_u9p7[0]	45568		
t_AsstFWVehSpd_Kph_u9p7[1]	45696		
t_AsstFWVehSpd_Kph_u9p7[2]	45824		
t_AsstFWVehSpd_Kph_u9p7[3]	45952		
t_AsstFWVehSpd_Kph_u9p7[4]	46080		
t_AsstFWVehSpd_Kph_u9p7[5]	46208		
t_AsstFWVehSpd_Kph_u9p7[6]	46336		
t_AsstFWVehSpd_Kph_u9p7[7]	46464		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3.0999999		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.0999999		
tgt AssistFirewall Per1 HwTorque HwNm f32.value	-2		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-8.80000019		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	77.1999969		
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 AsstFirewallActive UIs f32	tgt AssistFirewall Per1 AsstFirewallActive	Uls f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_M	trNm f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_M		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	-		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mt	•	
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 HwTorque HwNm f32	tgt AssistFirewall Per1 HwTorque HwNm		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_N	- /trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.92000008	3.92000008 ± 4.88E-04	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	267	267 ± 1	<b>~</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	
AssistFirewall_CombAsstSV_MtrNm_M_f32	-2.89990234	-2.89990234 ± 4.88E-04	<b>✓</b>
AssistFirewall HiFregKSV M str.LPF Str.SV Uls f32	3.01799989	3.01799989 ± 4.88E-04	
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.8829999	5.8829999 ± 4.88E-04	•
AssistFirewall PNCountStatus Cnt M lqc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.07999992	2.07999992 ± 4.88E-04	~
tgt AssistFirewall Per1 AsstFirewallActive Uls f32.value	1	1 ± 3.05E-05	
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-2.89990234	-2.89990234 ± 9.77E-04	·
NTC_Cnt_T_enum	0xC6	0xC6	
Param_Cnt_T_u08	0x01	0x01	_
Status_Cnt_T_enum	0x01	0x01	
NTC Cnt T enum	0xC9	0xC9	·
Param_Cnt_T_u08	0x01	0x01	_
Status Cnt T enum	0x01	0x01	•
		1	

T				~
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

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AssistFirewall\_Init1

 Project
 AssistFirewall

 Module
 AssistFireWall

 Test Object
 AssistFirewall\_Init1

#### Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

#### **Statistics**

Total Testcases	1	
Successful	1	~
Failed	0	
Not Executed	0	

#### **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\AssistFirewall
Configuration File	D:\Synergy_Work_Area\AssistFirewall\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\src\Ap_AssistFirewall.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -DBC_ASSISTFIREWALL_FAULTINJECTIONPOINT=STD_OFF -I\$(PROJECTROOT)\utp\contract \Ap_AssistFirewall -I\$(PROJECTROOT)\utp\contract -I\$(PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include -I\$ (Compiler Install Path)\include
File	\$(PROJECTROOT)\NxtrLib\src\interpolation.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -DBC_ASSISTFIREWALL_FAULTINJECTIONPOINT=STD_OFF -I\$(PROJECTROOT)\utp\contract \Ap_AssistFirewall -I\$(PROJECTROOT)\utp\contract -I\$(PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include -I\$ (Compiler Install Path)\include

Comments/Description/Spe	ecification
Name	Text
Module 'AssistFireWall'	Name of Tester:Ankita Bhardwaj Code File(s) Under Test:Ap_AssistFirewall.c Code File(s) Version:14 Module Design Document:Assist_Firewall_MDD.docx Module Design Document Version:14 Data Dictionary Version:16 Unit Test Plan Version:11 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.31 Total FLASH Used (Bytes):1568 Total RAM Used (Bytes):1568 Total RAM Used (Bytes):480 Special Test Requirements: Test Date:03-23-2015 Comments:"NOTE:1) Inline functions defined in GlobalMacro.h are not Unit Tested. 2)""CBD_Sandbox_dbg.map""map file is embedded for reference. 3) In ""AssistFirewall_Per1" function, ""Defeat_AsstTbl_Service_Cnt_Igc" always kept FALSE to make ""if((DefeatAsstTblSvc_Cnt_T_Igc <> D_FALSE_CNT_LGC) And (MECCounter_Cnt_T_enum <> ProductionMode))"" condition FALSE except Boundray Test for variables used in Condition and Path coverage. "
Test Object 'AssistFirewall_Init1'	

Attributes	
Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd

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AssistFirewall\_Init1

Attributes	
Name	Value
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	\$(ProgramFiles)\pls\UDE 3.2
Time Unit	Cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\AssistFirewall\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP



#### Test Case 1: Boundary Test

Performance Metrics (With "None" Instrumentation and WithPS Environment)
CPU Cycles: Specification

TC1.1 1813.00 Cycles TC1.2 1820.00 Cycles TC1.3 1820.00 Cycles TC1.4 1820.00 Cycles TC1.5 1820.00 Cycles TC1.6 1820.00 Cycles TC1.7 1820.00 Cycles TC1.8 1820.00 Cycles

Description Vector Description

TS1.1k\_AsstFWFiltKn\_Hz\_f32 = min TS1.2k\_AsstFWFiltKn\_Hz\_f32 = max TS1.3k\_AsstFWFiltKn\_Hz\_f32 = mid TS1.4k\_AsstFWFWActiveLPF\_Hz\_f32 = min TS1.5k\_AsstFWFWActiveLPF\_Hz\_f32 = max TS1.6k\_AsstFWFWActiveLPF\_Hz\_f32 = mid TS1.7AII min TS1.8All max

Test Step 1.1 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
k_AsstFWFWActiveLPF_Hz_f32	40.0999985		
k_AsstFWFiltKn_Hz_f32	0.10000001		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.395837128	0.395837128 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00062871	1.00062859 ± 6.10E-05	•
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	<b>~</b>

Test Step 1.2 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
k_AsstFWFWActiveLPF_Hz_f32	50.2999992		
k_AsstFWFiltKn_Hz_f32	100		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.46851933	0.46851933 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	2.09537983	2.09537959 ± 6.10E-05	✓
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	<b>✓</b>
AssistFirewall UprBoundKSV M str.K Uls f32	0.715390444	0.715390444 ± 1.53E-05	<b>✓</b>

Test Step 1.3 (Repeat Count = 1)			✓
Name	Input Value		
k_AsstFWFWActiveLPF_Hz_f32	60.4000015		
k_AsstFWFiltKn_Hz_f32	50.2999992		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.531869829	0.531869769 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.46851933	0.46851933 ± 1.53E-05	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.41246235	1.41246235 ± 6.10E-05	•
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.46851933	0.46851933 ± 1.53E-05	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.46851933	0.46851933 ± 1.53E-05	<b>✓</b>

Test Step 1.4 (Repeat Count = 1)			<b>✓</b>
Name	Input Value		
k_AsstFWFWActiveLPF_Hz_f32	0.10000001		
k_AsstFWFiltKn_Hz_f32	10.1999998		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.12030232	0.120302327 ± 1.53E-05	•
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.06748891	1.06748891 ± 6.10E-05	~
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.12030232	0.120302327 ± 1.53E-05	•
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.12030232	0.120302327 ± 1.53E-05	<b>~</b>





Test Step 1.5 (Repeat Count = 1)			✓
Name	Input Value		
k_AsstFWFWActiveLPF_Hz_f32	100		
k_AsstFWFiltKn_Hz_f32	20.2999992		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.22515893	0.225158915 ± 1.53E-05	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.14153636	1.14153647 ± 6.10E-05	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.22515893	0.225158915 ± 1.53E-05	✓
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.22515893	0.225158915 ± 1.53E-05	<b>✓</b>

Test Step 1.6 (Repeat Count = 1)			✓
Name	Input Value		
k_AsstFWFWActiveLPF_Hz_f32	50.2999992		
k_AsstFWFiltKn_Hz_f32	30.1000004		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.46851933	0.46851933 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.31493926	0.31493926 ± 1.53E-05	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.22104383	1.22104394 ± 6.10E-05	✓
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.31493926	0.31493926 ± 1.53E-05	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.31493926	0.31493926 ± 1.53E-05	<b>✓</b>

Test Step 1.7 (Repeat Count = 1)			✓
Name	Input Value		
k_AsstFWFWActiveLPF_Hz_f32	0.10000001		
k_AsstFWFiltKn_Hz_f32	0.100000001		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00062871	1.00062859 ± 6.10E-05	~
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	✓
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	~

Test Step 1.8 (Repeat Count = 1)			✓
Name	Input Value		
k_AsstFWFWActiveLPF_Hz_f32	100		
k_AsstFWFiltKn_Hz_f32	100		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	✓
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	2.09537983	2.09537959 ± 6.10E-05	✓
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	✓
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	✓