

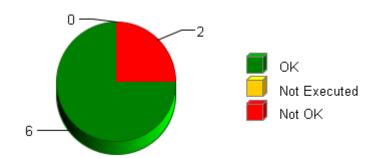
#### Summary

Total Test Objects: 8
Successful: 6

Failed: 2
Not Executed: 0

**Date:** 2014-10-14 **Time:** 23:47:43+0530

# **Overall Test Object Results (including Coverage)**



#### **Selected Project Items**

Test Collection "CBD\_UnitTest"

#### **Used Test Environments**

TI TMS 570 PLS UDE (Default)

#### **Batch Operation Settings**

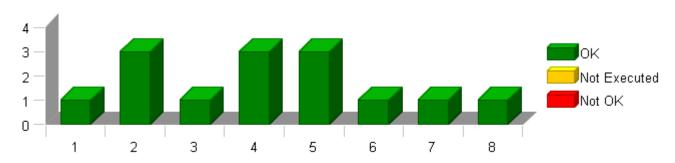
Check Interface: No
Generate Driver: Yes
Execute Test: Yes
Create New Test Run: No

**Instrumentation:** Test Object Only

Coverage: Statement Coverage, Branch Coverage, Modified Condition / Decision Coverage,

Multiple Condition Coverage

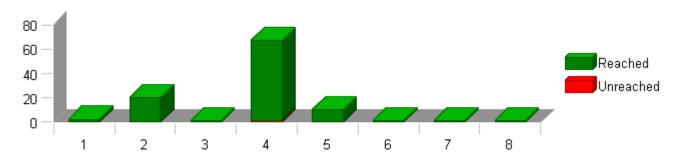
#### **Test Case Results for Each Test Object (without Coverage)**



The table above shows each test object on the x axis and the number of test cases of the respective test object on the y axis. Each bar is divided into passed, not executed and failed test cases. The test case results do not take into account any coverage result (i.e. if all test cases of a test object are passed in this table but the coverage is failed, the overall test object result will be failed).

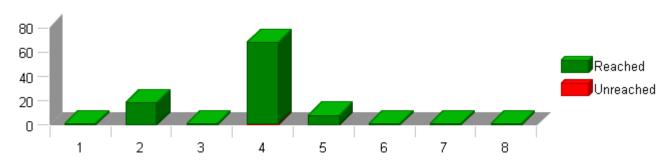


#### Statement (C0) Coverage: Total Statements for Each Test Object



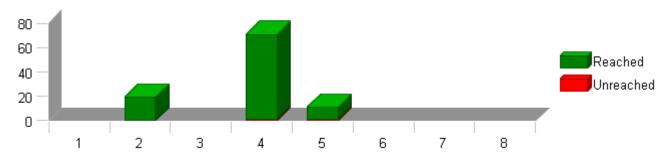
The table above shows each test object on the x axis and the number of statements of the respective test object on the y axis. Each bar is divided into reached statements (i.e. statements that have been executed during the test) and unreached statements.

#### Branch (C1) Coverage: Total Branches for Each Test Object



The table above shows each test object on the x axis and the number of branches of the respective test object on the y axis. Each bar is divided into reached branches (i.e. branches that have been executed during the test) and unreached branches.

#### MC/DC Coverage: Total Condition Combinations for Each Test Object

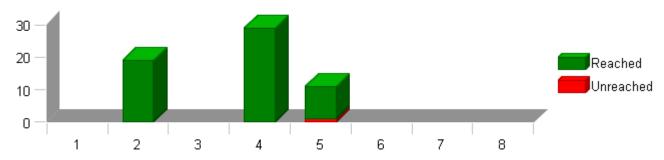


The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MC/DC coverage, each decision requires all contained atomic conditions to evaluate to both true and false independently of all other conditions. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.



#### MCC Coverage: Total Condition Combinations for Each Test Object



The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MCC coverage, each decision requires all contained atomic conditions to evaluate to all possible combinations of true and false values. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.



#### **Test Object List**

The following table lists all test objects with their test case and coverage results. The cumulated results for modules, folders and test collections are also displayed, the indentation within the name column indicates the parent relationship of the elements.

Please note that only test objects are numbered within the first column. This number is referenced on the x axis within the overview charts for test case and coverage results available on previous pages (if included into the report).

No.	Name	C0	C1	MC/DC	МСС	Test Cases Result
	DigColPsInt	99.02 %	98.98 %	98.01 %	98.3 %	14 of 14 passed
	CBD_UnitTest	99.02 %	98.98 %	98.01 %	98.3 %	14 of 14 passed
	DigColPsInt	99.02 %	98.98 %	98.01 %	98.3 %	14 of 14 passed
1	DigColPsInt_GetCustData	100 %	100 %	-	-	1 of 1 passed
2	<u>DigColPsInt_GetData</u>	100 %	100 %	100 %	100 %	3 of 3 passed
3	DigColPsInt Init	100 %	100 %	-	-	1 of 1 passed
4	DigColPsInt InterruptNotification	98.5 %	98.52 %	98.59 %	100 %	3 of 3 passed
5	<u>DigColPsInt_StartRequest</u>	100 %	100 %	90.9 %	90.9 %	3 of 3 passed
6	<u>SetupRead</u>	100 %	100 %	-	-	1 of 1 passed
7	<u>SetupWriteData</u>	100 %	100 %	-	-	1 of 1 passed
8	<u>SetupWriteRegister</u>	100 %	100 %	-	-	1 of 1 passed

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DigColPsInt\_GetData

 Project
 DigColPsInt

 Module
 DigColPsInt

 Test Object
 DigColPsInt\_GetData

#### Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %
MCC Coverage	100 %
MC/DC Coverage	100 %

#### **Statistics**

Total Testcases	3	
Successful	3	~
Failed	0	
Not Executed	0	

#### **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\C1xx_DigColPs
Configuration File D:\Synergy_Work_Area\C1xx_DigColPs\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xr	
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\DigColPs\src\Sa_DigColPsInt.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -DSTATIC= -D_inline= -I\$(PROJECTROOT)\DigColPs\utp\contract -I\$(PROJECTROOT)\DigColPs\utp\contract -I\$(PROJECTROOT)\DigColPs\utp\contract\Sa_DigColPs -I\$(PROJECTROOT)\DigColPs\utp\contract\Sa_DigColPs -I\$(PROJECTROOT)\StdDef\unclude -I\$(PROJECTROOT)\StdDef\undet\unclude -I\$(PROJECTROOT)\StdDef\unclude -I\$(PROJECTROOT)\StdDef\unclude -I\$(PROJECTROOT)\StdDef\undet\undle -I\$(PROJECTROOT)\StdDef\undle -I\$(PROJECTROOT)\StdDef\undle -I\$(PROJECTROOT)\StdDe

Comments/Description/Spe	ecification
Name	Text





Module 'DigColPsInt' 

Name of Tester:Priti Mangalekar Code File(s) Under Test:Sa\_DigColPsInt.c Code File(s) Version:7

Module Design Document:DigColPsInt\_MDD.docx Module Design Document Version:8

Data Dictionary Version:9 Unit Test Plan Version:2

Offit Test Flat Version:2
Optimization Level:Level 2
Compiler (CodeGen) Version:TMS470\_4.9.5
Model Type:Excel Macro
Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.30
Total FLASH Used (Bytes):N/A
Total RAM Used (Bytes):N/A

Total CALS Used (Bytes):N/A Special Test Requirements: Test Date:10/13/2014 Comments:

NOTE 1: In """"DigColPsInt\_StartRequest"""" function, path """"(Type\_Cnt\_T\_u08 > D\_NONE\_CNT\_U08) = TRUE && (Type\_Cnt\_T\_u08 <= D\_STATUSREG\_CNT\_U08) = FALSE""" cannot be covered because range of """"Type\_Cnt\_T\_u08"""" is '0-5' and value of """D\_STATUSREG\_CNT\_U08""" is '34'.

NOTE2: In function ""DigColPsInt\_GetData"",""DigColPsInt\_StartRequest"" and ""DigColPsInt\_InterruptNotification"" values for """12c\_Send(Length\_Cnt\_T\_u32)"""", """12c\_SetRecv(Length\_Cnt\_T\_u16)"""", """12c\_SetStatus(Status\_Cnt\_T\_u16)""", """12c\_SetUpMasterReceive(DataLength\_Cnt\_T\_u16)""" and 12c\_SetUpMasterTransmit(DataLength\_Cnt\_T\_u16) are ignored in few vectors as they

are taking garbage value when they are not updated with expected value in particular vector.

NOTE3: The return value of """"DigColPsInt\_GetData""" function is going out of range, anomaly """6156""" is raised for the same.

NOTE4:Range of DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum is considered as 0 to 36, as enum DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum is of type CommStepType which is of 37 elements.

NOTE5:In function ""DigColPsInt\_InterruptNotification"", path ""Case I2C\_RECV\_OVERRUN: True"" cannot be covered because range of ""Flags\_Cnt\_T\_b16"" is 0 to 64 given in MDD.

NOTE6:In function ""DigColPsInt\_InterruptNotification"", output variable ""DigColPsInt\_AttempOccurForCustDatRead\_Cnt\_M\_u08"" is going out

of range.'

Attributes		
Name	Value	
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5	
Float Precision 9		
InitObjDir \$(PROJECTROOT)\UnitTestEnv\static_build_files\obj		
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src	
Linker File \$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd		
Makefile Template \$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl		
Target Install Path \$(Compiler Install Path)\include		
Time Unit	Cycles	
Timer Enabled	false	
Timer Prescale	0	
Timer Resolution 1		
UDE Config File \$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg		
Workspace File D:\Synergy_Work_Area\Clxx_DigColPs\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP		



#### **Test Case 1: Metrics Test**

Description

Test Vector Description:

TS1.1"Shortest Execution Path:

IS1.1"Shortest Execution Path:

(DigColPsInt\_SensInitialized\_Cnt\_M\_lgc == FALSE)=True

(ElapsedTime\_mS\_T\_u16 >= (uint16)D\_SENSINITDELAY\_MS\_U08 )=False

(DigColPsInt\_NackOccurred\_Cnt\_M\_lgc == TRUE)=False

(DigColPsInt\_RecvOverrunError\_Cnt\_M\_lgc == TRUE)=False

(DigColPsInt\_BusBusySeqError\_Cnt\_M\_lgc == TRUE)=False

(DigColPsInt\_CmdFailOccurred\_Cnt\_M\_lgc == TRUE)=False

(DigColPsInt\_TransactionCnt\_Cnt\_M\_lgc == TRUE)=False

((DigColPsInt\_TransactionCnt\_Cnt\_M\_u08 == DigColPsInt\_PrevTransactionCnt\_Cnt\_M\_u08) && (DigColPsInt\_RecvdDataType\_Cnt\_M\_u08 != D\_NONE\_CNT\_U08)) =False"

TS1.2" oncest Execution Path:

TS1.2"Longest Execution Path:

TS1.2"Longest Execution Path:

(DigColPsInt\_SensInitialized\_Cnt\_M\_lgc == FALSE)=False

(DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum < INIT\_COMPLETE)=True

(ElapsedTime\_mS\_T\_u16 > (uint16)(k\_l2CHWInitTransactionTime\_Sec\_f32\*D\_SECTOMILLSEC\_CNT\_F32))=True

(DigColPsInt\_NackOccured\_Cnt\_M\_lgc == TRUE)=True

(DigColPsInt\_RecvOverrunError\_Cnt\_M\_lgc == TRUE)=True

(DigColPsInt\_BusBusySeqError\_Cnt\_M\_lgc == TRUE)=True

(DigColPsInt\_CmdFailOccurred\_Cnt\_M\_lgc == TRUE)=True

(DigColPsInt\_TransactionCnt\_Cnt\_M\_u08 == DigColPsInt\_PrevTransactionCnt\_Cnt\_M\_u08) && (DigColPsInt\_RecvdDataType\_Cnt\_M\_u08 != D\_NONE\_CNT\_U08)) = True"

Test Step 1.1 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	0
DigColPsInt_Buffer_Cnt_M_u08[1]	0
DigColPsInt_Buffer_Cnt_M_u08[2]	0
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_Igc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	0
DigColPsInt_CurrentSlave_Cnt_M_u08	0
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_NOT_INITIALIZED
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0
DigColPsInt_InitialTime_mS_M_u32	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	0
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	0
DigColPsInt TransactionCnt Cnt M u08	0
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	0
k_I2CHWInitTransactionTime_Sec_f32	0
target_DtrmnElapsedTime_mS_u16_ElapsedTime	0
target_GetSystemTime_mS_u32_CurrentTime	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	0

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Name	Input Value		
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0		
target I2c Send I2cRegPtr Cnt T str.PD	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	0		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	0		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
target i2cREG1 temp.OAR	0		
target_i2cREG1_temp.IMR	0		
target_i2cREG1_temp.STR	Ō		
target_i2cREG1_temp.CLKL	0		
target_i2cREG1_temp.CLKH	0		
target_i2cREG1_temp.CNT	0		
target_i2cREG1_temp.DRR	0		
target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR	0		
target_i2cREG1_temp.MDR	0		
target i2cREG1 temp.IVR	0		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	0		
target_i2cREG1_temp.PID11	0		
target_i2cREG1_temp.PID12	0		
target_i2cREG1_temp.DMAC	0		
target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR	0		
target i2cREG1 temp.DIN	0		
target i2cREG1 temp.DOUT	0		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	0	I=	1
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	0	0	~
DigColPsInt_Buffer_Cnt_M_u08[2]	0	0	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	•
DigColPsInt_CurrentSlave_Cnt_M_u08	0	0	-
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_NOT_INITIALIZED	INIT_NOT_INITIALIZED	~
DigColPsInt_GetData()	0	0	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPoint_PrevTransactionCnt_Cnt_M_u08	0	0	<b>*</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	<b>✓</b>
DigColPsInt_SensInitialized_Cnt_M_lgc I2c_Send(Length_Cnt_T_u32)	0	0	
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	0	0	-
target_ColSnsrDataPtr_Cnt_T_u16	0	0	-
target_DataTypePtr_Cnt_T_u08	0	0	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	0	0	~

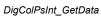
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target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.PDC         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DID12         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DUT         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR         0           target_l2c_Send_l2		0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DAR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DAR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DAR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIAAC         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DUT         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DUR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DDR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DAR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DAR         0           target_I2c_Send_I2		0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DUT         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DUR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DDR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DDR         0           target_I2c_Send_I2cRe		I f	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DID12         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.SET         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PD         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR         0		0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DID12         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DM         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.SET         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DD         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PD         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR         0		0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DDR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DDR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PD         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR         0		0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.SET         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PD         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR         0		0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.SET         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DDR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PD         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR         0		0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DUT         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DUT         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.SET         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DLR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DDR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PD         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR         0		0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.SET         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DDR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PD         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR         0		0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.SET         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PD         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR         0		0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.SET         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PD         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR         0		0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.SET         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PD         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR         0		0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.SET         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PD         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR         0		0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.SET         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PD         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR         0		0	-
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.SET         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.PD         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL         0           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR         0           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR         0		0	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.SET         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.PD         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL         0           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR         0           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR         0		0	
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.PD         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL         0           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR         0           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR         0		0	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.PD         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL         0           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR         0           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR         0		0	
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.PD         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL         0           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR         0           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR         0		0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR         0		0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL 0 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR 0 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR 0		0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR 0 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR 0		0	٠,
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR 0		0	
		0	٠,
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR 0		0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL 0		0	٠,
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH 0		0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT 0		0	٠,
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR 0		0	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR 0		0	٠,
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR 0	1	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR 0		0	٠,
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR 0		0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR 0		0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC 0		0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11 0		0	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12 0		0	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC 0		0	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN 0		0	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR		0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN 0		0	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT 0		0	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET 0		0	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR 0		0	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR 0		0	
0 = = 1 = 0 = ==		0	
3-2 -2			_
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL 0 target_SpurSnsrDataPtr_Cnt_T_u16 0		0	

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

Test Step 1.2 (Repeat Count = 1)	
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	255
DigColPsInt_Buffer_Cnt_M_u08[1]	255
DigColPsInt_Buffer_Cnt_M_u08[2]	255
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	65535
DigColPsInt_CurrentSlave_Cnt_M_u08	127
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADDATREG_READ
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1
DigColPsInt_InitialTime_mS_M_u32	4294967295
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	255
DigColPsInt RecvOverrunError Cnt M Igc	1





Name	Input Value
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	65535
DigColPsInt_TransactionCnt_Cnt_M_u08	255
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08 k_l2CHWInitTransactionTime_Sec_f32	127 10
target DtrmnElapsedTime mS u16 ElapsedTime	65535
target_GetSystemTime_mS_u32_CurrentTime	4294967295
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	32767
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	1023
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	65535 4095
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	3
target I2c Send I2cRegPtr Cnt T str.PSC	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	65535
target I2c Send I2cRegPtr Cnt T str.PID12	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1.
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	1023
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	32767
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	1023
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	4095
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	255 65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	255
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	1023
target_i2cREG1_temp.IMR	255
target_i2cREG1_temp.STR target_i2cREG1_temp.CLKL	32767 65535
targot_realtEG I_temp.OLINE	0000
target_i2cREG1_temp.CLKH	65535
target_i2cREG1_temp.CLKH target_i2cREG1_temp.CNT	65535 65535
target_i2cREG1_temp.CLKH target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	
target_i2cREG1_temp.CNT	65535

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Name	Input Value		
target_i2cREG1_temp.MDR	65535		
target_i2cREG1_temp.IVR	4095		
target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC	3 255		
target i2cREG1 temp.PID11	65535		
target i2cREG1 temp.PID12	255		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	3		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET target_i2cREG1_temp.CLR	3		
target i2cREG1 temp.ODR	3		
target i2cREG1 temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	255	255	~
DigColPsInt_Buffer_Cnt_M_u08[1]	255	255	~
DigColPsInt_Buffer_Cnt_M_u08[2]	255	255	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	<b>V</b>
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	· ·
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt GetData()	190	INIT_SENSOR2_EXTREADDATREG_READ 190	Ž
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	_
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	-
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	255	255	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_Igc	1	1	~
I2c_Send(Length_Cnt_T_u32)	0	0	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	0	0	<b>V</b>
target_ColSnsrDataPtr_Cnt_T_u16	65535 5	65535 5	<b>✓</b>
target_DataTypePtr_Cnt_T_u08 target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023	1023	Ž
target_I2C_Send_I2cRegPtr_Cnt_T_str.IMR	255	255	·
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	32767	32767	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	65535	65535	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	255	255	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	1023	1023	· ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	255 65535	255 65535	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	4095	4095	,
target I2c Send I2cRegPtr Cnt T str.EMDR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	255	255	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	65535	65535	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	255	255	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	3	3	<b>✓</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	3	3	,
target_12c_Serid_12cRegPti_Crit_1_str.DUT	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	1023	1023	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	255	255	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	32767 65535	32767 65535	~
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH	65535	65535	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	65535	65535	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	255	255	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	1023	1023	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	255	255	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	65535	65535	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	4095	4095	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	255 65535	255 65535	<b>*</b>
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID11 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID12	255	255	-
5			

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DigColPsInt\_GetData

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_SpurSnsrDataPtr_Cnt_T_u16	65535	65535	~

Τ					1
Actual Function	Count	Expected Function	Count	Resu	it
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	•	/

#### **Test Case 2: Boundary Test**

Description

Test Vector Description:

TS2.1DigColPsInt\_NackOccured\_Cnt\_M\_lgc=min
TS2.2DigColPsInt\_BusBusySeqError\_Cnt\_M\_lgc=max
TS2.3DigColPsInt\_BusBusySeqError\_Cnt\_M\_lgc=max
TS2.5DigColPsInt\_BusBusySeqError\_Cnt\_M\_lgc=max
TS2.5DigColPsInt\_TransactionCnt\_Cnt\_M\_u08=min
TS2.6DigColPsInt\_TransactionCnt\_Cnt\_M\_u08=min
TS2.6DigColPsInt\_TransactionCnt\_Cnt\_M\_u08=min
TS2.6DigColPsInt\_TransactionCnt\_Cnt\_M\_u08=mid
TS2.8DigColPsInt\_PrevTransactionCnt\_Cnt\_M\_u08=min
TS2.9DigColPsInt\_PrevTransactionCnt\_Cnt\_M\_u08=min
TS2.9DigColPsInt\_PrevTransactionCnt\_Cnt\_M\_u08=mid
TS2.10DigColPsInt\_ColSnsrData\_Cnt\_M\_u16=min
TS2.11DigColPsInt\_ColSnsrData\_Cnt\_M\_u16=min
TS2.12DigColPsInt\_SpurSnsrData\_Cnt\_M\_u16=mid
TS2.14DigColPsInt\_SpurSnsrData\_Cnt\_M\_u16=mid
TS2.15DigColPsInt\_SpurSnsrData\_Cnt\_M\_u16=mid
TS2.15DigColPsInt\_SpurSnsrData\_Cnt\_M\_u16=mid
TS2.16DigColPsInt\_SpurSnsrData\_Cnt\_M\_u16=mid
TS2.17DigColPsInt\_RecvdDataType\_Cnt\_M\_u08=min
TS2.18DigColPsInt\_RecvdDataType\_Cnt\_M\_u08=min
TS2.20DigColPsInt\_RecvdDataType\_Cnt\_M\_u08=min
TS2.20DigColPsInt\_SensInitialized\_Cnt\_M\_lgc=min
TS2.21DigColPsInt\_SensInitialized\_Cnt\_M\_lgc=min
TS2.22DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum=min
TS2.22DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum=min
TS2.22DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum=max
TS2.24DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum=max
TS2.24DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum=max
TS2.26k\_l2CHWinitTransactionTime\_Sec\_f32=min
TS2.26k\_l2CHWinitTransactionTime\_Sec\_f32=min
TS2.29DigColPsInt\_RecvOverrunError\_Cnt\_M\_lgc=min
TS2.30DigColPsInt\_RecvOverrunError\_Cnt\_M\_lgc=min
TS2.30DigColPsInt\_CmdFailOccurred\_Cnt\_M\_lgc=min
TS2.31DigColPsInt\_CmdFailOccurred\_Cnt\_M\_lgc=min
TS2.33DigmnElapsedTime\_mS\_u16=min
TS2.33DigmnElapsedTime\_mS\_u16=min
TS2.33E\_ColSensorl2CAddress\_Cnt\_u08=max
TS2.37k\_ColSensorl2CAddress\_Cnt\_u08=max
TS2.34DiffundedTime\_mS\_u32=min
TS2.34Dall Min
TS2.42All Min
TS2.42All Min

Test Step 2.1 (Repeat Count = 1)	v v v v v v v v v v v v v v v v v v v
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	5600
DigColPsInt_CurrentSlave_Cnt_M_u08	14
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	5486797
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	19

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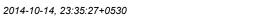


Name	Input Value
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	9687
DigColPsInt_TransactionCnt_Cnt_M_u08	12
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	119
k_I2CHWInitTransactionTime_Sec_f32	1.10000002
target_DtrmnElapsedTime_mS_u16_ElapsedTime	1247
target_GetSystemTime_mS_u32_CurrentTime	1475789
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	

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DispCaPerils Raffer, CM, M_00R1  20   20   20   20   20   20   20   20				
Septic   Common   C	Name	Input Value		
Sept.   Dec   De	target_i2cREG1_temp.DXR	78		
	target_i2cREG1_temp.MDR	495		
Image:   Deptile   Jessey   Deptile   Deptil	target_i2cREG1_temp.IVR	66		
Image: LORGEG  1 mem PUD11   105	target_i2cREG1_temp.EMDR			
Biggst   DeSEGE   Semp PD172   78				
Image_DeBCO_I   Image_DeBCO_				
	·			
Image   LapeRed   La				
Impagl_20R6G1_temp DOUT  Impagl_20R6G1_temp SET	0			
Image   DeBEG   DeBEG   Image   DeBEG   DeBEG   DeBEG   Image   DeBEG   DeBEG   Image   DeBEG   DeBE	·	•		
Image	0 ;			
Image   2.2REG   Impro   PO				
Separate				
Separation   Sep		0		
DepCoParis Baffer, CM, M_0080    20   20   20   20   20   20   20	target_i2cREG1_temp.PSL	0		
Dispose   Buffer Colf M_ 1987   30   30   30   30   30   30   30   3	Name	Actual Value	Expected Value	Result
DigicPelnit Buffer, CM, M_U0R2	DigColPsInt_Buffer_Cnt_M_u08[0]	36	· ·	~
DigicalPaint   Discription	DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	<b>✓</b>
DigCoPelnic CurrentStave, Cort. M_Lorum	DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	~
DigCoPaint CurrentStepNo. Cmt. M. enum	DigColPsInt_BusBusySeqError_Cnt_M_Igc	0	0	~
DigitalPaint   Delicates	DigColPsInt_CurrentSlave_Cnt_M_u08	119	119	~
Digitary	DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	•
DigCoPath Rent Concurs (Cont. Mu Use   DigCoPath Rent Cont. Cont. Mu Use   DigCoPath Rent Cont. Cont. Mu Use   DigCoPath Rent Cont. Mu Use   DigCoPath Rent Cont. Mu Use   DigCoPath Rent Seath Rent Cont. Mu Use   DigCoPath Rent Rent Rent Rent Rent Rent Rent Rent	DigColPsInt_GetData()	40	40	~
DigCoPsint_RecoPrerumEmc_Cnt_Muge	DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigCoPelant, Send-OvernumError_Cnt, Migc	DigColPsInt_NackOccured_Cnt_M_lgc		1 -	~
DigGoTelent, Sensitiatiated Cnt, M. Joe				~
1				
IZE_SetupMasterTransmit(DalaLength_Cnt_T_u16)		·		
Larget CoSnerDataPtC_CNT_U16   5600				
Surget Data Type Ptr. Cnt. T. U/8   Using Ftr. Send. (2RespPtr. Cnt. T. str. NAR   18				
target_12c_Send_12cRepPt_Cnt_T_str.NR         66         66           target_12c_Send_12cRepPt_Cnt_T_str.NMR         78         78           target_12c_Send_12cRepPt_Cnt_T_str.NTR         78         78           target_12c_Send_12cRepPt_Cnt_T_str.CNL         495         495           target_12c_Send_12cRepPt_Cnt_T_str.CNT         56         56           target_12c_Send_12cRepPt_Cnt_T_str.CNT         897         897           target_12c_Send_12cRepPt_Cnt_T_str.DRR         88         98           target_12c_Send_12cRepPt_Cnt_T_str.DRR         88         98           target_12c_Send_12cRepPt_Cnt_T_str.DRR         66         66           target_12c_Send_12cRepPt_Cnt_T_str.DRR         78         78           target_12c_Send_12cRepPt_Cnt_T_str.DRR         495         495           target_12c_Send_12cRepPt_Cnt_T_str.DRR         66         66           target_12c_Send_12cRepPt_Cnt_T_str.DRR         66         66           target_12c_Send_12cRepPt_Cnt_T_str.DRR         66         66           target_12c_Send_12cRepPt_Cnt_T_str.DRDR         0         0           target_12c_Send_12cRepPt_Cnt_T_str.DRDR         0         0           target_12c_Send_12cRepPt_Cnt_T_str.DRD         0         0           target_12c_Send_12cRepPt_Cnt_T_str.DRD         0				
target   12c   Send   12cRegPtr   Cnt   T str.MR				
target_ 2c_Send_ 2cRegPtr_Cnt_strSTR   78   495   49				
target   2c Send   12cRegPtr Cnt.T_str.CLKL				
target_12c_Send_12cRegPtr_Cnt_T_str.CNT				
target_12c_Send_12cRegPtr_Cnt_T_str.DRT				
target_12c_Send_12cRegPtr_Cnt_T str.DRR         98         98           target_12c_Send_12cRegPtr_Cnt_T str.SARR         66         66           target_12c_Send_12cRegPtr_Cnt_T str.MDR         495         495           target_12c_Send_12cRegPtr_Cnt_T str.MDR         495         495           target_12c_Send_12cRegPtr_Cnt_T str.MDR         0         0           target_12c_Send_12cRegPtr_Cnt_T str.MDR         0         0           target_12c_Send_12cRegPtr_Cnt_T str.PID11         56         56           target_12c_Send_12cRegPtr_Cnt_T str.PID12         78         78           target_12c_Send_12cRegPtr_Cnt_T str.DMAC         0         0           target_12c_Send_12cRegPtr_Cnt_T str.DMAC         0         0           target_12c_Send_12cRegPtr_Cnt_T str.DIN         0         0           target_12c_Send_12cRegPtr_Cnt_T str.DIN         1         1           target_12c_Send_12cRegPtr_Cnt_T str.DIN         1         1           target_12c_Send_12cRegPtr_Cnt_T str.DIN         1         1           target_12c_Send_12cRegPtr_Cnt_T str.DIN         1         1           target_12c_Send_12cRegPtr_Cnt_T str.DIN         0         0           target_12c_Send_12cRegPtr_Cnt_T str.DIR         0         0           target_12c_Send_12cRegPtr_Cnt_T str.DIR         0 <td></td> <td></td> <td></td> <td>•</td>				•
target_12c_Send_12cRegPtr_Cnt_T_str.DAR				-
target_!2c_Send_!2cRegPtr_Cnt_T_str.DXR         78           target_!2c_Send_!2cRegPtr_Cnt_T_str.MDR         495           target_!2c_Send_!2cRegPtr_Cnt_T_str.MDR         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDT         56           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDT         56           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDAC         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDAC         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDR         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDR         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDR         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDT         1           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDT         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDT         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DT         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDR         1           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDR         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DR         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DR         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DR         0           target_!2c_Send_!2cRegP				<b>✓</b>
target   Ze, Send   ZeRegPth_Cnt_T_str.EMDR         0         0           target   Ze, Send   ZeRegPth_Cnt_T_str.EMDR         0         0           target   Ze, Send   ZeRegPth_Cnt_T_str.PiD11         56         56           target   Ze, Send   ZeRegPth_Cnt_T_str.PiD12         78         78           target   Ze, Send   ZeRegPth_Cnt_T_str.PiD12         78         78           target   Ze, Send   ZeRegPth_Cnt_T_str.DMAC         0         0           target   Ze, Send   ZeRegPth_Cnt_T_str.DMAC         0         0           target   Ze, Send   ZeRegPth_Cnt_T_str.DIN         0         0           target   Ze, Send   ZeRegPth_Cnt_T_str.DIN         1         1           target   Ze, Send   ZeRegPth_Cnt_T_str.DOUT         0         0           target   Ze, Send   ZeRegPth_Cnt_T_str.DOUT         0         0           target   Ze, Send   ZeRegPth_Cnt_T_str.DOR         1         1           target   Ze, Send   ZeRegPth_Cnt_T_str.DOR         6         6           target   Ze, Sen		78	78	~
target_12c_Send_12cRegPtr_Cnt_T_str.PSDC	target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC         78         78           target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11         56         56           target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12         78         78           target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12         78         78           target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.CDR         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DRAC         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.PD         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.PD         0         0           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         66         66           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_s	target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11         56         56           target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12         78         78           target_l2c_Send_l2cRegPtr_Cnt_T_str.DMC         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DNT         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DNT         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DNT         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DODR         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR         66         66           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MR         78         78           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CkL         495         495           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         56         66           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         78         78           tar	target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12         78         78           target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC         0         0           otarget_l2c_Send_l2cRegPtr_Cnt_T_str.PUN         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DCR         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR         66         66           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         78         78           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CKL         495         495           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CkL         495         495           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CkL         495         495           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         78         78      <	target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_l2c_Send_l2cRepPtr_Cnt_T_str.DMAC       0       0         target_l2c_Send_l2cRepPtr_Cnt_T_str.DIN       0         target_l2c_Send_l2cRepPtr_Cnt_T_str.DIN       0         target_l2c_Send_l2cRepPtr_Cnt_T_str.DIN       1         target_l2c_Send_l2cRepPtr_Cnt_T_str.DOUT       0         0       0         target_l2c_Send_l2cRepPtr_Cnt_T_str.DUT       0         0       0         target_l2c_Send_l2cRepPtr_Cnt_T_str.DUT       0         target_l2c_Send_l2cRepPtr_Cnt_T_str.DLR       0         0       0         target_l2c_Send_l2cRepPtr_Cnt_T_str.DDR       1         target_l2c_Send_l2cRepPtr_Cnt_T_str.DDR       1         target_l2c_Send_l2cRepPtr_Cnt_T_str.DSL       0         0       0         target_l2c_SetupMasterTransmit_l2cRepPtr_Cnt_T_str.OAR       66         66       66         target_l2c_SetupMasterTransmit_l2cRepPtr_Cnt_T_str.STR       78         target_l2c_SetupMasterTransmit_l2cRepPtr_Cnt_T_str.CLKL       495         target_l2c_SetupMasterTransmit_l2cRepPtr_Cnt_T_str.CNT       897         target_l2c_SetupMasterTransmit_l2cRepPtr_Cnt_T_str.DRR       98         target_l2c_SetupMasterTransmit_l2cRepPtr_Cnt_T_str.DRR       98         target_l2c_SetupMasterTransmit_l2cRepPtr_Cnt_T_str.DRR       495	target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DUT         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DUT         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DD         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.PD         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DRL         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DRL         0         0           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         66         66           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         495         78           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLK         495         495           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         98         98           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         98         98           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         78         78				~
target_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       1       1         target_!2c_Send_!2cRegPtr_Cnt_T_str.DOUT       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.DOUT       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.DET       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.DR       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.DD       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.PD       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.PSL       0       0         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.OAR       66       66         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL       495       495         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT       897       897         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       98       98         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr				~
target_12c_Send_12cRegPtr_Cnt_T_str.DIN       1       1         target_12c_Send_12cRegPtr_Cnt_T_str.DOUT       0       0         target_12c_Send_12cRegPtr_Cnt_T_str.SET       0       0         target_12c_Send_12cRegPtr_Cnt_T_str.CLR       0       0         target_12c_Send_12cRegPtr_Cnt_T_str.DDR       1       1         target_12c_Send_12cRegPtr_Cnt_T_str.DD       0       0         target_12c_Send_12cRegPtr_Cnt_T_str.PSL       0       0         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.OAR       66       66         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.STR       78       78         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL       495       495         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL       495       495         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH       56       56         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT       897       897         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       98       98         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR       78       78         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR       78       78         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MDR       495       495 <t< td=""><td></td><td></td><td></td><td>~</td></t<>				~
target_!2c_Send_!2cRegPtr_Cnt_T_str.DOUT       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.SET       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.ODR       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.DDR       1       1         target_!2c_Send_!2cRegPtr_Cnt_T_str.DD       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.PSL       0       0         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.OAR       66       66         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL       495       495         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT       897       897         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       98       98         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR       495       495         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR       495       495         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       0       0				
target_!2c_Send_!2cRegPtr_Cnt_T_str.SET       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.CLR       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.DDR       1       1         target_!2c_Send_!2cRegPtr_Cnt_T_str.PD       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.PSL       0       0         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.OAR       66       66         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IMR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL       495       495         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL       495       495         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       56       56         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       98       98         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       98       98         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       495       495         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       66       66         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       66       66 <td></td> <td></td> <td></td> <td>-</td>				-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.DDR       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.PD       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL       495         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH       56         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       897         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       98         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       98         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       98         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.NDR       495         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       0         target_I2c_SetupMasterTransmit_I2cRegPtr_C				
target_!2c_Send_!2cRegPtr_Cnt_T_str.ODR       1       1         target_!2c_Send_!2cRegPtr_Cnt_T_str.PD       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.PSL       0       0         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.OAR       66       66         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.BIMR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL       495       495         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKH       56       56         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKH       56       56         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT       897       897         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       98       98         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       98       98         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR       495       495         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IVR       66       66         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       0       0         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       0       0         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR <td></td> <td></td> <td></td> <td></td>				
target_!2c_Send_!2cRegPtr_Cnt_T_str.PD       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.PSL       0       0         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.OAR       66       66         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IMR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL       495       495         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKH       56       56         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT       897       897         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       98       98         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR       66       66         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR       495       495         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       66       66         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       0       0         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       0       0         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       0       0         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T				
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL       0       0         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR       78       78         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR       78       78         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL       495       495         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH       56       56         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT       897       897         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR       98       98         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       78       78         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR       495       495         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DVR       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DNR       0       0         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR       0       0         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC       78       78				
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR  target_l2c_SetupMasterTrans				
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DNR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DNR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DNC  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DNC  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DNC  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DNC				
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL				
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL       495       495         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH       56       56         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT       897       897         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR       98       98         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       78       78         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR       495       495         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR       0       0         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC       78       78				~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH       56       56         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT       897       897         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR       98       98         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       78       78         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR       495       495         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR       0       0         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC       78       78				-
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT       897       897         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR       98       98         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       78       78         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR       495       495         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR       0       0         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC       78       78				V
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR 98 98 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR 66 66 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR 78 78 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR 495 495 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR 66 66 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR 0 0 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC 78 78				~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR 66 66 66				<b>✓</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR 78 78 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR 495 495 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR 66 66 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR 0 0 0 1 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC 78 78				~
target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.IVR	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR 0 0 0 varget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC 78 78	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC 78 78	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	66	66	~
	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR			~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 56 56				~
	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	

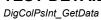




Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	•
target_SpurSnsrDataPtr_Cnt_T_u16	9687	9687	~

T			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	•
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	<b>✓</b>
GetSystemTime mS u32	1	GetSystemTime mS u32	1	_

Test Step 2.2 (Repeat Count = 1)	
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	40
DigColPsInt_Buffer_Cnt_M_u08[1]	50
DigColPsInt_Buffer_Cnt_M_u08[2]	60
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	7985
DigColPsInt_CurrentSlave_Cnt_M_u08	21
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	6489549
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	31
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt RecvdDataType Cnt M u08	1
DigColPsInt SensInitialized Cnt M Igc	1
DigColPsInt SpurSnsrData Cnt M u16	11230
DigColPsInt_TransactionCnt_Cnt_M_u08	29
OtrmnElapsedTime mS u16(ElapsedTime)	target DtrmnElapsedTime mS u16 ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
2c Send(I2cRegPtr Cnt T str)	target I2c Send I2cRegPtr Cnt T str
2c SetupMasterTransmit(I2cRegPtr Cnt T str)	target I2c SetupMasterTransmit I2cRegPtr Cnt T str
SpurSnsrDataPtr Cnt T u16	target SpurSnsrDataPtr Cnt T u16
2cREG1 temp	target i2cREG1 temp
ColSensorl2CAddress Cnt u08	126
C I2CHWInitTransactionTime Sec f32	1.5
arget_DtrmnElapsedTime_mS_u16_ElapsedTime	7841
arget GetSystemTime mS u32 CurrentTime	2478541
arget I2c Send I2cRegPtr Cnt T str.OAR	567
· · · ·	44
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2





Name	Input Value		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0		
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	129		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	6 567		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	44		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR target_i2cREG1_temp.IMR	567 44		
target_i2cREG1_temp.STR	4444		
target_i2cREG1_temp.CLKL	566		
target_i2cREG1_temp.CLKH	4466		
target_i2cREG1_temp.CNT	129		
target_i2cREG1_temp.DRR	6		
target_i2cREG1_temp.SAR	567		
target_i2cREG1_temp.DXR	44		
target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR	566 554		
target i2cREG1 temp.EMDR	1		
target_i2cREG1_temp.PSC	44		
target_i2cREG1_temp.PID11	4466		
target_i2cREG1_temp.PID12	44		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	2		
target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT	0		
target_i2cREG1_temp.BET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	40	40	~
DigColPsInt_Buffer_Cnt_M_u08[1]	50	50	~
DigColPsInt_Buffer_Cnt_M_u08[2]	60	60	✓ ✓
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08	21	21	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR1 READEXTERR READ	INIT SENSOR1 READEXTERR READ	~
DigColPsInt_GetData()	134	134	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	<b>✓</b>
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	29	29	<b>✓</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	<b>V</b>
target_ColSnsrDataPtr_Cnt_T_u16	7985 1	7985 1	<b>✓</b>
target_DataTypePtr_Cnt_T_u08 target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	, v
0	1 **	1 * *	

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Name	Actual Value	Expected Value	Resu
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	
target I2c Send I2cRegPtr Cnt T str.DOUT	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	
target I2c Send I2cRegPtr Cnt T str.PD	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	44	44	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	4444	4444	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	566	566	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	4466	4466	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	129	129	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	6	6	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	567	567	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	554	554	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	1	1	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	44	44	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	4466	4466	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	44	44	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	1	1	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	2	2	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	0	0	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	3	3	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3	3	
target SpurSnsrDataPtr Cnt T u16	11230	11230	

T				V
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

Test Step 2.3 (Repeat Count = 1)	
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	70
DigColPsInt_Buffer_Cnt_M_u08[1]	80
DigColPsInt_Buffer_Cnt_M_u08[2]	90
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	10370
DigColPsInt_CurrentSlave_Cnt_M_u08	28
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	7492301
DigColPsInt_NackOccured_Cnt_M_lgc	0

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DigColPsini_GelDala		
Name	Input Value	
0igColPsInt_PrevTransactionCnt_Cnt_M_u08	43	
igColPsInt_RecvOverrunError_Cnt_M_lgc	1	
0igColPsInt_RecvdDataType_Cnt_M_u08	2	
higColPsInt_SensInitialized_Cnt_M_lgc	1	
DigColPsInt_SpurSnsrData_Cnt_M_u16	12773	
DigColPsInt_TransactionCnt_Cnt_M_u08	33	
etrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime	
SetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime	
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str	
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target I2c SetupMasterTransmit I2cRegPtr Cnt T str	
SpurSnsrDataPtr_Cnt_T_u16	target SpurSnsrDataPtr Cnt T u16	
2cREG1_temp	target_i2cREG1_temp	
ColSensorI2CAddress Cnt u08	17	
	1.8999998	
arget_DtrmnElapsedTime_mS_u16_ElapsedTime	14435	
rget_GetSystemTime_mS_u32_CurrentTime	3481293	
liget_Scioysiciffiline_ino_us2_Gurrentfiline lirget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	
	89	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR		
irget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	
irget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	
irget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	
irget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	
irget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL		
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	
rrget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	
urget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	
rget I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	89	
riget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DMAC	2	
riget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.FUN	0	
riget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIR	0	
	1	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN		
rget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	2	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	
rget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	
rget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	
rget_i2cREG1_temp.OAR	65	
rrget_i2cREG1_temp.IMR	89	
arget_i2cREG1_temp.STR	67	
arget_i2cREG1_temp.CLKL	7	
	577	
arget_i2cREG1_temp.CLKH arget i2cREG1_temp.CNT	577 88	

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DeCoParie, Burler, C.M. M. (1981)   70   70   70   70   70   70   70   7	Name	Input Value		
Imper   CAPPICO   Hero NOPIC   Propriet				
Sept   1.000				
Laged LORGICAL HERD AND AND ADDRESS OF THE STATE ADDRESS OF THE STATE AND ADDRESS OF THE STATE A				
Biggst   DASCES   Semp PSO   Big   Semp   Semp PSO   Big   Big   Semp PSO   Big   Bi	· · ·			
target_DeléGid   man PRID11   1979  target_DeléGid   man PRID12   29    target_DeléGid   man PRID12   1979  target_DeléGid   man PRID13				
Image:   CARRIGO   Image   C		577		
	target_i2cREG1_temp.PID12	89		
	target_i2cREG1_temp.DMAC			
Image   DeBGG   Image   Imag				
Langer   CoREGI   Immp DOUT		-		
Langet   DEFECT   Semp SET				
Layer   Defect   Impr Core				
Instruction   Company	· · ·			
Septe   Desire   De		1		
	target_i2cREG1_temp.PD	2		
DeCoParie, Buffer, Col, M., U08(1)   80   80   80   80   80   80   80   8	target_i2cREG1_temp.PSL	0		
Dispositive	Name	Actual Value	Expected Value	Result
DipCoPiell, Buffer, Cr. M., vol.82]  DipCoPiell, Euglassy Gederic Cr. M., vol.82]  DipCoPiell, CurrentSieve, Cr. M., vol.82  DipCoPiell, CurrentSieve, Cr. M., vol.83  DipCoPiell, CurrentSieve, Cr. M., vol.84  DipCoPiell, Corticology Cr. M., vol.85  DipCoPiell, Corticology Cr. M., vol.85  DipCoPiell, Narchocoured, Cr. M., vol.85  DipCoPiell, RevCovernotiffer, Cr.	DigColPsInt_Buffer_Cnt_M_u08[0]	70		~
Dispositive Busbays Generic Cint Muge   0				~
DopCoPelant_ControlStepNo_Crit_Museum				~
Disposition: CurrentStephon, Cord. M. enum				~
Disposition Celebration  Disposition  Disposition Celebration  Disposition  Disposi				· ·
Disposition   Limitaries   Disposition   D				
DigColPaint, NackOccured, Crit, M, u68   33   33   33   33   33   33   33	5 - "			
DigCoPsint_RevCvenumError_Cnt_M_ube				-
DigCoPaint, RevOvernations Cnt, M. Jgc				•
target_ColsinorDalaPir_Cnl_T_u86         10370         10370           target_DalaTypePir_Cnl_T_u86         2         2           target_L02_Send_J2cRegPir_Cnl_T_str.MR         65         65           target_L02_Send_J2cRegPir_Cnl_T_str.MR         89         89           target_L02_Send_J2cRegPir_Cnl_T_str.MR         67         67         67           target_L02_Send_J2cRegPir_Cnl_T_str.Dtr.MR         67         67         7           target_L02_Send_J2cRegPir_Cnl_T_str.Dtr.MR         57         7         7           target_L02_Send_J2cRegPir_Cnl_T_str.Dtr.MR         88         88         88           target_L02_Send_J2cRegPir_Cnl_T_str.Dtr.MR         23         23         23           target_L02_Send_J2cRegPir_Cnl_T_str.Dtr.RR         65         65         65           target_L02_Send_J2cRegPir_Cnl_T_str.Dtr.RR         89         89         89           target_L02_Send_J2cRegPir_Cnl_T_str.Dtr.RR         44         44         44           target_L02_Send_J2cRegPir_Cnl_T_str.Dtr.RR         44         44         44           target_L02_Send_J2cRegPir_Cnl_T_str.Dtr.Dtr.Dtr.Dtr.Dtr.Dtr.Dtr.Dtr.Dtr.D		0	0	-
target DataTypePtr_Cnt_TutB         2         2           target_Los_Send_L2RcRpT_Cnt_T_str.NAR         65         65           target_Los_Send_L2RcRpT_Cnt_T_str.NMR         89         89           target_Los_Send_L2RcRpT_Cnt_T_str.STR         67         67           target_Los_Send_L2RcRpT_Cnt_T_str.STR         67         7           target_Los_Send_L2RcRpT_Cnt_T_str.CNT         88         88           target_Los_Send_L2RcRpT_Cnt_T_str.CNT         88         88           target_Los_Send_L2RcRpT_Cnt_T_str.DRR         23         23           target_Los_Send_L2RcRpT_Cnt_T_str.DRR         23         23           target_Los_Send_L2RcRpT_Cnt_T_str.DRR         23         89           target_Los_Send_L2RcRpT_Cnt_T_str.DRR         89         89           target_Los_Send_L2RcRpT_Cnt_T_str.DRR         77         7           target_Los_Send_L2RcRpT_Cnt_T_str.DRR         77         7           target_Los_Send_L2RcRpT_Cnt_T_str.DRR         2         2           target_Los_Send_L2RcRpT_Cnt_T_str.DRR         2         2           target_Los_Send_L2RcRpT_Cnt_T_str.DMAC         2         2           target_Los_Send_L2RcRpT_Cnt_T_str.DMAC         2         2           target_Los_Send_L2RcRpT_Cnt_T_str.DMA         2         2	DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	•
target Lize, Send, IzeRepPtr, Cnt, T., str. NAR         65         65           target, Ize, Send, IzeRepPtr, Cnt, T., str. NMR         89         89           target, Ize, Send, IzeRepPtr, Cnt, T., str. Str. NR         67         67           target, Ize, Send, IzeRepPtr, Cnt, T., str. ClkL         7         7           target, Ize, Send, IzeRepPtr, Cnt, T., str. ClkH         577         577           target, Ize, Send, IzeRepPtr, Cnt, T., str. ClkH         577         577           target, Ize, Send, IzeRepPtr, Cnt, T., str. DNR         88         88           starget, Ize, Send, IzeRepPtr, Cnt, T., str. DNR         89         89           target, Ize, Send, IzeRepPtr, Cnt, T., str. DNR         89         89           target, Ize, Send, IzeRepPtr, Cnt, T., str. DNR         7         7           target, Ize, Send, IzeRepPtr, Cnt, T., str. DNR         44         44         44           target, Ize, Send, IzeRepPtr, Cnt, T., str. DNR         2         2         2           target, Ize, Send, IzeRepPtr, Cnt, T., str. DND         2         2         2           target, Ize, Send, IzeRepPtr, Cnt, T., str. DNA         2         2         2           target, Ize, Send, IzeRepPtr, Cnt, T., str. DNA         2         2         2           target, Ize, Send, IzeRepPtr, Cnt, T., str. DNA         3<	target_ColSnsrDataPtr_Cnt_T_u16	10370	10370	•
target   2c   Send   2cRegPtr   Cnt   T   str   MR	target_DataTypePtr_Cnt_T_u08	2	2	~
target_12c_Send_12cRegPtr_Cnt_str.CtkL 7 7 7 1 target_12c_Send_12cRegPtr_Cnt_str.CtkL 7 7 7 1 target_12c_Send_12cRegPtr_Cnt_str.CtkL 7 7 7 1 target_12c_Send_12cRegPtr_Cnt_str.CtkL 7 7 1 target_12c_Send_12cRegPtr_Cnt_str.CtkT 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8	target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR			~
target   2c. Send   2cRegPtr_Cnt_T str.CLKL				<b>V</b>
target_12c_Send_12cRegPir_Cnt_T str.CLKH         577         577           target_12c_Send_12cRegPir_Cnt_T str.CNT         88         88           target_12c_Send_12cRegPir_Cnt_T str.DRR         23         23           target_12c_Send_12cRegPir_Cnt_T str.DXR         89         89           target_12c_Send_12cRegPir_Cnt_T str.DNR         89         89           target_12c_Send_12cRegPir_Cnt_T str.MDR         7         7           target_12c_Send_12cRegPir_Cnt_T str.DNR         44         44           target_12c_Send_12cRegPir_Cnt_T str.DNR         2         2           target_12c_Send_12cRegPir_Cnt_T str.DNDR         2         2           target_12c_Send_12cRegPir_Cnt_T str.DNDR         2         2           target_12c_Send_12cRegPir_Cnt_T str.DNDA         389         89           target_12c_Send_12cRegPir_Cnt_T str.DNAC         2         2           target_12c_Send_12cRegPir_Cnt_T str.DNAC         2         2           target_12c_Send_12cRegPir_Cnt_T str.DNA         0         0           target_12c_Send_12cRegPir_Cnt_T str.DNA         1         1           target_12c_Send_12cRegPir_Cnt_T str.DNA         1         1           target_12c_Send_12cRegPir_Cnt_T str.DNA         1         1           target_12c_Send_12cRegPir_Cnt_T str.DNA         0 <td></td> <td></td> <td></td> <td><b>~</b></td>				<b>~</b>
target_l2c_Send_l2cRepPr_Cnt_T str.DRT         88         88           target_l2c_Send_l2cRepPr_Cnt_T str.DRR         23         23           target_l2c_Send_l2cRepPr_Cnt_T str.DRR         65         65           target_l2c_Send_l2cRepPr_Cnt_T str.DRR         89         89           target_l2c_Send_l2cRepPr_Cnt_T str.DRR         7         7           target_l2c_Send_l2cRepPr_Cnt_T str.MDR         7         7           target_l2c_Send_l2cRepPr_Cnt_T str.BMDR         2         2           target_l2c_Send_l2cRepPr_Cnt_T str.BDMR         2         2           target_l2c_Send_l2cRepPr_Cnt_T str.DDT1         577         577           target_l2c_Send_l2cRepPr_Cnt_T str.DDT2         89         89           target_l2c_Send_l2cRepPr_Cnt_T str.DDT4         89         89           target_l2c_Send_l2cRepPr_Cnt_T str.DDN         0         0           target_l2c_Send_l2cRepPr_Cnt_T str.DDN         0         0           target_l2c_Send_l2cRepPr_Cnt_T str.DDN         1         1           target_l2c_Send_l2cRepPr_Cnt_T str.DDN         1         1           target_l2c_Send_l2cRepPr_Cnt_T str.DDN         1         1           target_l2c_Send_l2cRepPr_Cnt_T str.DDN         1         1           target_l2c_Send_l2cRepPr_Cnt_T str.DDN         2         2				<b>*</b>
target_l2c_Send_l2cRegPtr_Cnt_T str.DRR         23         23           target_l2c_Send_l2cRegPtr_Cnt_T str.SAR         65         65           target_l2c_Send_l2cRegPtr_Cnt_T str.DRR         89         89           target_l2c_Send_l2cRegPtr_Cnt_T str.DNR         89         89           target_l2c_Send_l2cRegPtr_Cnt_T str.DNR         7         7           target_l2c_Send_l2cRegPtr_Cnt_T str.DNR         44         44           target_l2c_Send_l2cRegPtr_Cnt_T str.DNR         2         2           target_l2c_Send_l2cRegPtr_Cnt_T str.DNDR         2         2           target_l2c_Send_l2cRegPtr_Cnt_T str.DND         577         577           target_l2c_Send_l2cRegPtr_Cnt_T str.DNAC         2         2         2           target_l2c_Send_l2cRegPtr_Cnt_T str.DNAC         2         2         2           target_l2c_Send_l2cRegPtr_Cnt_T str.DNAC         0         0         0           target_l2c_Send_l2cRegPtr_Cnt_T str.DNAC         2         2         2           target_l2c_Send_l2cRegPtr_Cnt_T str.DNAC         0         0         0           target_l2c_Send_l2cRegPtr_Cnt_T str.DNAC         2         2         2           target_l2c_Send_l2cRegPtr_Cnt_T str.DNAC         0         0         0           target_l2c_Send_l2cRegPtr_Cnt_T str.DNAC <td></td> <td></td> <td></td> <td></td>				
target_12c_Send_12cRegPtr_Cnt_T str.DXR         85         89           target_12c_Send_12cRegPtr_Cnt_T str.DXR         89         89           target_12c_Send_12cRegPtr_Cnt_T str.DXR         89         89           target_12c_Send_12cRegPtr_Cnt_T str.DXR         44         44           target_12c_Send_12cRegPtr_Cnt_T str.FMDR         2         2           target_12c_Send_12cRegPtr_Cnt_T str.FDC         89         89           target_12c_Send_12cRegPtr_Cnt_T str.FDD11         577         577           target_12c_Send_12cRegPtr_Cnt_T str.FDD12         89         89           target_12c_Send_12cRegPtr_Cnt_T str.DDAC         2         2           target_12c_Send_12cRegPtr_Cnt_T str.DIN         0         0           target_12c_Send_12cRegPtr_Cnt_T str.DIN         1         1           target_12c_Send_12cRegPtr_Cnt_T str.DOUT         2         2           target_12c_Send_12cRegPtr_Cnt_T str.DOUT         2         2           target_12c_Send_12cRegPtr_Cnt_T str.DOR         1         1           target_12c_Send_12cRegPtr_Cnt_T str.DOR         1         1           target_12c_Send_12cRegPtr_Cnt_T str.DOR         1         1           target_12c_Send_12cRegPtr_Cnt_T str.DOR         1         1           target_12c_SeutpMasterTransmit_12cRegPtr_Cnt_T str.DAR				
target_I2c_Send_I2cRegPtr_Cnt_Tstr.DXR         89         89           target_I2c_Send_I2cRegPtr_Cnt_Tstr.MDR         7         7           target_I2c_Send_I2cRegPtr_Cnt_Tstr.WR         44         44           target_I2c_Send_I2cRegPtr_Cnt_Tstr.EMDR         2         2           target_I2c_Send_I2cRegPtr_Cnt_Tstr.PDC         89         89           target_I2c_Send_I2cRegPtr_Cnt_Tstr.PD111         577         577           target_I2c_Send_I2cRegPtr_Cnt_Tstr.DD12         89         89           target_I2c_Send_I2cRegPtr_Cnt_Tstr.DMAC         2         2           target_I2c_Send_I2cRegPtr_Cnt_Tstr.DIN         0         0           target_I2c_Send_I2cRegPtr_Cnt_Tstr.DIN         1         1           target_I2c_Send_I2cRegPtr_Cnt_Tstr.DIN         1         1           target_I2c_Send_I2cRegPtr_Cnt_Tstr.DIN         1         1           target_I2c_Send_I2cRegPtr_Cnt_Tstr.DIN         2         2           target_I2c_Send_I2cRegPtr_Cnt_Tstr.Clr.         0         0           target_I2c_Send_I2cRegPtr_Cnt_Tstr.Clr.         0         0           target_I2c_Send_I2cRegPtr_Cnt_Tstr.Clr.         0         0           target_I2c_Send_I2cRegPtr_Cnt_Tstr.DAR         6         6           target_I2c_Send_I2cRegPtr_Cnt_Tstr.DAR         6         6				•
target_12c_Send_12cRegPtr_Cnt_T_str.IVR       44       44         target_12c_Send_12cRegPtr_Cnt_T_str.EMDR       2       2         target_12c_Send_12cRegPtr_Cnt_T_str.PDC       89       89         target_12c_Send_12cRegPtr_Cnt_T_str.PID11       577       577         target_12c_Send_12cRegPtr_Cnt_T_str.PID12       89       89         target_12c_Send_12cRegPtr_Cnt_T_str.DMAC       2       2         target_12c_Send_12cRegPtr_Cnt_T_str.DMAC       2       2         target_12c_Send_12cRegPtr_Cnt_T_str.DIN       0       0         target_12c_Send_12cRegPtr_Cnt_T_str.DIN       1       1         target_12c_Send_12cRegPtr_Cnt_T_str.DOUT       2       2         target_12c_Send_12cRegPtr_Cnt_T_str.DCT       2       2         target_12c_Send_12cRegPtr_Cnt_T_str.DCR       0       0         target_12c_Send_12cRegPtr_Cnt_T_str.DCR       0       0         target_12c_Send_12cRegPtr_Cnt_T_str.DCR       1       1         target_12c_Send_12cRegPtr_Cnt_T_str.DIT_str.DCR       2       2         target_12c_Send_12cRegPtr_Cnt_T_str.DAR       65       65         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.OAR       65       65         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DCR       7       7         target_12c_		89	89	•
target_12c_Send_12cRegPtr_Cnt_T_str.EMDR         2         2           target_12c_Send_12cRegPtr_Cnt_T_str.PSC         89         89           target_12c_Send_12cRegPtr_Cnt_T_str.PID11         577         577           target_12c_Send_12cRegPtr_Cnt_T_str.PID12         89         89           target_12c_Send_12cRegPtr_Cnt_T_str.DIMAC         2         2           target_12c_Send_12cRegPtr_Cnt_T_str.DIM         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DIN         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DIN         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DOUT         2         2           target_12c_Send_12cRegPtr_Cnt_T_str.DOUT         2         2           target_12c_Send_12cRegPtr_Cnt_T_str.DCR         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DCR         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DCR         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DD         2         2           target_12c_Send_12cRegPtr_Cnt_T_str.DAR         65         65           target_12c_Send_12cRegPtr_Cnt_T_str.DAR         89         89           target_12c_Send_basterTransmit_12cRegPtr_Cnt_T_str.DAR         89         89           target_12c_Send_basterTransmit_12cRegPtr_Cnt_T_s	target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	•
target_!2c_Send_!2cRegPtr_Cnt_Tstr.PSC         89         89           target_!2c_Send_!2cRegPtr_Cnt_Tstr.PID11         577         577           target_!2c_Send_!2cRegPtr_Cnt_Tstr.PID12         89         89           target_!2c_Send_!2cRegPtr_Cnt_Tstr.DMAC         2         2           target_!2c_Send_!2cRegPtr_Cnt_Tstr.DIN         0         0           target_!2c_Send_!2cRegPtr_Cnt_Tstr.DIN         0         0           target_!2c_Send_!2cRegPtr_Cnt_Tstr.DIN         1         1           target_!2c_Send_!2cRegPtr_Cnt_Tstr.DIN         1         1           target_!2c_Send_!2cRegPtr_Cnt_Tstr.DUT         2         2           target_!2c_Send_!2cRegPtr_Cnt_Tstr.DUT         2         2           target_!2c_Send_!2cRegPtr_Cnt_Tstr.DIN         0         0           target_!2c_Send_!2cRegPtr_Cnt_Tstr.DIN         1         1           target_!2c_Send_!2cRegPtr_Cnt_Tstr.DIT         2         2           target_!2c_Send_!2cRegPtr_Cnt_Tstr.DIT         2         2           target_!2c_Send_!2cRegPtr_Cnt_Tstr.DIT         2         2           target_!2c_Send_!2cRegPtr_Cnt_Tstr.DIT         2         2           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_Tstr.DIT         89         89           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_Tstr.Cnt         8	target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	•
target_!2e_Send_!2cRegPtr_CntT_str.PID11         577         577           target_!2e_Send_!2cRegPtr_CntT_str.PID12         89         89           target_!2e_Send_!2cRegPtr_CntT_str.DMAC         2         2           target_!2e_Send_!2cRegPtr_CntT_str.DM         0         0           target_!2e_Send_!2cRegPtr_CntT_str.DIN         0         0           target_!2e_Send_!2cRegPtr_Cnt_T_str.DIN         1         1           target_!2e_Send_!2cRegPtr_Cnt_T_str.DIN         1         1           target_!2e_Send_!2cRegPtr_Cnt_T_str.DUT         2         2           target_!2e_Send_!2cRegPtr_Cnt_T_str.DUT         2         2           target_!2e_Send_!2cRegPtr_Cnt_T_str.CR         0         0           target_!2e_Send_!2cRegPtr_Cnt_T_str.ODR         1         1           target_!2e_Send_!2cRegPtr_Cnt_T_str.DD         2         2           target_!2e_Send_!2cRegPtr_Cnt_T_str.DA         65         65           target_!2e_Send_!2cRegPtr_Cnt_T_str.DA         65         65           target_!2e_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR         89         89           target_!2e_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CkL         7         7           target_!2e_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CkL         7         7           target_!2e_SetupMasterTransmit_!2				~
target   2c Send   2cRegPtr_Cnt_T str.PID12         89         89           target   2c Send   2cRegPtr_Cnt_T _str.DMAC         2         2           target   2c Send   2cRegPtr_Cnt_T _str.DIN         0         0           target   2c Send   2cRegPtr_Cnt_T _str.DIN         0         0           target   2c Send   2cRegPtr_Cnt_T _str.DIN         1         1           target   2c Send   2cRegPtr_Cnt_T _str.DUT         2         2           target   2c Send   2cRegPtr_Cnt_T _str.DUT         2         2           target   2c Send   2cRegPtr_Cnt_T _str.DUT         0         0           target   2c Send   2cRegPtr_Cnt_T _str.ODR         1         1           target   2c Send   2cRegPtr_Cnt_T _str.DD         2         2           target   2c Send   2cRegPtr_Cnt_T _str.PSL         0         0           target   2c Send   2cRegPtr_Cnt_T _str.DAR         65         65           target   2c SetupMasterTransmit   2cRegPtr_Cnt_T _str.DAR         65         65           target   2c SetupMasterTransmit   2cRegPtr_Cnt_T _str.CKL         7         7           target   2c SetupMasterTransmit   2cRegPtr_Cnt_T _str.CKH         577         577           target   2c SetupMasterTransmit   2cRegPtr_Cnt_T _str.DAR         65         65           target   2c SetupMasterTransmit   2cRegPtr_Cnt_T _str.DAR         65<				~
target I2c_Send_I2cRegPtr_Cnt_T_str.FDMAC         2         2           target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN         0         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN         0         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN         1         1           target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT         2         2           target_I2c_Send_I2cRegPtr_Cnt_T_str.SET         2         2           target_I2c_Send_I2cRegPtr_Cnt_T_str.CDR         0         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DDR         1         1           target_I2c_Send_I2cRegPtr_Cnt_T_str.DD         2         2           target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL         0         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL         0         0           target_I2c_Send_I2cRegPtr_Cnt_T_str.DAR         65         65           target_I2c_Send_I2cRegPtr_Cnt_T_str.DAR         65         65           target_I2c_Send_I2cRegPtr_Cnt_T_str.DAR         89         89           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         65         65           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKI         7         7           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         88         88           target_I2c_SetupMasterTrans				•
target_12c_Send_12cRepPt_Cnt_T_str.DIR         0           target_12c_Send_12cRepPtr_Cnt_T_str.DIR         0           target_12c_Send_12cRepPtr_Cnt_T_str.DIN         1           target_12c_Send_12cRepPtr_Cnt_T_str.DUT         2           target_12c_Send_12cRepPtr_Cnt_T_str.DUT         2           target_12c_Send_12cRepPtr_Cnt_T_str.CLR         0           target_12c_Send_12cRepPtr_Cnt_T_str.DDR         1           target_12c_Send_12cRepPtr_Cnt_T_str.DDR         1           target_12c_Send_12cRepPtr_Cnt_T_str.DD         2           target_12c_Send_12cRepPtr_Cnt_T_str.DAR         0           target_12c_Send_12cRepPtr_Cnt_T_str.DAR         0           target_12c_SetupMasterTransmit_12cRepPtr_Cnt_T_str.DAR         65           target_12c_SetupMasterTransmit_12cRepPtr_Cnt_T_str.DAR         89           target_12c_SetupMasterTransmit_12cRepPtr_Cnt_T_str.CLKL         7           target_12c_SetupMasterTransmit_12cRepPtr_Cnt_T_str.CLKH         577           target_12c_SetupMasterTransmit_12cRepPtr_Cnt_T_str.DAR         88           target_12c_SetupMasterTransmit_12cRepPtr_Cnt_T_str.DAR         23           target_12c_SetupMasterTransmit_12cRepPtr_Cnt_T_str.DAR         89           target_12c_SetupMasterTransmit_12cRepPtr_Cnt_T_str.DAR         89           target_12c_SetupMasterTransmit_12cRepPtr_Cnt_T_str.DAR         7				· ·
target_12c_Send_12cRegPtr_Cnt_T_str.DIR         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DIN         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DOUT         2         2           target_12c_Send_12cRegPtr_Cnt_T_str.SET         2         2           target_12c_Send_12cRegPtr_Cnt_T_str.DLR         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DDR         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DD         2         2           target_12c_Send_12cRegPtr_Cnt_T_str.DD         2         2           target_12c_Send_12cRegPtr_Cnt_T_str.DD         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DAR         65         65           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         89         89           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.STR         67         67           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         7         7           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRT         88         88           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         23         23           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         89         89           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         7         7				
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN         1         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT         2         2         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.SET         2         2         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.DER         0         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DOR         1         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DD         2         2         2           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         65         65         65           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR         89         89         89           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         7         7         7           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         7         7         7           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT         88         88         88           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         23         23         23           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         89         89         89           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         7         7         44           target_l2c_SetupMasterT				-
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT         2         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.SET         2         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DD         2         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.PD         2         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR         65         65           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR         65         65           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         89         89           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         7         7           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         7         7           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         88         88           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         23         23           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR         89         89           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR         89         89           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR         7         7           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_st				
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET         2         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DD         2         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.PD         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL         0         0           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR         65         65           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.BIR         89         89           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         7         7           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         7         7           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH         577         577           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         23         23           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         23         23           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR         89         89           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR         7         7           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR         2         2           target_l2c_SetupMasterTransmit_l2			2	<b>✓</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR       1       2 <td></td> <td>2</td> <td>2</td> <td>-</td>		2	2	-
target_!2c_Send_!2cRegPtr_Cnt_T_str.PD       2       2         target_!2c_Send_!2cRegPtr_Cnt_T_str.PSL       0       0         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.OAR       65       65         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IMR       89       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR       67       67         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL       7       7         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKH       577       577         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT       88       88         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       23       23         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       23       23         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       89       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR       7       7         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IVR       44       44         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       2       2         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       2       2         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       2       2         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PD	target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       65       65         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR       89       89         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR       67       67         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL       7       7         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       88       88         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       23       23         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR       65       65         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       89       89         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       7       7         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       89       89         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       577       577	target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR			~
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.OAR       65       65         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IMR       89       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR       67       67         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL       7       7         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKH       577       577         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT       88       88         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       23       23         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.SAR       65       65         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       89       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR       7       7         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.NVR       44       44         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       2       2         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSC       89       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID11       577       577	target_I2c_Send_I2cRegPtr_Cnt_T_str.PD			•
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IMR       89       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR       67       67         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL       7       7         target_!2c_SetupMasterTransmit_!2cRegPtr_Cntstr.CLKH       577       577         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT       88       88         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       23       23         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.SAR       65       65         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       89       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR       7       7         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IVR       44       44         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       2       2         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSC       89       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID11       577       577				~
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL       7         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL       7         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKH       577         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT       88         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       23         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.SAR       65         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR       7         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.NVR       44         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       2         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       2         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSC       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSC       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID11       577				~
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL       7       7         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKH       577       577         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT       88       88         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       23       23         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.SAR       65       65         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       89       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR       7       7         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DVR       44       44         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       2       2         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSC       89       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID11       577       577				•
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKH       577       577         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT       88       88         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       23       23         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.SAR       65       65         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       89       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR       7       7         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IVR       44       44         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       2       2         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSC       89       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID11       577       577				Ž
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       88       88         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       23       23         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR       65       65         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       89       89         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       7       7         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       89       89         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       577       577				
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       23       23         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.SAR       65       65         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       89       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR       7       7         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IVR       44       44         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       2       2         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSC       89       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID11       577       577				-
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR       65       65         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       89       89         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR       7       7         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR       44       44         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR       2       2         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC       89       89         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11       577       577				•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       89       89         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       7       7         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       89       89         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       577       577				-
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR       7       7         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IVR       44       44         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       2       2         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSC       89       89         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID11       577       577				~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR       44       44       44         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR       2       2       2         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC       89       89       89         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11       577       577       577				•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC 89 89 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 577 577		44	44	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 577 577	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2		<b>~</b>
				~
target_IZc_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12 89 89				~
	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	<b>✓</b>

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_SpurSnsrDataPtr_Cnt_T_u16	12773	12773	~

Τ					1
Actual Function	Count	Expected Function	Count	Resu	it
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	•	/

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	3
DigColPsInt_Buffer_Cnt_M_u08[1]	6
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	12755
DigColPsInt_CurrentSlave_Cnt_M_u08	35
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_READ
ligColPsInt_InitFailedOnce_Cnt_M_Igc	0
DigColPsInt_InitialTime_mS_M_u32	8495053
ligColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	55
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SensInitialized_Cnt_M_Igc	0
igColPsInt_SpurSnsrData_Cnt_M_u16	14316
DigColPsInt_TransactionCnt_Cnt_M_u08	46
OtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
2cREG1_temp	target_i2cREG1_temp
_ColSensorI2CAddress_Cnt_u08	24
_I2CHWInitTransactionTime_Sec_f32	2.2999995
arget_DtrmnElapsedTime_mS_u16_ElapsedTime	21029
arget_GetSystemTime_mS_u32_CurrentTime	4484045
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10
rget_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	7846
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974
rget_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	10
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1

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Name	Input Value		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	2		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	1		
target_i2cREG1_temp.OAR	10		
target i2cREG1 temp.IMR	10		
target_i2cREG1_temp.STR	1223		
target i2cREG1 temp.CLKL	7846		
target i2cREG1 temp.CLKH	8974		
target i2cREG1 temp.CNT	98		
target_i2cREG1_temp.DRR	12		
target_i2cREG1_temp.SAR	10		
target i2cREG1 temp.DXR	10		
target i2cREG1 temp.MDR	7846		
target_i2cREG1_temp.IVR	55		
target_i2cREG1_temp.EMDR	1		
target i2cREG1 temp.PSC	10		
target i2cREG1 temp.PID11	8974		
target i2cREG1 temp.PID12	10		
target i2cREG1 temp.DMAC	1		
target i2cREG1 temp.FUN	1		
target_i2cREG1_temp.DIR	2		
target_i2cREG1_temp.DIN	1		
target i2cREG1 temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target i2cREG1 temp.ODR	1		
target i2cREG1 temp.PD	1		
target i2cREG1 temp.PSL	1		
Name	Actual Value	Expected Value	Dogult
	36	-	Result
DigColPsInt_Buffer_Cnt_M_u08[0]		36	
DigColPsInt_Buffer_Cnt_M_u08[1]	6	6	
DigColPsInt_Buffer_Cnt_M_u08[2]	9	9	<b>*</b>
DigColPsInt_BusBusySeqError_Cnt_M_lgc			
DigColPsInt_CurrentSlave_Cnt_M_u08	24	24	<b>V</b>
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	<b>V</b>
DigColPsInt_GetData()	6	6	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	<b>V</b>
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	<b>V</b>
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	46	46	<b>V</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	<b>V</b>
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	~
I2c_Send(Length_Cnt_T_u32)	1	1	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
target_ColSnsrDataPtr_Cnt_T_u16	12755	12755	~
target_DataTypePtr_Cnt_T_u08	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223	1223	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	~





Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98	98	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10	10	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	10	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846	7846	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55	55	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223	1223	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98	98	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10	10	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846	7846	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974	8974	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_SpurSnsrDataPtr_Cnt_T_u16	14316	14316	~

T				V
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	<b>✓</b>
GetSystemTime mS u32	1	GetSystemTime mS u32	1	<b>✓</b>

Test Step 2.5 (Repeat Count = 1)		✓
Name	Input Value	
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16	
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08	
DigColPsInt_Buffer_Cnt_M_u08[0]	11	
DigColPsInt_Buffer_Cnt_M_u08[1]	22	
DigColPsInt_Buffer_Cnt_M_u08[2]	33	
DigColPsInt_BusBusySeqError_Cnt_M_Igc	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	
DigColPsInt_ColSnsrData_Cnt_M_u16	15140	
DigColPsInt_CurrentSlave_Cnt_M_u08	42	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READEXTERR_READ	
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	
DigColPsInt_InitialTime_mS_M_u32	9497805	





Name	Input Value
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	67
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08 DigColPsInt SensInitialized Cnt M Igc	4
DigColPsInt_SpurSnsrData_Cnt_M_u16	15859
DigColPsInt_TransactionCnt_Cnt_M_u08	0
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensori2CAddress_Cnt_u08	31
k_I2CHWInitTransactionTime_Sec_f32 target_DtrmnElapsedTime_mS_u16_ElapsedTime	2.70000005 27623
target_GetSystemTime_mS_u32_CurrentTime	5486797
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34
target I2c Send I2cRegPtr Cnt T str.IMR	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	56
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	3 3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR target_I2c Send_I2cRegPtr_Cnt_T str.PD	2
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	24 847
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_1_str.MDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	56
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	2
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target I2c SetupMasterTransmit I2cRegPtr_Cnt_I_str.ODR target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	2
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	2
target i2cREG1 temp.OAR	34
target_i2cREG1_temp.IMR	24
target_i2cREG1_temp.STR	455
target_i2cREG1_temp.CLKL	847
target_i2cREG1_temp.CLKH	987
0 =	

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		( )	00
Name	Input Value		
target_i2cREG1_temp.DRR	34		
target_i2cREG1_temp.SAR	34		
target_i2cREG1_temp.DXR	24		
target_i2cREG1_temp.MDR	847		
target_i2cREG1_temp.IVR	56 2		
target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC	24		
target_i2cREG1_temp.PID11	987		
target i2cREG1 temp.PID12	24		
target i2cREG1 temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	3		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.CLR	3		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL	2		
	Actual Value	Expected Value	Popult
Name DigColPsInt_Buffer_Cnt_M_u08[0]	11	11	Result
DigColPsInt Buffer Cnt M u08[1]	22	22	-
DigColPsInt_Buffer_Cnt_M_u08[2]	33	33	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	•
DigColPsInt_CurrentSlave_Cnt_M_u08	42	42	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READEXTERR_READ	INIT_SENSOR2_READEXTERR_READ	•
DigColPsInt_GetData()	168	168	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1	1	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	0	0	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	<b>V</b>
target_ColSnsrDataPtr_Cnt_T_u16	15140 4	15140	✓ ✓
target_DataTypePtr_Cnt_T_u08 target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34	34	
target_l2c_Send_l2cRegPtr_Cnt_T_str.UMR	24	24	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455	455	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847	847	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987	987	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487	487	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34	34	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34	34	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24	24	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847	847	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56	56	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24	24	
target I2c Send I2cRegPtr Cnt T str.PID11	987	987	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24	24	•
target I2c Send I2cRegPtr Cnt T str.DMAC	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2 2	2	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34	34	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24	24	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455	455	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847	847	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987	987	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487	487	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34	34	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34	34	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24	24	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847	847	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2 24	2 24	· ·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987	987	
a.gozo_ootapmaotorrianomic_izotxogi ti_ont_1_ou.r.iD11			





Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24	24	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_SpurSnsrDataPtr_Cnt_T_u16	15859	15859	~

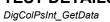
T				V
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

Name .	Innut Value
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	44
DigColPsInt_Buffer_Cnt_M_u08[1]	55
DigColPsInt_Buffer_Cnt_M_u08[2]	66
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	17525
DigColPsInt_CurrentSlave_Cnt_M_u08	49
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	10500557
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	79
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	17402
DigColPsInt_TransactionCnt_Cnt_M_u08	255
OtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target SpurSnsrDataPtr Cnt T u16
2cREG1 temp	target i2cREG1 temp
ColSensorl2CAddress_Cnt_u08	38
I2CHWInitTransactionTime Sec f32	3.099999
arget DtrmnElapsedTime mS u16 ElapsedTime	34217
arget GetSystemTime mS u32 CurrentTime	6489549
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
arget I2c Send I2cRegPtr Cnt T str.SAR	55
0 0	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	2309
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1

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Name	Innut Value		
Name target I2c Send I2cRegPtr Cnt T str.ODR	Input Value		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	2309 1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	3 66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	55		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	556		
target_i2cREG1_temp.CLKL target_i2cREG1_temp.CLKH	2309 1204		
target i2cREG1 temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC	3 66		
target i2cREG1 temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	3		
target_j2cREG1_temp.DOUT target_j2cREG1_temp.SET	3		
target i2cREG1 temp.CLR	1		
target i2cREG1 temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	~
DigColPsInt_Buffer_Cnt_M_u08[1]	55	55	~
DigColPoint_Buffer_Cnt_M_u08[2]	66 0	0	<b>V</b>
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08	38	38	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	<b>~</b>
DigColPsInt_GetData()	6	6	-
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	255	255	<b>*</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	<b>V</b>
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	<b>y</b>
I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
target_ColSnsrDataPtr_Cnt_T_u16	17525	17525	,
target_DataTypePtr_Cnt_T_u08	0	0	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	556	556	~





Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✓
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	66	66	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	556	556	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	87	87	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	67	67	✓
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	55	55	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	66	66	✓
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	2309	2309	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	5	5	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	3	3	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	66	66	✓
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	3	3	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	1	1	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	·
target SpurSnsrDataPtr Cnt T u16	17402	17402	

				✓
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c_Send	1	I2c_Send	1	<b>✓</b>
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	<b>✓</b>

Test Step 2.7 (Repeat Count = 1)		✓
Name	Input Value	
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16	
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08	
DigColPsInt_Buffer_Cnt_M_u08[0]	66	
DigColPsInt_Buffer_Cnt_M_u08[1]	77	
DigColPsInt_Buffer_Cnt_M_u08[2]	88	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	
DigColPsInt_ColSnsrData_Cnt_M_u16	19910	
DigColPsInt_CurrentSlave_Cnt_M_u08	56	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ	
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	

DigColPsInt GetData

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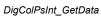


Input Value DigColPsInt\_InitialTime\_mS\_M\_u32 11503309 DigColPsInt\_NackOccured\_Cnt\_M\_lgc 91 DigColPsInt PrevTransactionCnt Cnt M u08 DigColPsInt\_RecvOverrunError\_Cnt\_M\_lgc DigColPsInt\_RecvdDataType\_Cnt\_M\_u08 5 DigColPsInt\_SensInitialized\_Cnt\_M\_lgc DigColPsInt\_SpurSnsrData\_Cnt\_M\_u16 18945  $DigColPsInt\_TransactionCnt\_Cnt\_M\_u08$ 120 DtrmnElapsedTime\_mS\_u16(ElapsedTime) target\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime GetSystemTime\_mS\_u32(CurrentTime) target\_GetSystemTime\_mS\_u32\_CurrentTime target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str I2c\_Send(I2cRegPtr\_Cnt\_T\_str) I2c\_SetupMasterTransmit(I2cRegPtr\_Cnt\_T\_str) target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str SpurSnsrDataPtr\_Cnt\_T\_u16 target\_SpurSnsrDataPtr\_Cnt\_T\_u16 i2cRFG1\_temp target i2cREG1 temp k\_ColSensorl2CAddress\_Cnt\_u08 45 k I2CHWInitTransactionTime Sec f32 3.5 target\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime 40811 target\_GetSystemTime\_mS\_u32\_CurrentTime 7492301 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.OAR 66 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IMR 78 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.STR 78 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKL 495 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKH 56 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CNT 897 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DRR 98 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SAR 66 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DXR 78 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.MDR 495 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IVR 66 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.EMDR 0 target I2c Send I2cRegPtr Cnt T str.PSC 78 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID11 56 target I2c Send I2cRegPtr Cnt T str.PID12 78 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DMAC 0 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.FUN 0 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIR 0 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIN 1  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DOUT$ 0 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SET 0 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLR 0 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.ODR 1 target I2c Send I2cRegPtr Cnt T str.PD 0 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSL 0 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.OAR 66 78  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IMR$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.STR 78  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKL$ 495 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKH 56 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CNT 897 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DRR 98 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SAR 66  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DXR$ 78  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.MDR$ 495  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IVR$ 66 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.EMDR 0  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSC$ 78 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID11 56  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID12$ 78 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DMAC 0  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.FUN$ 0  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIR$ 0 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIN 1  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DOUT$ 0 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SET 0 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLR 0 target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR 1 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PD 0 target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL 0 target\_i2cREG1\_temp.OAR 66 target\_i2cREG1\_temp.IMR 78 target\_i2cREG1\_temp.STR 78 target i2cREG1 temp.CLKL 495 target\_i2cREG1\_temp.CLKH 56

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Name	Input Value		
target_i2cREG1_temp.CNT	897		
target_i2cREG1_temp.DRR	98		
target_i2cREG1_temp.SAR	66		
target_i2cREG1_temp.DXR	78		
target_i2cREG1_temp.MDR	495		
target_i2cREG1_temp.IVR	66		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	78		
target_i2cREG1_temp.PID11	56		
target_i2cREG1_temp.PID12	78 0		
target_i2cREG1_temp.DMAC	0		
target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target i2cREG1 temp.DOUT	0		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	66	66	result
DigColPsInt_Buffer_Cnt_M_u08[1]	77	77	-
DigColPsInt_Buffer_Cnt_M_u08[2]	88	88	
DigColPsInt BusBusySeqError Cnt M Igc	0	0	
DigColPsInt_CurrentSlave_Cnt_M_u08	56	56	-
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ	INIT_SENSOR1_READERROR_READ	·
DigColPsInt_GetData()	168	168	
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	•
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	_
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	120	120	•
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	_
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	•
target_ColSnsrDataPtr_Cnt_T_u16	19910	19910	_
target_DataTypePtr_Cnt_T_u08	5	5	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target I2c Send I2cRegPtr Cnt T str.CNT	897	897	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target I2c Send I2cRegPtr Cnt T str.MDR	495	495	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	~





Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>
target_SpurSnsrDataPtr_Cnt_T_u16	18945	18945	<b>✓</b>

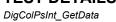
T .					V
Actual Function	Count	Expected Function	Count	Resu	lt
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1		<b>~</b>

Test Step 2.8 (Repeat Count = 1)	
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	40
DigColPsInt_Buffer_Cnt_M_u08[1]	50
DigColPsInt_Buffer_Cnt_M_u08[2]	60
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	22295
DigColPsInt_CurrentSlave_Cnt_M_u08	63
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	12506061
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	0
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SensInitialized_Cnt_M_Igc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	20488
DigColPsInt_TransactionCnt_Cnt_M_u08	51
OtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c SetupMasterTransmit(I2cRegPtr Cnt T str)	target I2c SetupMasterTransmit I2cRegPtr Cnt T str
_ : : : :	
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
2cREG1_temp	target_i2cREG1_temp
ColSensorI2CAddress_Cnt_u08	52
x_I2CHWInitTransactionTime_Sec_f32	3.9000001
arget_DtrmnElapsedTime_mS_u16_ElapsedTime	47405
arget_GetSystemTime_mS_u32_CurrentTime	8495053
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
arget I2c Send I2cRegPtr Cnt T str.PID11	4466
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PUR	2
	0
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
arget_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	





Name				
Bayes   Descript   Control   Contr	Name	Input Value		
Bayes   10.5 Seed.   12.5 See	target I2c Send I2cRegPtr Cnt T str.CLR	2		
Barget 126. Send Endergif* Col. T. pt. 2070   3		0		
Signate   Designate   Company   Cont   Tay   Min Review   September   Tay   Septem		3		
Separation   Separation   Temperature   Te		3		
Segreg   Dec. Selechbert Formum   Defenge   Col.     Dec.	target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	567		
Linguis   Ling		44		
Signate   R.S. Seluphides Trainers   Carlog Per Cott				
suger_DC_SeabAbater Travans_DERegit_Collsec_Atts  taget_DC_SeabAbater Travans_DERegit_Collsec_Atts  taget_DC_SeabAbat				
Single_De_SelephAnner*  Transmill_DeRepit_Coll_tail_DRR				
Suggroup   Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Regifter Cont_1 to NRR   Sering   Lick Superhaster   Transmil Lick Superhaster   Transmil Lick Superhaster   Transmil Lick Superh				
Separation   Separation   Care Company   Separation   S				
Linguis   Ling				
Image: Lipe_SetupAbsetTransmill_LiPelegiPc_OuTstr_NMR				
Image   12.0 Setup Market Transmit   2014-00pt   Col. T. at 2 At 17 At				
Bargel ILS Selan/MarketTransmit (2016-09P Col. T. at PSPC				
Lingual L.C. SebupAbuseEr Transmic Lingual Pric Cut   T. pt PDI1   4466				
Image   12.5. Setua Market Transmit   2.674 ppt; Col.   3.47 PD11	· ·			
Integral_E.SSehipMasterTransmil_E2RespPr_CNI_T_str MDNC   1				
Image   125. SetupMaterTransmil   207espth   0.11   1.5   1.0				
Image   Line				
Image   125. SebupMaseFrammin   126. Regif* Ont   1 str DIN   0   1   1   1   1   1   1   1   1   1				
Image   Lips   SeleyMaster Transmit   IzoRegith   Cent   T. ptr DN   1   1   1   1   1   1   1   1   1				
Image L. 22. SelepublaseEr Transmill. Exclesion Fr. Com. T. set DOUT   1   1   1   1   1   1   1   1   1				
Image   1.25. SebupAbasterTransmil   2640ptp. Col.T.   st SET   1   1   1   1   1   1   1   1   1				
Image_Lize_SetupAbaserTransmil_EcRegPtr_Cnt_T_str.DR	· ·			
target_Lz_SetupMasterTransmit_EckepPr_Cnt_T_str.PDR         0           target_Lz_SetupMasterTransmit_EckepPr_Cnt_T_str.PSL         3           target_Lz_SetupMasterTransmit_EckepPr_Cnt_T_str.PSL         3           target_Lz_REG_I_tamp_OLR         567           target_Lz_REG_I_tamp_OLR         444           target_Lz_REG_I_tamp_LTKI         566           target_Lz_REG_I_tamp_CLTKI         566           target_Lz_REG_I_tamp_CLTKI         4466           target_Lz_REG_I_tamp_CLTKI         120           target_Lz_REG_I_tamp_CLTKI         120           target_Lz_REG_I_tamp_CLTKI         567           target_Lz_REG_I_tamp_CLTKI         567           target_Lz_REG_I_tamp_CLTKI         446           target_Lz_REG_I_tamp_CLTKI         567           target_Lz_REG_I_tamp_CLTKI         567           target_Lz_REG_I_tamp_CLTKI         568           target_Lz_REG_I_tamp_CLTKI         544           target_Lz_REG_I_tamp_CLTKI         444           target_Lz_REG_I_tamp_CLTKI         446           target_Lz_REG_I_tamp_CLTKI         446           target_Lz_REG_I_tamp_CLTKI         446           target_Lz_REG_I_tamp_CLTKI         446           target_Lz_REG_I_tamp_CLTKI         446           target_Lz_REG_I_tamp_CLTKI				
barget_128_SetupMasterTransmit_  ZcRegPir_Cnt_Tetr_PDL   3				
starget_L22-REG_1 temp_DIAR				
Integral_L2006C1_Lemp_DAR				
Add   Add				
Larget_L2CREG1_temp.CLKL   See   S	target_i2cREG1_temp.OAR			
target_22REG1_temp.CLKI	target_i2cREG1_temp.IMR	44		
Sarget   JackEGG   Lemp.CLKH	target_i2cREG1_temp.STR	4444		
Image  120REG1_temp.CNT   129   120REG1_temp.DRR	target_i2cREG1_temp.CLKL	566		
Sarget_JacREG1_temp.DRR	target_i2cREG1_temp.CLKH	4466		
target_ ZeREG1_temp.SAR	target_i2cREG1_temp.CNT	129		
Larget_ ZeREG1_temp_DXR	target_i2cREG1_temp.DRR	6		
target_ 2cREG1_temp.NDR	target_i2cREG1_temp.SAR	567		
target_ 2cREG1_temp_EMDR	target_i2cREG1_temp.DXR	44		
target_!2cREG1_temp_EMDR	target_i2cREG1_temp.MDR	566		
target_l2cREG1_temp_PISC	target_i2cREG1_temp.IVR	554		
target_!2cREG1_temp.PID11         446           target_!2cREG1_temp.PID12         44           target_!2cREG1_temp.DMC         1           target_!2cREG1_temp.DIN         2           target_!2cREG1_temp.DIN         0           target_!2cREG1_temp.DOUT         1           target_!2cREG1_temp.DOT         1           target_!2cREG1_temp.DCR         2           target_!2cREG1_temp.DCR         2           target_!2cREG1_temp.DOR         0           target_!2cREG1_temp.DD         3           target_!2cREG1_temp.PD         3           target_!2cREG1_temp.PD         3           target_!2cREG1_temp.PD         3           target_!2cREG1_temp.DIN         6           Name         Actual Value         Expected Value         Resi           DigColPsint_Buffer_Cnt_M_u08(0)         36         36         8           DigColPsint_Buffer_Cnt_M_u08(1)         50	target_i2cREG1_temp.EMDR	1		
target_!2cREG1_temp.PID12	target_i2cREG1_temp.PSC	44		
target_!zcREG1_temp.DMAC	target_i2cREG1_temp.PID11	4466		
target_l2cREG1_temp.FUN	target_i2cREG1_temp.PID12	44		
target_izcREG1_temp.DIR         2           target_izcREG1_temp.DIN         0           target_izcREG1_temp.DOUT         1           target_izcREG1_temp.SET         1           target_izcREG1_temp.DCR         2           target_izcREG1_temp.DDR         0           target_izcREG1_temp.DP         3           target_izcREG1_temp.PSL         3           Name         Actual Value         Expected Value         Resi           DigColPsInt_Buffer_Cnt_M_u08[0]         36         36         0           DigColPsInt_Buffer_Cnt_M_u08[2]         60         60         60           DigColPsInt_Buffer_Cnt_M_u08[2]         0         0         0           DigColPsInt_CurrentSlave_Cnt_M_u08         52         52         DigColPsInt_CurrentSlave_Cnt_M_u08         52         52           DigColPsInt_CelData()         6         6         6         6         6           DigColPsInt_CelData()         6         <	target_i2cREG1_temp.DMAC	1		
target_izcREG1_temp.DIR         2           target_izcREG1_temp.DIN         0           target_izcREG1_temp.DOUT         1           target_izcREG1_temp.SET         1           target_izcREG1_temp.DCR         2           target_izcREG1_temp.DDR         0           target_izcREG1_temp.DP         3           target_izcREG1_temp.PSL         3           Name         Actual Value         Expected Value         Resi           DigColPsInt_Buffer_Cnt_M_u08[0]         36         36         0           DigColPsInt_Buffer_Cnt_M_u08[2]         60         60         60           DigColPsInt_Buffer_Cnt_M_u08[2]         0         0         0           DigColPsInt_CurrentSlave_Cnt_M_u08         52         52         DigColPsInt_CurrentSlave_Cnt_M_u08         52         52           DigColPsInt_CelData()         6         6         6         6         6           DigColPsInt_CelData()         6         <	target i2cREG1 temp.FUN	1		
target_!2cREG1_temp.DUT	target i2cREG1 temp.DIR	2		
target_i2cREG1_temp.DOUT	target i2cREG1 temp.DIN	0		
target_i2cREG1_temp.SET		1		
target_l2cREG1_temp.CDR		1		
target_i2cREG1_temp.DDR target_i2cREG1_temp.PDD 3 target_i2cREG1_temp.PSL 3 Name  Actual Value  Expected Value  Resi DigcolPsInt_Buffer_Cnt_M_u08[0] DigcolPsInt_Buffer_Cnt_M_u08[2] DigcolPsInt_Buffer_Cnt_M_u08[2] DigcolPsInt_Buffer_Cnt_M_u08[2] DigcolPsInt_BusBusySeqError_Cnt_M_lgc DigcolPsInt_CurrentSlave_Cnt_M_u08 DigcolPsInt_CurrentSlave_Cnt_M_u08 DigcolPsInt_GurrentSlave_Cnt_M_u08 DigcolPsInt_GurrentSlave_Cnt_M_u08 DigcolPsInt_GetData() DigcolPsInt_InitFailedOnce_Cnt_M_lgc DigcolPsInt_InitFailedOnce_Cnt_M_lgc DigcolPsInt_NackOccured_Cnt_M_lgc DigcolPsInt_NackOccured_Cnt_M_lgc DigcolPsInt_RevOverrunError_Cnt_M_lgc DigcolPsInt_RevOverrunError_Cnt_M_lgc DigcolPsInt_RevOverrunError_Cnt_M_lgc DigcolPsInt_RevOverrunError_Cnt_M_lgc DigcolPsInt_Sensinitialized_Cnt_M_lgc DigcolPsInt_Sensinitialized_Cnt_M_lgc DigcolPsInt_Sensinitialized_Cnt_M_lgc DigcolPsInt_Sensinitialized_Cnt_M_lgc DigcolPsInt_Sensinitialized_Cnt_M_lgc DigcolPsInt_PrevTransmit(DataLength_Cnt_T_u16) 12c_Send(Length_Cnt_T_u32) 1 1 12c_Send(Length_Cnt_T_u16 22295 22295 1arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	· ·			
target_i2cREG1_temp.PD         3           target_i2cREG1_temp.PSL         3           Name         Actual Value         Expected Value         Resilem           DigColPsInt_Buffer_Cnt_M_u08[0]         36         36         36           DigColPsInt_Buffer_Cnt_M_u08[1]         50         50         50           DigColPsInt_Buffer_Cnt_M_u08[2]         60         60         60           DigColPsInt_BusBusySeqError_Cnt_M_uge         0         0         0           DigColPsInt_CurrentSlave_Cnt_M_u08         52         52         52           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR1_READERROR_SETREG         INIT_SENSOR1_READERROR_SETREG         6         5         1         5				
Name				
Name         Actual Value         Expected Value         Resident           DigColPsInt_Buffer_Cnt_M_u08[0]         36         36         36           DigColPsInt_Buffer_Cnt_M_u08[1]         50         50         50           DigColPsInt_BusbusySeqError_Cnt_M_u08[2]         60         60         60           DigColPsInt_BusbusySeqError_Cnt_M_u08         52         52         52           DigColPsInt_CurrentStave_Cnt_M_u08         52         52         52           DigColPsInt_GetData()         6         6         6           DigColPsInt_GetData()         6         6         6           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0         0         0           DigColPsInt_NackOccured_Cnt_M_lgc         0         0         0           DigColPsInt_PrevTransactionCnt_Cnt_M_u08         51         51         51           DigColPsInt_SensInitialized_Cnt_M_lgc         0         0         0           DigColPsInt_SensInitialized_Cnt_M_lgc         1         1         1           12c_Send(Length_Cnt_T_u32)         1         1         1           12c_Send(Length_Cnt_T_u16)         2         22295         22295           target_DataTypePtr_Cnt_T_u08         2         2         2	· ·			
DigColPsInt_Buffer_Cnt_M_u08[0]         36         36           DigColPsInt_Buffer_Cnt_M_u08[1]         50         50           DigColPsInt_Buffer_Cnt_M_u08[2]         60         60           DigColPsInt_BusBusySeqError_Cnt_M_lgc         0         0           DigColPsInt_CurrentSlave_Cnt_M_u08         52         52           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR1_READERROR_SETREG         INIT_SENSOR1_READERROR_SETREG           DigColPsInt_GetData()         6         6           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0         0           DigColPsInt_NackOccured_Cnt_M_lgc         0         0           DigColPsInt_PrevTransactionCnt_Cnt_M_u08         51         51           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0           DigColPsInt_Sensinitalized_Cnt_M_lgc         1         1           DigColPsInt_Sensinitalized_Cnt_M_lgc         1         1           DigColPsInt_Sensinitalized_Cnt_M_lgc         1         1           DigColPsInt_Sensinitalized_Cnt_M_lgc         1         1           12c_Send(Length_Cnt_T_u32)         1         1           12c_SetupMasterTransmit(DataLength_Cnt_T_u16)         1         1           1arget_DataTypePtr_Cnt_T_u08         2         2	·		Expected Value	Dogult
DigColPsInt_Buffer_Cnt_M_u08[1]         50         50           DigColPsInt_Buffer_Cnt_M_u08[2]         60         60           DigColPsInt_BusBusySeqError_Cnt_M_lgc         0         0           DigColPsInt_CurrentSlave_Cnt_M_u08         52         52           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR1_READERROR_SETREG         INIT_SENSOR1_READERROR_SETREG           DigColPsInt_GetData()         6         6           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0         0           DigColPsInt_NackOccured_Cnt_M_lgc         0         0           DigColPsInt_PrevTransactionCnt_Cnt_M_u08         51         51           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0           DigColPsInt_SensInitalized_Cnt_M_lgc         1         1           I2c_Send(Length_Cnt_T_u32)         1         1           I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)         1         1           target_ColSnsrDataPtr_Cnt_T_u16         22295         22295           target_DataTypePtr_Cnt_T_u08         2         2           target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR         567         567			-	Result
DigColPsInt_Buffer_Cnt_M_u08[2]         60         60           DigColPsInt_BusBusySeqError_Cnt_M_lgc         0         0           DigColPsInt_CurrentSlave_Cnt_M_u08         52         52           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR1_READERROR_SETREG         INIT_SENSOR1_READERROR_SETREG           DigColPsInt_GetData()         6         6           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0         0           DigColPsInt_NackOccured_Cnt_M_lgc         0         0           DigColPsInt_PrevTransactionCnt_Cnt_M_u08         51         51           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0           DigColPsInt_SensInitialized_Cnt_M_lgc         1         1           DigColPsInt_SensInitialized_Cnt_M_lgc         1         1           12c_Send(Length_Cnt_T_u32)         1         1           12c_SetupMasterTransmit(DataLength_Cnt_T_u16)         1         1           target_ColSnsrDataPtr_Cnt_T_u16         22295         22295           target_DataTypePtr_Cnt_T_u08         2         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR         567				
DigColPsInt_BusBusySeqError_Cnt_M_lgc         0         0           DigColPsInt_CurrentSlave_Cnt_M_u08         52         52           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR1_READERROR_SETREG         INIT_SENSOR1_READERROR_SETREG           DigColPsInt_GetData()         6         6           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0         0           DigColPsInt_NackOccured_Cnt_M_lgc         0         0           DigColPsInt_PrevTransactionCnt_Cnt_M_u08         51         51           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0           DigColPsInt_SensInitialized_Cnt_M_lgc         1         1           12c_Send(Length_Cnt_T_u32)         1         1           12c_SetupMasterTransmit(DataLength_Cnt_T_u16)         1         1           target_ColSnsrDataPtr_Cnt_T_u16         22295         22295           target_DataTypePtr_Cnt_T_u08         2         2           target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR         567         567				~
DigColPsInt_CurrentSlave_Cnt_M_u08         52         52           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR1_READERROR_SETREG         INIT_SENSOR1_READERROR_SETREG           DigColPsInt_GetData()         6         6           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0         0           DigColPsInt_NackOccured_Cnt_M_lgc         0         0           DigColPsInt_PrevTransactionCnt_Cnt_M_u08         51         51           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0           DigColPsInt_SensInitialized_Cnt_M_lgc         1         1           12c_Send(Length_Cnt_T_u32)         1         1           12c_SetupMasterTransmit(DataLength_Cnt_T_u16)         1         1           target_ColSnsrDataPtr_Cnt_T_u16         22295         22295           target_DataTypePtr_Cnt_T_u08         2         2           target_12c_Send_I2cRegPtr_Cnt_T_str.OAR         567         567				<b>_</b>
DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR1_READERROR_SETREG           DigColPsInt_GetData()         6           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0           DigColPsInt_NackOccured_Cnt_M_lgc         0           DigColPsInt_PrevTransactionCnt_Cnt_M_u08         51           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0           DigColPsInt_SensInitialized_Cnt_M_lgc         1           DigColPsInt_SensInitialized_Cnt_M_lgc         1           12c_Send(Length_Cnt_T_u32)         1           12c_SetupMasterTransmit(DataLength_Cnt_T_u16)         1           target_ColSnsrDataPtr_Cnt_T_u16         22295           target_DataTypePtr_Cnt_T_u08         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR         567				~
DigColPsInt_GetData()       6       6         DigColPsInt_InitFailedOnce_Cnt_M_lgc       0       0         DigColPsInt_NackOccured_Cnt_M_lgc       0       0         DigColPsInt_PrevTransactionCnt_Cnt_M_u08       51       51         DigColPsInt_RecvOverrunError_Cnt_M_lgc       0       0         DigColPsInt_SensInitialized_Cnt_M_lgc       1       1         I2c_Send(Length_Cnt_T_u32)       1       1         I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)       1       1         target_ColSnsrDataPtr_Cnt_T_u16       22295       22295         target_DataTypePtr_Cnt_T_u08       2       2         target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR       567       567				~
DigColPsInt_InitFailedOnce_Cnt_M_lgc         0         0           DigColPsInt_NackOccured_Cnt_M_lgc         0         0           DigColPsInt_PrevTransactionCnt_Cnt_M_u08         51         51           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0           DigColPsInt_SensInitialized_Cnt_M_lgc         1         1           I2c_Send(Length_Cnt_T_u32)         1         1           I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)         1         1           target_ColSnsrDataPtr_Cnt_T_u16         22295         22295           target_DataTypePtr_Cnt_T_u08         2         2           target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR         567         567	DigColPsInt_CurrentStepNo_Cnt_M_enum			~
DigColPsInt_NackOccured_Cnt_M_lgc         0         0           DigColPsInt_PrevTransactionCnt_Cnt_M_u08         51         51           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0           DigColPsInt_SensInitialized_Cnt_M_lgc         1         1           I2c_Send(Length_Cnt_T_u32)         1         1           I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)         1         1           target_ColSnsrDataPtr_Cnt_T_u16         22295         22295           target_DataTypePtr_Cnt_T_u08         2         2           target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR         567         567				~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08         51         51           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0           DigColPsInt_SensInitialized_Cnt_M_lgc         1         1           I2c_Send(Length_Cnt_T_u32)         1         1           I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)         1         1           target_ColSnsrDataPtr_Cnt_T_u16         22295         22295           target_DataTypePtr_Cnt_T_u08         2         2           target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR         567         567				~
DigCoIPsInt_RecvOverrunError_Cnt_M_igc         0         0           DigCoIPsInt_SensInitialized_Cnt_M_igc         1         1           I2c_Send(Length_Cnt_T_u32)         1         1           I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)         1         1           target_ColSnsrDataPtr_Cnt_T_u16         22295         22295           target_DataTypePtr_Cnt_T_u08         2         2           target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR         567         567				~
DigColPsInt_SensInitialized_Cnt_M_lgc         1         1           I2c_Send(Length_Cnt_T_u32)         1         1           I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)         1         1           target_ColSnsrDataPtr_Cnt_T_u16         22295         22295           target_DataTypePtr_Cnt_T_u08         2         2           target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR         567         567	DigColPsInt_PrevTransactionCnt_Cnt_M_u08	51	51	~
I2c_Send(Length_Cnt_T_u32)       1       1         I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)       1       1         target_ColSnsrDataPtr_Cnt_T_u16       22295       22295         target_DataTypePtr_Cnt_T_u08       2       2         target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR       567       567	DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)       1       1         target_ColSnsrDataPtr_Cnt_T_u16       22295       22295         target_DataTypePtr_Cnt_T_u08       2       2         target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR       567       567	DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	~
target_ColSnsrDataPtr_Cnt_T_u16       22295       22295         target_DataTypePtr_Cnt_T_u08       2       2         target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR       567       567	I2c_Send(Length_Cnt_T_u32)	1	1	~
target_ColSnsrDataPtr_Cnt_T_u16       22295       22295         target_DataTypePtr_Cnt_T_u08       2       2         target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR       567       567	I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
target_DataTypePtr_Cnt_T_u08       2       2         target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR       567       567		22295	22295	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR 567 567		2	2	~
		567	567	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR 44 44		44	44	~





Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.PID11	4466	4466	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.DMAC	1	1	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.FUN	1	1	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.DIR	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	~
target I2c Send I2cRegPtr Cnt T str.CLR	2	2	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.ODR	0	0	~
target I2c Send I2cRegPtr Cnt T str.PD	3	3	•
target I2c Send I2cRegPtr Cnt T str.PSL	3	3	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	567	567	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	566	566	_
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	4466	4466	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	129	129	_
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	6	6	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	567	567	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	44	44	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	554	554	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	_
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	44	44	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	4466	4466	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	44	44	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	1	1	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	·
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	2	2	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	0	0	<b>V</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	2	2	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	0	0	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	3	3	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3	3	
target SpurSnsrDataPtr Cnt T u16	20488	20488	
targot_operonorbatar ti_ont_1_u10	20400	20700	

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	-
I2c_Send	1	I2c_Send	1	<b>✓</b>
GetSystemTime mS u32	1	GetSystemTime mS u32	1	<b>~</b>

Test Step 2.9 (Repeat Count = 1)		V
Name	Input Value	
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16	
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08	
DigColPsInt_Buffer_Cnt_M_u08[0]	70	
DigColPsInt_Buffer_Cnt_M_u08[1]	80	
DigColPsInt_Buffer_Cnt_M_u08[2]	90	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	
DigColPsInt_ColSnsrData_Cnt_M_u16	24680	
DigColPsInt_CurrentSlave_Cnt_M_u08	70	
DigColPsInt CurrentStepNo Cnt M enum	INIT SENSOR1 READEXTERR SETREG	





Name	Input Value
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	13508813
DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt PrevTransactionCnt Cnt M u08	0 255
DigColPsInt RecvOverrunError Cnt M Igc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	22031
DigColPsInt_TransactionCnt_Cnt_M_u08	65
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp k ColSensorl2CAddress Cnt u08	target_i2cREG1_temp 59
k_I2CHWInitTransactionTime_Sec_f32	4.3000019
target_DtrmnElapsedTime_mS_u16_ElapsedTime	53999
target_GetSystemTime_mS_u32_CurrentTime	9497805
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	89
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	89 7
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0 1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR target_I2c Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	89
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL target_i2cREG1_temp.OAR	0 65
target_izertEd1_temp.OAR	
tarnet_i2cREG1_temn_IMR	89
target_i2cREG1_temp.IMR target_i2cREG1_temp.STR	89 67

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5.1. 1. <u>2.1.</u> 1.			
Name	Input Value		
target_i2cREG1_temp.CLKH	577		
target_i2cREG1_temp.CNT	88		
target_i2cREG1_temp.DRR	23		
target_i2cREG1_temp.SAR	65		
target_i2cREG1_temp.DXR	89		
target_i2cREG1_temp.MDR	7		
target_i2cREG1_temp.IVR	44		
target_i2cREG1_temp.EMDR	2		
target_i2cREG1_temp.PSC	89		
target_i2cREG1_temp.PID11	577		
target_i2cREG1_temp.PID12	89		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	2		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt Buffer Cnt M u08[0]	70	70	\(\sigma\)
DigColPsInt Buffer Cnt M u08[1]	80	80	~
DigColPsInt_Buffer_Cnt_M_u08[2]	90	90	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt_CurrentSlave_Cnt_M_u08	70	70	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR1 READEXTERR SETREG	INIT_SENSOR1_READEXTERR_SETREG	~
	168	168	
DigColPoint_GetData()	0	0	~
DigColPoint_InitFailedOnce_Cnt_M_lgc	0	0	
DigColPoint_NackOccured_Cnt_M_lgc	65	65	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	0	0	
DigColPsInt_RecvOverrunError_Cnt_M_lgc			~
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	
target_ColSnsrDataPtr_Cnt_T_u16	24680	24680	<b>✓</b>
target_DataTypePtr_Cnt_T_u08	3	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	65	65	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	89	89	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	67	67	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	7	7	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	88	88	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	23	23	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	65	65	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	89	89	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	7	7	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	577	577	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	89	89	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0	0	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	0	0	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	1	1	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
<u> </u>	1	1	

DigColPsInt\_GetData



Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	•
target_SpurSnsrDataPtr_Cnt_T_u16	22031	22031	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

Test Step 2.10 (Repeat Count = 1)	
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	3
DigColPsInt_Buffer_Cnt_M_u08[1]	6
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	27065
DigColPsInt_CurrentSlave_Cnt_M_u08	77
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_SETREG
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
higColPsInt_InitialTime_mS_M_u32	14511565
higColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	130
bigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	23574
DigColPsInt_TransactionCnt_Cnt_M_u08	79
OtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
SetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
2cREG1_temp	target_i2cREG1_temp
ColSensorI2CAddress Cnt u08	66
I I2CHWInitTransactionTime Sec f32	4.69999981
arget DtrmnElapsedTime mS u16 ElapsedTime	741
arget_GetSystemTime_mS_u32_CurrentTime	10500557
arget I2c Send I2cRegPtr Cnt T str.OAR	54
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
arget I2c Send I2cRegPtr Cnt T str.STR	8
arget I2c Send I2cRegPtr Cnt T str.CLKL	554
arget I2c Send I2cRegPtr Cnt T str.CLKH	344
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123
arget I2c Send I2cRegPtr Cnt T str.DRR	45
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54
arget I2c Send I2cRegPtr Cnt T str.DXR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554
arget I2c Send I2cRegPtr Cnt T str.IVR	788
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344
arget I2c Send I2cRegPtr Cnt T str.PID12	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
arget I2c Send I2cRegPtr Cnt T str.DIN	2
arget_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	3





Name	Input Value		
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3		
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	3		
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	1		
target_12c_Send_12cRegPtr_Cnt_T_str.PSL	2		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	54		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	8		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c SetupMasterTransmit_l2cRegPtr_Cnt_T str.CLKH	344		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	123		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	66		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR target_l2c SetupMasterTransmit_l2cRegPtr_Cnt_T str.IVR	788		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.FMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	2		
target_i2cREG1_temp.OAR	54		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	8		
target_i2cREG1_temp.CLKL	554		
target_i2cREG1_temp.CLKH target_i2cREG1_temp.CNT	123		
target i2cREG1 temp.DRR	45		
target_i2cREG1_temp.SAR	54		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	554		
target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR	788		
target i2cREG1 temp.PSC	66		
target_i2cREG1_temp.PID11	344		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	3		
target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	3		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL	1 2		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	3	3	√ V
DigColPsInt_Buffer_Cnt_M_u08[1]	6	6	~
DigColPsInt_Buffer_Cnt_M_u08[2]	9	9	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	<b>V</b>
DigColPsInt_CurrentStave_Cnt_M_u08	77 INIT_SENSOR2_READERROR_SETREG	77 INIT_SENSOR2_READERROR_SETREG	<b>*</b>
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData()	6	6	-
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	79	79	<b>~</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_lgc	1 27065	1 27065	<b>~</b>
target_ColSnsrDataPtr_Cnt_T_u16 target_DataTypePtr_Cnt_T_u08	27065	4	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	54	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8	8	~

DigColPsInt\_GetData



Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554	554	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	344	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	123	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	45	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	54	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	554	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	788	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344	344	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54	54	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8	8	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554	554	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344	344	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123	123	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45	45	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54	54	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554	554	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788	788	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344	344	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	2	2	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_SpurSnsrDataPtr_Cnt_T_u16	23574	23574	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime mS u16	1	DtrmnElapsedTime mS u16	1	<b>✓</b>

Test Step 2.11 (Repeat Count = 1)	V v v v v v v v v v v v v v v v v v v v
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	11
DigColPsInt_Buffer_Cnt_M_u08[1]	22
DigColPsInt_Buffer_Cnt_M_u08[2]	33
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	0
DigColPsInt_CurrentSlave_Cnt_M_u08	84
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	15514317
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	93
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1

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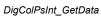


Name	Input Value
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	25117
DigColPsInt_TransactionCnt_Cnt_M_u08	93
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	73
k_I2CHWInitTransactionTime_Sec_f32	5.0999999
target_DtrmnElapsedTime_mS_u16_ElapsedTime	1248
target_GetSystemTime_mS_u32_CurrentTime	11503309
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	3
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	100 7788
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	2767
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	556
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	564
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3 100
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556
	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12 target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_12c_Send_12cRegPtr_Cnt_T_str.FUN	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	1
target_12c_Send_12cRegPtr_Cnt_T_str.DIN	3
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	2
target_12c_Send_12cRegPtr_Cnt_T_str.SET	0
target_12c_Send_12cRegPtr_Cnt_T_str.CLR	1
target_i2c_Send_i2cRegPtr_Cnt_T_str.ODR	3
target_i2c_Send_i2cRegPtr_Cnt_T_str.PD	0
target I2c Send I2cRegPtr Cnt T str.PSL	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	100
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	7788
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	2767
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	100
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	2767
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	9
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	100
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	3
target_i2cREG1_temp.IMR	100
target_i2cREG1_temp.STR	7788
target i2cREG1 temp.CLKL	2767
	556
target i2cREG1 temp.CLKH	111
target_i2cREG1_temp.CLKH target_i2cREG1_temp.CNT	564
target_i2cREG1_temp.CNT	
	564 88 3





Name	Input Value		
target_i2cREG1_temp.MDR	2767		
target_i2cREG1_temp.IVR	9		
target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC	100		
target i2cREG1_temp.PID11	556		
target_i2cREG1_temp.PID12	100		
target i2cREG1 temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	3		
target_i2cREG1_temp.PD	0 3		
target_i2cREG1_temp.PSL		Francis d Value	Daguilé
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	36 22	36 22	<b>*</b>
DigColPsInt_Buffer_Cnt_M_u08[2]	33	33	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	-
DigColPsInt CurrentSlave Cnt M u08	73	73	-
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	•
DigColPsInt_GetData()	40	40	-
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	<b>~</b>
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	93	93	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	~
I2c_Send(Length_Cnt_T_u32)	1	1	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	<b>V</b>
target_ColSnsrDataPtr_Cnt_T_u16	0	0	<b>✓</b>
target_DataTypePtr_Cnt_T_u08 target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	3	Ž
target_I2C_Send_I2cRegPtr_Cnt_T_str.IMR	100	100	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	7788	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	556	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	564	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	88	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	100	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	2767	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	9	<b>•</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	0	0	Ž
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	100 556	100 556	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	-
target I2c Send I2cRegPtr Cnt T str.DIR	1	1	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	-
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	3	3	<b>V</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	100 7788	100 7788	· ·
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	2767	2767	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	556	556	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	88	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100	100	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	2767	2767	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	100	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	556 100	556 100	· ·





Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✓
target_SpurSnsrDataPtr_Cnt_T_u16	25117	25117	✓

Τ	Τ		V	
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c_Send	1	I2c_Send	1	•
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	~

Test Step 2.12 (Repeat Count = 1)	
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	44
DigColPsInt_Buffer_Cnt_M_u08[1]	55
DigColPsInt_Buffer_Cnt_M_u08[2]	66
DigColPsInt BusBusySeqError Cnt M Igc	1
DigColPsInt CmdFailOccurred Cnt M Igc	0
DigColPsInt ColSnsrData Cnt M u16	65535
DigColPsInt CurrentSlave Cnt M u08	91
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READEXTERR_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt InitialTime mS M u32	16517069
DigColPsInt NackOccured Cnt M Igc	1
DigColPsInt PrevTransactionCnt Cnt M u08	113
DigColPsInt_RecvOverrunError_Cnt_M_Igc	0
DigColPsInt RecvdDataType Cnt M u08	1
DigColPsInt SensInitialized Cnt M Igc	1
DigColPsInt SpurSnsrData Cnt M u16	26660
DigColPsInt TransactionCnt Cnt M u08	107
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c Send(I2cRegPtr Cnt T str)	target I2c Send I2cRegPtr Cnt T str
I2c SetupMasterTransmit(I2cRegPtr Cnt T str)	target I2c SetupMasterTransmit I2cRegPtr Cnt T str
SpurSnsrDataPtr Cnt T u16	target_ize_Setupinaster Harishite_izeRegrit_Crit_1_sti
i2cREG1 temp	target_i2cREG1_temp
k ColSensorl2CAddress Cnt u08	80
k_I2CHWInitTransactionTime_Sec_f32	5.5
target DtrmnElapsedTime mS u16 ElapsedTime	1755
target GetSystemTime mS u32 CurrentTime	12506061
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	678
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	6788
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	7878
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	678
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	778
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	6788
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
	1





Name	Input Value		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2		
	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	678		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	45		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	6788		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	7878		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	678		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	45		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	778		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	45		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	6788		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	45		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	0		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	1		
	1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1		
target_i2cREG1_temp.OAR	678		
target_i2cREG1_temp.IMR	45		
target_i2cREG1_temp.STR	66		
target_i2cREG1_temp.CLKL	56		
target_i2cREG1_temp.CLKH	6788		
target_i2cREG1_temp.CNT	7878		
target_i2cREG1_temp.DRR	12		
target_i2cREG1_temp.SAR	678		
target_i2cREG1_temp.DXR	45		
target_i2cREG1_temp.MDR	56		
target_i2cREG1_temp.IVR	778		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	45		
target_i2cREG1_temp.PID11	6788		
target_i2cREG1_temp.PID12	45		
target_i2cREG1_temp.DMAC	1		
target i2cREG1 temp.FUN	1		
target i2cREG1 temp.DIR	0		
target i2cREG1 temp.DIN	1		
target_i2cREG1_temp.DOUT	1		
target i2cREG1 temp.SET	1		
target i2cREG1 temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	2		
target_i2cREG1_temp.PSL	1		
		From a stand Walter	December
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	44	44	
DigColPsInt_Buffer_Cnt_M_u08[1]	55	55	~
DigColPsInt_Buffer_Cnt_M_u08[2]	66	66	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	<b>~</b>
DigColPsInt_CurrentSlave_Cnt_M_u08	91	91	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READEXTERR_READ	INIT_SENSOR2_READEXTERR_READ	~
DigColPsInt_GetData()	6	6	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	107	107	~
DigColPsInt_RecvOverrunError_Cnt_M_Igc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	<b>✓</b>
target_ColSnsrDataPtr_Cnt_T_u16	65535	65535	•
target_DataTypePtr_Cnt_T_u08	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	678	678	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	45	45	~

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	56	56	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	7878	7878	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	678	678	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	45	45	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	56	56	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	778	778	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	45	45	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	6788	6788	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	45	45	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	678	678	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	45	45	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	66	66	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	56	56	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	7878	7878	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	678	678	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	45	45	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	56	56	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	778	778	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	45	45	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	6788	6788	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	45	45	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	<b>✓</b>
target SpurSnsrDataPtr Cnt T u16	26660	26660	

T				V
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime mS u16	1	DtrmnElapsedTime mS u16	1	<b>✓</b>

Test Step 2.13 (Repeat Count = 1)	
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	20000
DigColPsInt_CurrentSlave_Cnt_M_u08	98
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_SETREG
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	17519821
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	131

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Name	Input Value	
DigColPsInt_RecvOverrunError_Cnt_M_Igc	1	
DigColPsInt_RecvdDataType_Cnt_M_u08	2	
DigColPsInt_SensInitialized_Cnt_M_lgc	0	
DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08	28203 121	
DtrmnElapsedTime_mS_u16(ElapsedTime)	target DtrmnElapsedTime mS u16 ElapsedTime	
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime	
I2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str	
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str	
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16	
i2cREG1_temp	target_i2cREG1_temp	
k_ColSensorl2CAddress_Cnt_u08	87	
k_I2CHWInitTransactionTime_Sec_f32	5.9000001	
target_DtrmnElapsedTime_mS_u16_ElapsedTime	2262	
target_GetSystemTime_mS_u32_CurrentTime target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	13508813 66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	0 78	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	56	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1 0	
target_12c_Send_12cRegPtr_Cnt_T_str.PSL	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	495 66	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.tvR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0 0	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	
target_i2cREG1_temp.OAR	66	
target_i2cREG1_temp.IMR	78	
target_i2cREG1_temp.STR	78	
target_i2cREG1_temp.CLKL	495	
target_i2cREG1_temp.CLKH	56	
target_i2cREG1_temp.CNT	897	
target_i2cREG1_temp.DRR	98	
target_i2cREG1_temp.SAR	66	

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Name	Input Value		
target_i2cREG1_temp.DXR	78		
target_i2cREG1_temp.MDR	495		
target_i2cREG1_temp.IVR	66		
target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC	78		
target_i2cREG1_temp.PID11	56		
target i2cREG1 temp.PID12	78		
target_i2cREG1_temp.DMAC	0		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	0		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR	0		
target i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	~
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	-
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	-
DigColPsInt_BusBusySeqError_Cnt_M_Igc	0	0	-
DigColPsInt_CurrentSlave_Cnt_M_u08	87	87	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	~
DigColPsInt_GetData()	40	40	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	121	121	<b>V</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	· ·
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	
I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	
target_ColSnsrDataPtr_Cnt_T_u16	20000	20000	-
target_DataTypePtr_Cnt_T_u08	2	2	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	<b>*</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	78 495	78 495	-
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	0	0	<b>*</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	<b>V</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	66	66	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	· ·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495 66	· ·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	0	0	7
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	78	78	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	-
0 T T	<u> </u>	1	

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	•
target_SpurSnsrDataPtr_Cnt_T_u16	28203	28203	•

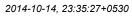
Τ				V
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c_Send	1	I2c_Send	1	~
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	~

Name	Input Value
ColSnsrDataPtr Cnt T u16	target ColSnsrDataPtr Cnt T u16
DataTypePtr Cnt T u08	target DataTypePtr Cnt T u08
DigColPsInt Buffer Cnt M u08[0]	40
DigColPsInt Buffer Cnt M u08[1]	50
DigColPsInt Buffer Cnt M u08[2]	60
DigColPsInt BusBusySeqError Cnt M lgc	1
DigColPsInt CmdFailOccurred Cnt M lgc	0
DigColPsInt_CilidraliOccurred_Cili_wi_igc	33568
DigColPsInt_CurrentSlave_Cnt_M_u08	105
	INIT SENSOR2 EXTREADADDRREG SENDCMD
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
	18522573
DigColPsInt_InitialTime_mS_M_u32	
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	149
DigColPsInt_RecvOverrunError_Cnt_M_lgc	
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	0
DigColPsInt_TransactionCnt_Cnt_M_u08	135
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
2cREG1_temp	target_i2cREG1_temp
<_ColSensorI2CAddress_Cnt_u08	94
<pre>c_I2CHWInitTransactionTime_Sec_f32</pre>	6.30000019
arget_DtrmnElapsedTime_mS_u16_ElapsedTime	2769
arget_GetSystemTime_mS_u32_CurrentTime	14511565
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2

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Name target I2c Send I2cRegPtr Cnt T str.DIN	Input Value 0		
target_12c_Send_12cRegPtr_Cnt_1_str.DIN target_12c_Send_12cRegPtr_Cnt_T_str.DOUT	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2		
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	44 4444		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	4466		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	554 1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1 2		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	567		
target_i2cREG1_temp.IMR	44		
target_i2cREG1_temp.STR	4444		
target_i2cREG1_temp.CLKL	566		
target_i2cREG1_temp.CLKH	4466 129		
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	6		
target_i2cREG1_temp.SAR	567		
target i2cREG1 temp.DXR	44		
target_i2cREG1_temp.MDR	566		
target_i2cREG1_temp.IVR	554		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	44		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12	4466 44		
target_i2cREG1_temp.DMAC	1		
target i2cREG1 temp.FUN	1		
target_i2cREG1_temp.DIR	2		
target_i2cREG1_temp.DIN	0		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL	3 3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	40	40	Result
DigColPsInt_Buffer_Cnt_M_u08[1]	50	50	<b>*</b>
DigColPsInt Buffer Cnt M u08[2]	60	60	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt_CurrentSlave_Cnt_M_u08	105	105	~
DigColPsInt_CurrentStepNo_Cnt_M_enum		INIT_SENSOR2_EXTREADADDRREG_SEN	~
DigColPsInt_GetData()	6	6	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	<b>V</b>
DigColPsInt_NackOccured_Cnt_M_lgc	0 135	0 135	<i>y</i>
DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	<b>*</b>
DigColPsInt SensInitialized Cnt M lgc	1	1	~
target_ColSnsrDataPtr_Cnt_T_u16	33568	33568	~
target_DataTypePtr_Cnt_T_u08	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	~

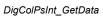




Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	✓
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	44	44	✓
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	566	566	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✓
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	1	1	✓
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_SpurSnsrDataPtr_Cnt_T_u16	0	0	~

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

Test Step 2.15 (Repeat Count = 1)		~
Name	Input Value	
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16	
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08	
DigColPsInt_Buffer_Cnt_M_u08[0]	70	
DigColPsInt_Buffer_Cnt_M_u08[1]	80	
DigColPsInt_Buffer_Cnt_M_u08[2]	90	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	
DigColPsInt_ColSnsrData_Cnt_M_u16	45897	
DigColPsInt_CurrentSlave_Cnt_M_u08	112	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_READ	
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1	
DigColPsInt_InitialTime_mS_M_u32	19525325	
DigColPsInt_NackOccured_Cnt_M_lgc	0	





Name	Input Value
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	167
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	65535
DigColPsInt_TransactionCnt_Cnt_M_u08	149
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	101
k_I2CHWInitTransactionTime_Sec_f32	6.6999981
target_DtrmnElapsedTime_mS_u16_ElapsedTime	3276
target_GetSystemTime_mS_u32_CurrentTime target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	15514317 65
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	89
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	67
target I2c Send I2cRegPtr Cnt T str.CLKL	7
target I2c Send I2cRegPtr Cnt T str.CLKH	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	1
target I2c_Send_I2cRegPtr_Cnt_T_str.PD target I2c Send I2cRegPtr Cnt T str.PSL	2 0
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	577
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	1 2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2 0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL target_l2cREG1_temp.OAR	65
	89
target_i2cREG1_temp.IMR	89 67
target_i2cREG1_temp.IMR target_i2cREG1_temp.STR	67
target_i2cREG1_temp.IMR target_i2cREG1_temp.STR target_i2cREG1_temp.CLKL	
target_i2cREG1_temp.IMR target_i2cREG1_temp.STR	67 7

DigColPsInt\_GetData





Name	Input Value		
target_i2cREG1_temp.SAR	65		
target_i2cREG1_temp.DXR	89		
target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR	44		
target i2cREG1 temp.EMDR	2		
target i2cREG1 temp.PSC	89		
target_i2cREG1_temp.PID11	577		
target_i2cREG1_temp.PID12	89		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	2 2		
target_i2cREG1_temp.SET target_i2cREG1_temp.CLR	0		
target i2cREG1 temp.ODR	1		
target_i2cREG1_temp.PD	2		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt Buffer Cnt M u08[0]	36	36	~
DigColPsInt_Buffer_Cnt_M_u08[1]	80	80	•
DigColPsInt_Buffer_Cnt_M_u08[2]	90	90	•
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt_CurrentSlave_Cnt_M_u08	101	101	•
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	~
DigColPsInt_GetData()	40	40	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	149	149	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	<b>→</b>
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	
I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
target_ColSnsrDataPtr_Cnt_T_u16	45897	45897	
target_DataTypePtr_Cnt_T_u08	4	4	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	· ·
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	2	2	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>Y</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	89 67	89 67	-
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	7	7	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	~
		I	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	44 2 89	2 89	~

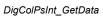
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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✓
target_SpurSnsrDataPtr_Cnt_T_u16	65535	65535	<b>✓</b>

Т			V	
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	•
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	<b>✓</b>
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	-

Name a	Invest Walter
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	44
DigColPsInt_Buffer_Cnt_M_u08[1]	55
DigColPsInt_Buffer_Cnt_M_u08[2]	66
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	58226
DigColPsInt_CurrentSlave_Cnt_M_u08	119
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADADDRREG_SENDCMD
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
ligColPsInt_InitialTime_mS_M_u32	20528077
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	185
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	35000
igColPsInt_TransactionCnt_Cnt_M_u08	163
trmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
SetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
2cREG1_temp	target_i2cREG1_temp
_ColSensorl2CAddress_Cnt_u08	108
_I2CHWInitTransactionTime_Sec_f32	7.099999
arget_DtrmnElapsedTime_mS_u16_ElapsedTime	3783
arget_GetSystemTime_mS_u32_CurrentTime	16517069
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
arget I2c Send I2cRegPtr Cnt T str.MDR	2309
arget I2c Send I2cRegPtr Cnt T str.IVR	5
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
arget I2c Send I2cRegPtr Cnt T str.FUN	1





Name	Input Value		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1 2		
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	87		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	67 55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	66		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	55 66		
target_i2cREG1_temp.IMR target_i2cREG1_temp.STR	556		
target i2cREG1 temp.CLKL	2309		
target i2cREG1 temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC	66		
target i2cREG1 temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR	1 2		
target_i2cREG1_temp.PD	3		
target i2cREG1 temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	44	44	~
DigColPsInt_Buffer_Cnt_M_u08[1]	55	55	~
DigColPsInt_Buffer_Cnt_M_u08[2]	66	66	~
DigColPsInt_BusBusySeqError_Cnt_M_Igc	0	0	<b>~</b>
DigColPsInt_CurrentSlave_Cnt_M_u08	119	119	<b>V</b>
DigColPsInt_CurrentStepNo_Cnt_M_enum		INIT_SENSOR1_EXTREADADDRREG_SEN	
DigColPsInt_GetData()	6	6 0	<b>*</b>
DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc	0	0	Ž
DigColPsInt_NackOccureu_Cnt_wi_gc  DigColPsInt PrevTransactionCnt Cnt M u08	163	163	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	<b>✓</b>
target_ColSnsrDataPtr_Cnt_T_u16	58226	58226	~
target_DataTypePtr_Cnt_T_u08	1	1	<b>✓</b>

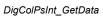




Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.PID12	66	66	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.DMAC	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	
target I2c Send I2cRegPtr Cnt T str.DIR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.SET	3	3	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	_
target I2c Send I2cRegPtr Cnt T str.PD	3	3	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.PSL	3	3	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	55	55	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	2309	2309	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	1204	1204	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	67	67	<b>→</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	55	55	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	2309	2309	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	5	5	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	66	66	<b>V</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	3	3	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_I_str.PD target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	
	35000	35000	
target_SpurSnsrDataPtr_Cnt_T_u16	33000	33000	

T				·
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime mS u16	1	DtrmnElapsedTime mS u16	1	•

Test Step 2.17 (Repeat Count = 1)		~
Name	Input Value	
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16	
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08	
DigColPsInt_Buffer_Cnt_M_u08[0]	66	
DigColPsInt_Buffer_Cnt_M_u08[1]	77	
DigColPsInt_Buffer_Cnt_M_u08[2]	88	
DigColPsInt_BusBusySeqError_Cnt_M_Igc	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	
DigColPsInt_ColSnsrData_Cnt_M_u16	62548	
DigColPsInt_CurrentSlave_Cnt_M_u08	126	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_DUMMY_SEND	
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	
DigColPsInt_InitialTime_mS_M_u32	21530829	





Name	Input Value
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	203
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	37896
DigColPsInt_TransactionCnt_Cnt_M_u08	177
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	115
k_I2CHWInitTransactionTime_Sec_f32	7.5
target_DtrmnElapsedTime_mS_u16_ElapsedTime	4290
target_GetSystemTime_mS_u32_CurrentTime	17519821
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	78
target_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56
target_i2cREG1_temp.CNT	897

DigColPsInt\_GetData





DigCoPaint   CurrentSlave   Cnt   M   J08				
Image: Control   Imag	Name	Input Value		
Sept.   Company   Compan	target_i2cREG1_temp.DRR	98		
September   Sept	target_i2cREG1_temp.SAR	66		
Sept   Company   Company	target_i2cREG1_temp.DXR	78		
	target_i2cREG1_temp.MDR	495		
	target_i2cREG1_temp.IVR	66		
Septiment	target_i2cREG1_temp.EMDR			
	· ·			
	·			
Image   Jack Pol   James DIN				
	0 =			
Sept   DRECT   New SET   1900   190	· ·			
Integral_CREFG1_temp.SET				
Image: Joseph College   Joseph College	· ·			
Imaged_2026EGI_stemp_OPC	· ·			
Internal Confect   Internal PD	· ·			
March   Marc				
Nation   DepCoPrint Buffer Cott M 100(0)   35   35   35   35   35   35   35   3				
DigicDaPini, Burler, Cult, MucRIP    77   77   77   77   77   77   77			I=	- u
DigicalPath, Bartle, Chit, MucRi   1			· ·	Result
DigicoPinit_Buffer_Crit_M_unit2				V
DepCoPaint_CurrentSise_Coft_M_Ug8				
DigCoPeInt, CurrentSiene, CM, M, UB				<b>*</b>
DepCoPaint_Colleging   DepCoPaint_Colleging   DepCoPaint_Colleging   DepCoPaint_Colleging   DepCoPaint_Colleging   DepCoPaint_Colleging   DepCoPaint_Colleging   DepCoPaint_Intelligence_Coll_Mige				
DigCoPeNt, InstituteOnce, Crit, Migo				
DigicalPaint, Institute Core. Crit. Mige   0   0   0   0   0   0   0   0   0				
DigCoPoInt, NeckCocured_Cnt_Migo				
DigCoPeint, PrevTransactionCrit_Crit_M_upc   0   0   0   0   0   0   0   0   0				
DigColPhilint Sensinitational Cm   M   Upc   1				-
DigCoPsint Sensinitalized Cnt   Migo				
1				-
12c, SetupMasterTransmit(DataLength_Cnt_Tu16)		·		
target_ColSnsr/DataPtr_Cnt_T_u16         62548         62548           target_DataPtyPertr_Cnt_T_u08         0         0           target_L2c_Sand_L2cRepPtr_Cnt_T_str_MR         66         66           target_L2c_Sand_L2cRepPtr_Cnt_T_str_MR         78         78           target_L2c_Sand_L2cRepPtr_Cnt_T_str_MR         78         78           target_L2c_Sand_L2cRepPtr_Cnt_T_str_CtkL         495         495           target_L2c_Send_L2cRepPtr_Cnt_T_str_CtkL         495         56           target_L2c_Sand_L2cRepPtr_Cnt_T_str_CtkL         495         56           target_L2c_Send_L2cRepPtr_Cnt_T_str_CtkL         495         56           target_L2c_Send_L2cRepPtr_Cnt_T_str_CtkL         495         56           target_L2c_Send_L2cRepPtr_Cnt_T_str_CtkL         495         56           target_L2c_Send_L2cRepPtr_Cnt_T_str_CtkL         495         496           target_L2c_Send_L2cRepPtr_Cnt_T_str_Attr_Cnt         66         66           target_L2c_Send_L2cRepPtr_				-
target L2s Send J2cRegPtr Cnt_Tstr.NAR         66         66         4           target L2s Send J2cRegPtr Cnt_Tstr.NAR         66         66         4           target J2s Send J2cRegPtr Cnt_Tstr.NAR         78         78         78           target J2s Send J2cRegPtr Cnt_Tstr.Str.NAR         78         78         78           target J2s Send J2cRegPtr Cnt_Tstr.CLKH         56         56         56           target J2s Send J2cRegPtr Cnt_Tstr.CLKH         56         56         56           target J2s Send J2cRegPtr Cnt_Tstr.DRR         89         89         98           target J2s Send J2cRegPtr Cnt_Tstr.DRR         98         98         98           target J2s Send J2cRegPtr Cnt_Tstr.DRR         66         66         66           target J2s Send J2cRegPtr Cnt_Tstr.DRR         495         495           target J2s Send J2cRegPtr Cnt_Tstr.DRR         66         66         66           target J2s S				
Larget   2e_ Send   2eRegPtr_Cnt_T_str.OAR				-
target_Ize_Send_2cRegPtr_Cntstr.NMR         78         78           target_Ize_Send_2cRegPtr_Cntstr.STR         78         78           target_Ize_Send_2cRegPtr_Cntstr.CkL         495         495           target_Ize_Send_2cRegPtr_Cntstr.CkH         56         56         56           target_Ize_Send_2cRegPtr_Cntstr.CkT         897         897         897           target_Ize_Send_2cRegPtr_Cnt_T_str.DRR         98         98         98           target_Ize_Send_2cRegPtr_Cnt_T_str.DRR         98         98         98           target_Ize_Send_1zcRegPtr_Cnt_T_str.DRR         66         66         66           target_Ize_Send_1zcRegPtr_Cnt_T_str.DRR         495         495           target_Ize_Send_1zcRegPtr_Cnt_T_str.DRR         495         495           target_Ize_Send_1zcRegPtr_Cnt_T_str.DRR         66         66         66           target_Ize_Send_1zcRegPtr_Cnt_T_str.DRR         68         66         66           target_Ize_Send_1zcRegPtr_Cnt_T_str.DRR         0         0         0           target_Ize_Send_1zcRegPtr_Cnt_T_str.DRR         66         66         66           target_Ize_Send_1zcRegPtr_Cnt_T_str.DRR         0         0         0           target_Ize_Send_1zcRegPtr_Cnt_T_str.DRR         0         0         <				
target_12c_Send_12cRegPtr_Cnt_T_str.STR         78           target_12c_Send_12cRegPtr_Cnt_T_str.CLKL         495           target_12c_Send_12cRegPtr_Cnt_T_str.CLKH         56           target_12c_Send_12cRegPtr_Cnt_T_str.CNT         897           target_12c_Send_12cRegPtr_Cnt_T_str.DRR         98           target_12c_Send_12cRegPtr_Cnt_T_str.DRR         98           target_12c_Send_12cRegPtr_Cnt_T_str.DXR         78           target_12c_Send_12cRegPtr_Cnt_T_str.DMR         78           target_12c_Send_12cRegPtr_Cnt_T_str.DMR         495           target_12c_Send_12cRegPtr_Cnt_T_str.DMR         495           target_12c_Send_12cRegPtr_Cnt_T_str.DMDR         0           target_12c_Send_12cRegPtr_Cnt_T_str.DMDR         0           target_12c_Send_12cRegPtr_Cnt_T_str.DMDR         0           target_12c_Send_12cRegPtr_Cnt_T_str.DMDR         0           target_12c_Send_12cRegPtr_Cnt_T_str.DMD         0           target_12c_Send_12cRegPtr_Cnt_T_str.DMD         0           target_12c_Send_12cRegPtr_Cnt_T_str.DMD         0           target_12c_Send_12cRegPtr_Cnt_T_str.DMD         0           target_12c_Send_12cRegPtr_Cnt_T_str.DMD         0           target_12c_Send_12cRegPtr_Cnt_T_str.DMD         0           target_12c_Send_12cRegPtr_Cnt_T_str.DMT         0           target_1				-
target   12c   Send   2cRegPtr Cnt T   str.CtKl				
target_12c_Send_12cRegPtr_Cnt_T_str.CNT         897         897           target_12c_Send_12cRegPtr_Cnt_T_str.CNT         897         897           target_12c_Send_12cRegPtr_Cnt_T_str.DNR         98         98           target_12c_Send_12cRegPtr_Cnt_T_str.DNR         78         78           target_12c_Send_12cRegPtr_Cnt_T_str.DNR         78         78           target_12c_Send_12cRegPtr_Cnt_T_str.DNR         495         495           target_12c_Send_12cRegPtr_Cnt_T_str.DNR         66         66           target_12c_Send_12cRegPtr_Cnt_T_str.DNR         66         66           target_12c_Send_12cRegPtr_Cnt_T_str.DNR         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DNDR         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DD114         56         56           target_12c_Send_12cRegPtr_Cnt_T_str.DNAC         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DNAC         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DNAC         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DNA         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DNA         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DNA         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DNA <t< td=""><td></td><td></td><td></td><td>-</td></t<>				-
larget_ 2c_Send_ 2cRegPtr_Cnt_T_str.DRT				
target_I2c_Send_I2cRegPr_Cnt_str.DRR         98         98           target_I2c_Send_I2cRegPtr_Cnt_str.DXR         66         66           target_I2c_Send_I2cRegPtr_Cnt_str.DXR         78         78           target_I2c_Send_I2cRegPtr_Cnt_str.MDR         495         495           target_I2c_Send_I2cRegPtr_Cnt_str.DNR         66         66         66           target_I2c_Send_I2cRegPtr_Cnt_str.DNR         0         0         0           target_I2c_Send_I2cRegPtr_Cnt_str.DNR         0         0         0           target_I2c_Send_I2cRegPtr_Cnt_str.DD1         56         56         56           target_I2c_Send_I2cRegPtr_Cnt_str.DD12         78         78         78           target_I2c_Send_I2cRegPtr_Cnt_str.DNAC         0         0         0           target_I2c_Send_I2cRegPtr_Cnt_str.DNAC         0         0         0 <td></td> <td></td> <td></td> <td>V</td>				V
target_l2c_Send_l2cRegPtr_Cnt_Tstr.DXR         78         18				-
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR         78         78           target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR         495         495           target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR         66         66           target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.PDC         78         78           target_l2c_Send_l2cRegPtr_Cnt_T_str.PD11         56         56           target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIT         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIT         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIT         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.OR         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIT         0				~
target_!2c_Send_!2cRegPtr_Cnt_T_str.MDR         495         495           target_!2c_Send_!2cRegPtr_Cnt_T_str.WR         66         66         66           target_!2c_Send_!2cRegPtr_Cnt_T_str.MDR         0         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.PDC         78         78         78           target_!2c_Send_!2cRegPtr_Cnt_T_str.PID12         78         78         78           target_!2c_Send_!2cRegPtr_Cnt_T_str.PID12         78         78         78           target_!2c_Send_!2cRegPtr_Cnt_T_str.PID12         78         78         78           target_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC         0         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DIN         0         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DIN         1         1         1           target_!2c_Send_!2cRegPtr_Cnt_T_str.DOUT         0         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DE         0         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDR         1         1         1           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDR         0         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DAR         6         6         0           target_!2c_SeupMasterT				-
target_12c_Send_12cRegPtr_Cnt_T_str.EMDR         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.EMDR         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.PDC         78         78           target_12c_Send_12cRegPtr_Cnt_T_str.PID11         56         56           target_12c_Send_12cRegPtr_Cnt_T_str.PID12         78         78           target_12c_Send_12cRegPtr_Cnt_T_str.DMAC         0         0           0         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DIN         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DIN         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DUT         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DUT         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DCR         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DCR         1         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DCR         1         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DOR         1         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DOR         1         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DCR         0         0         1           target_12c_Send				<b>~</b>
target_J2c_Send_J2cRegPtr_CntT_str.EMDR         0           target_J2c_Send_J2cRegPtr_CntT_str.PID11         56           target_J2c_Send_J2cRegPtr_CntT_str.PID12         78           target_J2c_Send_J2cRegPtr_CntT_str.DID12         78           target_J2c_Send_J2cRegPtr_CntT_str.DIMAC         0           target_J2c_Send_J2cRegPtr_CntT_str.DIMAC         0           target_J2c_Send_J2cRegPtr_CntT_str.DIN         0           target_J2c_Send_J2cRegPtr_CntT_str.DIN         1           target_J2c_Send_J2cRegPtr_CntT_str.DIN         1           target_J2c_Send_J2cRegPtr_CntT_str.DOUT         0           target_J2c_Send_J2cRegPtr_CntT_str.SET         0           target_J2c_Send_J2cRegPtr_CntT_str.SET         0           target_J2c_Send_J2cRegPtr_CntT_str.CLR         0           target_J2c_Send_J2cRegPtr_CntT_str.DOR         1           target_J2c_Send_J2cRegPtr_CntT_str.DOR         1           target_J2c_Send_J2cRegPtr_Cnt_T_str.DAR         0           target_J2c_SetupMasterTransmit_J2cRegPtr_Cnt_T_str.OAR         66           target_J2c_SetupMasterTransmit_J2cRegPtr_Cnt_T_str.CLK         495           target_J2c_SetupMasterTransmit_J2cRegPtr_Cnt_T_str.CLK         56           target_J2c_SetupMasterTransmit_J2cRegPtr_Cnt_T_str.CLK         56           target_J2c_SetupMasterTransmit_J2cRegPtr_Cnt_T_str.DAR <td></td> <td></td> <td></td> <td>~</td>				~
target_12c_Send_12cRegPtr_Cnt_T_str.PSC         78         78           target_12c_Send_12cRegPtr_Cnt_T_str.PID11         56         56           target_12c_Send_12cRegPtr_Cnt_T_str.PID12         78         78           target_12c_Send_12cRegPtr_Cnt_T_str.PID12         78         78           target_12c_Send_12cRegPtr_Cnt_T_str.PIDNC         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DNA         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DN         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DN         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DOUT         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.SET         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DR         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DR         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DD         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DA         0         0           target_12c_Send_12cRegPtr_Cnt_T_str.DA         6         6           target_12c_Send_bMasterTransmit_12cRegPtr_Cnt_T_str.DA         66         6           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DK         78         78           target_12c_SetupMasterTransmit_12cRegPtr_Cn	· · ·	0	0	<b>✓</b>
target_!2c_Send_!2cRegPtr_Cnt_T_str.PID11         56         56           target_!2c_Send_!2cRegPtr_Cnt_T_str.PID12         78         78           target_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DIN         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DIN         1         1           target_!2c_Send_!2cRegPtr_Cnt_T_str.DUT         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DUT         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.SET         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.CLR         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDR         1         1           target_!2c_Send_!2cRegPtr_Cnt_T_str.DD         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.PSL         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DA         0         0           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.OAR         66         66           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLK         495         495           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLK         495         495           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR         98         98           target	target I2c Send I2cRegPtr Cnt T str.PSC	78	78	~
target_!2c_Send_!2cRegPtr_Cnt_T_str.PID12         78         78           target_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.FUN         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DIN         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DIN         1         1           target_!2c_Send_!2cRegPtr_Cnt_T_str.DOUT         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.SET         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DR         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.ODR         1         1           target_!2c_Send_!2cRegPtr_Cnt_T_str.DD         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.PD         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DAR         66         66           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR         78         78           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLK         495         495           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLK         495         495           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR         98         98           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR         66         66		56	56	<b>✓</b>
target_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DIR         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DIR         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DIN         1         1           target_!2c_Send_!2cRegPtr_Cnt_T_str.DOUT         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DUT         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DLR         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DLR         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDR         1         1           target_!2c_Send_!2cRegPtr_Cnt_T_str.DDR         1         1           target_!2c_Send_!2cRegPtr_Cnt_T_str.DD         0         0           target_!2c_Send_!2cRegPtr_Cnt_T_str.DLT         0         0           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.OAR         66         66           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DLT         495         495           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL         495         495           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DLR         89         98           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR         98         98		78	78	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DUT         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.SET         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DD         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR         0         0           target_l2c_SeupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR         66         66           target_l2c_SeupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR         78         78           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR         78         78           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         495         495           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT         897         897           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         98         98           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         98         98           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR         78         78           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR		0	0	<b>~</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.SET         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.DD         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL         0         0           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR         66         66           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR         78         78           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         495         495           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH         56         56           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT         897         897           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         98         98           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR         78         78           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR         78         78           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR         78         78           target_l2c_SetupMasterTransmit_l2cRegPtr	target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_!2c_Send_!2cRegPtr_Cnt_T_str.DOUT       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.SET       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.CLR       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.DDR       1       1         target_!2c_Send_!2cRegPtr_Cnt_T_str.PD       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.PSL       0       0         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.OAR       66       66         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IMR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL       495       495         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL       495       495         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT       897       897         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       98       98         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       78       78         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       78       78	target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.PD         0         0           target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL         0         0           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR         66         66           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR         78         78           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         495         495           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         495         495           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         56         56           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT         897         897           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         98         98           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR         66         66           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR         78         78           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR         78         78           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR         78         78           targ	target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target   2c Send   2cRegPtr Cnt T str.CLR       0         target   2c Send   2cRegPtr Cnt T str.ODR       1         target   2c Send   2cRegPtr Cnt T str.PD       0         target   2c Send   2cRegPtr Cnt T str.PSL       0         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.OAR       66         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.IMR       78         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.STR       78         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.CLKL       495         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.CLKH       56         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.CNT       897         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.DRR       98         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.DRR       98         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.DAR       66         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.DAR       78         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.DAR       78         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.DAR       78         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.MDR       495         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.NDR       495         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.NDR       66	target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.PD       0         0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL       0         0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR       66         66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL       495         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       897         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       98         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       98         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       495         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       495         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       66	target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD       0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR       78       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR       78       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL       495       495         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH       56       56         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       897       897         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       98       98         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       78       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       78       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       495       495         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       66       66	target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL       0       0         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR       78       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR       78       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL       495       495         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH       56       56         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       897       897         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       98       98         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       78       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       78       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       495       495         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       495       495         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       66       66	target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.OAR       66       66         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.IMR       78       78         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.STR       78       78         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL       495       495         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH       56       56         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT       897       897         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       98       98         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.SAR       66       66         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR       78       78         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MDR       495       495         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MDR       495       495         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MDR       495       495         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.IVR       66       66	target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR       78       78         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR       78       78         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL       495       495         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH       56       56         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT       897       897         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR       98       98         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       78       78         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR       495       495         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR       495       495         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR       66       66	target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR       78       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL       495       495         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH       56       56         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       897       897         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       98       98         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       78       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       495       495         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       66       66	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL       495       495         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH       56       56         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       897       897         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       98       98         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       78       78         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       495       495         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       66       66	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	~
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH       56       56         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT       897       897         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       98       98         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.SAR       66       66         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR       78       78         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MDR       495       495         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.IVR       66       66	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT       897       897         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR       98       98         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       78       78         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR       495       495         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR       66       66	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       98       98         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.SAR       66       66         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR       78       78         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MDR       495       495         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.IVR       66       66	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR 66 66 66	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR7878target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR495495target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR6666	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR 495 495 495 495 495 495 495 495 495 495	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR 66	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	~
	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR			~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR 0				~
	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	~

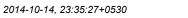
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Name	Actual Value	Expected Value	Result
	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	•	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>
target_SpurSnsrDataPtr_Cnt_T_u16	37896	37896	<b>~</b>

Т			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>~</b>
I2c_Send	1	I2c_Send	1	<b>✓</b>
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	•

Test Step 2.18 (Repeat Count = 1)	
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr Cnt T u08	target_DataTypePtr Cnt T u08
·	66
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt Buffer Cnt M u08[1]	77
	88
DigColPoint_Buffer_Cnt_M_u08[2]	1
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
	64896
DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt CurrentSlave Cnt M u08	17
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_SENDCMD 0
DigColPsInt_InitFailedOnce_Cnt_M_lgc	i -
DigColPsInt_InitialTime_mS_M_u32	22533581
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	221
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	45863
DigColPsInt_TransactionCnt_Cnt_M_u08	191
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	122
k_I2CHWInitTransactionTime_Sec_f32	7.9000001
target_DtrmnElapsedTime_mS_u16_ElapsedTime	4797
target_GetSystemTime_mS_u32_CurrentTime	18522573
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	0





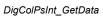
Name	Input Value		
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0		
target I2c SetupMasterTransmit I2cReqPtr Cnt T str.OAR	66		
	78		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR			
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
target_i2cREG1_temp.OAR	66		
target_i2cREG1_temp.IMR	78		
target i2cREG1 temp.STR	78		
target_i2cREG1_temp.CLKL	495		
target_i2cREG1_temp.CLKH	56		
target_i2cREG1_temp.CNT	897		
target i2cREG1 temp.DRR	98		
target i2cREG1 temp.SAR	66		
target i2cREG1 temp.DXR	78		
target i2cREG1 temp.MDR	495		
target_i2cREG1_temp.IVR	66		
target i2cREG1 temp.EMDR	0		
	78		
target_i2cREG1_temp.PSC			
target_i2cREG1_temp.PID11	56		
target_i2cREG1_temp.PID12	78		
target_i2cREG1_temp.DMAC	0		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	0		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	0		
Name			
	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]		Expected Value 36	Result
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	Actual Value	·	
	Actual Value 36	36	~
DigColPsInt_Buffer_Cnt_M_u08[1]	Actual Value 36 77	36 77	<b>*</b>
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	Actual Value 36 77 88	36 77 88	<b>*</b>
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc	Actual Value 36 77 88 0	36 77 88 0	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08	Actual Value 36 77 88 0 122	36 77 88 0 122	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum	Actual Value 36 77 88 0 122 INIT_SENSOR1_READERROR_SETREG	36 77 88 0 122 INIT_SENSOR1_READERROR_SETREG	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData()	Actual Value 36 77 88 0 122 INIT_SENSOR1_READERROR_SETREG 6	36 77 88 0 122 INIT_SENSOR1_READERROR_SETREG 6	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc	Actual Value 36 77 88 0 122 INIT_SENSOR1_READERROR_SETREG 6 0	36 77 88 0 122 INIT_SENSOR1_READERROR_SETREG 6 0	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc	Actual Value 36 77 88 0 122 INIT_SENSOR1_READERROR_SETREG 6 0 0	36 77 88 0 122 INIT_SENSOR1_READERROR_SETREG 6 0	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08	Actual Value 36 77 88 0 122 INIT_SENSOR1_READERROR_SETREG 6 0 0 191	36 77 88 0 122 INIT_SENSOR1_READERROR_SETREG 6 0 0	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc	Actual Value 36 77 88 0 122 INIT_SENSOR1_READERROR_SETREG 6 0 0 191	36 77 88 0 122 INIT_SENSOR1_READERROR_SETREG 6 0 0	· · · · · · · · · · · · · · · · · · ·



Name	Actual Value	Expected Value	Result
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	•
target_ColSnsrDataPtr_Cnt_T_u16	64896	64896	~
target_DataTypePtr_Cnt_T_u08	5	5	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	•
target I2c Send I2cRegPtr Cnt T str.STR	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	Ō	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_SpurSnsrDataPtr_Cnt_T_u16	45863	45863	~

au				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	•
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c_Send	1	l2c_Send	1	•
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	~

Test Step 2.19 (Repeat Count = 1)	
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	40
DigColPsInt_Buffer_Cnt_M_u08[1]	50
DigColPsInt_Buffer_Cnt_M_u08[2]	60





Name	Input Value
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt ColSnsrData Cnt M u16	65325
DigColPsInt_CurrentSlave_Cnt_M_u08	24
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR1 SENDCMD
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	23536333
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	239
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt SensInitialized Cnt M Igc	1
DigColPsInt SpurSnsrData Cnt M u16	55797
	205
DigColPsInt_TransactionCnt_Cnt_M_u08	
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target SpurSnsrDataPtr Cnt T u16
i2cREG1_temp	target_i2cREG1_temp
k ColSensori2CAddress Cnt u08	1
k_I2CHWInitTransactionTime_Sec_f32	8.30000019
target_DtrmnElapsedTime_mS_u16_ElapsedTime	5304
target_GetSystemTime_mS_u32_CurrentTime	19525325
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	129
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
	4466
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	2
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3

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DigColPsInt\_GetData Input Value target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL 567 target i2cREG1 temp.OAR target i2cREG1 temp.IMR 44 target\_i2cREG1\_temp.STR 4444 target\_i2cREG1\_temp.CLKL 566 target\_i2cREG1\_temp.CLKH 4466 target i2cREG1 temp.CNT 129 target\_i2cREG1\_temp.DRR 6 target\_i2cREG1\_temp.SAR 567 target i2cREG1 temp.DXR 44 target\_i2cREG1\_temp.MDR 566 554 target i2cREG1 temp.IVR target\_i2cREG1\_temp.EMDR 44 target\_i2cREG1\_temp.PSC target\_i2cREG1\_temp.PID11 4466 44 target i2cREG1 temp.PID12 target\_i2cREG1\_temp.DMAC target\_i2cREG1\_temp.FUN 1 target\_i2cREG1\_temp.DIR 2 target\_i2cREG1\_temp.DIN 0 target\_i2cREG1\_temp.DOUT target\_i2cREG1\_temp.SET 1 target\_i2cREG1\_temp.CLR 2 target\_i2cREG1\_temp.ODR 0 target\_i2cREG1\_temp.PD 3 target\_i2cREG1\_temp.PSL 3 **Actual Value Expected Value** Result Name DigColPsInt Buffer Cnt M u08[0] 40 40 DigColPsInt\_Buffer\_Cnt\_M\_u08[1] 50 50 DigColPsInt Buffer Cnt M u08[2] 60 60  ${\sf DigColPsInt\_BusBusySeqError\_Cnt\_M\_lgc}$ 0 0 DigColPsInt CurrentSlave Cnt M u08 24 24 INIT\_SENSOR1\_SENDCMD DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum INIT\_SENSOR1\_SENDCMD DigColPsInt GetData() 40 40 DigColPsInt\_InitFailedOnce\_Cnt\_M\_Igc 1 1 DigColPsInt\_NackOccured\_Cnt\_M\_lgc 0 0  $DigColPsInt\_PrevTransactionCnt\_Cnt\_M\_u08$ 205 205 0  ${\tt DigColPsInt\_RecvOverrunError\_Cnt\_M\_Igc}$ 0 DigColPsInt\_SensInitialized\_Cnt\_M\_lgc 1 target\_ColSnsrDataPtr\_Cnt\_T\_u16 65325 65325 target\_DataTypePtr\_Cnt\_T\_u08 3 3 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.OAR 567 567 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IMR 44 44 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.STR 4444 4444 **~** 566 566 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKL  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKH$ 4466 4466 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CNT 129 129 V  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DRR$ 6 6 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SAR 567 567 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DXR 44 44 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.MDR 566 566 target I2c Send I2cRegPtr Cnt T str.IVR 554 554 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.EMDR 1 target I2c Send I2cRegPtr Cnt T str.PSC 44 44 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID11 4466 4466 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID12 44 44 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DMAC 1 1 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.FUN 1 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIR 2 2 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIN 0 0 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DOUT 1 1 **~** target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SET 2 2 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.ODR 0 0 3 3 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PD target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSL 3 3 567 567  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.OAR$ 

44

4444

566

4466

129

6

44

4444

566

4466

129

6

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IMR

target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR

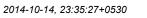
target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKL

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKH

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CNT

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DRR$ 

~





Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_SpurSnsrDataPtr_Cnt_T_u16	55797	55797	~

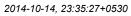
T				V
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	70
DigColPsInt_Buffer_Cnt_M_u08[1]	80
DigColPsInt_Buffer_Cnt_M_u08[2]	90
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	5600
DigColPsInt_CurrentSlave_Cnt_M_u08	31
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	24539085
DigColPsInt NackOccured Cnt M Igc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	19
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt SpurSnsrData Cnt M u16	9687
DigColPsInt TransactionCnt Cnt M u08	12
DtrmnElapsedTime mS u16(ElapsedTime)	target DtrmnElapsedTime mS u16 ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target GetSystemTime mS u32 CurrentTime
I2c Send(I2cRegPtr Cnt T str)	target I2c Send I2cRegPtr Cnt T str
l2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr Cnt T u16	target SpurSnsrDataPtr Cnt T u16
2cREG1 temp	target i2cREG1 temp
k ColSensorl2CAddress Cnt u08	115
k_I2CHWInitTransactionTime_Sec_f32	8.69999981
target_DtrmnElapsedTime_mS_u16_ElapsedTime	5811
target GetSystemTime mS u32 CurrentTime	20528077
target I2c Send I2cRegPtr Cnt T str.OAR	65
target I2c Send I2cRegPtr Cnt T str.IMR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
target I2c Send I2cRegPtr Cnt T str.CLKH	577
target I2c Send I2cRegPtr Cnt T str.CNT	88
target I2c Send I2cRegPtr Cnt T str.DRR	23
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
arget I2c Send I2cRegPtr Cnt T str.MDR	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89
target I2c Send I2cRegPtr Cnt T str.PID11	577
target I2c Send I2cRegPtr Cnt T str.PID12	89

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target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN target_l2c_Send_l2cRegPtr_Cnt_T_str.DUT target_l2c_Send_l2cRegPtr_Cnt_T_str.SET target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR target_l2c_Send_l2cRegPtr_Cnt_T_str.PD target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	Input Value 2 0 1 2		
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT target_l2c_Send_l2cRegPtr_Cnt_T_str.SET target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR	0 0 1 2		
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT target_l2c_Send_l2cRegPtr_Cnt_T_str.SET target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR target_l2c_Send_l2cRegPtr_Cnt_T_str.DDR	0 1 2		
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT target_l2c_Send_l2cRegPtr_Cnt_T_str.SET target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	1 2		
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT target_l2c_Send_l2cRegPtr_Cnt_T_str.SET target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	2		
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT target_l2c_Send_l2cRegPtr_Cnt_T_str.SET target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR target_l2c_Send_l2cRegPtr_Cnt_T_str.PD			
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR target_l2c_Send_l2cRegPtr_Cnt_T_str.PD			
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2		
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1		
	2		
0 0	0		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	65		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	577		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	88		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	89		
	577		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	2		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	2		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
target_i2cREG1_temp.OAR	65		
target_i2cREG1_temp.IMR	89		
target_i2cREG1_temp.STR	67		
target_i2cREG1_temp.CLKL	7		
target_i2cREG1_temp.CLKH	577		
target_i2cREG1_temp.CNT	88		
target_i2cREG1_temp.DRR	23		
target_i2cREG1_temp.SAR	65		
target_i2cREG1_temp.DXR	89		
target_i2cREG1_temp.MDR	7		
target_i2cREG1_temp.IVR	44		
target_i2cREG1_temp.EMDR	2		
target_i2cREG1_temp.PSC	89		
target_i2cREG1_temp.PID11	577		
target_i2cREG1_temp.PID12	89		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.CLR	0		
target i2cREG1 temp.ODR	1		
target_i2cREG1_temp.PD	2		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	Result
	80	80	~
DigColPsInt_Buffer_Cnt_M_u08[1]	90	90	
DigColPoint_Buffer_Cnt_M_u08[2]	90	0	<b>V</b>
DigColPsInt_BusBusySeqError_Cnt_M_lgc			
DigColPsInt_CurrentSlave_Cnt_M_u08	115	115	<b>V</b>
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	~
DigColPsInt_GetData()	0	0	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	12	12	~
DisColDolat DoorOremanError Oct M. In-	0	0	~
DigColPsInt_RecvOverrunError_Cnt_M_Igc DigColPsInt_SensInitialized_Cnt_M_Igc	1	1	<b>✓</b>





Name	Actual Value	Expected Value	Result
I2c_Send(Length_Cnt_T_u32)	1	1	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	<b>✓</b>
target_ColSnsrDataPtr_Cnt_T_u16	5600	5600	~
target_DataTypePtr_Cnt_T_u08	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	89	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target I2c Send I2cRegPtr Cnt T str.CNT	88	88	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	-
target I2c Send I2cRegPtr Cnt T str.DMAC	2	2	~
target I2c Send I2cRegPtr Cnt T str.FUN	0	0	
	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN		2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2		
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2 0	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR		0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	0	0	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_SpurSnsrDataPtr_Cnt_T_u16	9687	9687	~

T ·				V
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	•
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	•
CatSystemTime mS u32	1	CatSystemTime mS u32	1	

Test Step 2.21 (Repeat Count = 1)	<b>→</b>
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	3
DigColPsInt_Buffer_Cnt_M_u08[1]	6





Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	7985
DigColPsInt_CurrentSlave_Cnt_M_u08	38
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	25541837
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	31
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	11230
DigColPsInt_TransactionCnt_Cnt_M_u08	29
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	122
k_I2CHWInitTransactionTime_Sec_f32	9.10000038
target_DtrmnElapsedTime_mS_u16_ElapsedTime	6318
target_GetSystemTime_mS_u32_CurrentTime	21530829
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1

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Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1		
target_i2cREG1_temp.OAR	10		
target_i2cREG1_temp.IMR	10 1223		
target_i2cREG1_temp.STR target_i2cREG1_temp.CLKL	7846		
target i2cREG1 temp.CLKH	8974		
target_i2cREG1_temp.CNT	98		
target_i2cREG1_temp.DRR	12		
target_i2cREG1_temp.SAR	10		
target_i2cREG1_temp.DXR	10		
target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR	7846 55		
target_i2cREG1_temp.EMDR	1		
target i2cREG1 temp.PSC	10		
target_i2cREG1_temp.PID11	8974		
target_i2cREG1_temp.PID12	10		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	1	_	
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	3 6	3	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[2]	9	9	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	•
DigColPsInt_CurrentSlave_Cnt_M_u08	38	38	•
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_READ	INIT_SENSOR1_READEXTERR_READ	•
DigColPsInt_GetData()	46	46	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1	1	~
DigColPsInt_NackOccured_Cnt_M_lgc	0 29	29	<b>✓</b>
DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	
DigColPsInt SensInitialized Cnt M Igc	1	1	•
target_ColSnsrDataPtr_Cnt_T_u16	7985	7985	•
target_DataTypePtr_Cnt_T_u08	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	10	· ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	1223 7846	1223 7846	<b>*</b>
target I2c Send I2cRegPtr Cnt T str.CLKH	8974	8974	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98	98	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846 55	7846 55	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10	10	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974	8974	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10	10	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>•</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	1	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10	10	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	1223 7846	1223 7846	Ž
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	8974	8974	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98	98	-
	'		-

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSL$ 

target\_SpurSnsrDataPtr\_Cnt\_T\_u16

DigColPsInt\_GetData

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**Actual Value Expected Value**  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DRR$ 12 12  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SAR$ 10 10  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DXR$ 10 10  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.MDR$ 7846 7846 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IVR 55 55  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.EMDR$ 10 10 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSC 8974  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID11$ 8974 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID12 10 10  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DMAC$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.FUN 1  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIR$ 2 2 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIN 1 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DOUT 1 1 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SET target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLR 2 2  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.ODR$ 1 1 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PD 1

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

11230

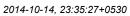
11230

Name	Input Value
ColSnsrDataPtr Cnt T u16	target ColSnsrDataPtr Cnt T u16
DataTypePtr Cnt T u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt Buffer Cnt M u08[0]	11
DigColPsInt_Buffer_Cnt_M_u08[1]	22
DigColPsInt Buffer Cnt M u08[2]	33
DigColPsInt BusBusySeqError Cnt M lgc	0
DigColPsInt CmdFailOccurred Cnt M lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	10370
DigColPsInt CurrentSlave Cnt M u08	45
DigColPsInt CurrentStepNo Cnt M enum	INIT NOT INITIALIZED
DigColPsInt InitFailedOnce Cnt M Igc	0
DigColPsInt InitialTime mS M u32	26544589
DigColPsInt NackOccured Cnt M lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	43
DigColPsInt RecvOverrunError Cnt M Igc	0
DigColPsInt RecvdDataType Cnt M u08	2
DigColPsInt SensInitialized Cnt M Igc	1
DigColPsInt SpurSnsrData Cnt M u16	12773
DigColPsInt_TransactionCnt_Cnt_M_u08	33
DtrmnElapsedTime mS u16(ElapsedTime)	target DtrmnElapsedTime mS u16 ElapsedTime
GetSystemTime mS u32(CurrentTime)	target GetSystemTime mS u32 CurrentTime
2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
2c SetupMasterTransmit(I2cRegPtr Cnt T str)	target I2c SetupMasterTransmit I2cRegPtr Cnt T str
SpurSnsrDataPtr Cnt T u16	target SpurSnsrDataPtr Cnt T u16
2cREG1 temp	target i2cREG1 temp
ColSensorI2CAddress Cnt u08	1
	9.5
<_I2CHWInitTransactionTime_Sec_f32	9.5 6825
arget_DtrmnElapsedTime_mS_u16_ElapsedTime	11.1
target_GetSystemTime_mS_u32_CurrentTime	22533581
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987

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Name	Input Value		
	24		
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12			
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2		
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2		
target I2c Send I2cRegPtr Cnt T str.SET	2		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3		
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	2		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	24		
	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2		
target_i2cREG1_temp.OAR	34		
	24		
target_i2cREG1_temp.IMR			
target_i2cREG1_temp.STR	455		
target_i2cREG1_temp.CLKL	847		
target_i2cREG1_temp.CLKH	987		
target_i2cREG1_temp.CNT	487		
target i2cREG1 temp.DRR	34		
target i2cREG1 temp.SAR	34		
target_i2cREG1_temp.DXR	24		
target_i2cREG1_temp.MDR	847		
target_i2cREG1_temp.IVR	56		
target_i2cREG1_temp.EMDR			
target i2cREG1 temp.PSC	2		
CONTROL CONTROL CO	2 24		
· ·	24		
target_i2cREG1_temp.PID11	24 987		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12	24 987 24		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC	24 987 24 2		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12	24 987 24		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC	24 987 24 2		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR	24 987 24 2 0 3		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN	24 987 24 2 0 3 3		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT	24 987 24 2 0 3 3 2		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET	24 987 24 2 0 3 3 2 2		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT	24 987 24 2 0 3 3 2 2 2 3		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET	24 987 24 2 0 3 3 2 2		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR	24 987 24 2 0 3 3 2 2 2 3		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.DDR	24 987 24 2 0 3 3 2 2 2 3 3		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL	24 987 24 2 0 3 3 2 2 2 3 3 2	Expected Value	Bassili
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL Name	24 987 24 2 0 3 3 2 2 2 3 3 2 2 2 Actual Value	Expected Value	Result
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DIN target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL Name DigColPsInt_Buffer_Cnt_M_u08[0]	24 987 24 2 0 3 3 2 2 2 3 3 2 2 2 Actual Value	11	~
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL Name	24 987 24 2 0 3 3 2 2 2 3 3 3 2 2 2 Actual Value 11 22	11 22	~
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL Name DigCoIPsInt_Buffer_Cnt_M_u08[0]	24 987 24 2 0 3 3 2 2 2 3 3 2 2 2 Actual Value	11	*
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigCoIPsInt_Buffer_Cnt_M_u08[0] DigCoIPsInt_Buffer_Cnt_M_u08[1] DigCoIPsInt_Buffer_Cnt_M_u08[2]	24 987 24 2 0 3 3 2 2 2 3 3 3 2 2 2 Actual Value 11 22	11 22	· · ·
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DIN target_i2cREG1_temp.DIN target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_BusBusySeqError_Cnt_M_lgc	24 987 24 2 0 3 3 2 2 2 3 3 3 2 2 2 Actual Value 11 22 33 0	11 22 33 0	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DIN target_i2cREG1_temp.DIN target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08	24 987 24 2 0 3 3 2 2 2 3 3 3 2 2 2 Actual Value 11 22 33 0 45	11 22 33 0 45	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DIN target_i2cREG1_temp.DIN target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum	24 987 24 2 0 3 3 2 2 2 3 3 3 2 2 Actual Value 11 22 33 0 45 INIT_NOT_INITIALIZED	11 22 33 0 45 INIT_NOT_INITIALIZED	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.CLR target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusbusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData()	24 987 24 2 0 3 3 2 2 2 2 3 3 3 2 2 Actual Value 11 22 33 0 45 INIT_NOT_INITIALIZED 0	11 22 33 0 45 INIT_NOT_INITIALIZED 0	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DMAC target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum	24 987 24 2 0 3 3 2 2 2 3 3 3 2 2 Actual Value 11 22 33 0 45 INIT_NOT_INITIALIZED	11 22 33 0 45 INIT_NOT_INITIALIZED	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData()	24 987 24 2 0 3 3 2 2 2 2 3 3 3 2 2 Actual Value 11 22 33 0 45 INIT_NOT_INITIALIZED 0	11 22 33 0 45 INIT_NOT_INITIALIZED 0	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.PID11  target_i2cREG1_temp.PID12  target_i2cREG1_temp.DMAC  target_i2cREG1_temp.FUN  target_i2cREG1_temp.DIR  target_i2cREG1_temp.DIN  target_i2cREG1_temp.DOUT  target_i2cREG1_temp.SET  target_i2cREG1_temp.CDR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.PD  target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_BusbusySeqError_Cnt_M_lgc  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_GetData()  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc	24 987 24 2 0 3 3 2 2 2 3 3 3 2 2 Actual Value 11 22 33 0 45 INIT_NOT_INITIALIZED 0 0	11 22 33 0 45 INIT_NOT_INITIALIZED 0	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.DOUT target_i2cREG1_temp.CLR target_i2cREG1_temp.CDR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL Name DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_GetData()	24 987 24 2 0 3 3 3 2 2 2 2  Actual Value 11 22 33 0 45 INIT_NOT_INITIALIZED 0 0 0	11 22 33 0 45 INIT_NOT_INITIALIZED 0 0	· · · · · · · · · · · · · · · · · · ·





Name	Actual Value	Expected Value	Result
DigColPsInt_SensInitialized_Cnt_M_Igc	1	1	~
target_ColSnsrDataPtr_Cnt_T_u16	10370	10370	~
target_DataTypePtr_Cnt_T_u08	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34	34	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24	24	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455	455	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847	847	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987	987	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487	487	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34	34	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34	34	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24	24	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847	847	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56	56	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24	24	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987	987	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24	24	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	•
target I2c Send I2cRegPtr Cnt T str.DIN	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>~</b>
target I2c Send I2cRegPtr Cnt T str.SET	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	~
target I2c Send I2cRegPtr Cnt T str.PSL	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34	34	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24	24	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455	455	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847	847	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987	987	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487	487	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34	34	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34	34	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24	24	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847	847	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56	56	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24	24	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987	987	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24	24	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	3	3	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	2	2	
target_SpurSnsrDataPtr_Cnt_T_u16	12773	12773	
target_opuronsiDataFtt_Offt_1_u10	12113	12113	

T					<b>✓</b>
Actual Function	Count	Expected Function	Count	Resu	ılt
DtrmnFlansedTime mS u16	1	DtrmnFlancedTime mS u16	1		~

Test Step 2.23 (Repeat Count = 1)		✓
Name	Input Value	
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16	
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08	
DigColPsInt_Buffer_Cnt_M_u08[0]	44	
DigColPsInt_Buffer_Cnt_M_u08[1]	55	
DigColPsInt_Buffer_Cnt_M_u08[2]	66	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	
DigColPsInt_ColSnsrData_Cnt_M_u16	12755	
DigColPsInt_CurrentSlave_Cnt_M_u08	52	





Nama	Innut Value
Name	Input Value
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	27547341
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	55
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	14316
DigColPsInt_TransactionCnt_Cnt_M_u08	46
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	14
k_I2CHWInitTransactionTime_Sec_f32	9.89999962
target_DtrmnElapsedTime_mS_u16_ElapsedTime	7332
target_GetSystemTime_mS_u32_CurrentTime	23536333
target I2c Send I2cRegPtr Cnt T str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_12c_Send_12cRegPtr_Cnt_T_str.CLKL	2309
target I2c Send I2cRegPtr Cnt T str.CLKH	1204
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	87
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	67
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	55
	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	2309
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	1204
target I2c SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLRH target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	87
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	67
target I2c SetupMasterTransmit_I2cRegPtr_Cnt_I_str.DRR target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	55
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
	000

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——————————————————————————————————————		•	
Name	Input Value		
target_i2cREG1_temp.CLKL	2309		
target_i2cREG1_temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55 66		
target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1 2		
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	Kesuit
DigColPsInt Buffer Cnt M u08[1]	55	55	~
DigColPsInt_Buffer_Cnt_M_u08[2]	66	66	_
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	•
DigColPsInt_CurrentSlave_Cnt_M_u08	14	14	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	•
DigColPsInt_GetData()	38	38	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	46	46	~
DigColPsInt_RecvOverrunError_Cnt_M_Igc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	~
I2c_Send(Length_Cnt_T_u32)	1	1	<b>V</b>
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	<b>V</b>
target_ColSnsrDataPtr_Cnt_T_u16 target_DataTypePtr_Cnt_T_u08	12755	12755	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	_
target I2c Send I2cRegPtr Cnt T str.CLKL	2309	2309	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	66	66 1204	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_I_str.PID11 target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	1204 66	1204 66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target I2c Send I2cRegPtr Cnt T str.FUN	1	1	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	3	3	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>*</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	87 67	87 67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_1_str.DRR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
		1	

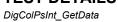
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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_SpurSnsrDataPtr_Cnt_T_u16	14316	14316	~

T	T Control of the Cont		~	
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>~</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c_Send	1	I2c_Send	1	<b>~</b>
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	~

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	20000
DigColPsInt_CurrentSlave_Cnt_M_u08	59
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_READ
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1
DigColPsInt_InitialTime_mS_M_u32	28550093
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	131
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	28203
DigColPsInt_TransactionCnt_Cnt_M_u08	121
OtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
2cREG1_temp	target_i2cREG1_temp
_ColSensorl2CAddress_Cnt_u08	21
_I2CHWInitTransactionTime_Sec_f32	1.20000005
arget_DtrmnElapsedTime_mS_u16_ElapsedTime	7839
arget_GetSystemTime_mS_u32_CurrentTime	24539085
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
arget_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78





Manual Color   Manu	Nama	Innut Value		
Simple Line Simple Configuration Configura	Name	Input Value		
target (D. Send Edelegie') OCT 1 at DIMO target (D. Send Edelegie') OCT 1 at D				
Design   D				
sage De Send Exchange (Co. 17 at 50 DR) to rough DE, Send Exchange				
September   Sept				
taged 10.5 Send Defenging Out 1 at 5017				
Banger   100, Sept.   Declaration   Common   Common   Common   Declaration   Declara				
Langel LDC Send Distription Con   1 miles   1				
Image   Dec   Send   Calleging Cont				
Image   12.5. Seed   12.5. Se				
Image   17.00   Section   17				
Image: Light   Company   Control				
Bage   19.00   Balle				
Bage  12.5 Selpublisher Transmit (ZeRegiPt Out 7 st 07 to 17 to 17 to 19 to				
Base  R.D. SebupAsserTransmit (24RepTr CnT T st CLK).   495				
tagsqt, D.S. Settlandfort Transmit, J.C.RegiPt, O.T., Tay, KO.K.H  signey, E.O. Settlandfort Transmit, J.C.RegiPt, O.T., Tay, D.D.R				
Biology L.D.S. Schup/Macin Transmill L.P.Reg/Pt Col.T. yab CNT   987				
Integral   2.5. ships/Master Transmill (28766)PP. CmT   247.08 NR   98   18764   2.5. ships/Master Transmill (28766)PP. CmT   247.08 NR   98   18764   2.5. ships/Master Transmill (28766)PP. CmT   247.00 NR   98   18764   2.5. ships/Master Transmill (28766)PP. CmT   247.00 NR   98   18764   2.5. ships/Master Transmill (28766)PP. CmT   247.00 NR   98   18764   2.5. ships/Master Transmill (28766)PP. CmT   247.00 NR   98   18764   2.5. ships/Master Transmill (28766)PP. CmT   247.00 NR   98   18764   2.5. ships/Master Transmill (28766)PP. CmT   247.00 NR   98   18764   2.5. ships/Master Transmill (28766)PP. CmT   247.00 NR   98   18764   2.5. ships/Master Transmill (28766)PP. CmT   247.00 NR   98   18764   2.5. ships/Master Transmill (28766)PP. CmT   247.00 NR   247.00 NR   247.00 NR   247.00 NR   247.0				
Sept   1969				
target, 12.9. SetupMasetTrannin_L20HegPt* Cnt_T at nXMR	· ·			
Image   12. Setup-Mased Transmit, 228-reg Pr. Cnt. T. air MDR   495	· · - · · - · - · - · - · · - · · - ·			
taged_12_SebupMasterTransmu_1226epPP_Cont_1_str.PMR				
Langer   Life   Setup Masser Frammure   Life   Langer   Lang				
taged_L2_SebupMaseFramami_L2cRegPP_CnTstr_PSC				
Image   22. Sebup Master Transmil, 22Reg Pr. Cort_T_str D1011   56				
target_L2s_SetupMasterTransmit_R2rRepPr_CnT_str_PD12  ranget_L2s_SetupMasterTransmit_R2rRepPr_CnT_str_PUN  target_L2s_SetupMasterTransmit_R2rRepPr_CnT_str_PUN  target_L2s_RepUN  target_L2s_				
target_L2c_SebupMasterTransmit_L2cRegPtr_CnLT_str_PUN 0 0 1				
target_L2c_SebupMasterTransmit_L2cRegPr_CnLT_str.DIR 0   larget_L2c_SebupMasterTransmit_L2cRegPr_CnLT_str.DIR 1   larget_L2c_SebupMasterTransmit_L2cRegPr_CnLT_str.DIR 1   larget_L2c_SebupMasterTransmit_L2cRegPr_CnLT_str.DIR 1   larget_L2c_SebupMasterTransmit_L2cRegPr_CnLT_str.DIR 0   larget_L2c_SebupMasterTransmit_L2c_SebupMasterTransmit_L2c_SebupMasterTransmit_L2c_SebupMasterTransmit_L2c_SebupMasterTransmit_L2c_SebupMasterTransmit_L2c_SebupMasterTransmit_L2c_SebupMasterTransmit_L2c_SebupMasterTransmit_L2c_SebupMasterTransmit_L2c_SebupMasterTransmit_L2c_Sebu				
Integral_Lipe_SetupMeaterTransmit_LipeRepPr_Cnit_str.DIN   1   1   1   1   1   1   1   1   1				
target_IZe_SetupMasterTransmit_IZeRegPtr_Cnt_T_str.DNT				
Ising Ling   Ling   Ling   Seluph Master Transmit   LicRegPtr_Cnit_ str.DUT   0   0   1   1   1   1   1   1   1   1				
large_L2s_SetupMasterTransmit_!2cReapPr_Colt_T_str.SET         0           large_L2s_SetupMasterTransmit_!2cReapPr_Colt_T_str.DOR         1           large_L2s_SetupMasterTransmit_!2cReapPr_Colt_T_str.DOR         1           large_L2s_SetupMasterTransmit_!2cReapPr_Colt_T_str.DOR         0           large_L2s_SetupMasterTransmit_!2cReapPr_Colt_T_str.DEL         0           large_L2cREG_Lenn_DAR         66           large_L2cREG_Lenn_DAR         78           large_L2cREG_Lenn_DAR         78           large_L2cREG_Lenn_DCLKI         495           large_L2cREG_Lenn_DCLKI         56           large_L2cREG_Lenn_DCLKI         56           large_L2cREG_Lenn_DAR         66           large_L2cREG_Lenn_DAR         66           large_L2cREG_Lenn_DAR         66           large_L2cREG_Lenn_DAR         66           large_L2cREG_Lenn_DAR         66           large_L2cREG_Lenn_DAR         78           large_L2cREG_Lenn_DAR         78           large_L2cREG_Lenn_DAR         78           large_L2cREG_Lenn_DAR         78           large_L2cREG_Lenn_DAR         78           large_L2cREG_Lenn_DAR         0           large_L2cREG_Lenn_DAR         0           large_L2cREG_Lenn_DAR         0 <tr< td=""><td></td><td></td><td></td><td></td></tr<>				
Integral_I2e_SetupMasterTransmit_I2eRegPtr_Cnt_T_str.DR				
target_Daz_SetupMasterTransmit_!2cRegPr_Cnt_Tstr.DD         0           target_Ez_SetupMasterTransmit_!2cRegPr_Cnt_Tstr.PD         0           target_Ez_SetupMasterTransmit_!2cRegPr_Cnt_Tstr.PSL         0           target_EzREGT_temp_CAR         66           target_EzREGT_temp_CLKL         495           target_EzREGT_temp_CLKL         495           target_EzREGT_temp_CLKL         897           target_EzREGT_temp_CNT         897           target_EzREGT_temp_DNR         98           target_EzREGT_temp_DNR         66           target_EzREGT_temp_DNR         495           target_EzREGT_temp_DNR         495           target_EzREGT_temp_DNR         495           target_EzREGT_temp_DNDR         66           target_EzREGT_temp_ENDR         78           target_EzREGT_temp_ENDR         78           target_EzREGT_temp_ENDR         0           target_EzREGT_temp_ENDR				
Barget   2e. SetupMasterTransmit   2eRegPtr_Cntstr.PD				
largeL 2c_SetupMasterTransmit_l2cRegPtr_Cnt_Tstr.PSL   0				
Integred   Care   Car				
target_j2cREG1_temp.IMR				
Isrget_ ZeREG1_temp.STR   485				
target_J2cREG1_temp_CLKL target_J2cREG1_temp_CLKH target_J2cREG1_temp_DRR target_J2cREG1_temp_DRR 498 target_J2cREG1_temp_DRR 498 target_J2cREG1_temp_DRR 495 target_J2cREG1_temp_DRR 495 target_J2cREG1_temp_DRR 495 target_J2cREG1_temp_DRR 495 target_J2cREG1_temp_DRR 66 target_J2cREG1_temp_DRR 678 target_J2cREG1_temp_DRR 686 target_J2cREG1_temp_DRR 788 target_J2cREG1_temp_DRR 788 target_J2cREG1_temp_DRC 788 target_J2cREG				
target_12cREG1_temp.CNT				
target_!ZcREG1_temp.DRT 98 target_!ZcREG1_temp.DRR 98 target_!ZcREG1_temp.DXR 66 target_!ZcREG1_temp.DXR 495 target_!ZcREG1_temp.DXR 495 target_!ZcREG1_temp.DMDR 495 target_!ZcREG1_temp.DMDR 66 target_!ZcREG1_temp.EMDR 0 target_!ZcREG1_temp.EMDR 10 target_!ZcREG1_temp.PMDR 10 target_!ZcREG1_temp.PMDR 10 target_!ZcREG1_temp.PMDR 10 target_!ZcREG1_temp.PDI11 10 target_!ZcREG1_temp.DMAC 10 target_!ZcREG1_temp.DMAC 10 target_!ZcREG1_temp.DIN 10 target_!ZcREG1_temp.DIR 10 target_!				
target_ 2cREG1_temp_DRR				
target_ 2cREG1_temp_DXR				
target_i2cREG1_temp_DXR				
target_l2cREG1_temp.MDR         495           target_l2cREG1_temp.IVR         66           target_l2cREG1_temp.EMDR         0           target_l2cREG1_temp.PSC         78           target_l2cREG1_temp.PID11         56           target_l2cREG1_temp.PID12         78           target_l2cREG1_temp.PID1AC         0           target_l2cREG1_temp.DIN         0           target_l2cREG1_temp.DIN         1           target_l2cREG1_temp.DIN         1           target_l2cREG1_temp.DOT         0           target_l2cREG1_temp.DOT         0           target_l2cREG1_temp.DCR         0           target_l2cREG1_temp.DCR         0           target_l2cREG1_temp.DR         1           target_l2cREG1_temp.PD         0           target_l2cREG1_temp.PDR         0           target_l2cREG1_temp.PSL         0           Name         Actual Value         Expected Value         Result           DigColPsint_Buffer_Cnt_M_u08[0]         10         10         V           DigColPsint_Buffer_Cnt_M_u08[1]         20         20         V           DigColPsint_Buffer_Cnt_M_u08[2]         30         30         V           DigColPsint_CurrentSlave_Cnt_M_u08         59         59				
target_i2cREG1_temp_EMDR         0           target_i2cREG1_temp_EMDR         78           target_i2cREG1_temp_PID11         56           target_i2cREG1_temp_PID12         78           target_i2cREG1_temp_DMAC         0           target_i2cREG1_temp_DINR         0           target_i2cREG1_temp_DIR         0           target_i2cREG1_temp_DIN         1           target_i2cREG1_temp_DOUT         0           target_i2cREG1_temp_				
target_l2cREG1_temp.EMDR         0           target_l2cREG1_temp.PSC         78           target_l2cREG1_temp.PID11         56           target_l2cREG1_temp.DID12         78           target_l2cREG1_temp.DMAC         0           target_l2cREG1_temp.DIN         0           target_l2cREG1_temp.DIN         1           target_l2cREG1_temp.DOUT         0           target_l2cREG1_temp.DCLR         0           target_l2cREG1_temp.DDR         1           target_l2cREG1_temp.DDR         1           target_l2cREG1_temp.DDR         0           target_l2cREG1_temp.DDR         1           target_l2cREG1_temp.DDR         1           target_l2cREG1_temp.DD         0           target_l2cREG1_temp.DD         0           target_l2cREG1_temp.DD         1           target_l2cREG1_temp.DDR         1           target_l2cREG1_temp.DDR         1           target_l2cREG1_temp.DD         0				
target_izcREG1_temp.PID11         56           target_izcREG1_temp.PID12         78           target_izcREG1_temp.PID12         78           target_izcREG1_temp.DIMAC         0           target_izcREG1_temp.FUN         0           target_izcREG1_temp.DIR         1           target_izcREG1_temp.DOUT         0           target_izcREG1_temp.DOUT         0           target_izcREG1_temp.CLR         0           target_izcREG1_temp.DOR         1           target_izcREG1_temp.DOR         1           target_izcREG1_temp.PD         0           target_izcREG1_temp.PSL         0           Name         Actual Value         Expected Value         Result           DigColPsInt_Buffer_Cnt_M_u08[0]         10         10         V           DigColPsInt_Buffer_Cnt_M_u08[1]         20         20         V           DigColPsInt_Busfler_Cnt_M_u08[2]         30         30         V           DigColPsInt_Busfley_SeqError_Cnt_M_u08         59         59         V           DigColPsInt_CurrentStepNo_Cnt_M_u08         59         59         V           DigColPsInt_LiftFailedOne_Cnt_M_enum         INIT_SENSOR2_CHECKSTAT_READ         INIT_SENSOR2_CHECKSTAT_READ         V           DigColPsInt_InitFailedOne_Cn				
target_i2cREG1_temp.PID11         56           target_i2cREG1_temp.PID12         78           target_i2cREG1_temp.DMAC         0           target_i2cREG1_temp.FUN         0           target_i2cREG1_temp.DIR         0           target_i2cREG1_temp.DIN         1           target_i2cREG1_temp.DOUT         0           target_i2cREG1_temp.ECR         0           target_i2cREG1_temp.DDR         1           target_i2cREG1_temp.DDR         1           target_i2cREG1_temp.PD         0           target_i2cREG1_temp.PSL         0           Name         Actual Value         Expected Value         Result           DigColPsInt_Buffer_Cnt_M_u08[0]         10         10         ✓           DigColPsInt_Buffer_Cnt_M_u08[2]         30         30         ✓           DigColPsInt_BusbusySeqError_Cnt_M_u08[2]         30         30         ✓           DigColPsInt_CurrentSlave_Cnt_M_u08         59         ✓           DigColPsInt_GetData()         136         JINT_SENSOR2_CHECKSTAT_READ         VINT_SENSOR2_CHECKSTAT_READ           DigColPsInt_InitFailedOnce_Cnt_M_log         1         1         ✓           DigColPsInt_InitFailedOnce_Cnt_M_log         0         0         ✓           DigColPsInt_				
target_i2cREG1_temp.PID12         78           target_i2cREG1_temp.DMAC         0           target_i2cREG1_temp.DIN         0           target_i2cREG1_temp.DIN         1           target_i2cREG1_temp.DOUT         0           target_i2cREG1_temp.DET         0           target_i2cREG1_temp.DET         0           target_i2cREG1_temp.DDR         1           target_i2cREG1_temp.DDR         1           target_i2cREG1_temp.PD         0           target_i2cREG1_temp.PD         0           target_i2cREG1_temp.PSL         0           Name         Actual Value         Expected Value         Result           DigColPsInt_Buffer_Cnt_M_u08[0]         10         10         ✓           DigColPsInt_Buffer_Cnt_M_u08[1]         20         20         ✓           DigColPsInt_Buffer_Cnt_M_u08[2]         30         30         ✓           DigColPsInt_BusbusySeqError_Cnt_M_u08         59         59         ✓           DigColPsInt_CurrentSlave_Cnt_M_u08         59         ✓         ✓           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR2_CHECKSTAT_READ         INIT_SENSOR2_CHECKSTAT_READ         INIT_SENSOR2_CHECKSTAT_READ         V           DigColPsInt_InitFailedOnce_Cnt_M_log         1         1<				
target_i2cREG1_temp.DMAC         0           target_i2cREG1_temp.FUN         0           target_i2cREG1_temp.DIR         0           target_i2cREG1_temp.DIN         1           target_i2cREG1_temp.DOUT         0           target_i2cREG1_temp.SET         0           target_i2cREG1_temp.CLR         0           target_i2cREG1_temp.DDR         1           target_i2cREG1_temp.PD         0           target_i2cREG1_temp.PSL         0           Name         Actual Value         Expected Value         Result           DigColPsInt_Buffer_Cnt_M_u08[0]         10         10         v           DigColPsInt_Buffer_Cnt_M_u08[1]         20         20         v           DigColPsInt_Buffer_Cnt_M_u08[2]         30         30         v           DigColPsInt_BusBusySeqError_Cnt_M_igc         0         0         v           DigColPsInt_CurrentSlave_Cnt_M_u08         59         59         v           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR2_CHECKSTAT_READ         INIT_SENSOR2_CHECKSTAT_READ           DigColPsInt_InitFailedOnce_Cnt_M_igc         1         1         v           DigColPsInt_NackOccured_Cnt_M_igc         1         1         0				
target_i2cREG1_temp.FUN         0           target_i2cREG1_temp.DIR         0           target_i2cREG1_temp.DIN         1           target_i2cREG1_temp.DOUT         0           target_i2cREG1_temp.SET         0           target_i2cREG1_temp.CLR         0           target_i2cREG1_temp.ODR         1           target_i2cREG1_temp.PD         0           target_i2cREG1_temp.PSL         0           Name         Actual Value         Expected Value         Result           DigColPsInt_Buffer_Cnt_M_u08[0]         10         10         v           DigColPsInt_Buffer_Cnt_M_u08[1]         20         20         v           DigColPsInt_Buffer_Cnt_M_u08[2]         30         30         v           DigColPsInt_BusBusySeqError_Cnt_M_loc         0         0         v           DigColPsInt_CurrentSlave_Cnt_M_u08         59         59         v           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR2_CHECKSTAT_READ         INIT_SENSOR2_CHECKSTAT_READ           DigColPsInt_IntFailedOnce_Cnt_M_loc         1         1         v           DigColPsInt_IntFailedOnce_Cnt_M_loc         0         0         v				
target_i2cREG1_temp.DIR       0         target_i2cREG1_temp.DOUT       0         target_i2cREG1_temp.SET       0         target_i2cREG1_temp.DDR       0         target_i2cREG1_temp.DDR       1         target_i2cREG1_temp.PD       0         target_i2cREG1_temp.PSL       0         Name       Actual Value       Expected Value       Result         DigColPsInt_Buffer_Cnt_M_u08[0]       10       10				
target_i2cREG1_temp.DIN         1           target_i2cREG1_temp.DOUT         0           target_i2cREG1_temp.SET         0           target_i2cREG1_temp.CLR         0           target_i2cREG1_temp.DDR         1           target_i2cREG1_temp.PD         0           target_i2cREG1_temp.PSL         0           Name         Actual Value         Expected Value         Result           DigColPsInt_Buffer_Cnt_M_u08[0]         10         10         V           DigColPsInt_Buffer_Cnt_M_u08[1]         20         20         V           DigColPsInt_BusBurySeqError_Cnt_M_u08[2]         30         30         V           DigColPsInt_BusBusySeqError_Cnt_M_lgc         0         0         V           DigColPsInt_CurrentStave_Cnt_M_u08         59         59         V           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR2_CHECKSTAT_READ         INIT_SENSOR2_CHECKSTAT_READ         V           DigColPsInt_InitFailedOnce_Cnt_M_lgc         1         1         V           DigColPsInt_NackOccured_Cnt_M_lgc         0         0         V				
target_i2cREG1_temp.DOUT         0           target_i2cREG1_temp.SET         0           target_i2cREG1_temp.CLR         0           target_i2cREG1_temp.ODR         1           target_i2cREG1_temp.PD         0           target_i2cREG1_temp.PSL         0           Name         Actual Value         Expected Value         Result           DigColPsInt_Buffer_Cnt_M_u08[0]         10         10         ✓           DigColPsInt_Buffer_Cnt_M_u08[1]         20         20         ✓           DigColPsInt_Buffer_Cnt_M_u08[2]         30         30         ✓           DigColPsInt_BusBusyseqError_Cnt_M_igc         0         0         ✓           DigColPsInt_CurrentSlave_Cnt_M_u08         59         59         ✓           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR2_CHECKSTAT_READ         INIT_SENSOR2_CHECKSTAT_READ           DigColPsInt_InitFailedOnce_Cnt_M_lgc         1         1         ✓           DigColPsInt_NackOccured_Cnt_M_lgc         0         0         ✓				
target_i2cREG1_temp.SET       0         target_i2cREG1_temp.CLR       0         target_i2cREG1_temp.ODR       1         target_i2cREG1_temp.PD       0         target_i2cREG1_temp.PSL       0         Name       Actual Value       Expected Value       Result         DigColPsInt_Buffer_Cnt_M_u08[0]       10       10       ✓         DigColPsInt_Buffer_Cnt_M_u08[1]       20       20       ✓         DigColPsInt_Buffer_Cnt_M_u08[2]       30       30       ✓         DigColPsInt_BusBusySeqError_Cnt_M_lgc       0       0       ✓         DigColPsInt_CurrentSlave_Cnt_M_u08       59       59       ✓         DigColPsInt_CurrentStepNo_Cnt_M_enum       INIT_SENSOR2_CHECKSTAT_READ       INIT_SENSOR2_CHECKSTAT_READ       ✓         DigColPsInt_GetData()       136       136       ✓         DigColPsInt_InitFailedOnce_Cnt_M_lgc       1       1       ✓         DigColPsInt_NackOccured_Cnt_M_lgc       0       0       ✓				
target_i2cREG1_temp.CLR       0         target_i2cREG1_temp.ODR       1         target_i2cREG1_temp.PD       0         target_i2cREG1_temp.PSL       0         Name       Actual Value       Expected Value       Result         DigColPsInt_Buffer_Cnt_M_u08[0]       10       10       10       v         DigColPsInt_Buffer_Cnt_M_u08[1]       20       20       v         DigColPsInt_Buffer_Cnt_M_u08[2]       30       30       v         DigColPsInt_BusBusySeqError_Cnt_M_lgc       0       0       v         DigColPsInt_CurrentSlave_Cnt_M_u08       59       59       v         DigColPsInt_CurrentStepNo_Cnt_M_enum       INIT_SENSOR2_CHECKSTAT_READ       v         DigColPsInt_GetData()       136       136       v         DigColPsInt_InitFailedOnce_Cnt_M_lgc       1       1       v         DigColPsInt_NackOccured_Cnt_M_lgc       0       0       v				
target_i2cREG1_temp.ODR         1           target_i2cREG1_temp.PD         0           target_i2cREG1_temp.PSL         0           Name         Actual Value         Expected Value         Result           DigColPsInt_Buffer_Cnt_M_u08[0]         10         10         10         v           DigColPsInt_Buffer_Cnt_M_u08[1]         20         20         v           DigColPsInt_Buffer_Cnt_M_u08[2]         30         30         v           DigColPsInt_BusBusySeqError_Cnt_M_lgc         0         0         v           DigColPsInt_CurrentSlave_Cnt_M_u08         59         59         v           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR2_CHECKSTAT_READ         INIT_SENSOR2_CHECKSTAT_READ         v           DigColPsInt_GetData()         136         136         v           DigColPsInt_InitFailedOnce_Cnt_M_lgc         1         1         v           DigColPsInt_NackOccured_Cnt_M_lgc         0         0         v				
target_i2cREG1_temp.PD         0           target_i2cREG1_temp.PSL         0           Name         Actual Value         Expected Value         Result           DigColPsInt_Buffer_Cnt_M_u08[0]         10         10         10         v           DigColPsInt_Buffer_Cnt_M_u08[1]         20         20         v           DigColPsInt_Buffer_Cnt_M_u08[2]         30         30         v           DigColPsInt_BusBusySeqError_Cnt_M_lgc         0         0         v           DigColPsInt_CurrentSlave_Cnt_M_u08         59         59         v           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR2_CHECKSTAT_READ         INIT_SENSOR2_CHECKSTAT_READ         v           DigColPsInt_GetData()         136         136         v           DigColPsInt_InitFailedOnce_Cnt_M_lgc         1         1         v           DigColPsInt_NackOccured_Cnt_M_lgc         0         0         v				
target_i2cREG1_temp.PSL         0           Name         Actual Value         Expected Value         Result           DigColPsInt_Buffer_Cnt_M_u08[0]         10         10         10           DigColPsInt_Buffer_Cnt_M_u08[1]         20         20         20           DigColPsInt_Buffer_Cnt_M_u08[2]         30         30         30           DigColPsInt_BusBusySeqError_Cnt_M_lgc         0         0         0           DigColPsInt_CurrentSlave_Cnt_M_u08         59         59         59           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR2_CHECKSTAT_READ         INIT_SENSOR2_CHECKSTAT_READ         V           DigColPsInt_GetData()         136         136         ✓           DigColPsInt_InitFailedOnce_Cnt_M_lgc         1         1         ✓           DigColPsInt_NackOccured_Cnt_M_lgc         0         0         ✓	·			
Name         Actual Value         Expected Value         Result           DigColPsInt_Buffer_Cnt_M_u08[0]         10         10         ✓           DigColPsInt_Buffer_Cnt_M_u08[1]         20         20         ✓           DigColPsInt_Buffer_Cnt_M_u08[2]         30         30         ✓           DigColPsInt_BusBusySeqError_Cnt_M_lgc         0         0         ✓           DigColPsInt_CurrentSlave_Cnt_M_u08         59         59         ✓           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR2_CHECKSTAT_READ         INIT_SENSOR2_CHECKSTAT_READ         ✓           DigColPsInt_GetData()         136         136         ✓           DigColPsInt_InitFailedOnce_Cnt_M_lgc         1         1         ✓           DigColPsInt_NackOccured_Cnt_M_lgc         0         0         ✓				
DigColPsInt_Buffer_Cnt_M_u08[0]         10         10         ✓           DigColPsInt_Buffer_Cnt_M_u08[1]         20         20         ✓           DigColPsInt_Buffer_Cnt_M_u08[2]         30         30         ✓           DigColPsInt_BusBusySeqError_Cnt_M_lgc         0         0         ✓           DigColPsInt_CurrentSlave_Cnt_M_u08         59         59         ✓           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR2_CHECKSTAT_READ         INIT_SENSOR2_CHECKSTAT_READ         ✓           DigColPsInt_GetData()         136         136         ✓           DigColPsInt_InitFailedOnce_Cnt_M_lgc         1         1         ✓           DigColPsInt_NackOccured_Cnt_M_lgc         0         0         ✓			I=	
DigColPsInt_Buffer_Cnt_u08[1]         20         20         ✓           DigColPsInt_Buffer_Cnt_M_u08[2]         30         30         ✓           DigColPsInt_BusBusySeqError_Cnt_M_lgc         0         0         ✓           DigColPsInt_CurrentSlave_Cnt_M_u08         59         59         ✓           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR2_CHECKSTAT_READ         INIT_SENSOR2_CHECKSTAT_READ         ✓           DigColPsInt_GetData()         136         136         ✓           DigColPsInt_InitFailedOnce_Cnt_M_lgc         1         1         ✓           DigColPsInt_NackOccured_Cnt_M_lgc         0         0         ✓			•	Result
DigColPsInt_Buffer_Cnt_M_u08[2]         30         30         ✓           DigColPsInt_BusBusySeqError_Cnt_M_lgc         0         0         ✓           DigColPsInt_CurrentSlave_Cnt_M_u08         59         59         ✓           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR2_CHECKSTAT_READ         INIT_SENSOR2_CHECKSTAT_READ         ✓           DigColPsInt_GetData()         136         136         ✓           DigColPsInt_InitFailedOnce_Cnt_M_lgc         1         1         ✓           DigColPsInt_NackOccured_Cnt_M_lgc         0         0         ✓				~
DigColPsInt_BusBusySeqError_Cnt_M_lgc         0         0         ✓           DigColPsInt_CurrentSlave_Cnt_M_u08         59         59         ✓           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR2_CHECKSTAT_READ         INIT_SENSOR2_CHECKSTAT_READ         ✓           DigColPsInt_GetData()         136         136         ✓           DigColPsInt_InitFailedOnce_Cnt_M_lgc         1         1         ✓           DigColPsInt_NackOccured_Cnt_M_lgc         0         0         ✓				~
DigColPsInt_CurrentSlave_Cnt_M_u08  59  DigColPsInt_CurrentStepNo_Cnt_M_enum  INIT_SENSOR2_CHECKSTAT_READ  DigColPsInt_GetData()  136  136  DigColPsInt_InitFailedOnce_Cnt_M_lgc  1  DigColPsInt_NackOccured_Cnt_M_lgc  0  DigColPsInt_NackOccured_Cnt_M_lgc  0				
DigColPsInt_CurrentStepNo_Cnt_M_enum     INIT_SENSOR2_CHECKSTAT_READ     INIT_SENSOR2_CHECKSTAT_READ       DigColPsInt_GetData()     136     136       DigColPsInt_InitFailedOnce_Cnt_M_lgc     1     1       DigColPsInt_NackOccured_Cnt_M_lgc     0     0				
DigColPsInt_GetData()         136         36           DigColPsInt_InitFailedOnce_Cnt_M_lgc         1         1           DigColPsInt_NackOccured_Cnt_M_lgc         0         0				
DigColPsInt_InitFailedOnce_Cnt_M_lgc         1         1         ✓           DigColPsInt_NackOccured_Cnt_M_lgc         0         0         ✓				
DigColPsInt_NackOccured_Cnt_M_lgc 0 0 ✓				
0				
DIGCOIPSINI_Prev I ransactionCnt_Cnt_M_uu8 121 121				
	DIGCOIPSINT_PrevTransactionCnt_Cnt_M_u08	121	121	

DigColPsInt\_GetData



Name	Actual Value	Expected Value	Result
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	~
target_ColSnsrDataPtr_Cnt_T_u16	20000	20000	~
target_DataTypePtr_Cnt_T_u08	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	495	495	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	66	66	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	78	78	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	-
target_SpurSnsrDataPtr_Cnt_T_u16	28203	28203	~

T				V
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	-

Test Step 2.25 (Repeat Count = 1)		✓
Name	Input Value	
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16	
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08	
DigColPsInt_Buffer_Cnt_M_u08[0]	40	
DigColPsInt_Buffer_Cnt_M_u08[1]	50	
DigColPsInt_Buffer_Cnt_M_u08[2]	60	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	
DigColPsInt_ColSnsrData_Cnt_M_u16	14752	

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DigColPsInt GetData Input Value DigColPsInt\_CurrentSlave\_Cnt\_M\_u08  ${\tt DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum}$ INIT\_SENSOR1\_DUMMY\_SEND DigColPsInt\_InitFailedOnce\_Cnt\_M\_lgc DigColPsInt\_InitialTime\_mS\_M\_u32 29552845 DigColPsInt NackOccured Cnt M lgc DigColPsInt\_PrevTransactionCnt\_Cnt\_M\_u08 11 DigColPsInt\_RecvOverrunError\_Cnt\_M\_lgc 1 DigColPsInt\_RecvdDataType\_Cnt\_M\_u08 1 DigColPsInt\_SensInitialized\_Cnt\_M\_lgc  $DigColPsInt\_SpurSnsrData\_Cnt\_M\_u16$ 21478 DigColPsInt\_TransactionCnt\_Cnt\_M\_u08 DtrmnElapsedTime\_mS\_u16(ElapsedTime) target\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime GetSystemTime\_mS\_u32(CurrentTime) target\_GetSystemTime\_mS\_u32\_CurrentTime I2c\_Send(I2cRegPtr\_Cnt\_T\_str) target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str I2c\_SetupMasterTransmit(I2cRegPtr\_Cnt\_T\_str) target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str SpurSnsrDataPtr\_Cnt\_T\_u16 target\_SpurSnsrDataPtr\_Cnt\_T\_u16 i2cREG1\_temp target\_i2cREG1\_temp k\_ColSensorl2CAddress\_Cnt\_u08 28 k\_I2CHWInitTransactionTime\_Sec\_f32 0 target\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime 8346  $target\_GetSystemTime\_mS\_u32\_CurrentTime$ 25541837 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.OAR 567  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IMR$ 44 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.STR 4444 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKL 566 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKH 4466 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CNT 129 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DRR 6 target I2c Send I2cRegPtr Cnt T str.SAR 567 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DXR 44 target I2c Send I2cRegPtr Cnt T str.MDR 566 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IVR 554 target I2c Send I2cRegPtr Cnt T str.EMDR 1 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSC 44 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID11 4466 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID12 44 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DMAC target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.FUN 1 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIR 2 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIN 0 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DOUT 1 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SET 1 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLR 2 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.ODR 0  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PD$ 3 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSL 3  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.OAR$ 567  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IMR$ 44 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.STR 4444 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKL 566 target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH 4466  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CNT$ 129 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DRR 6  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SAR$ 567 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DXR 44  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.MDR$ 566 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IVR 554  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.EMDR$ 1 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSC 44

4466

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44

target i2cREG1 temp.OAR

target\_i2cREG1\_temp.IMR

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID11$ 

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID12$ 

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DMAC$ 

 $target\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str.FUN$ 

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIR

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIN

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SET$ 

target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.ODR$ 

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PD

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSL$ 

target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT

DigColPsInt\_GetData





Name	Input Value		
target_i2cREG1_temp.STR	4444		
target_i2cREG1_temp.CLKL	566		
target_i2cREG1_temp.CLKH	4466		
target_i2cREG1_temp.CNT	129		
target_i2cREG1_temp.DRR	6		
target_i2cREG1_temp.SAR	567 44		
target_i2cREG1_temp.DXR	566		
target_i2cREG1_temp.MDR	554		
target_i2cREG1_temp.IVR	1		
target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC	44		
target i2cREG1 temp.PID11	4466		
target i2cREG1 temp.PID12	44		
target i2cREG1 temp.DMAC	1		
target i2cREG1 temp.FUN	1		
target i2cREG1 temp.DIR	2		
target_i2cREG1_temp.DIN	0		
target_i2cREG1_temp.DOUT	1		
target i2cREG1 temp.SET	1		
target i2cREG1 temp.CLR	2		
target i2cREG1 temp.ODR	0		
target i2cREG1 temp.PD	3		
target i2cREG1 temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	40	40	Rosuit
DigColPsInt_Buffer_Cnt_M_u08[1]	50	50	-
DigColPsInt Buffer Cnt M u08[2]	60	60	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	-
DigColPsInt_CurrentSlave_Cnt_M_u08	66	66	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_DUMMY_SEND	INIT_SENSOR1_DUMMY_SEND	<b>*</b>
DigColPsInt GetData()	170	170	
DigColPsInt InitFailedOnce Cnt M Igc	0	0	<b>V</b>
DigColPsInt NackOccured Cnt M Igc	0	0	
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	14	14	<b>✓</b>
DigColPsInt RecvOverrunError Cnt M Igc	0	0	
DigColPsInt SensInitialized Cnt M Igc	1	1	<b>~</b>
target_ColSnsrDataPtr_Cnt_T_u16	14752	14752	
target_DataTypePtr_Cnt_T_u08	1	1	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.OAR	567	567	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	129	129	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	V
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	· ·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	

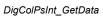
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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_SpurSnsrDataPtr_Cnt_T_u16	21478	21478	<b>✓</b>

T T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

Test Step 2.26 (Repeat Count = 1)	
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	70
DigColPsInt_Buffer_Cnt_M_u08[1]	80
DigColPsInt_Buffer_Cnt_M_u08[2]	90
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1.
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	17542
DigColPsInt_CurrentSlave_Cnt_M_u08	73
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_SENDCMD
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0
DigColPsInt_InitialTime_mS_M_u32	30555597
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	17
DigColPsInt RecvOverrunError Cnt M Igc	1
DigColPsInt RecvdDataType Cnt M u08	4
DigColPsInt SensInitialized Cnt M Igc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	22177
DigColPsInt TransactionCnt Cnt M u08	18
OtrmnElapsedTime mS u16(ElapsedTime)	target DtrmnElapsedTime mS u16 ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
2c Send(I2cRegPtr Cnt T str)	target I2c Send I2cRegPtr Cnt T str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target I2c SetupMasterTransmit I2cRegPtr Cnt T str
SpurSnsrDataPtr Cnt T u16	target SpurSnsrDataPtr Cnt T u16
2cREG1 temp	target_i2cREG1_temp
ColSensorI2CAddress Cnt u08	35
C I2CHWInitTransactionTime Sec f32	10
arget_DtrmnElapsedTime_mS_u16_ElapsedTime	8853
arget GetSystemTime mS u32 CurrentTime	26544589
arget I2c Send I2cRegPtr Cnt T str.OAR	65
arget I2c Send I2cRegPtr Cnt T str.IMR	89
arget I2c Send I2cRegPtr Cnt T str.STR	67
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
arget I2c Send I2cRegPtr Cnt T str.CLKH	577
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88
arget I2c Send I2cRegPtr Cnt T str.DRR	23
arget I2c Send I2cRegPtr Cnt T str.SAR	65
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
arget_12c_Send_12cRegPtr_Cnt_1_str.bbk	7
arget_l2c_Send_l2cRegPtr_Cnt_T_str.lvlR arget_l2c_Send_l2cRegPtr_Cnt_T_str.lVR	44
	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	89
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577 89
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	The state of the s
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0





Name	Input Value		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1		
target I2c Send I2cRegPtr Cnt T str.DOUT	2		
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0		
target I2c Send I2cRegPtr Cnt T str.ODR	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	577		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	23		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	65		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2 2		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
target_i2cREG1_temp.OAR	65		
target_i2cREG1_temp.IMR	89		
target_i2cREG1_temp.STR	67		
target_i2cREG1_temp.CLKL	7		
target_i2cREG1_temp.CLKH	577		
target_i2cREG1_temp.CNT	88		
target_i2cREG1_temp.DRR	23		
target_i2cREG1_temp.SAR	65		
target_i2cREG1_temp.DXR	89		
target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR	44		
target i2cREG1 temp.EMDR	2		
target i2cREG1 temp.PSC	89		
target_i2cREG1_temp.PID11	577		
target_i2cREG1_temp.PID12	89		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	70	70	Result
DigColPsInt_Buffer_Cnt_M_u08[1]	80	80	·
DigColPsInt_Buffer_Cnt_M_u08[2]	90	90	-
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	•
DigColPsInt_CurrentSlave_Cnt_M_u08	73	73	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_SEN	INIT_SENSOR2_EXTREADCTRLREG_SEN	~
DigColPsInt_GetData()	12	12	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	18	18	<b>~</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	<b>V</b>
target_ColSnsrDataPtr_Cnt_T_u16	17542	17542	· ·
target_DataTypePtr_Cnt_T_u08 target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	4 65	~
targot_120_0cmu_1201t0gr ti_OHL_1_5tt.OAIN	00	100	





Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	89	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.STR	67	67	
target I2c Send I2cRegPtr Cnt T str.CLKL	7	7	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.CLKH	577	577	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.DRR	23	23	
target I2c Send I2cRegPtr Cnt T str.SAR	65	65	<b>v</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.IVR	44	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	<b>v</b>
target I2c Send I2cRegPtr Cnt T str.PID12	89	89	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>v</b>
target I2c Send I2cRegPtr Cnt T str.DIN	1	1	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.ODR	1	1	
target I2c Send I2cRegPtr Cnt T str.PD	2	2	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	577	577	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	23	23	<u> </u>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	89	89	<u> </u>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	7	7	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	89	89	<u> </u>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	0	0	
	0	0	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR		1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1 2	2	
	2 2	2	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	
	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL		i i	
target_SpurSnsrDataPtr_Cnt_T_u16	22177	22177	

T and the second se				
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

Test Step 2.27 (Repeat Count = 1)	· Carlotte and the control of the co
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	44
DigColPsInt_Buffer_Cnt_M_u08[1]	55
DigColPsInt_Buffer_Cnt_M_u08[2]	66
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	20332
DigColPsInt_CurrentSlave_Cnt_M_u08	80
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_SETREG
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	31558349
DigColPsInt_NackOccured_Cnt_M_lgc	1

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Name	Input Value
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	23
DigColPsInt RecvOverrunError Cnt M Igc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	22876
DigColPsInt TransactionCnt Cnt M u08	22
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	42
k_I2CHWInitTransactionTime_Sec_f32	2.5
target_DtrmnElapsedTime_mS_u16_ElapsedTime	9360
target_GetSystemTime_mS_u32_CurrentTime	27547341
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123 45
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	54 66
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	66 554
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	788
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	66
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2
target_i2cREG1_temp.OAR	54
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	8
target_i2cREG1_temp.CLKL	554
target_i2cREG1_temp.CLKH	344
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	123 45

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Name	Input Value		
target_i2cREG1_temp.SAR	54		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	554		
target i2cREG1 temp.IVR	788		
target i2cREG1 temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	344		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
	1		
target_i2cREG1_temp.FUN	3		
target_i2cREG1_temp.DIR	2		
target_i2cREG1_temp.DIN			
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	3		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	2		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	44	44	~
DigColPsInt_Buffer_Cnt_M_u08[1]	55	55	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[2]	66	66	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	•
DigColPsInt_CurrentSlave_Cnt_M_u08	80	80	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_SET		~
DigColPsInt_GetData()	162	162	-
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1	1	•
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	_
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	22	22	•
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	_
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	•
target_ColSnsrDataPtr_Cnt_T_u16	20332	20332	-
	2	2	-
target_DataTypePtr_Cnt_T_u08	54	54	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR		8	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8	554	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	344	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	123	123	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	45	45	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	54	54	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	66	66	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	554	554	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	788	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	344	344	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	66	66	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1	1	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	3	3	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	2	2	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54	54	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8	8	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554	554	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344	344	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123	123	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45	45	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54	54	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554	554	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788	788	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344	344	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	•

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>✓</b>
target_SpurSnsrDataPtr_Cnt_T_u16	22876	22876	~

T				
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	66
DigColPsInt_Buffer_Cnt_M_u08[1]	77
DigColPsInt_Buffer_Cnt_M_u08[2]	88
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	23122
DigColPsInt_CurrentSlave_Cnt_M_u08	87
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_READ
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0
DigColPsInt_InitialTime_mS_M_u32	32561101
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	29
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
)igColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SensInitialized_Cnt_M_lgc	1
igColPsInt_SpurSnsrData_Cnt_M_u16	23575
DigColPsInt_TransactionCnt_Cnt_M_u08	26
OtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
2cREG1_temp	target_i2cREG1_temp
_ColSensorI2CAddress_Cnt_u08	49
_I2CHWInitTransactionTime_Sec_f32	0.69999988
arget_DtrmnElapsedTime_mS_u16_ElapsedTime	9867
arget_GetSystemTime_mS_u32_CurrentTime	28550093
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3

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Name	Input Value		
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	100 2767		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	556		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	3		
target_i2cREG1_temp.IMR	100		
target_i2cREG1_temp.STR	7788		
target_i2cREG1_temp.CLKL	2767		
target_i2cREG1_temp.CLKH	556		
target_i2cREG1_temp.CNT	564		
target_i2cREG1_temp.DRR	88		
target_i2cREG1_temp.SAR	100		
target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR	2767		
target i2cREG1_temp.ivR	9		
target i2cREG1 temp.EMDR	0		
target_i2cREG1_temp.PSC	100		
target i2cREG1 temp.PID11	556		
target i2cREG1 temp.PID12	100		
target i2cREG1 temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	3		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	66	66	-
DigColPsInt_Buffer_Cnt_M_u08[1]	77	77	~
			<b> </b>
DigColPsInt_Buffer_Cnt_M_u08[2]	88	88	
DigColPsInt_BusBusySeqError_Cnt_M_Igc	0	88 0	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08	0 87	88 0 87	~
DigColPsInt_BusBusySeqError_Cnt_M_Igc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum	0 87 INIT_SENSOR2_EXTREADCTRLREG_REA	88 0 87 INIT_SENSOR2_EXTREADCTRLREG_REA	•
DigColPsInt_BusBusySeqError_Cnt_M_Igc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData()	0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130	88 0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130	• •
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc	0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0	88 0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0	
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc	0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0	88 0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0	0
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08	0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26	88 0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26	
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc	0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26	88 0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0	
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SensInitIalized_Cnt_M_lgc	0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0 1	88 0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0 1	
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SensInitIalized_Cnt_M_lgc target_ColSnsrDataPtr_Cnt_T_u16	0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0 1 23122	88 0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0 1 23122	
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_u08 DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SensInitialized_Cnt_M_lgc target_ColSnsrDataPtr_Cnt_T_u16 target_DataTypePtr_Cnt_T_u08	0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0 1 23122 5	88 0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0 1 23122 5	
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_u08 DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SensInitialized_Cnt_M_lgc target_ColSnsrDataPtr_Cnt_T_u16 target_DataTypePtr_Cnt_T_u08 target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0 1 23122 5 3	88 0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0 1 23122 5 3	0
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SensInitialized_Cnt_M_lgc target_ColSnsrDataPtr_Cnt_T_u16 target_DataTypePtr_Cnt_T_u08 target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0 1 23122 5 3 100	88 0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0 1 23122 5 3 100	
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SensInitialized_Cnt_M_lgc target_ColSnsrDataPtr_Cnt_T_u16 target_DataTypePtr_Cnt_T_u08 target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0 1 23122 5 3 100 7788	88 0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0 1 23122 5 3 100 7788	
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SensInitialized_Cnt_M_lgc target_ColSnsrDataPtr_Cnt_T_u16 target_DataTypePtr_Cnt_T_u08 target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR target_I2c_Send_I2cRegPtr_Cnt_T_str.JMR target_I2c_Send_I2cRegPtr_Cnt_T_str.STR target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0 1 23122 5 3 100 7788 2767	88 0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0 1 23122 5 3 100 7788 2767	
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SensInitialized_Cnt_M_lgc target_ColSnsrDataPtr_Cnt_T_u16 target_DataTypePtr_Cnt_T_u08 target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0 1 23122 5 3 100 7788	88 0 87 INIT_SENSOR2_EXTREADCTRLREG_REA 130 0 0 26 0 1 23122 5 3 100 7788	

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	88	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	100	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	2767	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	9	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	100	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	556	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	100	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	556	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	88	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100	100	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767	2767	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	100	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556	556	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	100	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_SpurSnsrDataPtr_Cnt_T_u16	23575	23575	~

Τ				•	•
Actual Function	Count	Expected Function	Count	Resul	t
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime mS u16	1		,

Test Step 2.29 (Repeat Count = 1)	✓
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_Igc	1
DigColPsInt_CmdFailOccurred_Cnt_M_Igc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	25912
DigColPsInt_CurrentSlave_Cnt_M_u08	94
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADDATREG_SETREG
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1
DigColPsInt_InitialTime_mS_M_u32	33563853
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	35
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	24274





Name	Input Value
DigColPsInt_TransactionCnt_Cnt_M_u08	30
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	56
k_I2CHWInitTransactionTime_Sec_f32	1.10000002
target_DtrmnElapsedTime_mS_u16_ElapsedTime	10374
target_GetSystemTime_mS_u32_CurrentTime	29552845
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	678
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	45 66
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	56
target I2c Send I2cRegPtr Cnt T str.CLKH	6788
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	7878
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12
target I2c Send I2cRegPtr Cnt T str.SAR	678
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	778
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	6788
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	45
target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	1
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	678
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	6788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	7878
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	678
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	778
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	45
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	6788 45
target   2c SetupMasterTransmit   2cRegPtr Cnt   str.PID12 target   12c SetupMasterTransmit   12cRegPtr Cnt T str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	0
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1
target_i2cREG1_temp.OAR	678
target_i2cREG1_temp.IMR	45
target_i2cREG1_temp.STR	66
target_i2cREG1_temp.CLKL	56
target_i2cREG1_temp.CLKH	6788
target_i2cREG1_temp.CNT	7878
target_i2cREG1_temp.DRR	12
target_i2cREG1_temp.SAR	678
target_i2cREG1_temp.DXR	45
target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR	56 778
target_i2cREG1_temp.EMDR	1

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5			
Name	Input Value		
target_i2cREG1_temp.PSC	45		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12	6788 45		
target_i2cREG1_temp.DMAC	1		
target i2cREG1 temp.FUN	1		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1 2		
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL	1		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	Kesuit
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	-
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	-
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	-
DigColPsInt_CurrentSlave_Cnt_M_u08	56	56	-
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	•
DigColPsInt_GetData()	44	44	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	•
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	30	30	-
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	•
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	<b>V</b>
I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	-
target_ColSnsrDataPtr_Cnt_T_u16	25912	25912	
target_DataTypePtr_Cnt_T_u08	0	0	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	678	678	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	45	45	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	66	66	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	56	56	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	7878	7878	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	678	678	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	45 56	45	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	778	778	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	45	45	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	6788	6788	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	45	45	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	1 2	1 2	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	678	678	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	45	45	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	66	66	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	56	56	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	7878	7878	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	678	678	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	45	45	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	56	56	<b>•</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	778	778	Ž
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	45	45	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	6788	6788	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	45	45	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	0	0	•

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	<b>✓</b>
target_SpurSnsrDataPtr_Cnt_T_u16	24274	24274	<b>✓</b>

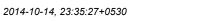
T				V
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	<b>✓</b>
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	<b>✓</b>

Test Step 2.30 (Repeat Count = 1)	
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	40
DigColPsInt_Buffer_Cnt_M_u08[1]	50
igColPsInt_Buffer_Cnt_M_u08[2]	60
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
igColPsInt_ColSnsrData_Cnt_M_u16	28702
igColPsInt_CurrentSlave_Cnt_M_u08	101
igColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG
igColPsInt_InitFailedOnce_Cnt_M_lgc	0
igColPsInt_InitialTime_mS_M_u32	34566605
igColPsInt_NackOccured_Cnt_M_lgc	1
igColPsInt_PrevTransactionCnt_Cnt_M_u08	41
igColPsInt_RecvOverrunError_Cnt_M_lgc	0
igColPsInt_RecvdDataType_Cnt_M_u08	4
igColPsInt_SensInitialized_Cnt_M_lgc	1
igColPsInt_SpurSnsrData_Cnt_M_u16	24973
igColPsInt_TransactionCnt_Cnt_M_u08	34
trmnElapsedTime_mS_u16(ElapsedTime)	target DtrmnElapsedTime mS u16 ElapsedTime
etSystemTime mS u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target I2c SetupMasterTransmit I2cRegPtr Cnt T str
purSnsrDataPtr Cnt T u16	target SpurSnsrDataPtr Cnt T u16
ccREG1 temp	target i2cREG1 temp
ColSensorI2CAddress Cnt u08	63
I2CHWInitTransactionTime Sec f32	1.5
arget_DtrmnElapsedTime_mS_u16_ElapsedTime	10881
arget GetSystemTime mS u32 CurrentTime	30555597
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
rget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
rget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
rget_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	495
	56
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	897
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	
irget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
irget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
irget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
rget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
rget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0

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Name	Input Value		
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78 78		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	495		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR target_l2c SetupMasterTransmit_l2cRegPtr_Cnt_T str.PSC	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	1		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PD	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
target_i2cREG1_temp.OAR	66		
target_i2cREG1_temp.IMR	78		
target_i2cREG1_temp.STR	78		
target_i2cREG1_temp.CLKL	495		
target_i2cREG1_temp.CLKH	56		
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	897 98		
target_i2cREG1_temp.SAR	66		
target i2cREG1 temp.DXR	78		
target_i2cREG1_temp.MDR	495		
target_i2cREG1_temp.IVR	66		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	78		
target_i2cREG1_temp.PID11	56		
target_i2cREG1_temp.PID12	78		
target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target i2cREG1 temp.DIN	1		
target_i2cREG1_temp.DOUT	0		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL		le	l
Name	Actual Value	Expected Value 40	Result
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	40 50	50	-
DigColPsInt_Buffer_Cnt_M_u08[2]	60	60	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	·
DigColPsInt_CurrentSlave_Cnt_M_u08	101	101	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG	READ_SENSOR1_SETREG	~
DigColPsInt_GetData()	2	2	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	<b>V</b>
DigColPoint_PrevTransactionCnt_Cnt_M_u08	34	0	<b>V</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	1	~
	1		
DigColPsInt_SensInitialized_Cnt_M_lgc	28702		
DigColPsInt_SensInitialized_Cnt_M_lgc target_ColSnsrDataPtr_Cnt_T_u16	28702	28702 4	~
DigColPsInt_SensInitialized_Cnt_M_lgc		28702	~
DigColPsInt_SensInitialized_Cnt_M_lgc target_ColSnsrDataPtr_Cnt_T_u16 target_DataTypePtr_Cnt_T_u08	28702 4	28702 4	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
DigColPsInt_SensInitialized_Cnt_M_lgc target_ColSnsrDataPtr_Cnt_T_u16 target_DataTypePtr_Cnt_T_u08 target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	28702 4 66	28702 4 66	~
DigColPsInt_SensInitialized_Cnt_M_lgc target_ColSnsrDataPtr_Cnt_T_u16 target_DataTypePtr_Cnt_T_u08 target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	28702 4 66 78	28702 4 66 78	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \





Name	Actual Value	Expected Value	Result
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	56	56	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0	0	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	<b>Y</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	¥
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	V
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897 98	98	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	-
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	495	495	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	66	66	-
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	0	0	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	78	78	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	78	78	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>V</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	0	0	-
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	1	1	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_SpurSnsrDataPtr_Cnt_T_u16	24973	24973	~

T .				V
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 2.31 (Repeat Count = 1)		V
Name	Input Value	
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16	
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08	
DigColPsInt_Buffer_Cnt_M_u08[0]	70	
DigColPsInt_Buffer_Cnt_M_u08[1]	80	
DigColPsInt_Buffer_Cnt_M_u08[2]	90	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	
DigColPsInt_ColSnsrData_Cnt_M_u16	31492	
DigColPsInt_CurrentSlave_Cnt_M_u08	108	
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_GETDATA	
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1	
DigColPsInt_InitialTime_mS_M_u32	35569357	
DigColPsInt_NackOccured_Cnt_M_lgc	0	
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	47	
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	
DigColPsInt_RecvdDataType_Cnt_M_u08	0	
DigColPsInt_SensInitialized_Cnt_M_lgc	0	

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DigColPsInt GetData Input Value DigColPsInt\_SpurSnsrData\_Cnt\_M\_u16 25672 DigColPsInt\_TransactionCnt\_Cnt\_M\_u08 DtrmnElapsedTime\_mS\_u16(ElapsedTime) target DtrmnElapsedTime mS u16 ElapsedTime GetSystemTime\_mS\_u32(CurrentTime) target\_GetSystemTime\_mS\_u32\_CurrentTime I2c\_Send(I2cRegPtr\_Cnt\_T\_str) target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str I2c\_SetupMasterTransmit(I2cRegPtr\_Cnt\_T\_str) target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str SpurSnsrDataPtr\_Cnt\_T\_u16 target\_SpurSnsrDataPtr\_Cnt\_T\_u16 i2cREG1 temp target\_i2cREG1\_temp k\_ColSensorl2CAddress\_Cnt\_u08 70 k I2CHWInitTransactionTime Sec f32 1 89999998 target\_DtrmnElapsedTime\_mS\_u16\_ElapsedTime 11388 31558349 target GetSystemTime mS u32 CurrentTime target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.OAR 567 target I2c Send I2cRegPtr Cnt T str.IMR 44 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.STR 4444 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKL 566 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKH 4466 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CNT 129 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DRR 6 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SAR 567 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DXR 44 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.MDR 566 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IVR 554 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.EMDR 44 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSC target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID11 4466 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID12 44 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DMAC target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.FUN 1 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIR 2 target I2c Send I2cRegPtr Cnt T str.DIN 0 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DOUT target I2c Send I2cRegPtr Cnt T str.SET 1 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLR 2 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.ODR 0 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PD 3  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSL$ 3  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.OAR$ 567  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IMR$ 44 target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR 4444  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKL$ 566 4466 target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CNT$ 129 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DRR 6  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SAR$ 567 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DXR 44 566  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.MDR$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IVR 554  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.EMDR$ 1 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSC 44 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID11 4466 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID12 44  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DMAC$ 1  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.FUN$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIR 2  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIN$ 0 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DOUT 1  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SET$ 1 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLR 2  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.ODR$ 0 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PD 3 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSL 3 target\_i2cREG1\_temp.OAR 567 target i2cREG1 temp.IMR 44 target\_i2cREG1\_temp.STR 4444 target i2cREG1 temp.CLKL 566 target\_i2cREG1\_temp.CLKH 4466 target i2cREG1 temp.CNT 129 target\_i2cREG1\_temp.DRR 6

> 567 44

566

554

target\_i2cREG1\_temp.SAR

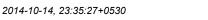
target\_i2cREG1\_temp.DXR target\_i2cREG1\_temp.MDR

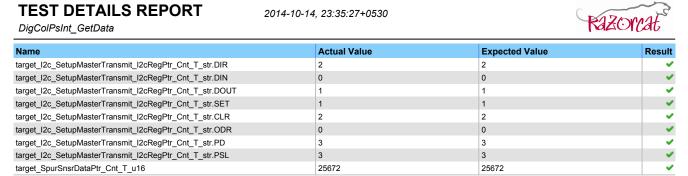
target\_i2cREG1\_temp.IVR

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DigColPsint_GetData		(alc)	UNU
Name	Input Value		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	44		
target_i2cREG1_temp.PID11	4466		
target_i2cREG1_temp.PID12	44		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	2		
target_i2cREG1_temp.DIN	0		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	80	80	✓
DigColPsInt_Buffer_Cnt_M_u08[2]	90	90	<b>✓</b>
DigColPsInt_BusBusySeqError_Cnt_M_Igc	0	0	✓
DigColPsInt_CurrentSlave_Cnt_M_u08	70	70	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	✓
DigColPsInt_GetData()	44	44	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	✓
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	38	38	✓
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_Igc	1	1	✓
I2c_Send(Length_Cnt_T_u32)	1	1	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✓
target_ColSnsrDataPtr_Cnt_T_u16	31492	31492	~
target_DataTypePtr_Cnt_T_u08	0	0	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	





T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	•
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c_Send	1	l2c_Send	1	~
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	~

Test Step 2.32 (Repeat Count = 1)	la constant de la con
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	3
DigColPsInt_Buffer_Cnt_M_u08[1]	6
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	34282
DigColPsInt_CurrentSlave_Cnt_M_u08	115
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0
DigColPsInt_InitialTime_mS_M_u32	36572109
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	53
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	26371
DigColPsInt_TransactionCnt_Cnt_M_u08	42
OtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
2c Send(I2cRegPtr Cnt T str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
_ , , , , , , , , , , , , , , , , , , ,	
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
2cREG1_temp	target_i2cREG1_temp
C_ColSensorI2CAddress_Cnt_u08	77
x_I2CHWInitTransactionTime_Sec_f32	2.29999995
arget_DtrmnElapsedTime_mS_u16_ElapsedTime	0
arget_GetSystemTime_mS_u32_CurrentTime	32561101
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7
arget I2c Send I2cRegPtr Cnt T str.IVR	44
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
arget I2c Send I2cRegPtr Cnt T str.PSC	89
arget I2c Send I2cRegPtr Cnt T str.PID11	577
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2





DigColPsInt_CurrentSlave_Cnt_M_u08  115  115  115  V  DigColPsInt_CurrentStepNo_Cnt_M_enum  INIT_SENSOR1_READERROR_SETREG  DigColPsInt_GetData()  34  34	Name	Input Value		
Langer, Die, Sender (Jacksephn, Comp. 1 - Jan Pieter, Der 1 - Jan Pieter, Die, Steller, Dieser, Dieser	target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0		
Sept   12-86	target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR			
Sept   Descriptions   Transmit Discopin Cent   Ten DAR   Sept   Descriptions   Ten DAR   Sep				
Bingst 129. Subplobated Frameric Calegory Co. T. an IMR   180	· · · ·			
taget_DE_SequebaserTransmert_Descript_Cort_T_sec_TEXT target_DE_SequebaserTransmert_Descript_Cort_T_sec_TEXT target_DE_SequebaseT_T_sec_TEXT target_DE_Seq_TEXT_T_sec_TEXT_T_sec				
Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 1 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 1 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 2 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 2 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 2 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 2 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 2 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 2 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 2 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 2 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 2 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 2 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 2 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 2 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 2 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 3 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 3 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 3 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 3 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 3 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 3 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 3 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 3 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 3 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 3 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 4 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 4 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and LOK. 4 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and Lok. 4 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and Lok. 4 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and Lok. 4 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and Lok. 4 Hange, Die, Shaphdester Transent, Deckley, Dr. J. and Lok. 4 Hange, Die, Shaphdester Transent,				
burger   Dec.   Section   Section   Continue   Contin				
taggs   De_SeapAdamor Transmill_CoRegings   Cmil_ and SMR   50				
Image   Dec. Selephotes Framering   Celephotes   Celeph	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88		
taged_128_8abpAdestransmit_D28eggt_Conf_12 st DNR	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23		
Langer, I.Z Seubphane Transmill, I.Zerlegy C. OLT, 2 ab 700	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR			
tayed, 10. SetupAdateFramenia (2016-1971 CMT 1 ± 147-1874) tayed, 10. SetupAdateFramenia (2016-1971				
Image   Dec. SetupAttent Transmull DeReignPr, CMT_set PADR   20   20   20   20   20   20   20   2	· · ·			
target_L2s_shupAnterTransmit_L2Rep0Pr_CnTst_PBC target_L2s_shupAnterTransmit_L2Rep0Pr_CnTst_PBD12 target_L2s_shupAnterTransmit_L2Rep0Pr_CnTst_PBD12 target_L2s_shupAnterTransmit_L2Rep0Pr_CnTst_PBD12 target_L2s_shupAnterTransmit_L2Rep0Pr_CnTst_PBD12 target_L2s_shupAnterTransmit_L2Rep0Pr_CnTst_DN target_L2s_shupAnterTransmit_L2rep0Pr_CnTshupAnterTransmit_L2s_cnD target_L2s_shupAnterTransmit_L2rep0Pr_CnTshupAnterTransmit_L2s_cnD target_L2s_shupAnterTransmit_L2re				
larget 12.5 Sebus/Matter Transmit 12.6Reg/Pt Celt _ 1 set PID11	· · ·			
Image   L.S SelayAbasterTransing   John Paper   Lost - T. Jun Pin Pin Pin Pin Pin Pin Pin Pin Pin Pi				
tinged_R2_SetupMasterTransmut_R2People_Costset_DIR  tinged_R2_SetupMasterTransmut_R2People_Costset_DIR  tinged_R2_SetupMasterTransmut_R2People_Costset_DIR  tinged_R2_SetupMasterTransmut_R2People_Costset_DOUT*  2 tinged_R2_SetupMasterTransmut_R2People_Costset_DOUT*  2 tinged_R2_SetupMasterTransmut_R2People_Costset_DOUT*  2 tinged_R2_SetupMasterTransmut_R2People_Costset_DOUT*  2 tinged_R2_SetupMasterTransmut_R2People_Costset_DOUT*  2 tinged_R2_Set_DispMasterTransmut_R2People_Costset_DOUT*  2 tinged_R2_Set_DispMasterTransmut_R2People_Costset_DOUT*  2 tinged_R2_Set_DispMasterTransmut_R2People_Costset_DOUT*  2 tinged_R2_Set_DispMasterTransmut_R2People_Costset_DOUT*  2 tinged_R2_Set_DispMasterTransmut_R2People_Costset_DOUT*  2 tinged_R2_Set_DispMasterTransmut_R2People_Costset_DOUT*  3 tinged_R2_Set_DispMasterTransmut_R2People_Costset_DOUT*  4 tinged_R2_Set_DispMasterTransmut_R2_Set_Dout*  4 tinged_R2_Set_DispMasterTransmut_R2_Set_Dout*  4 tinged_R2_Set_DispMasterTransmut_R2_Set_Dout*  4 tinged_R2_Set_DispMasterTransmut_R2_Set_Dout*  4 tinged_R2_Set_DispMasterTransmut_R2_Set_Dout*  4 tinged_R2_Set_DispMasterTransmut_R2_Set_Dout*  5 tinge	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89		
Image   Les SebugMasterTransmit   ZerRegitPr Cost   T at DIN	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
target_L2s_SetupMateFrammit_L2RepQP*_Cnt_T_str.DNT   1	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN			
Lingual Lingual Sect				
Image   Ling				
Larges   Lag. SetupMeater Transmil   Larges   Pro. Cont.   1 str. Cont.				
Integral_Eo_SebupMasterTransmal_EoRegPir_Conl_T_sir_DOR				
Image_Lipe_SehupAssierTransmit_LipeRepPr_Cnl_T_str.PD				
Images   LazeREG1   Jamp DAR				
larget_ZeREG1   lamp, LINR	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
Bargel_22REG1_lamp_DCLKL   7   7   7   7   7   7   7   7   7	target_i2cREG1_temp.OAR	65		
Images   JackREG1   temp CILK	target_i2cREG1_temp.IMR			
Internal Local Edit   Internal CLKH   S77   Internal Local Edit   Internal CLKH   Internal C				
Integret   J2CRECG   temp. DNR   23				
target_J2cREG1_temp.DRR 65 target_J2cREG1_temp.DRR 89 target_J2cREG1_temp.DRR 97 target_J2cREG1_temp.DRR 97 target_J2cREG1_temp.DRR 97 target_J2cREG1_temp.EMDR 97 target_J2cREG1_temp.EMDR 97 target_J2cREG1_temp.EMDR 97 target_J2cREG1_temp.EMDR 97 target_J2cREG1_temp.PD11 97 target_J2cREG1_temp.PD12 98 target_J2cREG1_temp.DMAC 97 target_J2cREG1_temp.DMAC 97 target_J2cREG1_temp.DIR 97 target_J2cREG1_temp.DIR 97 target_J2cREG1_temp.DIR 97 target_J2cREG1_temp.DIR 97 target_J2cREG1_temp.DIR 97 target_J2cREG1_temp.DIR 97 target_J2cREG1_temp.DUT 97 target_J2cREG1_temp.PSL 97 target_J2cREG1_temp.DUT 97 target_J2cREG1_temp.DUT 97 target_J2cREG				
target_J2cREG temp_DXR				
target_IZCREG1_temp.DXR         99           target_IZCREG1_temp.MDR         7           target_IZCREG1_temp.RMR         44           target_IZCREG1_temp.EMDR         2           target_IZCREG1_temp.PID11         577           target_IZCREG1_temp.PID12         89           target_IZCREG1_temp.DID12         89           target_IZCREG1_temp.DIN         0           target_IZCREG1_temp.DIN         0           target_IZCREG1_temp.DIN         1           target_IZCREG1_temp.DUT         2           target_IZCREG1_temp.DUT         2           target_IZCREG1_temp.DUT         2           target_IZCREG1_temp.DCR         0           target_IZCREG1_temp.DCR         1           target_IZCREG1_temp.DDR         1           target_IZCREG1_temp.DDR         1           target_IZCREG1_temp.DDR         2           target_IZCREG1_temp.DDR         1           target_IZCREG1_temp.DDR         1           target_IZCREG1_temp.DDR         1           target_IZCREG1_temp.DDB         2           target_IZCREG1_temp.DDB         2           target_IZCREG1_temp.DDB         1           target_IZCREG1_temp.DDB         1           target_IZCREG1_temp.DDB				
target_J2cREG1_temp.MDR         7           target_J2cREG1_temp.WR         44           target_J2cREG1_temp.PDRC         2           target_J2cREG1_temp.PDSC         89           target_J2cREG1_temp.PDI11         577           target_J2cREG1_temp.PDIN2         89           target_J2cREG1_temp.DMAC         2           target_J2cREG1_temp.DIN         0           target_J2cREG1_temp.DIN         1           target_J2cREG1_temp.DIN         1           target_J2cREG1_temp.DCR         0           target_J2cREG1_temp.DCR         0           target_J2cREG1_temp.DCR         0           target_J2cREG1_temp.DDR         1           target_J2cREG1_temp.DDR         1           target_J2cREG1_temp.DDR         1           target_J2cREG1_temp.DDR         0           target_J2cREG1_temp.DDR         1           target_J2cREG1_temp.DBS.         0           Namo         Actual Value         Expected Value         Result           DjGcOPsint_Buffer_Cnt_M_u08(0)         3         3         4           DjGcOPsint_Buffer_Cnt_M_u08(1)         6         6         4           DjGcOPsint_Buffer_Cnt_M_u08(1)         6         6         4           DjGcOPsint_				
target_j2cREG1_temp_EMDR         2           target_j2cREG1_temp_PSC         89           target_j2cREG1_temp_PID11         577           target_j2cREG1_temp_PID12         89           target_j2cREG1_temp_DIDAC         2           target_j2cREG1_temp_DIR         0           target_j2cREG1_temp_DIN         1           target_j2cREG1_temp_DIN         1           target_j2cREG1_temp_DOT         2           target_j2cREG1_temp_DET         2           target_j2cREG1_temp_DOR         1           target_j2cREG1_temp_DD         2           target_j2cREG1_temp_DD         2           target_j2cREG1_temp_DS         0           Namo         Actual Value         Expected Value         Result           DigCoPsint_Buffer_Cnt_M_u08(0)         3         3         9           NgCoPsint_Buffer_Cnt_M_u08(1)         6         6         9           DigCoPsint_Buffer_Cnt_M_u08(1)         9         9         9           DigCoPsint_CurrentSlave_Cnt_M_u08         115         115         115           DigCoPsint_CurrentSlave_Cnt_M_u08         115         115         11           DigCoPsint_CurrentSlave_Cnt_M_u08         115         115         1           DigCoPsint_Naco		7		
target_ ZeREG1_temp.PID11   577	target_i2cREG1_temp.IVR	44		
target_l2cREG1_temp.PID11         577           target_l2cREG1_temp.PID12         89           target_l2cREG1_temp.DMC         2           target_l2cREG1_temp.DIR         0           target_l2cREG1_temp.DIR         1           target_l2cREG1_temp.DIN         1           target_l2cREG1_temp.DOUT         2           target_l2cREG1_temp.DOUT         2           target_l2cREG1_temp.DOR         0           target_l2cREG1_temp.DOR         1           target_l2cREG1_temp.PD         2           target_l2cREG1_temp.PSL         0           Name         Actual Value         Expected Value         Result           DigColPsint_Buffer_Ont_M_u08(0)         3         3         V           DigColPsint_Buffer_Cnt_M_u08(1)         6         6         V           DigColPsint_Buffer_Cnt_M_u08(2)         9         9         V           DigColPsint_CurrentSlave_Cnt_M_u08         115         115         V           DigColPsint_CurrentSlave_Cnt_M_u08         115         115         V           DigColPsint_CurrentSlave_Cnt_M_u08         115         115         N           DigColPsint_NotCourrentSlave_Cnt_M_u08         34         V           DigColPsint_NotCourrentSlave_Cnt_M_u08 <td< td=""><td>target_i2cREG1_temp.EMDR</td><td>2</td><td></td><td></td></td<>	target_i2cREG1_temp.EMDR	2		
target_!2cREG1_temp.PID12         89           target_!2cREG1_temp.DMAC         2           target_!2cREG1_temp.DIN         0           target_!2cREG1_temp.DIN         1           target_!2cREG1_temp.DOUT         2           target_!2cREG1_temp.DCR         2           target_!2cREG1_temp.DCR         0           target_!2cREG1_temp.DCR         1           target_!2cREG1_temp.DDR         1           target_!2cREG1_temp.DDR         2           target_!2cREG1_temp.PD         2           target_!2cREG1_temp.PSL         0           Name         Actual Value         Expected Value         Result           DigColPsint_Buffer_Cnt_M_u08[0]         3         3         3         9<				
target_!2cREG1_temp_DMAC         2           target_!2cREG1_temp_FUN         0           target_!2cREG1_temp_DIR         0           target_!2cREG1_temp_DOUT         1           target_!2cREG1_temp_DOUT         2           target_!2cREG1_temp_DET         2           target_!2cREG1_temp_ODR         1           target_!2cREG1_temp_PD         2           target_!2cREG1_temp_PD         2           Name         Actual Value         Expected Value         Result           DigColPsInt_Buffer_Cnt_M_u08[0]         3         3         V           DigColPsInt_Buffer_Cnt_M_u08[1]         6         6         V         V           DigColPsInt_Buffer_Cnt_M_u08[2]         9         9         V         V         V         D         V         D         V         D         V         D         V         D         V         D         V         V         D         V         D	· ·			
target_ 2cREG1_temp.FUN	0 =			
target_!2cREG1_temp.DIR         0           target_!2cREG1_temp.DIN         1           target_!2cREG1_temp.DOUT         2           target_!2cREG1_temp.CLR         0           target_!2cREG1_temp.DDR         1           target_!2cREG1_temp.DDR         1           target_!2cREG1_temp.PD         2           target_!2cREG1_temp.PSL         0           Name         Actual Value         Expected Value         Result           DigColPsInt_Buffer_Ont_M_u08[0]         3         3         ✓           DigColPsint_Buffer_Ont_M_u08[1]         6         6         ✓         ✓           DigColPsint_Buffer_Ont_M_u08[2]         9         9         ✓         ✓         DigColPsint_Buffer_Ont_M_u08[2]         9         9         ✓         DigColPsint_Dsurgen_Sequence_Cnt_M_u08         115         11         11         11         11         11         11         11         11         11         11         11         11         11 <td></td> <td></td> <td></td> <td></td>				
target_lzcREG1_temp.DIN         1           target_lzcREG1_temp.DOUT         2           target_lzcREG1_temp.SET         2           target_lzcREG1_temp.DCLR         0           target_lzcREG1_temp.DDR         1           target_lzcREG1_temp.PD         2           target_lzcREG1_temp.PSL         0           Name         Actual Value         Expected Value         Result           DigcolPsInt_Buffer_Cnt_M_u08[0]         3         3         V           DigcolPsInt_Buffer_Cnt_M_u08[1]         6         6         V         P				
target_i2cREG1_temp.DOUT         2           target_i2cREG1_temp.SET         2           target_i2cREG1_temp.DOR         1           target_i2cREG1_temp.DOR         1           target_i2cREG1_temp.PD         2           target_i2cREG1_temp.PSL         0           Name         Actual Value         Expected Value         Result           DigColPsInt_Buffer_Cnt_M_u08[0]         3         3         V           DigColPsInt_Buffer_Cnt_M_u08[1]         6         6         V           DigColPsInt_Buffer_Cnt_M_u08[2]         9         9         V           DigColPsInt_Buffer_Cnt_M_u08[2]         9         9         V           DigColPsInt_CurrentSlave_Cnt_M_u08         115         115         115         V           DigColPsInt_CurrentSlepNo_Cnt_M_enum         INIT_SENSOR1_READERROR_SETREG         INIT_SENSOR1_READERROR_SETREG         V         DigColPsInt_Init_BailedOnce_Cnt_M_lgc         0         0         0         V         DigColPsInt_NackOccured_Cnt_M_lgc         0         0         0         V         DigColPsInt_Readerror_Cnt_M_lgc         0         0         0         V         DigColPsInt_Readerror_Cnt_M_lgc         0         0         0         V         DigColPsInt_Readerror_Cnt_M_lgc         0         0         0	<b>0</b>			
target_i2cREG1_temp.CDR		2		
target_i2cREG1_temp.PDR	target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.PD         2           target_i2cREG1_temp.PSL         0           Name         Actual Value         Expected Value         Result           DigcolPsInt_Buffer_Cnt_M_u08[0]         3         3         3         3         3         9 <td< td=""><td>target_i2cREG1_temp.CLR</td><td>0</td><td></td><td></td></td<>	target_i2cREG1_temp.CLR	0		
Name				
Name         Actual Value         Expected Value         Result           DigColPsInt_Buffer_Cnt_M_u08[0]         3         3         4           DigColPsInt_Buffer_Cnt_M_u08[1]         6         6         4           DigColPsInt_Buffer_Cnt_M_u08[2]         9         9         9           DigColPsInt_Buffer_Cnt_M_u08[2]         9         9         9           DigColPsInt_Buffer_Cnt_M_u08[2]         0         0         0           DigColPsInt_Buffer_Cnt_M_u08         115         115         115           DigColPsInt_CurrentSlave_Cnt_M_u08         115         115         115           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR1_READERROR_SETREG         INIT_SENSOR1_READERROR_SETREG         V           DigColPsInt_GetData()         34         34         34         34           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0         0         0         0           DigColPsInt_NackOccured_Cnt_M_lgc         0         0         0         0           DigColPsInt_RecovoerrunError_Cnt_M_u08         42         42         42           DigColPsInt_Sensinitalized_Cnt_M_lgc         1         1         1           Larget_DatTypePtr_Cnt_T_u16         34282         34282         34282				
DigColPsInt_Buffer_Cnt_M_u08[0]   3   3   6   6     DigColPsInt_Buffer_Cnt_M_u08[1]   6   6   6     DigColPsInt_Buffer_Cnt_M_u08[2]   9   9   9     DigColPsInt_BusBusySeqError_Cnt_M_lgc   0   0   0     DigColPsInt_CurrentSlave_Cnt_M_u08   115   115     DigColPsInt_CurrentStepNo_Cnt_M_enum   INIT_SENSOR1_READERROR_SETREG   INIT_SENSOR1_READERROR_SETREG     DigColPsInt_GetData()   34   34   34   34     DigColPsInt_InitFailedOnce_Cnt_M_lgc   0   0   0   0     DigColPsInt_NackOccured_Cnt_M_lgc   0   0   0   0     DigColPsInt_PrevTransactionCnt_Cnt_M_u08   42   42   0     DigColPsInt_RecvOverrunError_Cnt_M_lgc   0   0   0   0     DigColPsInt_SensInitialized_Cnt_M_lgc   0   0   0     DigColPsInt_SensInitialized_Cnt_M_lgc   1   1   0     target_ColSnsrDataPtr_Cnt_T_u08   1   1   0     target_DataTypePtr_Cnt_T_str.OAR   65   65   0     target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR   89   89     target_I2c_Send_I2cRegPtr_Cnt_T_str.STR   67   67   0     DigColPsInt_DataTypePtr_Cnt_T_str.STR   67   67   0     DigColPsInt_DataTypePtr_Cnt_T_str.STR   67   67   0     DigColPsInt_SensInitialized_Cnt_T_str.STR   67   0     DigColPsInt_SensInitialized_Cnt_T_str.STR   67   0     DigColPsInt_SensInitialized_Cnt_T_str.STR   0   0     DigColPsInt_SensInitialized_Cn	_ · ·		I=	1
DigColPsInt_Buffer_Cnt_M_u08[1]         6         6           DigColPsInt_Buffer_Cnt_M_u08[2]         9         9           DigColPsInt_BusBusySeqError_Cnt_M_lgc         0         0           DigColPsInt_CurrentSlave_Cnt_M_u08         115         115           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR1_READERROR_SETREG         INIT_SENSOR1_READERROR_SETREG           DigColPsInt_GetData()         34         34           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0         0           DigColPsInt_NackOccured_Cnt_M_lgc         0         0           DigColPsInt_PrevTransactionCnt_Cnt_M_u08         42         42           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0           DigColPsInt_Sensinitialized_Cnt_M_lgc         0         0           DigColPsInt_Sensinitialized_Cnt_M_lgc         1         1           Target_ColSnsrDataPtr_Cnt_T_u16         34282         34282           Target_DataTypePtr_Cnt_T_u08         1         1           Target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR         65         65           Target_I2c_Send_I2cRegPtr_Cnt_T_str.STR         67         67			· ·	Result
DigColPsInt_Buffer_Cnt_M_u08[2]         9         9           DigColPsInt_BusBusySeqError_Cnt_M_u08         0         0           DigColPsInt_CurrentSlave_Cnt_M_u08         115         115           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR1_READERROR_SETREG         INIT_SENSOR1_READERROR_SETREG           DigColPsInt_GetData()         34         34           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0         0           DigColPsInt_NackOccured_Cnt_M_lgc         0         0           DigColPsInt_PrevTransactionCnt_Cnt_M_u08         42         42           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0           DigColPsInt_SensInitialized_Cnt_M_lgc         1         1           DigColSnsrDataPtr_Cnt_T_u16         34282         34282           target_DataTypePtr_Cnt_T_u08         1         1           target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR         65         65           target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR         89         89           target_I2c_Send_I2cRegPtr_Cnt_T_str.STR         67         67				-
DigColPsInt_BusBusySeqError_Cnt_M_lgc         0         0           DigColPsInt_CurrentSlave_Cnt_M_u08         115         115           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR1_READERROR_SETREG         INIT_SENSOR1_READERROR_SETREG           DigColPsInt_GetData()         34         34           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0         0           DigColPsInt_NackOccured_Cnt_M_lgc         0         0           DigColPsInt_PrevTransactionCnt_Cnt_M_u08         42         42           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0           DigColPsInt_SensInitialized_Cnt_M_lgc         1         1           DigColSnsrDataPtr_Cnt_T_u16         34282         34282           target_DataTypePtr_Cnt_T_u08         1         1           target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR         65         65           target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR         89         89           target_I2c_Send_I2cRegPtr_Cnt_T_str.STR         67         67				
DigColPsInt_CurrentSlave_Cnt_M_u08         115         115           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_SENSOR1_READERROR_SETREG         INIT_SENSOR1_READERROR_SETREG           DigColPsInt_GetData()         34         34           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0         0           DigColPsInt_NackOccured_Cnt_M_lgc         0         0           DigColPsInt_PrevTransactionCnt_Cnt_M_u08         42         42           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0           DigColPsInt_SensInitialized_Cnt_M_lgc         1         1           DigColSnsrDataPtr_Cnt_T_u16         34282         34282           target_DataTypePtr_Cnt_T_u08         1         1           target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR         65         65           target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR         89         89           target_I2c_Send_I2cRegPtr_Cnt_T_str.STR         67         67		-		<b>~</b>
DigColPsInt_GetData()       34       34       34         DigColPsInt_InitFailedOnce_Cnt_M_Igc       0       0       0         DigColPsInt_NackOccured_Cnt_M_Igc       0       0       0         DigColPsInt_PrevTransactionCnt_Cnt_M_u08       42       42       42         DigColPsInt_RecvOverrunError_Cnt_M_Igc       0       0       0         DigColPsInt_SensInitialized_Cnt_M_Igc       1       1       4         target_ColSnsrDataPtr_Cnt_T_u16       34282       34282       34282       4         target_DataTypePtr_Cnt_T_u08       1       1       1       4         target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR       65       65       4         target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR       89       89       89         target_I2c_Send_I2cRegPtr_Cnt_T_str.STR       67       67       4				~
DigColPsInt_InitFailedOnce_Cnt_M_lgc         0         0           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0         0           DigColPsInt_PrevTransactionCnt_Cnt_M_u08         42         42           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0           DigColPsInt_SensInitialized_Cnt_M_lgc         1         1           target_ColSnsrDataPtr_Cnt_T_u16         34282         34282           target_DataTypePtr_Cnt_T_u08         1         1           target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR         65         65           target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR         89         89           target_l2c_Send_l2cRegPtr_Cnt_T_str.STR         67         67		INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	•
DigColPsInt_NackOccured_Cnt_M_lgc         0         0         ✓           DigColPsInt_PrevTransactionCnt_Cnt_M_u08         42         42         ✓           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0         ✓           DigColPsInt_SensInitialized_Cnt_M_lgc         1         1         ✓           target_ColSnsrDataPtr_Cnt_T_u16         34282         34282         ✓           target_DataTypePtr_Cnt_T_u08         1         1         1         ✓           target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR         65         65         ✓         ✓           target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR         89         89         ✓         ✓           target_l2c_Send_l2cRegPtr_Cnt_T_str.STR         67         67         ✓         ✓	DigColPsInt_GetData()			-
DigColPsInt_PrevTransactionCnt_Cnt_M_u08       42       42       42         DigColPsInt_RecvOverrunError_Cnt_M_lgc       0       0       ✓         DigColPsInt_SensInitialized_Cnt_M_lgc       1       1       ✓         target_ColSnsrDataPtr_Cnt_T_u16       34282       34282       ✓         target_DataTypePtr_Cnt_T_u08       1       1       ✓         target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR       65       65       ✓         target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR       89       89       ✓         target_I2c_Send_I2cRegPtr_Cnt_T_str.STR       67       67       ✓				<b>~</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc         0         0         ✓           DigColPsInt_SensInitialized_Cnt_M_lgc         1         1         ✓           target_ColSnsrDataPtr_Cnt_T_u16         34282         34282         ✓           target_DataTypePtr_Cnt_T_u08         1         1         1         ✓           target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR         65         65         ✓           target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR         89         89         ✓           target_l2c_Send_l2cRegPtr_Cnt_T_str.STR         67         67         ✓			1	-
DigColPsInt_SensInitialized_Cnt_M_lgc         1         1         ✓           target_ColSnsrDataPtr_Cnt_T_u16         34282         34282         ✓           target_DataTypePtr_Cnt_T_u08         1         1         ✓           target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR         65         65         ✓           target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR         89         89         ✓           target_l2c_Send_l2cRegPtr_Cnt_T_str.STR         67         67         ✓				
target_ColSnsrDataPtr_Cnt_T_u16       34282       34282         target_DataTypePtr_Cnt_T_u08       1       1         target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR       65       65         target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR       89       89         target_l2c_Send_l2cRegPtr_Cnt_T_str.STR       67       67			1.	-
target_DataTypePtr_Cnt_T_u08       1       1         target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR       65       65         target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR       89       89         target_l2c_Send_l2cRegPtr_Cnt_T_str.STR       67       67				
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR       65       65         target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR       89       89         target_I2c_Send_I2cRegPtr_Cnt_T_str.STR       67       67				· ·
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR 89 89 47 4arget_l2c_Send_l2cRegPtr_Cnt_T_str.STR 67 67	·			~
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR 67				<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL 7	target_I2c_Send_I2cRegPtr_Cnt_T_str.STR			~
	target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	~

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	89	89	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	89	89	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	7	7	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	89	89	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	2	2	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	89	89	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	577	577	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	1	1	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	0	0	
target_SpurSnsrDataPtr_Cnt_T_u16	26371	26371	

T .				
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime mS u16	1	DtrmnElapsedTime mS u16	1	_

Test Step 2.33 (Repeat Count = 1)		V
Name	Input Value	
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16	
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08	
DigColPsInt_Buffer_Cnt_M_u08[0]	11	
DigColPsInt_Buffer_Cnt_M_u08[1]	22	
DigColPsInt_Buffer_Cnt_M_u08[2]	33	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	
DigColPsInt_ColSnsrData_Cnt_M_u16	37072	
DigColPsInt_CurrentSlave_Cnt_M_u08	122	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ	
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	
DigColPsInt_InitialTime_mS_M_u32	37574861	
DigColPsInt_NackOccured_Cnt_M_lgc	1	
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	59	
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	
DigColPsInt_RecvdDataType_Cnt_M_u08	2	







Name	Input Value				
target_i2cREG1_temp.IVR	5				
target_i2cREG1_temp.EMDR	3				
target_i2cREG1_temp.PSC	66				
target_i2cREG1_temp.PID11	1204				
target_i2cREG1_temp.PID12	66				
target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN	3				
target_i2cREG1_temp.DIR	1				
target i2cREG1 temp.DIN	2				
target_i2cREG1_temp.DOUT	3				
target_i2cREG1_temp.SET	3				
target_i2cREG1_temp.CLR	1				
target_i2cREG1_temp.ODR	2				
target_i2cREG1_temp.PD	3				
target_i2cREG1_temp.PSL	3	1	1-		
Name	Actual Value	Expected Value	Result		
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	<b>→</b>		
DigColPoint_Buffer_Cnt_M_u08[1]	22 33	33	<b>*</b>		
DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0			
DigColPsInt CurrentSlave Cnt M u08	84	84			
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	·		
DigColPsInt GetData()	6	6	-		
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	•		
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~		
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	46	46	~		
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~		
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	~		
I2c_Send(Length_Cnt_T_u32)	1	1	~		
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~		
target_ColSnsrDataPtr_Cnt_T_u16	37072	37072	~		
target_DataTypePtr_Cnt_T_u08	2	2	~		
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>✓</b>		
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66 556	556	,		
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	-		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	-		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>		
target I2c Send I2cRegPtr Cnt T str.DRR	67	67	-		
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	~		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	~		
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•		
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	~		
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	~		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	~		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>Y</b>		
target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	3	1	Ž		
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1			
target I2c Send I2cRegPtr Cnt T str.DIN	2	2			
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	-		
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3			
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	•		
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	~		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	~		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	~		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	~		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	~		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	~		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>✓</b>		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204 87			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	87 67	67	-		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	55	55	-		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	·		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	-		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	-		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~		

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✓
target_SpurSnsrDataPtr_Cnt_T_u16	27070	27070	✓

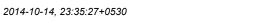
T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	~
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	~

Test Step 2.34 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
ColSnsrDataPtr Cnt T u16	target ColSnsrDataPtr Cnt T u16
DataTypePtr Cnt T u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt Buffer Cnt M u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt Buffer Cnt M u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt CmdFailOccurred Cnt M Igc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	39862
DigColPsInt CurrentSlave Cnt M u08	1
DigColPsInt CurrentStepNo Cnt M enum	INIT SENSOR2 READERROR READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	38577613
DigColPsInt NackOccured Cnt M Igc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	65
DigColPsInt RecvOverrunError Cnt M Igc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt SensInitialized Cnt M Igc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	27769
DigColPsInt TransactionCnt Cnt M u08	50
DtrmnElapsedTime mS u16(ElapsedTime)	target DtrmnElapsedTime mS u16 ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
l2c Send(l2cRegPtr Cnt T str)	target I2c Send I2cRegPtr Cnt T str
I2c SetupMasterTransmit(I2cRegPtr Cnt T str)	target I2c SetupMasterTransmit I2cRegPtr Cnt T str
SpurSnsrDataPtr Cnt T u16	target SpurSnsrDataPtr Cnt T u16
i2cREG1 temp	target i2cREG1 temp
k_ColSensorl2CAddress_Cnt_u08	91
k I2CHWInitTransactionTime Sec f32	3.099999
target DtrmnElapsedTime mS u16 ElapsedTime	14789
target GetSystemTime mS u32 CurrentTime	34566605
target I2c Send I2cRegPtr Cnt T str.OAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
target I2c Send I2cRegPtr Cnt T str.STR	78
target I2c Send I2cRegPtr Cnt T str.CLKL	495
target I2c Send I2cRegPtr Cnt T str.CLKH	56
target I2c Send I2cRegPtr Cnt T str.CNT	897
target I2c Send I2cRegPtr Cnt T str.DRR	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
target I2c Send I2cRegPtr Cnt T str.DXR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
target I2c Send I2cRegPtr Cnt T str.IVR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target I2c Send I2cRegPtr Cnt T str.PSC	78
target I2c Send I2cRegPtr_Cnt_T_str.PSC	56
target I2c Send I2cRegPtr_Cnt_T_str.PiD11	78
target I2c Send I2cRegPtr_Cnt_T_str.PiD12	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.DWAC	0
	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	1
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	0
angur_120_00110_120100gt tt_O11t_1_3tt.D001	

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Name	Input Value		
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	0		
target_I2C_Send_I2CRegPtr_Cnt_T_str.ODR	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	495		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	56 897		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	98		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56   78		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	0		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL target_i2cREG1_temp.OAR	66		
target_i2cREG1_temp.IMR	78		
target i2cREG1 temp.STR	78		
target_i2cREG1_temp.CLKL	495		
target_i2cREG1_temp.CLKH	56		
target_i2cREG1_temp.CNT	897		
target_i2cREG1_temp.DRR	98		
target_i2cREG1_temp.SAR	66		
target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR	78 495		
target i2cREG1 temp.IVR	66		
target i2cREG1 temp.EMDR	0		
target_i2cREG1_temp.PSC	78		
target_i2cREG1_temp.PID11	56		
target_i2cREG1_temp.PID12	78		
target_i2cREG1_temp.DMAC	0		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN	0		
target i2cREG1 temp.DOUT	0		
target i2cREG1 temp.SET	0		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	~
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc	30 0	30	<b>✓</b>
DigColPsInt_BusBusySeqError_Cnt_M_igc  DigColPsInt CurrentSlave Cnt M u08	1	1	-
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR2 READERROR READ	INIT SENSOR2 READERROR READ	~
DigColPsInt_GetData()	168	168	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	50	50	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	<b>V</b>
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	<b>V</b>
target_ColSnsrDataPtr_Cnt_T_u16	39862	39862	<b>✓</b>
target_DataTypePtr_Cnt_T_u08 target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3 66	3 66	~
target_I2c_Send_I2cRegPtr_Cnt_1_str.UAR target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.NTR	78	78	-
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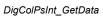




Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>
target_SpurSnsrDataPtr_Cnt_T_u16	27769	27769	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	<b>✓</b>

Test Step 2.35 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	40
DigColPsInt_Buffer_Cnt_M_u08[1]	50
DigColPsInt_Buffer_Cnt_M_u08[2]	60
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	34282
DigColPsInt_CurrentSlave_Cnt_M_u08	115
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0
DigColPsInt_InitialTime_mS_M_u32	39580365
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	53
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0





Name	Input Value
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	26371
DigColPsInt_TransactionCnt_Cnt_M_u08	42
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08 k_I2CHWInitTransactionTime_Sec_f32	0 2.2999995
target_DtrmnElapsedTime_mS_u16_ElapsedTime	18975
target_GetSystemTime_mS_u32_CurrentTime	35569357
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65
target I2c Send I2cRegPtr Cnt T str.IMR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44 2
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR target_l2c Send_l2cRegPtr_Cnt_T str.PSC	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	1
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	65 89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	44
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	2 0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_I_str.FUN target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	65
target_i2cREG1_temp.IMR	89
target_i2cREG1_temp.STR	67
target_i2cREG1_temp.CLKL	7
target_i2cREG1_temp.CLKH	577 88
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	88
target_i2cREG1_temp.SAR	65
target_i2cREG1_temp.DXR	89
J	

DigColPsInt\_GetData





Name	Input Value		
target_i2cREG1_temp.MDR	7		
target_i2cREG1_temp.IVR	44		
target_i2cREG1_temp.EMDR	2		
target_i2cREG1_temp.PSC	89		
target_i2cREG1_temp.PID11	577		
target_i2cREG1_temp.PID12	89		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT	2		
target i2cREG1 temp.SET	2		
target_i2cREG1_temp.CLR	0		
target i2cREG1 temp.ODR	1		
target_i2cREG1_temp.PD	2		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt Buffer Cnt M u08[0]	40	40	~
DigColPsInt_Buffer_Cnt_M_u08[1]	50	50	~
DigColPsInt_Buffer_Cnt_M_u08[2]	60	60	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt_CurrentSlave_Cnt_M_u08	115	115	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	~
DigColPsInt_GetData()	162	162	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	42	42	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_Igc	1	1	~
target_ColSnsrDataPtr_Cnt_T_u16	34282	34282	<b>Y</b>
target_DataTypePtr_Cnt_T_u08	1	1	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	65 89	65 89	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	7	7	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	<b>Y</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>Y</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	-
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	1	1	
target_12c_Send_12cRegPti_Cnt_T_str.DUT	2	2	-
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	2	2	J
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	<b>V</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	2	2	· ·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	577	577	Ž
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	-
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	2	2	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✓
target_SpurSnsrDataPtr_Cnt_T_u16	26371	26371	<b>✓</b>

T				V
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

Test Step 2.36 (Repeat Count = 1)	✓
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target ColSnsrDataPtr Cnt T u16
DataTypePtr Cnt T u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt Buffer Cnt M u08[0]	70
DigColPsInt_Buffer_Cnt_M_u08[1]	80
DigColPsInt_Buffer_Cnt_M_u08[2]	90
DigColPsInt BusBusySeqError Cnt M Igc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	37072
DigColPsInt CurrentSlave Cnt M u08	122
DigColPsInt CurrentStepNo Cnt M enum	INIT SENSOR1 CHECKSTAT READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	40583117
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt PrevTransactionCnt Cnt M u08	59
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt SpurSnsrData Cnt M u16	27070
DigColPsInt_TransactionCnt_Cnt_M_u08	46
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target I2c Send I2cRegPtr Cnt T str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr Cnt T u16	target SpurSnsrDataPtr Cnt T u16
i2cREG1_temp	target_i2cREG1_temp
k ColSensorl2CAddress Cnt u08	127
k I2CHWInitTransactionTime Sec f32	2.70000005
target_DtrmnElapsedTime_mS_u16_ElapsedTime	21458
target GetSystemTime mS u32 CurrentTime	36572109
target I2c Send I2cRegPtr Cnt T str.OAR	55
target I2c Send I2cRegPtr Cnt T str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target I2c Send I2cRegPtr Cnt T str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target I2c Send I2cRegPtr Cnt T str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3

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Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	1204 66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	2		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_1_str.ODR	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3		
target_i2cREG1_temp.OAR	55		
target_i2cREG1_temp.IMR	66		
target i2cREG1 temp.STR	556		
target_i2cREG1_temp.CLKL	2309		
target_i2cREG1_temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target i2cREG1 temp.DRR	67		
target i2cREG1 temp.SAR	55		
target i2cREG1 temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target i2cREG1 temp.IVR	5		
target i2cREG1 temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target i2cREG1 temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Resu
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	
DigColPsInt_Buffer_Cnt_M_u08[1]	80	80	
DigColPsInt_Buffer_Cnt_M_u08[2]	90	90	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	
DigColPsInt_GetData()	6	6	
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	46	46	
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	
I2c_Send(Length_Cnt_T_u32)	1	1	
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	
target_ColSnsrDataPtr_Cnt_T_u16	37072	37072	
target_DataTypePtr_Cnt_T_u08	2	2	
tangot_bata i yper ti_Ont_i_uuo	2	1	
	55	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR		55 66	
target_bata1ypertr_cht_1_uu8 target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	55		
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	55 66	66	
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	55 66 556	66 556	





Name	Actual Value	Expected Value	Result
target I2c Send I2cRegPtr Cnt T str.DRR	67	67	~
target I2c Send I2cRegPtr Cnt T str.SAR	55	55	•
target I2c Send I2cRegPtr Cnt T str.DXR	66	66	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target I2c Send I2cRegPtr Cnt T str.EMDR	3	3	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_SpurSnsrDataPtr_Cnt_T_u16	27070	27070	~

<b>T</b> ✓				
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	•
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	<b>✓</b>
GetSystemTime mS u32	1	GetSystemTime mS u32	1	_

Test Step 2.37 (Repeat Count = 1)	
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	44
DigColPsInt_Buffer_Cnt_M_u08[1]	55
DigColPsInt_Buffer_Cnt_M_u08[2]	66
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	39862
DigColPsInt_CurrentSlave_Cnt_M_u08	1
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	41585869
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	65





Name	Input Value	
DigColPsInt_RecvOverrunError_Cnt_M_Igc	1	
DigColPsInt_RecvdDataType_Cnt_M_u08	3	
DigColPsInt_SensInitialized_Cnt_M_lgc	1	
DigColPsInt_SpurSnsrData_Cnt_M_u16	27769	
DigColPsInt_TransactionCnt_Cnt_M_u08	50	
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime	
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime	
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str	
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str) SpurSnsrDataPtr Cnt T u16	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str	
i2cREG1_temp	target_SpurSnsrDataPtr_Cnt_T_u16 target_i2cREG1_temp	
k_ColSensorI2CAddress_Cnt_u08	91	
k_I2CHWInitTransactionTime_Sec_f32	3.0999999	
target_DtrmnElapsedTime_mS_u16_ElapsedTime	14789	
target_GetSystemTime_mS_u32_CurrentTime	37574861	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	78	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	1 0	
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
target I2c Send I2cRegPtr Cnt T str.PD	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	0	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	0 0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	0	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	
target_i2cREG1_temp.OAR	66	
target_i2cREG1_temp.IMR	78	
target_i2cREG1_temp.STR	78	
target_i2cREG1_temp.CLKL	495	
target_i2cREG1_temp.CLKH	56	
target_i2cREG1_temp.CNT	897	
target_i2cREG1_temp.DRR	98	
	66	

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3.1. 1. 2.1.1.			
Name	Input Value		
target_i2cREG1_temp.DXR	78		
target_i2cREG1_temp.MDR	495		
target_i2cREG1_temp.IVR	66		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	78		
target_i2cREG1_temp.PID11	56		
target_i2cREG1_temp.PID12	78		
target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN	0		
target i2cREG1_temp.DIR	0		
target i2cREG1 temp.DIN	1		
target_i2cREG1_temp.DOUT	0		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target i2cREG1 temp.PD	0		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	44	44	~
DigColPsInt_Buffer_Cnt_M_u08[1]	55	55	•
DigColPsInt_Buffer_Cnt_M_u08[2]	66	66	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	•
DigColPsInt_CurrentSlave_Cnt_M_u08	1	1	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_READ	INIT_SENSOR2_READERROR_READ	•
DigColPsInt_GetData()	168	168	•
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1	1	•
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	50	50	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	~
target_ColSnsrDataPtr_Cnt_T_u16	39862	39862	~
target_DataTypePtr_Cnt_T_u08	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	78	78	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC target_l2c Send_l2cRegPtr_Cnt_T str.PID11	78	78 56	-
· ·	56   78	78	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12 target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	0	0	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	
target I2c Send I2cRegPtr Cnt T str.DIR	0	0	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	•
target I2c Send I2cRegPtr Cnt T str.SET	0	0	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	~

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✓
target_SpurSnsrDataPtr_Cnt_T_u16	27769	27769	✓

T				V
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

Test Step 2.38 (Repeat Count = 1)	
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt Buffer Cnt M u08[0]	3
DigColPsInt_Buffer_Cnt_M_u08[1]	6
DigColPsInt Buffer Cnt M u08[2]	9
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	34282
DigColPsInt_CurrentSlave_Cnt_M_u08	115
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR1 READERROR SETREG
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	42588621
DigColPsInt_NackOccured_Cnt_M_lgc	1
	53
DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
	1
DigColPsInt_RecvdDataType_Cnt_M_u08	
DigColPsInt_SensInitialized_Cnt_M_lgc	0 26371
DigColPsInt_SpurSnsrData_Cnt_M_u16	
DigColPsInt_TransactionCnt_Cnt_M_u08	42
OtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
SetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
2cREG1_temp	target_i2cREG1_temp
ColSensorI2CAddress_Cnt_u08	77
c_I2CHWInitTransactionTime_Sec_f32	2.29999995
arget_DtrmnElapsedTime_mS_u16_ElapsedTime	9360
arget_GetSystemTime_mS_u32_CurrentTime	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
arget I2c Send I2cRegPtr Cnt T str.PSC	89
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
arget I2c Send I2cRegPtr Cnt T str.DIR	0
	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2 2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
arget_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2





Name	Input Value		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67		
	7		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	577		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
target_i2cREG1_temp.OAR	65		
target_i2cREG1_temp.IMR	89		
target i2cREG1 temp.STR	67		
	7		
target_i2cREG1_temp.CLKL			
target_i2cREG1_temp.CLKH	577		
target_i2cREG1_temp.CNT	88		
target_i2cREG1_temp.DRR	23		
target_i2cREG1_temp.SAR	65		
target_i2cREG1_temp.DXR	89		
target_i2cREG1_temp.MDR	7		
target_i2cREG1_temp.IVR	44		
target_i2cREG1_temp.EMDR	2		
target_i2cREG1_temp.PSC	89		
target i2cREG1 temp.PID11	577		
target i2cREG1 temp.PID12	89		
target i2cREG1 temp.DMAC	2		
0	0		
target_i2cREG1_temp.FUN			
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	2		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	-100011
DigColPsInt Buffer Cnt M u08[1]	6	6	~
	9	9	
DigColPsInt_Buffer_Cnt_M_u08[2]			<b>*</b>
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	
DigColPsInt_CurrentSlave_Cnt_M_u08	77	77	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	~
DigColPsInt_GetData()	34	34	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	42	42	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	•
I2c_Send(Length_Cnt_T_u32)	1	1	-
	1	1	· ·
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)			
target_ColSnsrDataPtr_Cnt_T_u16	34282	34282	<b>V</b>
target_DataTypePtr_Cnt_T_u08	1	1	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	<b>✓</b>





Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>~</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	0	0	· ·
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	1	1	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	2	2	· ·
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	2	2	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0	0	<b>V</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	1	1	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	2	2	<b>Y</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	0	0	.4
target_SpurSnsrDataPtr_Cnt_T_u16	26371	26371	✓

T ✓			V	
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	<b>✓</b>
GetSystemTime mS u32	1	GetSystemTime mS u32	1	<b>✓</b>

Test Step 2.39 (Repeat Count = 1)	✓
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	11
DigColPsInt_Buffer_Cnt_M_u08[1]	22
DigColPsInt_Buffer_Cnt_M_u08[2]	33
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	37072
DigColPsInt_CurrentSlave_Cnt_M_u08	122
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	43591373
DigColPsInt_NackOccured_Cnt_M_lgc	1





Name	Input Value
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	59
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	27070
DigColPsInt_TransactionCnt_Cnt_M_u08	46
OtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
2cREG1_temp	target_i2cREG1_temp
C_ColSensorI2CAddress_Cnt_u08	84
x_I2CHWInitTransactionTime_Sec_f32	2.70000005
arget_DtrmnElapsedTime_mS_u16_ElapsedTime	9867
arget_GetSystemTime_mS_u32_CurrentTime	4294967295
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1.
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
arget_i2cREG1_temp.OAR	55
arget i2cREG1 temp.IMR	66
	556
arget_i2cREG1_temp.STR	
arget_i2cREG1_temp.STR arget_i2cREG1_temp.CLKL	2309
arget_i2cREG1_temp.STR	

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Name	Input Value		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target i2cREG1 temp.IVR	5		
target i2cREG1 temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
	3		
target_i2cREG1_temp.DMAC			
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	•
DigColPsInt_Buffer_Cnt_M_u08[1]	22	22	•
DigColPsInt_Buffer_Cnt_M_u08[2]	33	33	~
DigColPsInt_BusBusySeqError_Cnt_M_Igc	0	0	~
DigColPsInt_CurrentSlave_Cnt_M_u08	84	84	~
DigColPsInt CurrentStepNo Cnt M enum	INIT SENSOR1 READERROR SETREG	INIT_SENSOR1_READERROR_SETREG	•
DigColPsInt_GetData()	6	6	_
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	-
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	46	46	•
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	-
	1	1	~
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	
I2c_Send(Length_Cnt_T_u32)			-
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	
target_ColSnsrDataPtr_Cnt_T_u16	37072	37072	•
target_DataTypePtr_Cnt_T_u08	2	2	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	55	55	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	-
		66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66		~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	66	66	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	5	5	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	66	66	<b>~</b>

DigColPsInt\_GetData



Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_SpurSnsrDataPtr_Cnt_T_u16	27070	27070	~

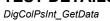
T				V
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	•
I2c_SetupMasterTransmit	1	l2c_SetupMasterTransmit	1	~
I2c_Send	1	l2c_Send	1	•
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	•

Test Step 2.40 (Repeat Count = 1)	
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt Buffer Cnt M u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt BusBusySeqError Cnt M lgc	0
DigColPsInt CmdFailOccurred Cnt M lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	39862
DigColPsInt_CurrentSlave_Cnt_M_u08	1
DigColPsInt CurrentStepNo Cnt M enum	INIT SENSOR2 READERROR READ
DigColPsInt InitFailedOnce Cnt M Igc	1
DigColPsInt_InitialTime_mS_M_u32	44594125
DigColPsint_InitialTime_ms_M_usz DigColPsint_NackOccured_Cnt_M_lgc	0
DigColPsInt_NackOccured_Crit_M_igc  DigColPsInt_PrevTransactionCnt_Cnt_M_u08	65
DigColPsInt_PrevTransactionCnt_Cnt_M_u06 DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvOverrunErrol_Cnt_M_igc  DigColPsInt RecvdDataType Cnt M u08	3
DigColPsInt SensInitialized Cnt M Igc	0
DigColPsInt SpurSnsrData Cnt M u16	27769
DigColPsInt_TransactionCnt_Cnt_M_u08	50
Digeon-sini_mansactionent_ent_in_uos  DtrmnElapsedTime mS u16(ElapsedTime)	target DtrmnElapsedTime mS u16 ElapsedTime
GetSystemTime mS u32(CurrentTime)	target GetSystemTime mS u32 CurrentTime
· · ·	
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp 91
k_ColSensorl2CAddress_Cnt_u08	3.099999
k_I2CHWInitTransactionTime_Sec_f32	
target_DtrmnElapsedTime_mS_u16_ElapsedTime	10374
target_GetSystemTime_mS_u32_CurrentTime	1478524
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	66
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	78
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	78
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0

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Name	Input Value		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0		
target I2c Send I2cRegPtr Cnt T str.DIN	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78 495		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	56		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	897		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_I_str.FUN target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
target_i2cREG1_temp.OAR	66		
target_i2cREG1_temp.IMR	78		
target_i2cREG1_temp.STR	78		
target_i2cREG1_temp.CLKL	495		
target_i2cREG1_temp.CLKH target_i2cREG1_temp.CNT	56   897		
target i2cREG1_temp.DRR	98		
target i2cREG1 temp.SAR	66		
target i2cREG1 temp.DXR	78		
target_i2cREG1_temp.MDR	495		
target_i2cREG1_temp.IVR	66		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	78		
target_i2cREG1_temp.PID11	56		
target_i2cREG1_temp.PID12	78		
target_i2cREG1_temp.DMAC	0		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN	0		
target i2cREG1 temp.DOUT	0		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	~
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	~
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt_CurrentSlave_Cnt_M_u08	91	91	<b>V</b>
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG 40	INIT_SENSOR1_READERROR_SETREG 40	<b>*</b>
DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_IntrailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc	0	0	
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	50	50	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	-
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	~
I2c_Send(Length_Cnt_T_u32)	1	1	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~





Name	Actual Value	Expected Value	Result
target_ColSnsrDataPtr_Cnt_T_u16	39862	39862	~
target_DataTypePtr_Cnt_T_u08	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target I2c Send I2cRegPtr Cnt T str.DOUT	0	0	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.SET	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_SpurSnsrDataPtr_Cnt_T_u16	27769	27769	•

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	•
GetSystemTime mS u32	1	GetSvstemTime mS u32	1	_

Test Step 2.41 (Repeat Count = 1)		<b>✓</b>
Name	Input Value	
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16	
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08	
DigColPsInt_Buffer_Cnt_M_u08[0]	0	
DigColPsInt_Buffer_Cnt_M_u08[1]	0	
DigColPsInt_Buffer_Cnt_M_u08[2]	0	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	





Name	Input Value
DigColPsInt_CmdFailOccurred_Cnt_M_Igc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	0
DigColPsInt_CurrentSlave_Cnt_M_u08	0
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT NOT INITIALIZED
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	0
DigColPsInt_NackOccured_Cnt_M_Igc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	0
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt SensInitialized Cnt M Igc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	0
	0
DigColPsInt_TransactionCnt_Cnt_M_u08	
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	0
	0
k_I2CHWInitTransactionTime_Sec_f32	
target_DtrmnElapsedTime_mS_u16_ElapsedTime	0
target_GetSystemTime_mS_u32_CurrentTime	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	0
	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target I2c Send I2cRegPtr Cnt T str.DIN	0
target I2c Send I2cRegPtr Cnt T str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	0
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	0
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	0
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	0
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	0
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	0
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			111111111111
Name	Input Value		
target_i2cREG1_temp.OAR	0		
target_i2cREG1_temp.IMR	0		
target_i2cREG1_temp.STR	0		
target_i2cREG1_temp.CLKL target_i2cREG1_temp.CLKH	0		
target_i2cREG1_temp.CNT	0		
target i2cREG1 temp.DRR	0		
target_i2cREG1_temp.SAR	0		
target_i2cREG1_temp.DXR	0		
target_i2cREG1_temp.MDR	0		
target_i2cREG1_temp.IVR	0		
target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC	0		
target_i2cREG1_temp.PID11	0		
target i2cREG1 temp.PID12	0		
target_i2cREG1_temp.DMAC	0		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	0		
target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	0	0	~
DigColPsInt_Buffer_Cnt_M_u08[1]	0	0	<b>V</b>
DigColPoint_Buffer_Cnt_M_u08[2]	0	0	<i>-</i>
DigColPsInt_BusBusySeqError_Cnt_M_Igc DigColPsInt_CurrentSlave_Cnt_M_u08	0	0	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT NOT INITIALIZED	INIT NOT INITIALIZED	·
DigColPsInt_GetData()	0	0	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	•
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	0	0	<b>Y</b>
DigColPsInt_RecvOverrunError_Cnt_M_Igc	0	0	<i>-</i>
DigColPsInt_SensInitialized_Cnt_M_lgc target_ColSnsrDataPtr_Cnt_T_u16	0	0	
target_DataTypePtr_Cnt_T_u08	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	0	0	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	0	0	· · · · · · · · · · · · · · · · · · ·
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	0	0	·
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>Y</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11 target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	0	0	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	0	0	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	0	0	<b>✓</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	0	0	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	0	0	
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.SAR	0	0	
		'	

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	0	0	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_SpurSnsrDataPtr_Cnt_T_u16	0	0	~

T				V
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

Test Step 2.42 (Repeat Count = 1)	
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	255
DigColPsInt_Buffer_Cnt_M_u08[1]	255
DigColPsInt_Buffer_Cnt_M_u08[2]	255
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	65535
DigColPsInt_CurrentSlave_Cnt_M_u08	127
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	4294967295
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	255
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	65535
DigColPsInt_TransactionCnt_Cnt_M_u08	255
OtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
2cREG1_temp	target_i2cREG1_temp
ColSensorl2CAddress_Cnt_u08	127
c_I2CHWInitTransactionTime_Sec_f32	10
arget_DtrmnElapsedTime_mS_u16_ElapsedTime	65535
arget_GetSystemTime_mS_u32_CurrentTime	4294967295
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	255
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	32767
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	65535
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	65535
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	255
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	1023
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	255
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	65535
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	4095
arget_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	255
arget_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	65535
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	255
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3

DigColPsInt\_GetData





Name	Input Value		
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3		
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3		
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3		
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	1023		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	255		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	32767		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	65535		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	65535		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	65535		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	255		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	1023		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	255 65535		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	4095		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	255		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	65535		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	255		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	1023		
target_i2cREG1_temp.IMR	255		
target_i2cREG1_temp.STR	32767		
target_i2cREG1_temp.CLKL target_i2cREG1_temp.CLKH	65535 65535		
target_i2cREG1_temp.CNT	65535		
target i2cREG1 temp.DRR	255		
target_i2cREG1_temp.SAR	1023		
target_i2cREG1_temp.DXR	255		
target_i2cREG1_temp.MDR	65535		
target_i2cREG1_temp.IVR	4095		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11	255 65535		
target_i2cREG1_temp.PID12	255		
target i2cREG1 temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	3		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	3		
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	255	255	~
DigColPsInt_Buffer_Cnt_M_u08[1]	255	255	~
DigColPsInt_Buffer_Cnt_M_u08[2]	255	255	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	<b>~</b>
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	<b>V</b>
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE	READ_COMPLETE	<b>V</b>
DigColPsInt_GetData()	62 1	62 1	<b>→</b>
DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc	0	0	<b>*</b>
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	255	255	· ·
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	~
target_ColSnsrDataPtr_Cnt_T_u16	65535	65535	~
	1		

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Name	Actual Value	Expected Value	Result
target DataTypePtr Cnt T u08	5	5	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.OAR	1023	1023	~
target I2c Send I2cRegPtr Cnt T str.IMR	255	255	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	32767	32767	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	65535	65535	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	255	255	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	1023	1023	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	255	255	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	65535	65535	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	4095	4095	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	255	255	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	65535	65535	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	255	255	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	1023	1023	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	255	255	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	32767	32767	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	65535	65535	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	255	255	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	1023	1023	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	255	255	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	65535	65535	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	4095	4095	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	255	255	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	65535	65535	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	255	255	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_SpurSnsrDataPtr_Cnt_T_u16	65535	65535	✓

T				V
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	<b>✓</b>



#### **Test Case 3: Path Test**

Description

Test Vector Description:

Test Vector Description:

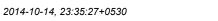
TS3.1"(DigColPsInt\_SensInitialized\_Cnt\_M\_lgc == FALSE)=True
(ElapsedTime\_mS\_T\_u16 >= (uint16)D\_SENSINITDELAY\_MS\_U08 )=True
(DigColPsInt\_NackOccured\_Cnt\_M\_lgc == TRUE)=False
(DigColPsInt\_NackOccured\_Cnt\_M\_lgc == TRUE)=False
(DigColPsInt\_RecvOverrunError\_Cnt\_M\_lgc == TRUE)=False
(DigColPsInt\_DMERIOCcurred\_Cnt\_M\_lgc == TRUE)=False
(DigColPsInt\_CmdFailoCcurred\_Cnt\_M\_u08 == DigColPsInt\_PrevTransactionCnt\_Cnt\_M\_u08) && (DigColPsInt\_RecvdDataType\_Cnt\_M\_u08 != D\_NONE\_CNT\_U08) )=False"
TS3.2"(DigColPsInt\_TransactionCnt\_Cnt\_M\_u08 == DigColPsInt\_PrevTransactionCnt\_Cnt\_M\_u08) && (DigColPsInt\_RecvdDataType\_Cnt\_M\_u08 != D\_NONE\_CNT\_U08) )=False"
TS3.2"(DigColPsInt\_CurrentStepNo\_Cnt\_M\_lgc == FALSE)=False
(DigColPsInt\_CurrentStepNo\_Cnt\_M\_lgc == TRUE)=True
(ElapsedTime\_mS\_T\_u16 > (uint16)(k\_12CHWInitTransactionTime\_Sec\_f32\*D\_SECTOMILLSEC\_CNT\_F32))=True
(DigColPsInt\_RecvOverrunError\_Cnt\_M\_lgc == TRUE)=False
(DigColPsInt\_BusBusySeqError\_Cnt\_M\_lgc == TRUE)=False
(DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum\_cnt\_True)
(DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum\_cnt\_True)
(DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum\_cnt\_True)
(ElapsedTime\_mS\_T\_u16 > (uint16)(k\_12CHWInitTransactionTime\_Sec\_f32\*D\_SECTOMILLSEC\_CNT\_F32))=False"
TS3.4"((DigColPsInt\_TransactionCnt\_Cnt\_M\_u08 == DigColPsInt\_PrevTransactionCnt\_Cnt\_M\_u08) =True && (DigColPsInt\_RecvDataType\_Cnt\_M\_u08 == D\_NONE\_CNT\_U08) =False)
TS3.5"(DigColPsInt\_SensInitialized\_Cnt\_M\_lgc == FALSE)=False
(DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum < INIT\_COMPLETE)=False"
TS3.6"(DigColPsInt\_SensInitialized\_Cnt\_M\_lgc == FALSE)=False
(DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum < INIT\_COMPLETE)=False"
TS3.6"(DigColPsInt\_SensInitialized\_Cnt\_M\_lgc == FALSE)=True
(ElapsedTime\_mS\_T\_u16 >= (uint16)(k\_12CHWIntTransactionCnt\_Cnt\_M\_u08) =False)
TS3.7"(DigColPsInt\_SensInitialized\_Cnt\_M\_lgc == FALSE)=True
(ElapsedTime\_mS\_T\_u16 >= (uint16)(k\_12CHWIntTransactionCnt\_Cnt\_M\_u08) =False)
TS3.7"(DigColPsInt\_SensInitialized\_Cnt\_M\_lgc == FALSE)=True

Name -	Invest Walter
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	5600
DigColPsInt_CurrentSlave_Cnt_M_u08	14
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0
DigColPsInt_InitialTime_mS_M_u32	5486797
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	19
DigColPsInt_RecvOverrunError_Cnt_M_Igc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	9687
DigColPsInt_TransactionCnt_Cnt_M_u08	12
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
2cREG1_temp	target_i2cREG1_temp
<pre>&lt;_ColSensorI2CAddress_Cnt_u08</pre>	119
<_I2CHWInitTransactionTime_Sec_f32	1.10000002
arget_DtrmnElapsedTime_mS_u16_ElapsedTime	1247
arget_GetSystemTime_mS_u32_CurrentTime	1475789
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
target I2c Send I2cRegPtr Cnt T str.CLKL	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
arget I2c Send I2cRegPtr Cnt T str.SAR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
arget I2c Send I2cRegPtr Cnt T str.IVR	66
target I2c Send I2cRegPtr Cnt T str.EMDR	0
target I2c Send I2cRegPtr Cnt T str.PSC	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
target I2c Send I2cRegPtr Cnt T str.PID12	78
target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	0
target I2c Send I2cRegPtr Cnt T str.FUN	0

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Name	Input Value		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0		
target I2c Send I2cRegPtr Cnt T str.CLR	0		
target I2c Send I2cRegPtr Cnt T str.ODR	1		
	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1		
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78		
	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
target_i2cREG1_temp.OAR	66		
target_i2cREG1_temp.IMR	78		
target_i2cREG1_temp.STR	78		
target_i2cREG1_temp.CLKL	495		
target_i2cREG1_temp.CLKH	56		
target_i2cREG1_temp.CNT	897		
target_i2cREG1_temp.DRR	98		
target_i2cREG1_temp.SAR	66		
target_i2cREG1_temp.DXR	78		
target_i2cREG1_temp.MDR	495		
target_i2cREG1_temp.IVR	66		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	78		
target_i2cREG1_temp.PID11	56		
target i2cREG1 temp.PID12	78		
target_i2cREG1_temp.DMAC	0		
target i2cREG1 temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target i2cREG1 temp.DIN	1		
· · · · · · · · · · · · · · · · · · ·			
target_i2cREG1_temp.DOUT			
	0		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	0 0 0		
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR	0 0 0 1		
target_i2cREG1_temp.CLR	0 0 0 1		
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR	0 0 0 1		
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD	0 0 0 1	Expected Value	Result
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL Name	0 0 0 1 0	Expected Value 36	Result
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL	0 0 0 1 0 0 <b>Actual Value</b>	· ·	~
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL Name DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	0 0 0 1 0 0 <b>Actual Value</b> 36 20	36 20	~
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	0 0 0 1 0 0 <b>Actual Value</b> 36 20	36 20 30	<b>*</b>
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc	0 0 0 1 0 0 <b>Actual Value</b> 36 20 30	36 20 30 0	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08	0 0 0 1 0 0 <b>Actual Value</b> 36 20 30 0	36 20 30 0 119	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum	0 0 0 1 0 0 <b>Actual Value</b> 36 20 30 0 119 INIT_SENSOR1_READERROR_SETREG	36 20 30 0 119 INIT_SENSOR1_READERROR_SETREG	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData()	0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	36 20 30 0 119 INIT_SENSOR1_READERROR_SETREG 40	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc	0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	36 20 30 0 119 INIT_SENSOR1_READERROR_SETREG 40 0	\rightarrow \right
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc	0 0 0 0 1 1 0 0 0 <b>Actual Value</b> 36 20 30 0 119 INIT_SENSOR1_READERROR_SETREG 40 0 0 0	36 20 30 0 119 INIT_SENSOR1_READERROR_SETREG 40 0	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08	0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	36 20 30 0 119 INIT_SENSOR1_READERROR_SETREG 40 0 0	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc	0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	36 20 30 0 119 INIT_SENSOR1_READERROR_SETREG 40 0 0	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08	0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	36 20 30 0 119 INIT_SENSOR1_READERROR_SETREG 40 0 0	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc	0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	36 20 30 0 119 INIT_SENSOR1_READERROR_SETREG 40 0 0	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SensInitialized_Cnt_M_lgc	0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	36 20 30 0 119 INIT_SENSOR1_READERROR_SETREG 40 0 0 12 0	· · · · · · · · · · · · · · · · · · ·

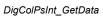




Name	Actual Value	Expected Value	Result
target_ColSnsrDataPtr_Cnt_T_u16	5600	5600	~
target_DataTypePtr_Cnt_T_u08	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target I2c Send I2cRegPtr Cnt T str.SAR	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	•
target I2c Send I2cRegPtr Cnt T str.FUN	0	0	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target I2c Send I2cRegPtr Cnt T str.DIN	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target I2c Send I2cRegPtr Cnt T str.SET	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	1	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	0	0	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	0	0	
	66	66	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	78	78	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	78	78	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR		495	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	98	98	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_SpurSnsrDataPtr_Cnt_T_u16	9687	9687	~

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	•
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c_Send	1	I2c_Send	1	•
GetSystemTime mS u32	1	GetSystemTime mS u32	1	<b>✓</b>

Test Step 3.2 (Repeat Count = 1)		<b>✓</b>
Name	Input Value	
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16	
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08	
DigColPsInt_Buffer_Cnt_M_u08[0]	40	
DigColPsInt_Buffer_Cnt_M_u08[1]	50	
DigColPsInt_Buffer_Cnt_M_u08[2]	60	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	





Name	Input Value
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	7985
DigColPsInt_CurrentSlave_Cnt_M_u08	21
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR1 READEXTERR READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	6489549
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	31
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	11230
DigColPsInt_TransactionCnt_Cnt_M_u08	29
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target i2cREG1 temp
k_ColSensorl2CAddress_Cnt_u08	126
k I2CHWInitTransactionTime Sec f32	1.5
target_DtrmnElapsedTime_mS_u16_ElapsedTime	7841
target_GetSystemTime_mS_u32_CurrentTime	2478541
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target I2c Send I2cRegPtr Cnt T str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target I2c Send I2cRegPtr Cnt T str.ODR	0
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target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	1
	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3

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Name	Input Value		
target_i2cREG1_temp.OAR	567		
target_i2cREG1_temp.IMR	44		
target_i2cREG1_temp.STR	4444		
target_i2cREG1_temp.CLKL target_i2cREG1_temp.CLKH	566 4466		
target_i2cREG1_temp.CNT	129		
target i2cREG1 temp.DRR	6		
target_i2cREG1_temp.SAR	567		
target_i2cREG1_temp.DXR	44		
target_i2cREG1_temp.MDR	566		
target_i2cREG1_temp.IVR	554		
target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC	44		
target_i2cREG1_temp.PID11	4466		
target_i2cREG1_temp.PID12	44		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	2		
target_i2cREG1_temp.DIN	0		
target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET	1		
target i2cREG1 temp.CLR	2		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	40	40	<b>~</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	50	50	<b>V</b>
DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc	60 0	60 0	<b>✓</b>
DigColPsInt_CurrentSlave_Cnt_M_u08	21	21	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_READ	INIT_SENSOR1_READEXTERR_READ	<b>~</b>
DigColPsInt_GetData()	134	134	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	•
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	29	29	<b>V</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SensInitialized_Cnt_M_lgc	0	0	<b>✓</b>
target_ColSnsrDataPtr_Cnt_T_u16	7985	7985	
target DataTypePtr Cnt T u08	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	4466 129	4466 129	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR target_I2c Send_I2cRegPtr_Cnt_T str.PSC	44	44	<b>*</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	4466	4466	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1 2	2	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	4444	4444	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	566	566	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	4466	4466 129	<b>*</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	129	129	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	-
	<u> </u>	<u> </u>	

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_SpurSnsrDataPtr_Cnt_T_u16	11230	11230	~

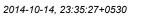
T				V
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target ColSnsrDataPtr Cnt T u16
DataTypePtr Cnt T u08	target DataTypePtr Cnt T u08
DigColPsInt Buffer Cnt M u08[0]	3
DigColPsInt_Buffer_Cnt_M_u08[1]	6
DigColPsInt Buffer Cnt M u08[2]	9
DigColPsInt BusBusySeqError Cnt M Igc	1
DigColPsInt CmdFailOccurred Cnt M lgc	0
DigColPsInt ColSnsrData Cnt M u16	27065
DigColPsInt_CurrentSlave_Cnt_M_u08	77
DigColPsInt CurrentStepNo Cnt M enum	INIT SENSOR2 READERROR SETREG
DigColPsInt InitFailedOnce Cnt M Igc	0
DigColPsInt InitialTime mS M u32	14511565
DigColPsInt NackOccured Cnt M lgc	1
DigColPsInt PrevTransactionCnt Cnt M u08	130
DigColPsInt RecvOverrunError Cnt M lgc	0
DigColPsInt RecvdDataType Cnt M u08	4
DigColPsInt SensInitialized Cnt M Igc	1
DigColPsInt SpurSnsrData Cnt M u16	23574
DigColPsInt TransactionCnt Cnt M u08	79
OtrmnElapsedTime mS u16(ElapsedTime)	target DtrmnElapsedTime mS u16 ElapsedTime
GetSystemTime mS u32(CurrentTime)	target GetSystemTime mS u32 CurrentTime
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target I2c SetupMasterTransmit I2cRegPtr Cnt T str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
2cREG1_temp	target_i2cREG1_temp
ColSensorl2CAddress_Cnt_u08	66
<pre>c_I2CHWInitTransactionTime_Sec_f32</pre>	4.69999981
arget_DtrmnElapsedTime_mS_u16_ElapsedTime	741
arget_GetSystemTime_mS_u32_CurrentTime	10500557
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3





Name	Input Value		
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3		
	2		
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN			
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1		
target I2c Send I2cRegPtr Cnt T str.PSL	2		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	54		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	66		
	8		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2		
target_i2cREG1_temp.OAR	54		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	8		
target_i2cREG1_temp.CLKL	554		
target_i2cREG1_temp.CLKH	344		
target_i2cREG1_temp.CNT	123		
target i2cREG1 temp.DRR	45		
target_i2cREG1_temp.SAR	54		
target i2cREG1 temp.DXR	66		
target i2cREG1 temp.MDR	554		
target i2cREG1 temp.IVR			
	788		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	344		
target_i2cREG1_temp.PID12	66		
target i2cREG1 temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target i2cREG1 temp.DIR	3		
target i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	3		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	2		
	_		Danulé
	Actual Value		Result
Name	Actual Value	Expected Value	-
DigColPsInt_Buffer_Cnt_M_u08[0]	3	3	•
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	3 6	3 6	~
DigColPsInt_Buffer_Cnt_M_u08[0]	3 6 9	3	<b>*</b>
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	3 6	3 6	~
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	3 6 9	3 6 9	<b>*</b>
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08	3 6 9 0 77	3 6 9 0 77	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum	3 6 9 0 77 INIT_SENSOR2_READERROR_SETREG	3 6 9 0 77 INIT_SENSOR2_READERROR_SETREG	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData()	3 6 9 0 77 INIT_SENSOR2_READERROR_SETREG 6	3 6 9 0 77 INIT_SENSOR2_READERROR_SETREG 6	***
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc	3 6 9 0 77 INIT_SENSOR2_READERROR_SETREG 6 0	3 6 9 0 77 INIT_SENSOR2_READERROR_SETREG 6 0	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc	3 6 9 0 77 INIT_SENSOR2_READERROR_SETREG 6 0 0	3 6 9 0 77 INIT_SENSOR2_READERROR_SETREG 6 0 0	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc	3 6 9 0 77 INIT_SENSOR2_READERROR_SETREG 6 0	3 6 9 0 77 INIT_SENSOR2_READERROR_SETREG 6 0	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc	3 6 9 0 77 INIT_SENSOR2_READERROR_SETREG 6 0 0	3 6 9 0 77 INIT_SENSOR2_READERROR_SETREG 6 0 0	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08	3 6 9 0 77 INIT_SENSOR2_READERROR_SETREG 6 0 0	3 6 9 0 77 INIT_SENSOR2_READERROR_SETREG 6 0 0	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData() DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc	3 6 9 0 77 INIT_SENSOR2_READERROR_SETREG 6 0 0 79	3 6 9 0 77 INIT_SENSOR2_READERROR_SETREG 6 0 0	· · · · · · · · · · · · · · · · · · ·





Name	Actual Value	Expected Value	Result
target_DataTypePtr_Cnt_T_u08	4	4	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	54	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8	8	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554	554	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	344	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	123	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	45	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	54	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	554	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	788	•
target I2c Send I2cRegPtr Cnt T str.EMDR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344	344	<b>~</b>
target I2c Send I2cRegPtr Cnt T str.PID12	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>V</b>
target I2c Send I2cRegPtr Cnt T str.FUN	1	1	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	
target I2c Send I2cRegPtr Cnt T str.DOUT	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>V</b>
target I2c Send I2cRegPtr Cnt T str.ODR	2	2	-
target I2c Send I2cRegPtr Cnt T str.PD	1	1	~
target_12c_Send_12cRegPtr_Cnt_T_str.PSL	2	2	-
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	54	54	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	8	8	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554	554	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344	344	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	123	123	
	45	45	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	54	54	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	554	554	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	788	788	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR		3	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	3		-
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	66	66	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	344	344	-
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	66	66	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	3	3	<b>V</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	1	1	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	3	3	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	2	2	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_SpurSnsrDataPtr_Cnt_T_u16	23574	23574	

Τ				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

Test Step 3.4 (Repeat Count = 1)		<b>✓</b>
Name	Input Value	
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16	
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08	
DigColPsInt_Buffer_Cnt_M_u08[0]	11	
DigColPsInt_Buffer_Cnt_M_u08[1]	22	
DigColPsInt_Buffer_Cnt_M_u08[2]	33	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	
DigColPsInt_ColSnsrData_Cnt_M_u16	0	
DigColPsInt_CurrentSlave_Cnt_M_u08	84	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ	
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1	





Name	Input Value
DigColPsInt_InitialTime_mS_M_u32	15514317
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	93
DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt RecvdDataType Cnt M u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	25117
DigColPsInt_TransactionCnt_Cnt_M_u08	93
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	73
k_I2CHWInitTransactionTime_Sec_f32	5.0999999
target_DtrmnElapsedTime_mS_u16_ElapsedTime	1248
target_GetSystemTime_mS_u32_CurrentTime	11503309
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	7788
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100
target I2c Send I2cRegPtr Cnt T str.MDR	2767
target_i2c_Send_i2cRegPtr_Cnt_T_str.IVR	9
target_i2c_Send_i2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	9
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	0
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	3
target_i2cREG1_temp.IMR	100
target_i2cREG1_temp.STR	7788
target_i2cREG1_temp.CLKL	2767
target_i2cREG1_temp.CLKH	556

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Name	Input Value		
target_i2cREG1_temp.CNT	564		
target_i2cREG1_temp.DRR	88		
target_i2cREG1_temp.SAR	3		
target i2cREG1 temp.DXR	100		
target i2cREG1 temp.MDR	2767		
target i2cREG1 temp.IVR	9		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	100		
target_i2cREG1_temp.PID11	556		
target_i2cREG1_temp.PID12	100		
target i2cREG1 temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	3		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	•
DigColPsInt_Buffer_Cnt_M_u08[1]	22	22	~
DigColPsInt_Buffer_Cnt_M_u08[2]	33	33	~
DigColPsInt_BusBusySeqError_Cnt_M_Igc	0	0	~
DigColPsInt_CurrentSlave_Cnt_M_u08	73	73	-
DigColPsInt CurrentStepNo Cnt M enum	INIT SENSOR1 READERROR SETREG	INIT_SENSOR1_READERROR_SETREG	<b>✓</b>
DigColPsInt_GetData()	40	40	-
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	•
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	-
	93	93	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08			
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	•
I2c_Send(Length_Cnt_T_u32)	1	1	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
target_ColSnsrDataPtr_Cnt_T_u16	0	0	~
target_DataTypePtr_Cnt_T_u08	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	3	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	100	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	7788	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	556	-
target I2c Send I2cRegPtr Cnt T str.CNT	564	564	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.DRR	88	88	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	3	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	100	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	2767	•
	9	9	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR		0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	100	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0	0	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	1	1	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	100	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	
	556	556	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	88	88	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	3	3	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	100	100	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	2767	2767	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	9	9	<b>~</b>

DigColPsInt\_GetData



Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	100	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556	556	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	100	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_SpurSnsrDataPtr_Cnt_T_u16	25117	25117	~

Τ				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	~
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	~

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target ColSnsrDataPtr Cnt T u16
DataTypePtr Cnt T u08	target DataTypePtr Cnt T u08
	40
DigColPsInt_Buffer_Cnt_M_u08[0]	50
DigColPsInt_Buffer_Cnt_M_u08[1]	
DigColPsInt_Buffer_Cnt_M_u08[2]	60
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	·
DigColPsInt_ColSnsrData_Cnt_M_u16	28702
DigColPsInt_CurrentSlave_Cnt_M_u08	101
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	34566605
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	41
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	24973
DigColPsInt_TransactionCnt_Cnt_M_u08	34
OtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
2cREG1_temp	target_i2cREG1_temp
_ColSensorl2CAddress_Cnt_u08	63
_I2CHWInitTransactionTime_Sec_f32	1.5
arget_DtrmnElapsedTime_mS_u16_ElapsedTime	10881
arget GetSystemTime mS u32 CurrentTime	30555597
arget I2c Send I2cRegPtr Cnt T str.OAR	66
arget I2c Send I2cRegPtr Cnt T str.IMR	78
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
arget I2c Send I2cRegPtr Cnt T str.CLKL	495
arget I2c Send I2cRegPtr Cnt T str.CLKH	56
arget I2c Send I2cRegPtr Cnt T str.CNT	897
arget I2c Send I2cRegPtr Cnt T str.DRR	98
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
arget I2c Send I2cRegPtr Cnt T str.IVR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FMDR	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
target_12c_Send_12cRegPtr_Cnt_1_str.PID11	78

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· _			
Name	Input Value		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0		
target I2c Send I2cRegPtr Cnt T str.DIN	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	56 897		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	98		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
target_i2cREG1_temp.OAR	66		
target_i2cREG1_temp.IMR	78		
target_i2cREG1_temp.STR	78		
target_i2cREG1_temp.CLKL	495		
target_i2cREG1_temp.CLKH	56 897		
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	98		
target i2cREG1 temp.SAR	66		
target i2cREG1 temp.DXR	78		
target_i2cREG1_temp.MDR	495		
target_i2cREG1_temp.IVR	66		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	78		
target_i2cREG1_temp.PID11	56		
target_i2cREG1_temp.PID12	78		
target_i2cREG1_temp.DMAC	0		
target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target i2cREG1 temp.DOUT	0		
target i2cREG1 temp.SET	0		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	40	40	~
DigColPsInt_Buffer_Cnt_M_u08[1]	50	50	~
DigColPsInt_Buffer_Cnt_M_u08[2]	60	60	· ·
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	<b>✓</b>
DigColPsInt_CurrentSlave_Cnt_M_u08	101	101 DEAD SENSOR1 SETRES	<b>Y</b>
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_GetData()	READ_SENSOR1_SETREG 2	READ_SENSOR1_SETREG 2	Ž
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	-
DigColPsInt NackOccured Cnt M Igc	0	0	
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	34	34	~
DigColPsInt_RecvOverrunError_Cnt_M_Igc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	~

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Name	Actual Value	Expected Value	Result
target_ColSnsrDataPtr_Cnt_T_u16	28702	28702	~
target_DataTypePtr_Cnt_T_u08	4	4	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.ODR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	78	78	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	78	78	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	_
target_SpurSnsrDataPtr_Cnt_T_u16	24973	24973	

T				V
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	-

Test Step 3.6 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	0
DigColPsInt_Buffer_Cnt_M_u08[1]	0
DigColPsInt_Buffer_Cnt_M_u08[2]	0
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	0
DigColPsInt_CurrentSlave_Cnt_M_u08	0
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_NOT_INITIALIZED





Depichent   Main   Service   Main   Service		
Taglocates	Name	Input Value
Taglocates	DigColPsInt_InitFailedOnce_Cnt_M_lgc	•
Disposition   Previous activation of the Muse		0
Dispositional Resonational Systems (1997)   1997   1998   1998   1999	DigColPsInt_NackOccured_Cnt_M_lgc	0
Depote   D	DigColPsInt_PrevTransactionCnt_Cnt_M_u08	0
Disposition   Secretarion   Secretarion   Disposition   Disposition   Secretarion   Disposition	DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
Disposition   Transcription   Cont. M. 19	DigColPsInt_RecvdDataType_Cnt_M_u08	0
Dipolitaria   Transaction Cr., Dr. M. J., List   Dismiliagues   Time   Utility   Uti	DigColPsInt_SensInitialized_Cnt_M_lgc	
Demonth programmer   100, 100, 100, 100, 100, 100, 100, 10	DigColPsInt_SpurSnsrData_Cnt_M_u16	
Geographic Time_meg_S25CUrrord Time	DigColPsInt_TransactionCnt_Cnt_M_u08	
Respect (1989-1997; Crt.T_st)   terget, Dec. Sendy (1989-1997; Crt.T_st)		
Image: Part		
SquaSherDatabeth_CotT_U10   topget_2cREG_1smp   topget_2cREG_1sm		
March   Colors   March   Colors   March   Colors   March   Colors   March   Colors   March		
K. COSEMPTICADISTICS. 2018  K. COSEMPTICADISTICS. 2018  Integr. Diffine Representation (Page 2018)  Integr. Di		
N. 2024WillTransactorTime, Sec. 92 target, Demicropacity my, St. 915, EspecialTime target, Aces, Section Time, Proc. 92, 22, CarrestTime target, Aces, Send. 2024eptp. Conf. 1, and ACM target, 120, Send. 202		
State   Dimension   Proceedings   Disposed Time   Disposed   Dis		
Target_GES-Memillane_MS_LSZ_CurrentTime  area   LeS_Semal_GES_PSP_COT_1 xt CAR  area   LeS_Semal_GES_PSP_COT_1 xt CAR  area   LeS_Semal_GES_PSP_COT_2 xt CAR  area   LeS_Semal		
Langer   Line   Send   DecRegiffer On   T_ str DNR		
		·
target_122_Sead_124Repth_COLT_1st CLK1         0           target_122_Sead_124Repth_COLT_1st CLK1         0           target_122_Sead_124Repth_COLT_1st CLK1         0           target_122_Sead_124Repth_COLT_1st DBR         0           target_122_Sead_124Repth_COLT_1st DBAC         0 </td <td></td> <td>·</td>		·
tanget [22. Send 12-Regilier_Cot_T at CNAH  on tanget [22. Send 12-Regil	0 = = = 0 = ==	
tanget_22_Send_126RegNP_CR_T_T at CNT  larget_12_Send_126RegNP_CR_T_T at DRR  larget_12_Send_126		·
Langel, IZC. Send, IZCRegiff, Cot, T., str. DRR  0 Integer, IZC. Send, IZCRegiff, Cot, T., str. DXR  1 Integer, IZC. Send, IZCRegiff, Cot, T., str. DXR  1 Integer, IZC. Send, IZCRegiff, Cot, T., str. DXR  1 Integer, IZC. Send, IZCRegiff, Cot, T., str. DXR  1 Integer, IZC. Send, IZCRegiff, Cot, T., str. DXR  1 Integer, IZC. Send, IZCRegiff, Cot, T., str. DXR  1 Integer, IZC. Send, IZCRegiff, Cot, T., str. DXR  1 Integer, IZC. Send, IZCRegiff, Cot, T., str. DXDI  1 Integer, IZC. Send, IZCRegiff, Cot, T., s		
toget_12. Send_12.RepPt_Cnlst_DNR  toget_12. S		
taopet I.2. Send J. ZeRegiPt. Col. T., str. MDR         0           target I.2. Send J. ZeRegiPt. Col. T., str. MDR         0           target I.2. Send J. ZeRegiPt. Col. T., str. EMDR         0           target I.2. Send J. ZeRegiPt. Col. T., str. PDD1         0           target I.2. Send J. ZeRegiPt. Col. T., str. PDD1         0           target J.2. Send J. ZeRegiPt. Col. T., str. PDD1         0           target J.2. Send J. ZeRegiPt. Col. T., str. DNA         0           target J.2. Send J. ZeRegiPt. Col. T., str. DNA         0           target J.2. Send J. ZeRegiPt. Col. T., str. DNA         0           target J.2. Send J. ZeRegiPt. Col. T., str. DNA         0           target J.2. Send J. ZeRegiPt. Col. T., str. DN         0           target J.2. Send J. ZeRegiPt. Col. T., str. DNA         0           target J.2. Send J. ZeRegiPt. Col. T., str. DOUT         0           target J.2. Send J. ZeRegiPt. Col. T., str. CR         0           target J.2. Send J. ZeRegiPt. Col. T., str. CR         0           target J.2. Send J. ZeRegiPt. Col. T., str. DO         0           target J.2. Send J. ZeRegiPt. Col. T., str. DN         0           target J.2. Send J. ZeRegiPt. Col. T., str. DN         0           target J.2. Send J. ZeregiPt. Col. T., str. DN         0           target J.2. Send J. ZeregiPt. Col. T., str. DN         0 <td>· ·</td> <td></td>	· ·	
taget_12e_Send_12eRegPt_Cntstr.MDR  larget_12e_Send_12eRegPt_Cntstr.MDR  larget_12e_Send_12eRegPt_Cntstr.DDR  larget_12e_SetupMasterTransmt_12eRegPt_Cntstr.DRR  larg		
Langet   22. Send   ZoRegipt CotT_strNR		
target_Lize_Send_LizeReptPt_Cnt_T_str_ENDR  target_Lize_Send_LizeReptPt_Cnt_T_str_PID11  target_Lize_Send_LizeReptPt_Cnt_T_str_PID12  target_Lize_Send_LizeReptPt_Cnt_T_str_PID12  target_Lize_Send_LizeReptPt_Cnt_T_str_PID12  target_Lize_Send_LizeReptPt_Cnt_T_str_PID12  target_Lize_Send_LizeReptPt_Cnt_T_str_PID18  target_Lize_Send_LizeReptPt_Cnt_T_str_PID18  target_Lize_Send_LizeReptPt_Cnt_T_str_DIDNC  target_Lize_Send_LizeR		
target_L2e_Send_J2eRegPtr_Cnt_T_str_PID11         0           target_L2e_Send_J2eRegPtr_Cnt_T_str_PID12         0           target_L2e_Send_J2eRegPtr_Cnt_T_str_PID12         0           target_L2e_Send_J2eRegPtr_Cnt_T_str_DNAC         0           target_L2e_Send_J2eRegPtr_Cnt_T_str_DNAC         0           target_L2e_Send_J2eRegPtr_Cnt_T_str_DNA         0           target_L2e_Set_JAMaster_Transmit_J2eRegPtr_Cnt_T_str_DNA         0           target_L2e_Set_JAMaster_Transmit_J2eRegPtr_Cnt_T_str.DNA         0           target_L2e_Set_JAMaster_Transmit_J2eRegPtr_Cnt_T_str.DNA         0		
target_L2c_Send_L2cRegPtr_Cntstr.PiD12  larget_L2c_Send_L2cRegPtr_Cntstr.PiD12  larget_L2c_Send_L2cRegPtr_Cntstr.PiD12  larget_L2c_Send_L2cRegPtr_Cntstr.PiD12  larget_L2c_Send_L2cRegPtr_Cntstr.PiD10  larget_L2c_Send_L2cRegPtr_Cntstr.PiD10  larget_L2c_Send_L2cRegPtr_Cntstr.DiD1  larget_L2c_Send_L2cRegPtr_Cntstr.DiD1  larget_L2c_Send_L2cRegPtr_Cntstr.DiD1  larget_L2c_Send_L2cRegPtr_Cntstr.DiD1  larget_L2c_Send_L2cRegPtr_Cntstr.DiD1  larget_L2c_Send_L2cRegPtr_Cntstr.CDR  larget_L2c_Send_L2cRegPtr_Cntstr.DiD1  larget_L2c_SetupMasterTransmit_L2cRegPtr_Cntstr.DiD1  larget_L2c_SetupMas		0
target_Re_Send_IzeRegPr_Cnt_T_strDNAC  target_Re_Send_IzeRegPr_Cnt_T_strDN  target_Re_Send_IzeRegPr_Cnt_T_strDNR  target_Re_Send_IzeRegPr_Cnt_T_strDNR  target_Re_Send_IzeRegPr_Cnt_T_strDNR  target_Re_Send_IzeRegPr_Cnt_T_strDNR  target_Re_Send_IzeRegPr_Cnt_T_strDNR  target_Re_Send_IzeRegPr_Cnt_T_strDNR  target_Re_Send_IxeRegPr_Cnt_T_strDNR  target_Re_Send_IxeRe		0
target, Ize, Send, IzeRegPtr, Cnt, T_str, DIR         0           target, Ize, Send, IzeRegPtr, Cnt, T_str, DIR         0           target, Ize, Send, IzeRegPtr, Cnt, T_str, DIN         0           target, Ize, Send, IzeRegPtr, Cnt, T_str, DUT         0           target, Ize, Send, IzeRegPtr, Cnt, T_str, SET         0           target, Ize, Send, IzeRegPtr, Cnt, T_str, CLR         0           target, Ize, Send, IzeRegPtr, Cnt, T_str, DIR         0           target, Ize, Send, IzeRegPtr, Cnt, T_str, DIP         0           target, Ize, Send, IzeRegPtr, Cnt, T_str, DIP         0           target, Ize, Send, IzeRegPtr, Cnt, T_str, DIR         0           target, Ize, SetupMasterTransmil, IzeRegPtr, Cnt, T_str, DAR         0           target, Ize, SetupMasterTransmil, IzeRegPtr, Cnt, T_str, STR         0           target, Ize, SetupMasterTransmil, IzeRegPtr, Cnt, T_str, CNt, 0         0           target, Ize, SetupMasterTransmil, IzeRegPtr, Cnt, T_str, CNt, 0         0           target, Ize, SetupMasterTransmil, IzeRegPtr, Cnt, T_str, CNT         0           target, Ize, SetupMasterTransmil, IzeRegPtr, Cnt, T_str, DRR         0           target, Ize, SetupMasterTransmil, IzeRegPtr, Cnt, T_str, DRR         0           target, Ize, SetupMasterTransmil, IzeRegPtr, Cnt, T_str, DIN         0           target, Ize, SetupMasterTransmil, IzeRegPtr, Cnt, T_str, DIN         0		0
target_Ize_Send_IzeRegPtr_Cnt_T_str.DIR         0           target_Ize_Send_IzeRegPtr_Cnt_T_str.DOUT         0           target_Ize_Send_IzeRegPtr_Cnt_T_str.DOUT         0           target_Ize_Send_IzeRegPtr_Cnt_T_str.DOUT         0           target_Ize_Send_IzeRegPtr_Cnt_T_str.CR         0           target_Ize_Send_IzeRegPtr_Cnt_str.CR         0           target_Ize_Send_IzeRegPtr_Cnt_T_str.DOR         0           target_Ize_Send_IzeRegPtr_Cnt	target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target, Izc., Send, IzcRegPtr_Cnt_T_str.DUN         0           target, Izc., Send, IzcRegPtr_Cnt_T_str.Str.T         0           target, Izc., Send, IzcRegPtr_Cnt_T_str.Str.T         0           target, Izc., Send, IzcRegPtr_Cnt_T_str.CDR         0           target, Izc., Send, IzcRegPtr_Cnt_T_str.DDR         0           target, Izc., Send, IzcRegPtr_Cnt_T_str.PD         0           target, Izc., Send, IzcRegPtr_Cnt_T_str.PD         0           target, Izc., Send, IzcRegPtr_Cnt_T_str.PDR         0           target, Izc., Send, IzcRegPtr_Cnt_T_str.DAR         0           target, Izc., SetupMasterTransmil, IzcRegPtr_Cnt_T_str.DAR         0           target, Izc., SetupMasterTransmil, IzcRegPtr_Cnt_T_str.CTK         0           target, Izc., SetupMasterTransmil, IzcRegPtr_Cnt_T_str.CtK         0           target, Izc., SetupMasterTransmil, IzcRegPtr_Cnt_T_str.CTK         0           target, Izc., SetupMasterTransmil, IzcRegPtr_Cnt_T_str.DAR         0	target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target   12c   Send   2cRegPtr   Cnt   T   str. SET   0	target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_12e_Send_12cRegPtr_Cnt_T_str.SET         0           target_12e_Send_12cRegPtr_Cnt_T_str.OLR         0           target_12e_Send_12cRegPtr_Cnt_T_str.DDR         0           target_12e_Send_12cRegPtr_Cnt_T_str.DDR         0           target_12e_Send_12cRegPtr_Cnt_T_str.DD         0           target_12e_Send_12cRegPtr_Cnt_T_str.DR         0           target_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         0           target_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         0           target_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         0           target_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         0           target_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT         0           target_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         0           target_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         0           target_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         0           target_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         0           target_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         0           target_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         0           target_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         0           target_12e_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         0           target_12e_SetupMasterTr	target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_12c_Send_12cRegPtr_Cnt_T_str.ODR         0           target_12c_Send_12cRegPtr_Cnt_T_str.ODR         0           target_12c_Send_12cRegPtr_Cnt_T_str.PD         0           target_12c_Send_12cRegPtr_Cnt_T_str.PSL         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         0	target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
larget   2c   Send   2cRegPtr_Cnt_T str. DDR	target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	
target_12c_Send_12cRegPtr_Cnt_T_str.PD         0           target_12c_Send_12cRegPtr_Cnt_T_str.PSL         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MR         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.STR         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CtKL         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDT         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDT         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDT         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDT         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDT         0<		
target_12c_Send_12cRegPtr_Cnt_T_str.PSL         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.OAR         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.STR         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CtRL         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CtRL         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CtRL         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRC         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDC         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDC         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDR         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDR         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDR<		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.NAR  1 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.NTR  1 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.NTR  1 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT  1 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT  1 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT  1 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.NTR  1 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.NTR  1 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNR  1 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNR  1 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.NDR  1 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.		
target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.STR		
target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.CkK_ target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.CkK_ target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.CkK_ target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.DkT  target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.DkR  target_ 2c_SetupMasterTransmit		
target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.CLKL   0   1   1   1   1   1   1   1   1   1		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DMR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DMR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DMR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDT 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDT 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDT 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DMR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DN 0 target_12c_Set		
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNR 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PNC 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PNC 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PNC 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PNC 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PNC 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PNC 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNAC 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNAC 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNAC 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNAC 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNA 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNA 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.SET 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.SET 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.SET 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNA 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNA 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNA 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.SET 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNA 0 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_		
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T.str.DXR		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.RDR  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.RDR  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID12  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID12  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID12  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID13  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID14  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID15  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID16  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID17  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID17  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID16  target_I2c_SetupMasterTransmit_I2c_RegPtr_Cnt_T_str.DID16  target_I2c_SetupMasterTransmit_I2c_RegPtr_Cnt_T_str.DID16  target_I2c_SetupMaster		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_		
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSC  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID11  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID12  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DID12  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DMAC  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIR  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIV  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DUT  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DUT  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DUT  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLR  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CDR  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DDR  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PD  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PD  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PD  target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL  target_!2c_REG1_temp.OAR  target_!2c_REG1_temp.STR		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC 1 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 3 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 4 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 5 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN 6 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN 6 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN 6 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT 6 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT 6 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET 6 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR 6 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOR 6 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOR 6 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOR 6 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOR 6 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOR 6 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOR 7 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOR 8 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOR 9 target_l2c_SetupMasterTransmit_l2c_RegPtr_Cnt_T_str.DOR 9 target_l2c_SetupMasterTransmit_l2c_RegPtr_Cnt_T_str.DOR 9 target_l2c_SetupMasterTransmit_l2c_RegPtr_Cnt_T_str.DOR 9 target_l2c_SetupMasterTransmit_l2c_RegPtr_Cnt_T_str.DOR 9 target_l2c_SetupMasterTransmit_l2c_RegPtr_Cnt_T_str.DOR 9 target_l2c_SetupMasterTransmit_l2c_Reg		·
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12		0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL 0 target_l2c_SetupMasterTransmit_l2c_RegPtr_Cnt_T_str.PSL 0 target_l2c_SetupMasterTransmit_l2c_RegPtr_Cn		0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUN 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL 0 target_l2c_REG1_temp.OAR 0 target_l2c_REG1_temp.IMR 0 target_l2c_REG1_temp.STR 0		0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cntstr.DIN 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cntstr.DOUT 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cntstr.SET 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cntstr.CLR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cntstr.ODR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cntstr.DDR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cntstr.PD 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cntstr.PSL 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cntstr.PSL 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cntstr.PSL 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cntstr.PSL 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cntstr.PSL 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cntstr.PSL 0 target_l2c_REG1_temp.OAR 0 target_l2c_REG1_temp.IMR 0 target_l2c_REG1_temp.STR 0	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL         0           target_I2cREG1_temp.OAR         0           target_I2cREG1_temp.IMR         0           target_I2cREG1_temp.STR         0	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL 0 target_l2c_SetupMasterTransmit_l2c_RegPtr_Cnt_T_str.PSL 0 target_l2c_SetupMasterTransmit_l2c_RegPtr_Cnt_T_str.PSL 0 target_l2c_SetupMasterTransmit_l2c_RegPtr_Cnt_T_str.PSL 0 target_l2c_SetupMasterTransmit_l2c_RegPtr_Cnt_T_str.PSL 0 target_l2c_SetupMasterTransmit_l2c_RegPtr_Cnt_T_str.PSL 0 target_l2c_SetupMasterTransmit_l2c_RegPtr_Cnt_T_str.PSL 0 target_l2c_SetupMasterTransmit_l2c_RegPtr_Cnt_	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL 0 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL 0 target_l2c_REG1_temp.OAR 0 target_l2c_REG1_temp.IMR 0 target_l2c_REG1_temp.STR 0		
target_I2c_SetupMasterTransmit_I2cRegPtr_CntT_str.ODR         0           target_I2c_SetupMasterTransmit_I2cRegPtr_CntT_str.PD         0           target_I2c_SetupMasterTransmit_I2cRegPtr_CntT_str.PSL         0           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL         0           target_I2cREG1_temp.OAR         0           target_I2cREG1_temp.IMR         0           target_I2cREG1_temp.STR         0		·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD 0 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL 0 target_I2c_REG1_temp.OAR 0 target_I2cREG1_temp.IMR 0 target_I2cREG1_temp.STR 0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL 0 target_i2cREG1_temp.OAR 0 target_i2cREG1_temp.IMR 0 target_i2cREG1_temp.STR 0		
target_i2cREG1_temp.OAR 0 target_i2cREG1_temp.IMR 0 target_i2cREG1_temp.STR 0		
target_i2cREG1_temp.IMR 0 target_i2cREG1_temp.STR 0		
target_i2cREG1_temp.STR 0		
target_tzck=Git_temp.CLKL   U	· ·	
	target_12CKEG1_temp.CLKL	U

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Name	Input Value		
target_i2cREG1_temp.CLKH	0		
target_i2cREG1_temp.CNT	0		
target_i2cREG1_temp.DRR	0		
target_i2cREG1_temp.SAR	0		
target_i2cREG1_temp.DXR	0		
target_i2cREG1_temp.MDR	0		
target_i2cREG1_temp.IVR	0		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	0		
target_i2cREG1_temp.PID11	0		
target_i2cREG1_temp.PID12	0		
target_i2cREG1_temp.DMAC	0		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	0		
target_i2cREG1_temp.DOUT	0		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	0		
	0		
target_i2cREG1_temp.PSL		1	
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	0	0	~
DigColPsInt_Buffer_Cnt_M_u08[1]	0	0	<b>✓</b>
DigColPsInt Buffer Cnt M u08[2]	0	0	~
DigColPsInt BusBusySegError Cnt M Igc	0	0	<b>~</b>
DigColPsInt_CurrentSlave_Cnt_M_u08	0	0	_
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_NOT_INITIALIZED	INIT_NOT_INITIALIZED	~
DigColPsInt_GetData()	0	0	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	0	0	<b>✓</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_SensInitialized_Cnt_M_lgc	0	0	<b>✓</b>
target_ColSnsrDataPtr_Cnt_T_u16	0	0	_
target_DataTypePtr_Cnt_T_u08	0	0	<b>✓</b>
	0	0	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR			~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	0	0	
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	0	0	-
target I2c Send I2cRegPtr Cnt T str.SAR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	0	0	_
target I2c Send I2cRegPtr Cnt T str.MDR	0	0	•
· ·		0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	0		
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	-
	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT			
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	0	0	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	0	0	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	0	0	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	0	0	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	0	0	9
	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	V	U U	

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**Actual Value Expected Value** target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSC 0 0  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID11$ 0  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID12$ 0 0  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DMAC$ 0 0 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.FUN 0 0  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIR$ 0 0 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIN 0 0  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DOUT$ 0 0 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SET 0 0  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLR$ n 0 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.ODR 0 0 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PD n n target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSL 0 0 target\_SpurSnsrDataPtr\_Cnt\_T\_u16

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	~

0

0

Test Step 3.7 (Repeat Count = 1)	
Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	255
DigColPsInt_Buffer_Cnt_M_u08[1]	255
DigColPsInt_Buffer_Cnt_M_u08[2]	255
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	65535
DigColPsInt_CurrentSlave_Cnt_M_u08	127
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	4294967295
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	255
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt SpurSnsrData Cnt M u16	65535
DigColPsInt TransactionCnt Cnt M u08	255
DtrmnElapsedTime mS u16(ElapsedTime)	target DtrmnElapsedTime mS u16 ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c Send(I2cRegPtr Cnt T str)	target I2c Send I2cRegPtr Cnt T str
I2c SetupMasterTransmit(I2cRegPtr Cnt T str)	target I2c SetupMasterTransmit I2cRegPtr Cnt T str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1 temp	target_i2cREG1_temp
k ColSensorI2CAddress Cnt u08	127
k I2CHWInitTransactionTime Sec f32	10
target DtrmnElapsedTime mS u16 ElapsedTime	65535
target GetSystemTime mS u32 CurrentTime	4294967295
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023
target I2c Send I2cRegPtr Cnt T str.IMR	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	32767
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535
target I2c Send I2cRegPtr Cnt T str.CLKH	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	65535
target I2c Send I2cRegPtr Cnt T str.DRR	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	1023
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	255
target I2c Send I2cRegPtr Cnt T str.MDR	65535
target I2c Send I2cRegPtr Cnt T str.IVR	4095
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target I2c Send I2cRegPtr Cnt T str.PSC	255
target I2c Send I2cRegPtr Cnt T str.PID11	65535
	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	3
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3

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			•
Name	Input Value		
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	1023		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	255 32767		
target_I2C_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	65535		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	65535		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	65535		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	255		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	1023		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	255		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	65535		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	4095		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	255 65535		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	255		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL target_i2cREG1_temp.OAR	3 1023		
target i2cREG1 temp.IMR	255		
target i2cREG1 temp.STR	32767		
target i2cREG1 temp.CLKL	65535		
target_i2cREG1_temp.CLKH	65535		
target_i2cREG1_temp.CNT	65535		
target_i2cREG1_temp.DRR	255		
target_i2cREG1_temp.SAR	1023		
target_i2cREG1_temp.DXR	255		
target_i2cREG1_temp.MDR	65535		
target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR	4095		
target i2cREG1 temp.PSC	255		
target i2cREG1 temp.PID11	65535		
target_i2cREG1_temp.PID12	255		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	3		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR	3		
target i2cREG1 temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	255	255	~
DigColPsInt_Buffer_Cnt_M_u08[1]	255	255	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[2]	255	255	<b>✓</b>
DigColPsInt_BusBusySeqError_Cnt_M_Igc	0	0	✓
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE	READ_COMPLETE	<b>~</b>
DigColPsInt_GetData()	62	62	<b>✓</b>
DigColPoint_InitFailedOnce_Cnt_M_lgc	1	1	~
DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_PrevTransactionCnt_Cnt_M_u08	255	0 255	~
DigColPsInt_Prev1ransactionCnt_Cnt_M_uo8  DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	Ž
DigColPsInt_RecvoverranEnd_Cnt_w_gc  DigColPsInt_SensInitialized Cnt M Igc	1	1	
target_ColSnsrDataPtr_Cnt_T_u16	65535	65535	
target_DataTypePtr_Cnt_T_u08	5	5	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023	1023	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	255	255	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	32767	32767	~

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**Actual Value Expected Value**  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKL$ 65535 65535 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKH 65535 65535 65535 65535 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CNT target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DRR 255 255 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SAR 1023 1023  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DXR$ 255 255 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.MDR 65535 65535  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IVR$ 4095 4095 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.EMDR 3  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSC$ 255 255 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID11 65535 65535  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID12$ 255 255 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DMAC 3 3 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.FUN 1 1 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIR 3 3 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIN 3 3 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DOUT 3 3 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SET 3 3  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLR$ 3 3 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.ODR 3 3 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PD 3 3 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSL 3 3 1023  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.OAR$ 1023 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IMR 255 255  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.STR$ 32767 32767  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKL$ 65535 65535 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKH 65535 65535  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CNT$ 65535 65535 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DRR 255 255 target\_#2c\_SetupMasterrMasterit\_rlandsteig\_Pt2c\_ReP\_T\_str.SAR eport te□ 110213\_str.IVR r**éβ@t** teP target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR 255 255 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.MDR 65535 65535 N t T str.IVR target I2c Send I2cl

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DigColPsInt\_StartRequest

Project DigColPsInt
Module DigColPsInt

Test Object DigColPsInt\_StartRequest

#### Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %
MCC Coverage	90.9 %
MC/DC Coverage	90.9 %

#### **Statistics**

Total Testcases	3
Successful	3
Failed	0
Not Executed	0

#### **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\C1xx_DigColPs
Configuration File	D:\Synergy_Work_Area\C1xx_DigColPs\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\DigColPs\src\Sa_DigColPs\Int.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -DSTATIC= -D_inline= -l\$(PROJECTROOT)\DigColPs\utp\contract -l\$(PROJECTROOT)\DigColPs\utp\contract -l\$(PROJECTROOT)\DigColPs\utp\contract\Sa_DigColPs -l\$(PROJECTROOT)\DigColPs\utp\contract\Sa_DigColPs -l\$(PROJECTROOT)\StdDef\underlinclude -l\$(PROJECTROOT)\StdDef\underlinclude -l\$(PROJECTROOT)\StdDef\underlinclude\TMS570_HerculesRegs -l\$(Compiler Install Path)\underlinclude

Comments/Description/Spe	ecification
Name	Text





Module 'DigColPsInt' 

Name of Tester:Priti Mangalekar Code File(s) Under Test:Sa\_DigColPsInt.c Code File(s) Version:7

Module Design Document:DigColPsInt\_MDD.docx Module Design Document Version:8

Data Dictionary Version:9 Unit Test Plan Version:2

Unit Lest Plan Version:2
Optimization Level:Level 2
Compiler (CodeGen) Version:TMS470\_4.9.5
Model Type:Excel Macro
Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.30
Total FLASH Used (Bytes):N/A
Total RAM Used (Bytes):N/A Total CALS Used (Bytes):N/A Special Test Requirements: Test Date:10/13/2014 Comments:

NOTE 1: In """"DigColPsInt\_StartRequest"""" function, path """"(Type\_Cnt\_T\_u08 > D\_NONE\_CNT\_U08) = TRUE && (Type\_Cnt\_T\_u08 <= D\_STATUSREG\_CNT\_U08) = FALSE""" cannot be covered because range of """"Type\_Cnt\_T\_u08"""" is '0-5' and value of """"D\_STATUSREG\_CNT\_U08""" is '34'.

NOTE2: In function ""DigColPsInt\_GetData"",""DigColPsInt\_StartRequest"" and ""DigColPsInt\_InterruptNotification"" values for """12c\_Send(Length\_Cnt\_T\_u32)"""", """12c\_SetRecv(Length\_Cnt\_T\_u16)"""", """12c\_SetStatus(Status\_Cnt\_T\_u16)""", """12c\_SetUpMasterReceive(DataLength\_Cnt\_T\_u16)""" and 12c\_SetUpMasterTransmit(DataLength\_Cnt\_T\_u16) are ignored in few vectors as they

are taking garbage value when they are not updated with expected value in particular vector.

NOTE3: The return value of """"DigColPsInt\_GetData""" function is going out of range, anomaly """6156""" is raised for the same.

NOTE4:Range of DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum is considered as 0 to 36, as enum DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum is of type CommStepType which is of 37 elements.

NOTE5:In function ""DigColPsInt\_InterruptNotification"", path ""Case I2C\_RECV\_OVERRUN: True"" cannot be covered because range of ""Flags\_Cnt\_T\_b16"" is 0 to 64 given in MDD.

NOTE6:In function ""DigColPsInt\_InterruptNotification"", output variable ""DigColPsInt\_AttempOccurForCustDatRead\_Cnt\_M\_u08"" is going out

of range.'

Attributes	
Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	\$(Compiler Install Path)\include
Time Unit	Cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\Clxx_DigColPs\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP



#### **Test Case 1: Metrics Test**

Description

Test Vector Description:

TS1.1"Shortest Execution Path:

((DigColPsInt\_SensInitialized\_Cnt\_M\_lgc == TRUE) && (DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum >= INIT\_COMPLETE))=False" TS1.2"Longest Execution Path:

IS1.2\*Longest Execution Path:
((DigColPsInt\_SensInitialized\_Cnt\_M\_lgc == TRUE) && (DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum >= INIT\_COMPLETE))=True
((Status\_Cnt\_T\_u16 & I2C\_BUSBUSY) == 0U)=True
((Type\_Cnt\_T\_u08 == D\_ANGLEDATA\_CNT\_U08) && (DigColPsInt\_PrevReqDataType\_Cnt\_M\_u08 == D\_ANGLEDATA\_CNT\_U08))=False
((Type\_Cnt\_T\_u08 > D\_NONE\_CNT\_U08) && (Type\_Cnt\_T\_u08 <= D\_STATUSREG\_CNT\_U08))=False"

Test Step 1.1 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	44
DigColPsInt_Buffer_Cnt_M_u08[1]	55
DigColPsInt_Buffer_Cnt_M_u08[2]	66
DigColPsInt_CurrentSlave_Cnt_M_u08	55
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_READ
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt SensInitialized Cnt M Igc	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
I2c_GetStatus()	655
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt I2c Send I2cRegPtr Cnt T str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	3
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	55
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target i2cREG1 temp.PSL	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	55
tgt I2c GetStatus I2cRegPtr Cnt T str.IMR	66
tgt I2c GetStatus I2cRegPtr Cnt T str.STR	556
tgt I2c GetStatus I2cRegPtr Cnt T str.CLKL	2309
tgt I2c GetStatus I2cRegPtr Cnt T str.CLKH	1204
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT	87
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	67
tgt I2c GetStatus I2cRegPtr Cnt T str.SAR	55
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR	66
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR	2309
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	5
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC	66
tgt I2c GetStatus I2cRegPtr Cnt T str.PID11	1204
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR	1

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Name	Input Value
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	3

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Name	Input Value		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	3		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	55		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	66 556		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	2309		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	1204		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	87		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	67		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1 2		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	1 2 3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	1 2 3 3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name	1 2 3 3 Actual Value	Expected Value	Result
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]	1 2 3 3 3 Actual Value 44	44	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	1 2 3 3 3 Actual Value 44 55	44 55	Result
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	1 2 3 3 3 Actual Value 44 55 66	44 55 66	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08	1 2 3 3 3 Actual Value 44 55 66 55	44 55 66 55	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum	1 2 3 3 3 <b>Actual Value</b> 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PevReqDataType_Cnt_M_u08	1 2 3 3 3 Actual Value 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1 2 3 3 3 <b>Actual Value</b> 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc l2c_Send(Length_Cnt_T_u32)	1 2 3 3 3 <b>Actual Value</b> 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_igc l2c_Send(Length_Cnt_T_u32) l2c_SetRecv(Length_Cnt_T_u32)	1 2 3 3 3 <b>Actual Value</b> 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_igc l2c_Send(Length_Cnt_T_u32) l2c_SetRecv(Length_Cnt_T_u32) l2c_SetupMasterReceive(DataLength_Cnt_T_u16)	1 2 3 3 3 <b>Actual Value</b> 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc l2c_Send(Length_Cnt_T_u32) l2c_SetRecv(Length_Cnt_T_u32) l2c_SetupMasterReceive(DataLength_Cnt_T_u16) l2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1 2 3 3 3 <b>Actual Value</b> 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 0 0	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc l2c_Send(Length_Cnt_T_u32) l2c_SetRecv(Length_Cnt_T_u32) l2c_SetupMasterReceive(DataLength_Cnt_T_u16) tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR	1 2 3 3 3 <b>Actual Value</b> 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 0 55	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc l2c_Send(Length_Cnt_T_u32) l2c_SetRecv(Length_Cnt_T_u32) l2c_SetupMasterReceive(DataLength_Cnt_T_u16) tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR	1 2 3 3 3 <b>Actual Value</b> 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 0 0	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 55	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc l2c_Send(Length_Cnt_T_u32) l2c_SetRecv(Length_Cnt_T_u32) l2c_SetRecv(Length_Cnt_T_u32) l2c_SetupMasterReceive(DataLength_Cnt_T_u16) tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.JMR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	1 2 3 3 3 <b>Actual Value</b> 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 0 55 66	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 55 66	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc l2c_Send(Length_Cnt_T_u32) l2c_SetRecv(Length_Cnt_T_u32) l2c_SetupMasterReceive(DataLength_Cnt_T_u16) tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR	1 2 3 3 3 <b>Actual Value</b> 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 0 55 66 556	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 55 66 556	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc l2c_Send(Length_Cnt_T_u32) l2c_SetRecv(Length_Cnt_T_u32) l2c_SetLepMasterTransmit(DataLength_Cnt_T_u16) tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.JMR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	1 2 3 3 3 3 4 Actual Value 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 0 0 55 66 556 2309	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 55 66 556 2309	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc l2c_Send(Length_Cnt_T_u32) l2c_SetRecv(Length_Cnt_T_u32) l2c_SetLepMasterTransmit(DataLength_Cnt_T_u16) tgt_l2c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT	1 2 3 3 3 3 Actual Value 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 0 0 0 0 0 0 55 66 556 2309 1204	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 55 66 556 2309 1204	
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tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStave_Cnt_M_u08 DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc l2c_Setnd(Length_Cnt_T_u32) l2c_SetupMasterTransmit(DataLength_Cnt_T_u16) l2c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR	1 2 3 3 3 3 3 Actual Value 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 55 66 556 2309 1204 87 67	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc l2c_Send(Length_Cnt_T_u32) l2c_SetRecv(Length_Cnt_T_u32) l2c_SetLepMasterTransmit(DataLength_Cnt_T_u16) tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR	1 2 3 3 3 3 Actual Value 44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 0 1 0 0 0 0 0 55 66 2309 1204 87 67 55	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 55 66 556 2309 1204 87 67 55	
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tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc l2c_Send(Length_Cnt_T_u32) l2c_SetRecv(Length_Cnt_T_u32) l2c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_l2c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNC tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11 tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12 tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET	1 2 3 3 3 3 4 Actual Value 44 55 66 55 65 6	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 0 55 66 556 2309 1204 87 67 55 66 2309 5 3 66 1204 66 3 1 1 1 2 3 3	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_PrevReqDataType_Cnt_T_u16) tgt_l2c_SetRecv(Length_Cnt_T_u32) 12c_SetupMasterTransmit(DataLength_Cnt_T_u16) tgt_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PDD11 tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PDD12 tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR	1 2 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 55 66 556 2309 1204 87 67 55 66 2309 5 3 66 1204 66 3 1 1 1 2 3 3 1	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_SkipRegisterWrite_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_T_u16) DigColPsInt_SkipRegisterWrite_Cnt_T_str.OAR DigColPsInt_SkipRegisterWrite_Cnt_T_str.OAR DigColPsInt_I2c_GetStatus_l2cRegPtr_Cnt_T_str.DLR DigColPsInt_I2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL DigLi2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL DigLi2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR DigLi2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR DigLi2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR DigLi2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR DigLi2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR DigLi2c_GetStatus_l2cRegPtr_Cnt_T_str.DNA DigLi2c_GetStatus_l2cRegPtr_Cnt_T_str.DNT DigLi2c_GetStatus_l2cRegPtr_Cnt_T_str.DNT DigLi2c_GetStatus_l2cRegPtr_Cnt_T_str.	1 2 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 55 66 556 2309 1204 87 67 55 66 2309 5 3 66 1204 66 3 1 1 1 2 3 3 1	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_igc l2c_Send(Length_Cnt_T_u32) l2c_SetRecv(Length_Cnt_T_u32) l2c_SetRecv(Length_Cnt_T_u32) l2c_SetupMasterReceive(DataLength_Cnt_T_u16) l2c_SetupMasterTransmit(DataLength_Cnt_T_u16) l2t_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR l1c_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR l1c_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL l1c_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL l1c_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL l1c_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT l1c_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR l1c_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR l1c_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR l1c_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNC l1c_GetStatus_l2cRegPtr_Cnt_T_str.DNC l1c_l2c_GetStatus_l2cRegPtr_Cnt_	1 2 2 3 3 3 3 4 4 4 5 5 5 6 6 6 5 5 5 INIT_SENSOR2_CHECKSTAT_READ 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 55 66 556 2309 1204 87 67 55 66 2309 5 3 66 1204 66 3 1 1 1 2 3 3 3 1	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlepNo_Cnt_M_enum DigColPsInt_SkipRegisterWrite_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_T_u16) DigColPsInt_SkipRegisterWrite_Cnt_T_u16) DigColPsInt_SkipRegisterWrite_Cnt_T_u16) DigColPsInt_SkipRegisterWrite_Cnt_T_u16) DigColPsInt_SkipRegisterWrite_Cnt_T_u16) DigColPsInt_SkipRegisterWrite_Cnt_T_str.DRR DigColPsInt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL Digt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR Digt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR Digt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DNR Digt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DNR Digt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DNAC Digt_I2c_GetSt	1 2 2 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 55 66 556 2309 1204 87 67 55 66 2309 5 3 66 1204 66 3 1 1 1 2 3 3 3 1	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_igc l2c_Send(Length_Cnt_T_u32) l2c_SetRecv(Length_Cnt_T_u32) l2c_SetRecv(Length_Cnt_T_u32) l2c_SetupMasterReceive(DataLength_Cnt_T_u16) l2c_SetupMasterTransmit(DataLength_Cnt_T_u16) l2t_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR l1c_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR l1c_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL l1c_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL l1c_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL l1c_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT l1c_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR l1c_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR l1c_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR l1c_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNC l1c_GetStatus_l2cRegPtr_Cnt_T_str.DNC l1c_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNC l1c_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNC l1c_l2c_GetStatus_l2cReg	1 2 2 3 3 3 3 4 4 4 5 5 5 6 6 6 5 5 5 INIT_SENSOR2_CHECKSTAT_READ 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	44 55 66 55 INIT_SENSOR2_CHECKSTAT_READ 0 1 0 0 0 0 0 55 66 556 2309 1204 87 67 55 66 2309 5 3 66 1204 66 3 1 1 1 2 3 3 3 1	

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Name	Actual Value	Expected Value	Result
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	556	556	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	<u> </u>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	·
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	3	3	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>~</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	66	66	-
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	66	66	-
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	-
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	-
	1	1	•
tgt I2c SetupMasterReceive I2cReqPtr Cnt T str.CLR			
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	2	2 3	<b>✓</b>

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Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	66	66	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	556	556	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	87	87	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	55	55	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	2309	2309	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	3	3	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	1204	1204	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	3	3	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3	3	•

Τ				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 1.2 (Repeat Count = 1)	<b>▼</b>
Name	Input Value
DigColPsInt Buffer Cnt M u08[0]	10
DigColPsInt Buffer Cnt M u08[1]	20
DigColPsInt Buffer Cnt M u08[2]	30
DigColPsInt CurrentSlave Cnt M u08	40
DigColPsInt CurrentStepNo Cnt M enum	INIT COMPLETE
DigColPsInt PrevReqDataType Cnt M u08	1
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt SkipRegisterWrite Cnt M Igc	0
I2c GetStatus()	123
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c Send(I2cRegPtr Cnt T str)	tgt I2c Send I2cRegPtr Cnt T str
I2c SetRecv(I2cRegPtr Cnt T str)	tgt I2c SetRecv I2cRegPtr Cnt T str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str
Type_Cnt_T_u08	0
i2cREG1 temp	target i2cREG1 temp
k_ColSensorI2CAddress_Cnt_u08	10
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	78
target_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56
target_i2cREG1_temp.CNT	897
target_i2cREG1_temp.DRR	98
target_i2cREG1_temp.SAR	66
target_i2cREG1_temp.DXR	78
target_i2cREG1_temp.MDR	495
target_i2cREG1_temp.IVR	66
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	78
target_i2cREG1_temp.PID11	56
target_i2cREG1_temp.PID12	78
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0

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DigColFSini_StartRequest		TOPCION
Name	Input Value	
target i2cREG1 temp.CLR	0	
target i2cREG1 temp.ODR	1	
target_i2cREG1_temp.PD	0	
target_i2cREG1_temp.PSL	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR	66	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	78	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	78	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	495	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	56	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	897	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	98	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	66	
gt I2c GetStatus I2cRegPtr Cnt T str.DXR	78	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	495	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	66	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	78	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	56	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	78	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET	0	
	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR		
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PD	0	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	
	66	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR		
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	495	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	
gt I2c Send I2cRegPtr Cnt T str.PID12	78	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	
	78	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR		
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	56	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	98	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	66	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495	
	66	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR		
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	
	56	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11		
	78	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	78 0	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12 gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC		
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11 gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12 gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	0	

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Name	Input Value		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	0		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	78		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.NRR	78		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	495		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	66		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495 66		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	0		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	495 56		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	897		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	78		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	56   78		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	/Count
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	-
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	-
DigColPsInt_CurrentSlave_Cnt_M_u08	10	10	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE	INIT_COMPLETE	~
DigColPsInt_PrevReqDataType_Cnt_M_u08	0	0	_
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	<b>•</b>
I2c_Send(Length_Cnt_T_u32)	0	0	· ·
I2c_SetRecv(Length_Cnt_T_u32) I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	0	0	Ž
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	0	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	66	66	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	78	78	-
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	78	78	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	56	56	<b>✓</b>

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Name	Actual Value	Expected Value	Result
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	897	897	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	98	98	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	66	66	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	78	78	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	495	495	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	66	66	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	78	78	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	56	56	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	78	78	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	78	78	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	78	78	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	_
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	_
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	·
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	78	78	
	0	0	_
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC			
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	0	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	<b>~</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	66	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	78	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78	78	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	56	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	897	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	98	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66	66	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78	78	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495	495	
tgt I2c SetRecv I2cRegPtr Cnt T str.IVR	66	66	<b>✓</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	78	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	56	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	78	78	<u> </u>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	0	0	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	0	0	- J
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	0	0	
	1	1	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN			
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	0	0	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	1	1	·
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>~</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	66	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	78	78	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78	78	<b>✓</b>

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Name	Actual Value	Expected Value	Result
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	495	495	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	56	56	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	897	897	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	98	98	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	66	66	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	78	78	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	495	495	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.lVR	66	66	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	78	78	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	56	56	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	78	78	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	0	0	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	0	0	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0	0	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	0	0	✓
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	495	495	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✓

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c GetStatus	1	I2c GetStatus	1	



#### **Test Case 2: Boundary Test**

Description

Test Vector Description:

TS2.1Type\_Cnt\_T\_u08=min
TS2.2Type\_Cnt\_T\_u08=max
TS2.3Type\_Cnt\_T\_u08=mid
TS2.4k\_ColSensorl2CAddress\_Cnt\_u08=min
TS2.5k\_ColSensorl2CAddress\_Cnt\_u08=max
TS2.6k\_ColSensorl2CAddress\_Cnt\_u08=min

TS2.6k\_ColSensorl2CAddress\_Cnt\_u08=mid
TS2.7DigColPsInt\_PrevReqDataType\_Cnt\_M\_u08=min
TS2.8DigColPsInt\_PrevReqDataType\_Cnt\_M\_u08=min
TS2.8DigColPsInt\_PrevReqDataType\_Cnt\_M\_u08=mid
TS2.10l2c\_GetStatus = min
TS2.11l2c\_GetStatus = min
TS2.12l2c\_GetStatus = mid
TS2.12l2c\_GetStatus = mid
TS2.13DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum=min
TS2.14DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum=max
TS2.15DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum=mid
TS2.16DigColPsInt\_SensInitialized\_Cnt\_M\_lgc=min
TS2.17DigColPsInt\_SensInitialized\_Cnt\_M\_lgc=max
TS2.18all min

TS2.18all min TS2.19all max

Test Step 2.1 (Repeat Count = 1)	Input Value
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_CurrentSlave_Cnt_M_u08	40
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
2c_GetStatus()	123
2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
ype_Cnt_T_u08	0
2cREG1_temp	target_i2cREG1_temp
_ColSensorl2CAddress_Cnt_u08	10
arget_i2cREG1_temp.OAR	66
arget_i2cREG1_temp.IMR	78
arget_i2cREG1_temp.STR	78
arget_i2cREG1_temp.CLKL	495
arget_i2cREG1_temp.CLKH	56
arget_i2cREG1_temp.CNT	897
arget_i2cREG1_temp.DRR	98
arget_i2cREG1_temp.SAR	66
arget_i2cREG1_temp.DXR	78
arget_i2cREG1_temp.MDR	495
arget_i2cREG1_temp.IVR	66
arget_i2cREG1_temp.EMDR	0
arget_i2cREG1_temp.PSC	78
arget_i2cREG1_temp.PID11	56
arget_i2cREG1_temp.PID12	78
arget_i2cREG1_temp.DMAC	0
arget_i2cREG1_temp.FUN	0
arget_i2cREG1_temp.DIR	0
arget_i2cREG1_temp.DIN	1.
arget_i2cREG1_temp.DOUT	0
arget_i2cREG1_temp.SET	0
arget_i2cREG1_temp.CLR	0
arget_i2cREG1_temp.ODR	1
arget_i2cREG1_temp.PD	0
arget_i2cREG1_temp.PSL	0
at I2c GetStatus I2cRegPtr Cnt T str.OAR	66
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	78
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	78
pt I2c GetStatus I2cRegPtr Cnt T str.CLKL	495
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	56
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	897
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	98
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	66
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR	78
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR	495

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Name	Input Value
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC	78
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	56 78
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12 tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC	0
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR	0
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR	1
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	495
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	56
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT tot_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	897 98
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	66
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	78
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	495
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	66
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	78
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	0 1
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	0
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	0
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	66
tgt I2c SetRecv I2cRegPtr Cnt T str.IMR	78
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	78
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	495
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	56
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	66
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	0 78
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	56
tgt l2c SetRecv l2cRegPtr Cnt T str.PID12	78
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	0
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	0
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	66
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	78
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	78
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	495 56
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	897
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	98
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	66
tate_cottapinidotori tooorio_izortogr ti_Ont_i_att.OATt	100

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lame	Input Value		
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78		
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495		
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66		
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0		
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78		
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56		
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78		
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0		
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0		
yt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0		
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1		
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0		
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0		
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0		
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1		
pt I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	0		
t_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0		
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495		
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56		
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66		
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78		
yt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495		
pt I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	66		
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
t_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78		
yt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56		
	78		
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12			
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0		
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0		
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
yt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
lame	Actual Value	Expected Value	Res
igColPsInt_Buffer_Cnt_M_u08[0]	10	10	
igColPsInt Buffer Cnt M u08[1]	20	20	
igColPsint_Buffer_Cnt_M_u08[2]	30	30	
igColPsInt_CurrentSlave_Cnt_M_u08	10	10	
igColPsInt CurrentStepNo Cnt M enum			
	INIT_COMPLETE	INIT_COMPLETE	
igColPsInt_PrevReqDataType_Cnt_M_u08	0	0	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	
igColPsInt_PrevReqDataType_Cnt_M_u08	0 0 0	0 0 0	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32)	0 0 0	0 0 0	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32) cc_SetRecv(Length_Cnt_T_u32)	0 0 0 0	0 0 0 0	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc c_Send(Length_Cnt_T_u32) c_SetRecv(Length_Cnt_T_u32) c_SetupMasterReceive(DataLength_Cnt_T_u16) c_SetupMasterTransmit(DataLength_Cnt_T_u16)	0 0 0 0 0	0 0 0 0 0	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc igColPsInt_SkipRegisterWrite_Cnt_M_lgc igColPsInt_SkipRegisterWrite_Cnt_T_u32) igColPsInt_SkipRegisterWrite_Cnt_T_u16) igColPsInt_SkipRegisterWrite_Cnt_T_u16) igt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	0 0 0 0 0 0	0 0 0 0 0 0 0	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32) cc_SetRecv(Length_Cnt_T_u32) cc_SetupMasterReceive(DataLength_Cnt_T_u16) cc_SetupMasterTransmit(DataLength_Cnt_T_u16) pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	0 0 0 0 0 0 0 0 66 78	0 0 0 0 0 0 0 0 66 78	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32) cc_SetRecv(Length_Cnt_T_u32) cc_SetupMasterReceive(DataLength_Cnt_T_u16) cc_SetupMasterTransmit(DataLength_Cnt_T_u16) pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	0 0 0 0 0 0 0 0 66 78	0 0 0 0 0 0 0 0 66 78	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32) cc_SetRecv(Length_Cnt_T_u32) cc_SetupMasterReceive(DataLength_Cnt_T_u16) cc_SetupMasterTransmit(DataLength_Cnt_T_u16) pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	0 0 0 0 0 0 0 0 66 78 78 495	0 0 0 0 0 0 0 66 78 78 495	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32) cc_SetRecv(Length_Cnt_T_u32) cc_SetupMasterReceive(DataLength_Cnt_T_u16) cc_SetupMasterTransmit(DataLength_Cnt_T_u16) pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	0 0 0 0 0 0 0 0 66 78 78 495 56	0 0 0 0 0 0 0 66 78 78 495	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32) cc_SetRecv(Length_Cnt_T_u32) cc_SetupMasterReceive(DataLength_Cnt_T_u16) cc_SetupMasterTransmit(DataLength_Cnt_T_u16) pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	0 0 0 0 0 0 0 0 66 78 78 495 56	0 0 0 0 0 0 0 66 78 78 495 56	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32) cc_SetRecv(Length_Cnt_T_u32) cc_SetupMasterReceive(DataLength_Cnt_T_u16) cc_SetupMasterTransmit(DataLength_Cnt_T_u16) pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR	0 0 0 0 0 0 0 66 78 78 495 56 897	0 0 0 0 0 0 0 66 78 78 495 56 897	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32) cc_SetRecv(Length_Cnt_T_u32) cc_SetupMasterReceive(DataLength_Cnt_T_u16) cc_SetupMasterTransmit(DataLength_Cnt_T_u16) st_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR st_I2c_GetStatus_I2cRegPtr_Cnt_T_str.NR st_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR st_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL st_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL st_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL st_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT st_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT st_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR st_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR st_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR st_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	0 0 0 0 0 0 0 66 78 78 495 56 897 98	0 0 0 0 0 0 0 66 78 78 495 56 897 98	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32) cc_SetRecv(Length_Cnt_T_u32) cc_SetupMasterReceive(DataLength_Cnt_T_u16) cc_SetupMasterTransmit(DataLength_Cnt_T_u16) st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MR st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR	0 0 0 0 0 0 0 66 78 78 495 56 897 98 66 78	0 0 0 0 0 0 0 66 78 78 495 56 897 98 66 78	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32) cc_SetRecv(Length_Cnt_T_u32) cc_SetupMasterReceive(DataLength_Cnt_T_u16) cc_SetupMasterTransmit(DataLength_Cnt_T_u16) st_12c_GetStatus_12cRegPtr_Cnt_T_str.OAR st_12c_GetStatus_12cRegPtr_Cnt_T_str.MR st_12c_GetStatus_12cRegPtr_Cnt_T_str.STR st_12c_GetStatus_12cRegPtr_Cnt_T_str.CLKL st_12c_GetStatus_12cRegPtr_Cnt_T_str.CLKL st_12c_GetStatus_12cRegPtr_Cnt_T_str.CLKL st_12c_GetStatus_12cRegPtr_Cnt_T_str.CNT st_12c_GetStatus_12cRegPtr_Cnt_T_str.CNT st_12c_GetStatus_12cRegPtr_Cnt_T_str.DRR st_12c_GetStatus_12cRegPtr_Cnt_T_str.DRR st_12c_GetStatus_12cRegPtr_Cnt_T_str.DRR st_12c_GetStatus_12cRegPtr_Cnt_T_str.DXR st_12c_GetStatus_12cRegPtr_Cnt_T_str.DXR st_12c_GetStatus_12cRegPtr_Cnt_T_str.DXR st_12c_GetStatus_12cRegPtr_Cnt_T_str.DDR	0 0 0 0 0 0 0 66 78 78 495 56 897 98 66 78 495	0 0 0 0 0 0 0 66 78 78 495 56 897 98 66 78	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32) cc_SetRecv(Length_Cnt_T_u32) cc_SetupMasterReceive(DataLength_Cnt_T_u16) cc_SetupMasterTransmit(DataLength_Cnt_T_u16) st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MR st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR st_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR	0 0 0 0 0 0 0 66 78 78 495 56 897 98 66 78	0 0 0 0 0 0 0 66 78 78 495 56 897 98 66 78	
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igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32) cc_SetRecv(Length_Cnt_T_u32) cc_SetupMasterReceive(DataLength_Cnt_T_u16) cc_SetupMasterTransmit(DataLength_Cnt_T_u16) pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CkL pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CkL pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CkL pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CkL pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CkL pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CkL pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR	0 0 0 0 0 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78	0 0 0 0 0 0 0 0 66 78 495 56 897 98 66 78 495 66	
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igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32) cc_SetRecv(Length_Cnt_T_u32) cc_SetupMasterReceive(DataLength_Cnt_T_u16) cc_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetStatus_I2cRegPtr_Cnt_T_str.OAR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CKL ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CKL ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PDC ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD11 ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11 ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	0 0 0 0 0 0 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78	0 0 0 0 0 0 0 66 78 495 56 897 98 66 78 495 66 0 78	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32) cc_SetRecv(Length_Cnt_T_u32) cc_SetupMasterReceive(DataLength_Cnt_T_u16) cc_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetStatus_I2cRegPtr_Cnt_T_str.OAR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PDC ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD11 ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11 ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	0 0 0 0 0 0 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78	0 0 0 0 0 0 0 66 78 495 56 897 98 66 78 495 66 0 78	
igColPsInt_PrevReqDataType_Cnt_M_u08 igColPsInt_SkipRegisterWrite_Cnt_M_lgc cc_Send(Length_Cnt_T_u32) cc_SetRecv(Length_Cnt_T_u32) cc_SetupMasterReceive(DataLength_Cnt_T_u16) cc_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetupMasterTransmit(DataLength_Cnt_T_u16) ct_SetStatus_I2cRegPtr_Cnt_T_str.OAR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CKL ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CKL ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PDC ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD11 ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11 ct_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	0 0 0 0 0 0 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78	0 0 0 0 0 0 0 66 78 495 56 897 98 66 78 495 66 0 78	

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Name	Actual Value	Expected Value	Result
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	0	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR	0	0	
tgt I2c GetStatus I2cRegPtr Cnt T str.PD	0	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	78	78	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	56	56	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	897	897	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SAR tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	66 78	78	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	495	495	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	1	1	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	1	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	66	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	78	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	78	78	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	495	495	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	56	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	897	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	98	98	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	66	66	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78 495	78 495	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR tgt_l2c_SetRecv_l2cRegPtr_Cnt_T str.IVR	66	66	
tgt I2c SetRecv I2cRegPtr Cnt T str.EMDR	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	78	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	56	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	78	78	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	0	0	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	0	0	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	0	0	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	0	0	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	0	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	66	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78	78	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78	78	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495	495	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56	56	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897	897	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	98	98	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66	66	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	78	78	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495	495	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	0	0	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	78	78	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	56	56	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78	78	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	•

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Name	Actual Value	Expected Value	Result
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	1	1	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0	0	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	1	1	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	495	495	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~

T				~
Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	~

Test Step 2.2 (Repeat Count = 1)	<b>▼</b>
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	40
DigColPsInt_Buffer_Cnt_M_u08[1]	50
DigColPsInt_Buffer_Cnt_M_u08[2]	60
DigColPsInt_CurrentSlave_Cnt_M_u08	55
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_Igc	1
I2c_GetStatus()	554
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	5
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	20
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.MDR	566
target_i2cREG1_temp.IVR	554
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	44

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DigCoiPsini_StartRequest		( MAC ( Mac
Name	Input Value	
target i2cREG1 temp.PID11	4466	
target_i2cREG1_temp.PID12	44	
target_i2cREG1_temp.DMAC	1	
target_i2cREG1_temp.FUN	1	
target_i2cREG1_temp.DIR	2	
target_i2cREG1_temp.DIN	0	
target_i2cREG1_temp.DOUT	1	
target_i2cREG1_temp.SET	1	
target_i2cREG1_temp.CLR	2	
target_i2cREG1_temp.ODR	0	
target_i2cREG1_temp.PD	3	
target_i2cREG1_temp.PSL	3	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR	567	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	44	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	4444	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	566	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	129	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR	6	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	567	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR	44	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	566	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR	554	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FMDR	1	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC	44	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	4466	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	44	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	2	
	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN		
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	1	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	2	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	567	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	44	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	4466	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	
	6	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR		
gt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	
	44	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC		
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	44	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	
gt I2c Send I2cRegPtr Cnt T str.DIN	0	
· · · ·	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT		
gt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	2	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	0	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	3	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	4444	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	566	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	4466	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	567	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	
gt_ize_octiveev_izervegi ti_ont_i_str.b/tiv		
gg_lzc_octreev_lzchegf ti_ont_1_str.bkr	566	

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DigColPsInt\_StartRequest

		(	10-10
Name	Input Value		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	4466		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	566		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	567		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	44		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	566		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	554		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
Name	Actual Value	Expected Value	Resul
DigColPsInt_Buffer_Cnt_M_u08[0]	34	34	Nesul
DigColPsInt_Buffer_Cnt_M_u08[1]	50	50	
DigColPsInt_Buffer_Cnt_M_u08[2]	60	60	
DigColPsInt_GurrentSlave_Cnt_M_u08	20	20	
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG	READ_SENSOR1_SETREG 5	
DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkinRegisterWrite_Cnt_M_loc	5	0	
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc I2c Send(Length Cnt T u32)	1	1	
120 Ochu(Lengur Ont 1 d32)			

 $I2c\_Send(Length\_Cnt\_T\_u32)$ 

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Name	Actual Value	Expected Value	Result
I2c_SetRecv(Length_Cnt_T_u32)	0	0	<b>✓</b>
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	0	0	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>V</b>
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH	566 4466	566 4466	<b>*</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>~</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR	44	44	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR	554	554	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR	1	1	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC	44	44	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	4466 44	4466 44	<b>*</b>
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12 tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC	1	1	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	-
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT	1	1	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET	1	1	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR	2	2	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	3	3	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	567	567	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>*</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	4444 566	4444 566	~
tgt_I2c_Sent_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	V
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	6	6	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	554	554	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	44 4466	44 4466	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11 tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	44	44	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	1	1	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>V</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PD tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3	3	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	567	567	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	566	566	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	129	129	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	567	567	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	<b>V</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	44	44	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	44	4466	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	44	44	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
		1	<b>~</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	•	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	2	2	~
			~

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Name	Actual Value	Expected Value	Result
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	1	1	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	2	2	_
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>✓</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
tgt I2c SetRecv I2cRegPtr Cnt T str.PSL	3	3	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>*</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.NRN  tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	
	129	129	_
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT			
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	-
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>~</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	566	566	<b>~</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	554	554	<b>~</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	1	1	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✓
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	✓
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	✓
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	✓
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✓
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	0	0	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	567	567	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	44	44	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	4444	4444	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	566	566	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	_
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	44	44	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	_
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	~
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	1	1	
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	44	44	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	1	1	-
	1	1	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	2	2	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	0	0	<b>~</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✓

T				V
Actual Function	Count	Expected Function	Coun	Result
I2c_GetStatus	1	I2c_GetStatus	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c. Send	1	I2c. Send	1	

Test Step 2.3 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	70
DigColPsInt_Buffer_Cnt_M_u08[1]	80
DigColPsInt_Buffer_Cnt_M_u08[2]	90
DigColPsInt_CurrentSlave_Cnt_M_u08	60
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE

DigColPsInt\_StartRequest

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DigColFSIII_StattRequest	
Name	Input Value
igColPsInt_PrevReqDataType_Cnt_M_u08	3
higColPsInt_SensInitialized_Cnt_M_lgc	1
bigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
2c_GetStatus()	766
2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(l2cRegPtr_Cnt_T_str) 2c_SetupMasterReceive(l2cRegPtr_Cnt_T_str)	tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
ype_Cnt_T_u08	3
ccREG1_temp	target_i2cREG1_temp
_ColSensorl2CAddress_Cnt_u08	30
arget_i2cREG1_temp.OAR	65
arget_i2cREG1_temp.IMR	89
rget_i2cREG1_temp.STR	67
rget_i2cREG1_temp.CLKL	7
rget_i2cREG1_temp.CLKH	577
rget_i2cREG1_temp.CNT	88
rget_i2cREG1_temp.DRR	23
rget_i2cREG1_temp.SAR	65
rget_i2cREG1_temp.DXR	89
rget_i2cREG1_temp.MDR	7
arget_i2cREG1_temp.IVR	44
arget_i2cREG1_temp.EMDR	2
arget_i2cREG1_temp.PSC	89
urget_i2cREG1_temp.PID11	577
irget_i2cREG1_temp.PID12	89
arget_i2cREG1_temp.DMAC	2 0
arget_i2cREG1_temp.FUN	0
arget_i2cREG1_temp.DIR arget_i2cREG1_temp.DIN	1
rget_i2cREG1_temp.DOUT	2
rget_i2cREG1_temp.SET	2
arget i2cREG1 temp.CLR	0
arget_i2cREG1_temp.ODR	1
arget_i2cREG1_temp.PD	2
arget i2cREG1 temp.PSL	0
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	65
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	89
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	67
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	7
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	577
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	88
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	23
t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	65
t_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR	89
t_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR	7
t_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR	44
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	2
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	89
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	577
t_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12	89
t_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC	2
t_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN t l2c GetStatus_l2cRegPtr_Cnt_T_str.DIR	0
	1
t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
t_l2c_GetStatus_l2cRegPtr_Cnt_T_str.bET	2
t_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR	0
t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1
t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	2
t_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	0
t_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	65
t_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	89
t_l2c_Send_l2cRegPtr_Cnt_T_str.STR	67
t_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	7
t_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	577
ıt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88
pt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23
yt_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	65
pt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
pt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7
gt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44

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Name	Input Value	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
tgt I2c Send I2cRegPtr Cnt T str.PD	2	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	67	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	7	
	577	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	88	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.STR	67	
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	7	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	577	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	88	
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.DRR	23	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	65	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	7	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	44	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	2	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	577	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	89	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	2	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	67	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	7	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	577	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	23	
TO THE SHIPMASTER PARENT LICEPOPER COLUMN SAR	65	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	

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Name				
Signate   September   Septem	Name	Input Value		
19, Dr. Spinspharenermen (Descripting Cent. of an international processing Cent. of	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7		
Sign	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44		
12   12   12   13   13   14   15   15   15   15   15   15   15	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2		
### 1942 C.S. ExploRetare Transment (24-06-07) C. J. EMPLAN  19. C.S. ExploRetare Transment (24-06-07) C. J. EMPLAN  19. C.S. ExploRetare Transment (24-06-07) C. J. J. EMPLAN  19. C.S. ExploRetare Transment (24-06-07)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89		
### DE GENERALEMENT FORMER   DESCRIPTION OF   ### DE GENERALEMENT   DESCRIPTION OF   ### DE GENE	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577		
Mile   Description   Descrip	tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	89		
B. D. S. SENSANSON TRAINERS   D. S. S. SENSANSON TRAINERS   D. S. SENSANSON TRAINERS   D. S. SENSANS	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
March   Description   Descri	tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	0		
The Committee of Teacher Content of Teacher Court	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
10   2.5 establaster Transmit (Zetagoph Cot T at SCT P   1	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
Dec	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
19   D. S. SELIPA MARTEN TOWN   D. T.   B. F.	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2		
10, IZ. SepulyAsserTreamIL (ZeRopt Co. T. ± BPD   2	tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	0		
Dec	tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	1		
Actual Value   Expected Value   Expected Value   Expected Value   Result		2		
Name				
Digitable   Berlin Cirt   M. 1980     80   80   90   90   90   90   90			Expected Value	Result
DigoClaPini, Buffer, Chit M_U08 1   00   90   V   DigoClaPini, Durine (Save_Crit M_U08)   00   90   V   DigoClaPini, CurrentSave_Crit M_U08   20   30   30   V   DigoClaPini, CurrentSave_Crit M_U08   3   3   3   V   DigoClaPini, ProvReqUatal Type_Crit M_U08   3   0   0   0   V   22. Sendicult_englin_CritU22   1   1   1   V   22. Sendicult_englin_CritU22   0   0   0   0   V   23. Sendicult_englin_CritU22   0   0   0   0   V   24. Sendicult_englin_CritU23   0   0   0   0   V   25. Sendicult_englin_CritU23   0   0   0   0   V   26. Sendicult_englin_CritU23   0   0   0   0   V   26. Sendicult_englin_CritU23   0   0   0   0   V   26. Sendicult_englin_CritU24   0   0   0   0   V   26. Sendicult_englin_CritT4 trOAR   0   0   0   0   V   26. Sendicult_englin_CritT4 trOAR   0   0   0   0   V   26. Sendicult_englin_CritT4 trOAR   0   0   0   0   0   V   27. 28. Cendicult_englin_CritT4 trOAR   0   0   0   0   0   0   0   0   0   28. Englishate_Endergin_CritT4 trOAR   0   0   0   0   0   0   0   0   0			· · · · · · · · · · · · · · · · · · ·	
DoColfenian, Current/Stephen, Crit. M. u008				
DepoPaper   CurrentShine, Crit M_UBB				
DigCoParini, Currentise Pub. Cut II, Manum				
DepoClariest, Province Charlanger Cent, M. 198   3   3   2				
DispOnderListung Cont, Murge  1				
Institute   Inst				
22. SelfeyAbsterTanent(Data (T.) (12)				
Inc.   Setuphidate Framewill Oblait Legit, C.H	_ , , , ,			
I	I2c_SetRecv(Length_Cnt_T_u32)			
Signature   Constitution   Excellength Cont.   Tuth CoARE	I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	0	0	
Fig.   20. CellStatus   2.CRegPtPt Cnt   T_str MR   89   89   7   7   7   7   7   7   7   7   7	I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	
Section   Sect	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	65	65	~
Fig.   CelSalata   ZeRegPtr Cnt_T str CNK   7   7   7   7   9   9   9   9   9   9	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	89	89	
Section   Sect	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	67	67	✓
Total   Committee   Committe	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	577	577	<b>✓</b>
	tgt I2c GetStatus I2cRegPtr Cnt T str.CNT	88	88	
Fig. 126_GelStatus   12cRepPPL_CNLT_SIT_SAR   89   89   89   89   89   89   89   8		23	23	<b>✓</b>
			65	
Institute   Inst				<b>✓</b>
Igt   12c GelStatus   12cRegPtr_Cnt_Tstr.NVR				
Sq.   12c. GetStatus   12cRegPt Cnt_T str.EMDR   2   2   2   V   Igt_12c, GetStatus   12cRegPt Cnt_T str.PSC   89   89   9   V   Igt_12c, GetStatus   12cRegPt Cnt_T str.PDC   1577   577   577   577   V   Igt_12c, GetStatus   12cRegPt Cnt_T str.PDC   1577   15		44	44	~
Institute   Inst				
Total   Tota				
tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DID12         89         89           vgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DMAC         2         2           vgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DNA         0         0           vgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DIR         0         0           vgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DIN         1         1           vgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DOUT         2         2           vgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DOUT         2         2           vgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DODR         0         0           vgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DODR         1         1           vgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DODR         1         1           vgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DOR         0         0           vgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DAR         6         65           vgt_12c_Send_12cRegPtr_Cnt_T_str.DAR         89         89           vgt_12c_Send_12cRegPtr_Cnt_T_str.Dar         6         65           vgt_12c_Send_12cRegPtr_Cnt_T_str.Dar         6         65           vgt_12c_Send_12cRegPtr_Cnt_T_str.Dar         7         7           vgt_12c_Send_12cRegPtr_Cnt_T_str.Dar         88         88           vgt_12c_Send_12cRegPtr_Cnt_T_str.Dar         2 <td></td> <td></td> <td></td> <td></td>				
tgl. 12c. GetStatus 12cRegPTr_Cnt_Tstr.DMAC         2         2           tgl. 12c. GetStatus 12cRegPtr_Cnt_Tstr.DIR         0         0           tgl. 12c. GetStatus 12cRegPtr_Cnt_Tstr.DIR         0         0           tgl. 12c. GetStatus 12cRegPtr_Cnt_Tstr.DIR         0         0           tgl. 12c. GetStatus 12cRegPtr_Cnt_Tstr.DOWT         2         2           tgl. 12c. GetStatus 12cRegPtr_Cnt_Tstr.DOWT         2         2           tgl. 12c. GetStatus 12cRegPtr_Cnt_Tstr.CLR         0         0           tgl. 12c. GetStatus 12cRegPtr_Cnt_Tstr.DOWT         1         1           tgl. 12c. GetStatus 12cRegPtr_Cnt_Tstr.DOWT         2         2           tgl. 12c. GetStatus 12cRegPtr_Cnt_Tstr.DOWT         1         1           tgl. 12c. GetStatus 12cRegPtr_Cnt_Tstr.DOWT         2         2           tgl. 12c. Send 12cRegPtr_Cnt_Tstr.DOWT         2         2           tgl. 12c. Send 12cRegPtr_Cnt_Tstr.IMR         85         86           tgl. 12c. Send 12cRegPtr_Cnt_Tstr.IMR         89         89           tgl. 12c. Send 12cRegPtr_Cnt_Tstr.Clk         7         7           tgl. 12c. Send 12cRegPtr_Cnt_Tstr.Clk         7         7           tgl. 12c. Send 12cRegPtr_Cnt_Tstr.DRR         23         23           tgl. 12c. Send 12cRegPtr_Cnt_Tstr.DRR				
tgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.FUN         0         0         Vtgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.DIR         0         0         0         Vtgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.DIN         1         1         1         Vtgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.DOUT         2         2         Vtgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.DOUT         2         2         Vtgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.SET         2         2         Vtgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.CLR         0         0         Vtgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.DOR         1         1         1         Vtgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.DOR         1         1         1         Vtgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.DOR         1         1         1         Vtgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.DOR         6         0         0         Vtgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.DOR         6         6         6         Vtgl_12c_Send_12cRegPtr_Cnt_Tstr.DAR         6         6         6         Vtgl_12c_Send_12cRegPtr_Cnt_Tstr.DAR         6         6         6         Vtgl_12c_Send_12cRegPtr_Cnt_Tstr.DAR         6         6         6         Vtgl_12c_Send_12cRegPtr_Cnt_Tstr.DAR         6         6         7         Vtgl_12c_Send_12cRegPtr_Cnt_Tstr.DAR         6         6         6         Vtgl_12c_Send_12cRegPtr_Cnt_Tstr.DAR         8         8         8         8         8         8         8<				
tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DIR         0         0         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.DIN         1         1         1         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.DOUT         2         2         2         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.SET         2         2         2         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.DER         0         0         0         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.DDR         1         1         1         1         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.DDR         1         1         1         1         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.DDR         2         2         2         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.DAR         0         0         0         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.DAR         0         0         0         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.DAR         65         65         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.DAR         65         65         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.DAR         89         89         89         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.DAR         89         89         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.DAR         67         67         67         67         47         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.DAR         88         88         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.DAR         88         88         Vtg_12c_GetStatus_12cRegPtr_Cnt_T_str.DAR         65				
tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DDN         1         1         1         vtgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DDUT         2         2         vtgt_12c_GetStatus_12cRegPtr_Cnt_T_str.SET         2         ytgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DDR         0         0         vtgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DDR         1         1         1         ytgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DDR         1         1         1         ytgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DDR         1         1         1         ytgt_12c_GetStatus_12cRegPtr_Cnt_T_str.Dt_DT_str.DDR         1         1         1         ytgt_12c_GetStatus_12cRegPtr_Cnt_T_str.Dt_D				
tgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.DOUT         2         2           tgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.SET         2         2           tgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.CLR         0         0           tgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.DOR         1         1           tgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.DD         2         2           tgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.DAR         6         0           tgl_12c_GetStatus_12cRegPtr_Cnt_Tstr.DAR         65         65           tgl_12c_Send_12cRegPtr_Cnt_Tstr.DAR         65         65           tgl_12c_Send_12cRegPtr_Cnt_Tstr.CLR         7         67           tgl_12c_Send_12cRegPtr_Cnt_Tstr.CLK         7         7           tgl_12c_Send_12cRegPtr_Cnt_Tstr.CLK         7         7           tgl_12c_Send_12cRegPtr_Cnt_Tstr.DAR         88         88           tgl_12c_Send_12cRegPtr_Cnt_Tstr.DAR         23         23           tgl_12c_Send_12cRegPtr_Cnt_Tstr.DAR         89         89           tgl_12c_Send_12cRegPtr_Cnt_Tstr.DAR         65         65           tgl_12c_Send_12cRegPtr_Cnt_Tstr.DAR         89         89           tgl_12c_Send_12cRegPtr_Cnt_Tstr.DAR         44         44           tgl_12c_Send_12cRegPtr_Cnt_Tstr.DAR         2         2				-
tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.CLR         0         0         0         vtgt_12c_GetStatus_12cRegPtr_Cnt_T_str.CLR         0         0         0         vtgt_12c_GetStatus_12cRegPtr_Cnt_T_str.ODR         1         1         1         vtgt_12c_GetStatus_12cRegPtr_Cnt_T_str.ODR         1         1         1         vtgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DD         2         2         2         vtgt_12c_GetStatus_12cRegPtr_Cnt_T_str.ORR         65         65         65         vtgt_12c_Send_12cRegPtr_Cnt_T_str.ORR         89         89         89         vtgt_12c_Send_12cRegPtr_Cnt_T_str.DRR         89         89         vtgt_12c_Send_12cRegPtr_Cnt_T_str.CLKL         7         7         7         vtgt_12c_Send_12cRegPtr_Cnt_T_str.CLKL         7         7         7         vtgt_12c_Send_12cRegPtr_Cnt_T_str.CNT         88         89         89         89         89         89         89         89				
tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.CLR         0         0         V           tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DDR         1         1         1         V           tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DD         2         2         2         V <td></td> <td></td> <td></td> <td></td>				
tgt 12c_GetStatus_12cRegPtr_Cnt_T_str.ODR         1         1         1         vtgt 12c_GetStatus_12cRegPtr_Cnt_T_str.PD         2         2         2         vtgt 12c_GetStatus_12cRegPtr_Cnt_T_str.PSL         0         0         vtgt 12c_GetStatus_12cRegPtr_Cnt_T_str.PSL         0         0         vtgt 12c_GetStatus_12cRegPtr_Cnt_T_str.DAR         65         65         vtgt 12c_Send_12cRegPtr_Cnt_T_str.IMR         89         89         vtgt 12c_Send_12cRegPtr_Cnt_T_str.DIR         67         67         67         vtgt 12c_Send_12cRegPtr_Cnt_T_str.CLKL         7         7         vtgt 12c_Send_12cRegPtr_Cnt_T_str.CLKH         577         577         vtgt 12c_Send_12cRegPtr_Cnt_T_str.CNT         88         88         vtgt 12c_Send_12cRegPtr_Cnt_T_str.DRR         23         23         23         vtgt 12c_Send_12cRegPtr_Cnt_T_str.DRR         23         23         23         vtgt 12c_Send_12cRegPtr_Cnt_T_str.DXR         89         89         89         vtgt 12c_Send_12cRegPtr_Cnt_T_str.DXR         89         89         89         vtgt 12c_Send_12cRegPtr_Cnt_T_str.DNR         7         7         vtgt 12c_Send_12cRegPtr_Cnt_T_str.DNR         2         2         2         vtgt 12c_Send_12cRegPtr_Cnt_T_str.DNR         2         2         2         vtgt 12c_Send_12cRegPtr_Cnt_T_str.DNC         2         2         vtgt 12c_Send_12cRegPtr_Cnt_T_str.DNAC         2         2         2         vtgt 12c_Send_1				
tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PD         2         2         vtgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PSL           tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR         65         65         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.DAR         65         65         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.IMR         89         89         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.IMR         89         89         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.DAR         67         67         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.CLKL         7         7         7         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.CLKH         577         577         577         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.DAR         88         88         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.DAR         23         23         23         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.DAR         65         65         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.DAR         89         89         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.DAR         89         89         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.DAR         44         44         44         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.PAR         2         2         2         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11         577         577         577         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11         577         577         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID12         89         89         89         vtgt_!2c_Send_!2cRegPtr_Cnt_T_str.DINC         2         2 <td></td> <td></td> <td></td> <td></td>				
tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PSL       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.OAR       65       65         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.IMR       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.Str.R       67       67         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CLKL       7       7         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CLKH       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CNT       88       88         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DRR       23       23         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DRR       23       23         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DXR       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DXR       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.MDR       7       7         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.MDR       7       7         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PSC       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       0       0				
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.OAR       65       65         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.IMR       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.STR       67       67         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CLKL       7       7         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CLKH       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CNT       88       88         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DRR       23       23         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DAR       65       65         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DXR       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.MDR       7       7         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.MDR       7       7         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PSC       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DID42       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIDAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DINAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       0       0				
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.IMR       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.STR       67       67         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CLKL       7       7         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CLKH       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CNT       88       88         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DRR       23       23         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DRR       65       65         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DXR       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.MDR       7       7         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.IVR       44       44         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PSC       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID12       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       0       0				
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CLKL       67       67         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CLKL       7       7         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CLKH       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CNT       88       88         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DRR       23       23         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DXR       65       65         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DXR       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.MDR       7       7         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.NVR       44       44         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID12       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       1       1				
tgt 12c_Send_12cRegPtr_Cnt_T_str.CLKL       7       7         tgt_12c_Send_12cRegPtr_Cnt_T_str.CLKH       577       577         tgt_12c_Send_12cRegPtr_Cnt_T_str.CNT       88       88         tgt_12c_Send_12cRegPtr_Cnt_T_str.DRR       23       23         tgt_12c_Send_12cRegPtr_Cnt_T_str.SAR       65       65         tgt_12c_Send_12cRegPtr_Cnt_T_str.DXR       89       89         tgt_12c_Send_12cRegPtr_Cnt_T_str.MDR       7       7         tgt_12c_Send_12cRegPtr_Cnt_T_str.IVR       44       44         tgt_12c_Send_12cRegPtr_Cnt_T_str.EMDR       2       2         tgt_12c_Send_12cRegPtr_Cnt_T_str.EMDR       2       2         tgt_12c_Send_12cRegPtr_Cnt_T_str.PSC       89       89         tgt_12c_Send_12cRegPtr_Cnt_T_str.PID11       577       577         tgt_12c_Send_12cRegPtr_Cnt_T_str.PID12       89       89         tgt_12c_Send_12cRegPtr_Cnt_T_str.DMAC       2       2         tgt_12c_Send_12cRegPtr_Cnt_T_str.DMAC       2       2         tgt_12c_Send_12cRegPtr_Cnt_T_str.DIR       0       0         tgt_12c_Send_12cRegPtr_Cnt_T_str.DIR       0       0         tgt_12c_Send_12cRegPtr_Cnt_T_str.DIR       0       0				
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CLKH       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CNT       88       88         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DRR       23       23         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.SAR       65       65         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DXR       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.MDR       7       7         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.IVR       44       44         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PSC       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID12       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.FUN       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       1       1				
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.CNT       88       88         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DRR       23       23         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.SAR       65       65         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DXR       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.MDR       7       7         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.IVR       44       44         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PSC       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID12       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.FUN       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       1       1	tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DRR       23       23         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.SAR       65       65         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DXR       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.MDR       7       7         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.IVR       44       44         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PSC       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID12       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.FUN       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       1       1	tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.SAR       65       65         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DXR       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.MDR       7       7         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.IVR       44       44         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PSC       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID12       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.FUN       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       1       1	tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	88	88	<b>✓</b>
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DXR     89     89       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.MDR     7     7       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.IVR     44     44       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR     2     2       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PSC     89     89       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11     577     577       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID12     89     89       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC     2     2       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC     2     2       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.FUN     0     0       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR     0     0       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR     0     0       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN     1     1	tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	23	23	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DXR       89       89         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.MDR       7       7         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IVR       44       44       44         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR       2       2       2         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC       89       89       4         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11       577       577       577         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12       89       89       4         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC       2       2       2         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN       0       0       4         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR       0       0       4         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR       0       0       4         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN       1       1       4	tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	65	65	~
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.MDR     7     7       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.IVR     44     44       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR     2     2       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PSC     89     89       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11     577     577       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID12     89     89       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC     2     2       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.FUN     0     0     V       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR     0     0     V       tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN     1     1     V		89	89	~
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.IVR       44       44       44         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PSC       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID12       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.FUN       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       1       1		7	7	<b>~</b>
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PSC       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID12       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.FUN       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       1       1			44	<b>~</b>
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PSC       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID12       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.FUN       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       1       1				<b>✓</b>
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID11       577       577         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID12       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.FUN       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       1       1				
tgt_!2c_Send_!2cRegPtr_Cnt_T_str.PID12       89       89         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.FUN       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       1       1				
tgt_!2c_Send_i2cRegPtr_Cnt_T_str.DMAC       2       2         tgt_!2c_Send_i2cRegPtr_Cnt_T_str.FUN       0       0         tgt_!2c_Send_i2cRegPtr_Cnt_T_str.DIR       0       0         tgt_!2c_Send_i2cRegPtr_Cnt_T_str.DIN       1       1				
tgt_!2c_Send_i2cRegPtr_Cnt_T_str.FUN       0       0       ✓         tgt_!2c_Send_i2cRegPtr_Cnt_T_str.DIR       0       0       ✓         tgt_!2c_Send_i2cRegPtr_Cnt_T_str.DIN       1       1       ✓				
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR       0       0         tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN       1       1				
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN 1 1				
19[_120_00110_1201109f II_0111_1_511.D001]				
	tgt_izo_ocita_izot/cgr ti_otit_i_sti.boot	4	4	

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Name	Actual Value	Expected Value	Resul
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	•
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	•
gt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	1	1	•
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	•
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65	65	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89 67	89 67	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7	7	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	577	577	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	88	88	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	23	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	65	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89	89	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7	7	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44	44	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	2	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89	89	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577	577	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89	89	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	0	0	•
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	0	0	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	2	2	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	•
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	65	•
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	89	•
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	67	67	•
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7	7	•
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577	577	•
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	88	88	•
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23	23	•
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65	65	•
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	89	89	•
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	7	7	•
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	44	44	•
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	•
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89	89	,
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577	577	'
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89	89	,
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	'
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	•
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	•
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	0	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR			
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1 2	2	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	65	65	
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR			
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89 67	89 67	
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7	7	
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	577	577	
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	88	88	
gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	23	23	
gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.bRR  gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	65	65	
gt_lzc_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.5AR gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	89	89	
gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR  gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	7	7	
gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	44	44	
gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.tvR  gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	2	2	
gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	89	89	
gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	577	577	
	89	89	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	2	2	
at 12c SetunMasterTransmit 12cReaPtr Cnt   etr 1MAC			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	

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Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	•

T				V
Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	~
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c_Send	1	I2c_Send	1	<b>✓</b>

Test Step 2.4 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	3
DigColPsInt_Buffer_Cnt_M_u08[1]	6
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_CurrentSlave_Cnt_M_u08	69
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	4
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
2c_GetStatus()	788
2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt I2c SetRecv I2cRegPtr Cnt T str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	1
2cREG1_temp	target_i2cREG1_temp
c_ColSensorl2CAddress_Cnt_u08	0
arget_i2cREG1_temp.OAR	10
arget_i2cREG1_temp.IMR	10
	1223
arget_i2cREG1_temp.STR	
arget_i2cREG1_temp.CLKL	7846
arget_i2cREG1_temp.CLKH	8974
arget_i2cREG1_temp.CNT	98
arget_i2cREG1_temp.DRR	12
arget_i2cREG1_temp.SAR	10
arget_i2cREG1_temp.DXR	10
arget_i2cREG1_temp.MDR	7846
arget_i2cREG1_temp.IVR	55
arget_i2cREG1_temp.EMDR	1
arget_i2cREG1_temp.PSC	10
arget_i2cREG1_temp.PID11	8974
arget_i2cREG1_temp.PID12	10
arget_i2cREG1_temp.DMAC	1
arget_i2cREG1_temp.FUN	1
arget_i2cREG1_temp.DIR	2
arget_i2cREG1_temp.DIN	1
arget_i2cREG1_temp.DOUT	1
arget_i2cREG1_temp.SET	1
arget_i2cREG1_temp.CLR	2
	1
arget_i2cREG1_temp.ODR	
arget_i2cREG1_temp.PD	1
arget_i2cREG1_temp.PSL	1
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	10
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	10
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	1223
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	8974
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	98
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR	12
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	10
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	10
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	7846
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	55

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Name	Input Value	
gt I2c GetStatus I2cRegPtr Cnt T str.EMDR	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	10	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	8974	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	10	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	
	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR		
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT	1	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	8974	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10	
	8974	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11		
gt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	10	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
gt I2c Send I2cRegPtr Cnt T str.PD	1	
	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL		
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	10	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	10	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	1223	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	8974	
gt I2c SetRecv I2cRegPtr Cnt T str.CNT	98	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	
pt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10	
	10	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR		
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846	
pt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55	
pt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	
t_12c_SetRecv_12cRegPtr_Cnt_T_str.FUN	1	
t_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	2	
	1	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN		
yt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	
pt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	
pt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1	
t_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10	
t_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	10	
	1223	
t_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR		
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	10	
	10	

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		(	10-10
Name	Input Value		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	8974		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.PID12	10		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.DIN	1		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	1		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.SET	1		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	2		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	1		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	1		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.PSL	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	10		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	7846		
	8974		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	98		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	12		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	10		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	7846		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	10		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	2		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	32	32	-
DigColPsInt Buffer Cnt M u08[1]	6	6	·
DigColPsInt_Buffer_Cnt_M_u08[2]	9	9	-
DigColPsInt_CurrentSlave_Cnt_M_u08	0	0	•
DigColPsInt CurrentStepNo Cnt M enum	READ_SENSOR1_SETREG	READ_SENSOR1_SETREG	-
DigColPsInt PrevReqDataType Cnt M u08	1	1	-
DigColPsInt SkipRegisterWrite Cnt M Igc	0	0	_
I2c Send(Length Cnt T u32)	1	1	-
I2c_SetRecv(Length_Cnt_T_u32)	0	0	
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	0	0	<b>✓</b>
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	10	10	-
tgt I2c GetStatus I2cRegPtr Cnt T str.IMR	10	10	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	1223	1223	-
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	7846	7846	
	8974	8974	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	98		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT		98	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	12	12	<b>*</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	10	10	<b>✓</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	10	10	<b>✓</b>
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR	7846	7846	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	55	55	<b>~</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	10	10	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	8974	8974	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	10	10	-
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	-

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Name	Actual Value	Expected Value	Result
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET		1	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR	2	2	<b>*</b>
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR	1	1	Ž
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PD tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10	10	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	10	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223	1223	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98	98	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	12	12	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10	10	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	10	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846	7846	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55	55	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>V</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10	10	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974	8974	<b>V</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10	10	· ·
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC		1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	~
tgt_l2c_Send_l2cRegPtt_Cnt_T_str.DIN	1	1	-
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	1	1	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	1	1	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	10	10	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10	10	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223	1223	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	<b>V</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98	98	<b>V</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	12	<b>*</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	10	10 10	
tgt I2c SetRecv I2cRegPtr Cnt T str.MDR	7846	7846	J
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55	55	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10	10	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974	8974	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10	10	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	1	1	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR		2	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	<b>V</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	2	2	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	1	1	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	1	1	- J
tgt_l2c_Setrecv_l2cRegrtl_Cflt_1_str.P3L tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	10	10	-
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	10	10	<b>V</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223	1223	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	<b>V</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98	98	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	12	12	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10	10	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10	10	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846	7846	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55	55	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10	10	<b>V</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	8974	8974	<b>V</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	10	10	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	1	1	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	2	2	- J
GOctaphilacteri Coctive_12ctCogi ti_Ont_1_str.Dit	-	-	

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DigColPsInt\_StartRequest **Actual Value Expected Value** tgt\_l2c\_SetupMasterReceive\_l2cRegPtr\_Cnt\_T\_str.DIN  $tgt\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.DOUT$ tgt\_l2c\_SetupMasterReceive\_l2cRegPtr\_Cnt\_T\_str.SET 1 tgt\_l2c\_SetupMasterReceive\_l2cRegPtr\_Cnt\_T\_str.CLR 2 2

tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>~</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	1	1	✓
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10	10	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10	10	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223	1223	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98	98	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10	10	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10	10	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55	55	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10	10	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974	8974	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10	10	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	~

T			V	
Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	~
SetupWriteRegister	1	SetupWriteRegister	1	•
I2c_SetupMasterTransmit	1	l2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	~

Test Step 2.5 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	11
DigColPsInt_Buffer_Cnt_M_u08[1]	22
DigColPsInt_Buffer_Cnt_M_u08[2]	33
DigColPsInt_CurrentSlave_Cnt_M_u08	33
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_Igc	0
I2c_GetStatus()	887
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	2
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	127
target_i2cREG1_temp.OAR	34
target_i2cREG1_temp.IMR	24
target_i2cREG1_temp.STR	455
target_i2cREG1_temp.CLKL	847
target_i2cREG1_temp.CLKH	987
target_i2cREG1_temp.CNT	487
target_i2cREG1_temp.DRR	34
target_i2cREG1_temp.SAR	34
target_i2cREG1_temp.DXR	24
target_i2cREG1_temp.MDR	847
target_i2cREG1_temp.IVR	56

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DigColPsini_StartRequest		
Name	Input Value	
arget_i2cREG1_temp.EMDR	2	
arget_i2cREG1_temp.PSC	24	
arget_i2cREG1_temp.PID11	987	
arget_i2cREG1_temp.PID12	24	
arget_i2cREG1_temp.DMAC	2	
arget_i2cREG1_temp.FUN	0	
arget_i2cREG1_temp.DIR	3	
arget_i2cREG1_temp.DIN	3	
arget_i2cREG1_temp.DOUT	2	
arget_i2cREG1_temp.SET	2	
·	3	
arget_i2cREG1_temp.CLR		
arget_i2cREG1_temp.ODR	3	
arget_i2cREG1_temp.PD	2	
arget_i2cREG1_temp.PSL	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	34	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	24	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	455	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	847	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH	987	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	487	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	34	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	34	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	24	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	847	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	56	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	24	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	987	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	24	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	3	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	3	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	3	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	3	
gt I2c GetStatus I2cRegPtr Cnt T str.PD	2	
	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	34	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR		
gt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	34	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24	
yt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	
yt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	
t_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	
yt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	
t_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	3	
pt_l2c_send_l2cRegPtr_Cnt_T_str.ODR	3	
	2	
t_l2c_Send_l2cRegPtr_Cnt_T_str.PD		
t_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	34	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	24	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	455	
pt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	847	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	987	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	487	
pt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	34	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	34	
gt_ize_octiveev_izervegi ti ont i str.o/iv		

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DigColPsInt\_StartRequest

Name	Input Value		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	847		
tgt I2c SetRecv I2cRegPtr Cnt T str.IVR	56		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	2		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	24		
	987		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11			
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	24		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	2		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	0		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	2		
tgt I2c SetRecv I2cRegPtr Cnt T str.CLR	3		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	3		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	34		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	24		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	455		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	847		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	987		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	487		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	34		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.SAR	34		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	24		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	847		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.lVR	56		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	24		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	987		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	24		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	2		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	987		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	30	30	-
DigColPsInt_Buffer_Cnt_M_u08[1]	22	22	
DigColPsInt_Buffer_Cnt_M_u08[2]	33	33	
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	<b>*</b>
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG	READ_SENSOR1_SETREG	
District Call Color Described Data Time Cot M 1100			

DigColPsInt\_PrevReqDataType\_Cnt\_M\_u08

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Name	Actual Value	Expected Value	Result
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	•
I2c_Send(Length_Cnt_T_u32)	1	1	•
I2c_SetRecv(Length_Cnt_T_u32)	0	0	
2c_SetupMasterReceive(DataLength_Cnt_T_u16)  2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR	34	34	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR	24	24	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	455	455	
tgt I2c GetStatus I2cRegPtr Cnt T str.CLKL	847	847	
tgt I2c GetStatus I2cRegPtr Cnt T str.CLKH	987	987	
tgt I2c GetStatus I2cRegPtr Cnt T str.CNT	487	487	٠,
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR	34	34	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	34	34	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR	24	24	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR	847	847	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	56	56	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	2	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	24	24	•
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	987	987	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12	24	24	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC	2	2	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34	34	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24	24	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455	455	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847	847	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987	987	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	487	487	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34	34	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34	34	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	24	24	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	847	847	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56	56	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	2	2	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	24	24	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	987	987	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	24	24	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	2	2	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	3	3	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	3	3	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	· ·
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	2	2	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3 2	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2		· ·
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	2	2	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	34	34	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	24	24	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	455	455	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	847	847	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	987	987	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	487	487 34	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	34	34	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	24	24	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	847	847	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR			
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	56	56	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR			
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	24	24	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	987 24	987 24	
tot 12c SatBacy 12cBagBtr Cat T atr BID42		44	· ·
		2	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12 tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	2 0	2	•



Name	Actual Value	Expected Value	Result
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	2	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	34	34	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	24	24	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	455	455	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	847	847	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	987	987	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	487	487	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	34	34	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	34	34	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	24	24	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	847	847	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	56	56	-
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	<b>✓</b>
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.PSC	24	24	-
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	987	987	-
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	24	24	_
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	2	2	-
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.FUN	0	0	_
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	-
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	2	2	-
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.SET	2	2	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	-
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	3	3	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	_
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34	34	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	24	24	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.NR  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	455	455	
	847	847	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	987	987	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	487	487	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34	34	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	34	34	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	24	24	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	847	847	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	56	56	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	2	2	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24	24	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987	987	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24	24	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	2	2	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	-
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	-
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>✓</b>

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	-
I2c Send	1	I2c Send	1	<b>V</b>

Test Step 2.6 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	44
DigColPsInt_Buffer_Cnt_M_u08[1]	55
DigColPsInt_Buffer_Cnt_M_u08[2]	66

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DigCoiPsini_StartRequest	
Name	Input Value
DigColPsInt_CurrentSlave_Cnt_M_u08	55
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
2c_GetStatus()	655
2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str) 2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	3
2cREG1_temp	target_i2cREG1_temp
c_ColSensorl2CAddress_Cnt_u08	55
arget_i2cREG1_temp.OAR	55
arget_i2cREG1_temp.IMR	66
arget_i2cREG1_temp.STR	556
arget_i2cREG1_temp.CLKL	2309
arget_i2cREG1_temp.CLKH	1204
arget_i2cREG1_temp.CNT	87
arget_i2cREG1_temp.DRR	67
arget_i2cREG1_temp.SAR	55
arget_i2cREG1_temp.DXR	66
arget_i2cREG1_temp.MDR	2309
arget_i2cREG1_temp.IVR	5
arget_i2cREG1_temp.EMDR	3
arget_i2cREG1_temp.PSC	66
arget_i2cREG1_temp.PID11	1204
arget_i2cREG1_temp.PID12	66
arget_i2cREG1_temp.DMAC	3
arget_i2cREG1_temp.FUN	1
arget_i2cREG1_temp.DIR	1
arget_i2cREG1_temp.DIN	2
arget_i2cREG1_temp.DOUT	3 3
arget_i2cREG1_temp.SET arget_i2cREG1_temp.CLR	1
arget_i2cREG1_temp.ODR	2
arget_i2cREG1_temp.PD	3
arget i2cREG1 temp.PSL	3
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR	55
gt I2c GetStatus I2cRegPtr Cnt T str.IMR	66
gt I2c GetStatus I2cRegPtr Cnt T str.STR	556
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	87
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR	67
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SAR	55
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR	66
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR	2309
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR	5
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR	3
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	66
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	66
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC	3
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	1
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	2
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	1
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	2
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3 3
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	55
pt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
gt_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	556
gt_l2c_Send_l2cRegPtr_Cnt_T_str.STR gt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	2309
	1204
gt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH gt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	87
	67
at IZC Sena IZCREAPIT UNT I STEDRE	•
gt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR gt_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	55

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19, D.S., Send, Distright, Coll., 19 MAR  10, D.S., Send, Distright, Coll., 19 MAR  11, D.S., Send, Distright, Coll., 19 MAR  12, D.S., Send, Distright, Coll., 19 MAR  13, D.S., Send, Distright, Coll., 19 MAR  14, D.S., Send, Distright, Coll., 19 MAR  15, D.S., Send, Distright, Coll., 19 MAR  16, D.S., Send, Distright, Coll., 19 MAR  17, D.S., Send, Distright, Coll., 19 MAR  18, D.S., Send, Distright, Coll., 19 MAR  19, D.S., Send, Distright, Coll., 19 MAR  10, D.S., Send, Distright, Coll., 19 MAR  10, D.S., Send, Distright, Coll., 19 MAR  11, D.S., Send, Distright, Coll., 19 MAR  12, D.S., Send, Distright, Coll., 19 MAR  13, D.S., Send, Distright, Coll., 19 MAR  14, D.S., Send, Distright, Coll., 19 MAR  15, D.S., Send, Distright, Coll., 19 MAR  16, D.S., Send, Distright, Coll., 19 MAR  17, D.S., Send, Distright, Coll., 19 MAR  18, D.S., Send, Distright, Coll., 19 MAR  19, D.S., Send, Distright, Col	Name	Input Value
19_00_See_00_000000_COLT_pic ENTON   10_00_See_00_000000_COLT_pic ENTON   10_00_See_00_000000_COLT_pic ENTON   10_00_See_00_000000_COLT_pic ENTON   10_00_See_00_000000_COLT_pic ENTON   10_00_See_00_0000000_COLT_pic ENTON   10_00_See_00_000000000000000000000000000		•
Dig   Color   Declaracy   Cut   1 as PDC   100		
Big   Dec   Seed   Deckey  Cort   _     Dec   Dec   Deckey   Deckey   Cort   _   Dec   Deckey   Deckey   Cort   _   Deckey   De		
### Dis Co. Send. (2016) Pr. CO. T. J. M. POTO 2 ### Dis Co. Send. (2016) Pr. CO. T. J. M. POTO 2 ### Dis Co. Send. (2016) Pr. CO. T. J. M. POTO 3 ### Dis Co. Send. (2016) Pr. CO. T. J		
March   Desire   De		
19   Dec. Send, Directophy Col. T. J. E. PONN   1   1   1   1   1   1   1   1   1		
10  22, Send (2016apt)** COLT_I AP ENN   1   1   1   1   22, Send (2016apt)** COLT_I AP ENN   2   1   1   1   1   1   1   1   1   1		
10  22, Seed ORTSRIP COLT_I DONN   2		
19   10.5 Semil   2018(1997) C. Out   1. de 10 No   2     19   10.5 Semil   2018(1997) C. Out   1. de 10 No   1     19   10.5 Semil   2018(1997) C. Out   1. de 10 No   1     19   10.5 Semil   2018(1997) C. Out   1. de 10 No   1     19   10.5 Semil   2018(1997) C. Out   1. de 10 No   1     19   10.5 Semil   2018(1997) C. Out   1. de 10 No   1     10   10.5 Semi		
10, 12, 12, 13, 14, 15, 15, 15, 15, 15, 15, 15, 15, 15, 15		
19_12_S. Send_ J. Zörejipi* C. C. T. Jar. SCR		
19_UR_S. Send   26Reptp* ConT_1 at CORR   10_UR_S. Send   26Reptp* ConT_		
10   12   Senit   Zorlegith Colf_1 to PD   3   10   2   2   2   2   2   2   2   2   2		
Sept   25 Fine		
Section   Carellage   Total   Section   Sect	tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	
Selfaco   Zelfacin   Col. 1, str. OAR	tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	
Section   Company   Comp	tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	
19.12. Selfacor, 12. PROPRIES OFT, 13. PRICOLIS. 2009 19.12. Selfacor, 12. PROPRIES OFT, 13. PRICOLIS. 2019 19.12. Selfacor, 12. PROPRIES OFT, 13. PRICOLIS. 19.12. Selfacor, 12. PRICOLIS. 2019 2019 2019 2019 2019 2019 2019 2019	tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	55
192 R.S. SERROV, JCROSPIT, CH. T. Jat CLICH 192 R.S. SERROV, JCROSPIT, CH. T. Jat CLICH 192 R.S. SERROV, JCROSPIT, CH. T. Jat CNT 193 R.S. SERROV, JCROSPIT, CH. T. Jat CNT 193 R.S. SERROV, JCROSPIT, CH. T. Jat CNT 194 R.S. SERROV, JCROSPIT, CH. T. Jat CNT 194 R.S. SERROV, JCROSPIT, CH. T. Jat CNT 195 R.S. SERROV, JCROSPIT,	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
192 LS, Selface, Uzckleghtr, Cht, T. str. DAN 192 LS, Selface, Uzckleghtr, Cht, T. str. DRR 193 LS, Selface, Uzckleghtr, Cht, T. str. DRR 194 LS, Selface, Uzckleghtr, Cht, T. str. DRR 195 LS, Selface, Uzckleghtr, Cht, T. str. DRR 195 LS, Selface, Uzckleghtr, Cht, T. str. DRR 196 LS, Selface, Uzckleghtr, Cht, T. str. DRR 196 LS, Selface, Uzckleghtr, Cht, T. str. DRR 197 LS, Selface, Uzckleghtr, Cht, T. str. DRR 197 LS, Selface, Uzckleghtr, Cht, T. str. DRR 198 LS, Selface, Date, Dr. Cht, T. str. DRR 198 LS, Selface, Date, Dr. Cht, T. str. DRR 198 LS, Selface, Date, Dr. Cht, T. str. DRR 198 LS, Selface, Date, Dr. Cht, T. str. DRR 198 LS, Selface, Date, Dr. Cht, T. str. DRR 198 LS, Selface, Date, Dr. Cht, T. str. DRR 198 LS, Selface, Date, Dr. Cht, T. str. DRR 198 LS, Selface, Date, Dr. Cht, T. s	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
192   12. S. Seffero,   Z. CRESPIT, C. I.T. J. S. DRR	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
19   I.S. Selfero, I.Z. Selfero, I.C. T. SEL SER	tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	1204
Spin   Dec. Serieses   December   Cent   Test   SAR	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
Sp.   Roc. Seffleov.   Defengift. Cnt.   st. SAR	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
For   Dec   Selfrect   Cartegriff   Cort   Test MDR   2399		55
Supplies		66
Sp.   Zp. SerRecv   ZeRegPPC_CNT_SET_NET		2309
For   12		3
Total   Common   Co		
Sgt   12c   SelfRecv   22cRegPtr   Cnt_T str.DIMAC   3   1   1   1   1   1   1   1   1   1		
Include   Self Rev.   Jackeght   Chil   T. Str. DIR   1   1   1   1   2   2   3   3   3   3   3   3   3   3		
Ig  12		
Igt   Izc   SetReov   IzcRegPtr_Cnt_T str. DOUT		
tgt_12c_SetRecv_12cRegPtr_Cnt_T_str.SET         3           tgt_12c_SetRecv_12cRegPtr_Cnt_T_str.CtR         1           tgt_12c_SetRecv_12cRegPtr_Cnt_T_str.DDR         2           tgt_12c_SetRecv_12cRegPtr_Cnt_T_str.DD         3           tgt_12c_SetRecv_12cRegPtr_Cnt_T_str.DD         3           tgt_12c_SetRecv_12cRegPtr_Cnt_T_str.DL         5           tgt_12c_SetUpMasterReceive_12cRegPtr_Cnt_T_str.DLR         5           tgt_12c_SetUpMasterReceive_12cRegPtr_Cnt_T_str.DLR         66           tgt_12c_SetUpMasterReceive_12cRegPtr_Cnt_T_str.DLR         66           tgt_12c_SetUpMasterReceive_12cRegPtr_Cnt_T_str.CLKH         2309           tgt_12c_SetUpMasterReceive_12cRegPtr_Cnt_T_str.CLKH         1204           tgt_12c_SetUpMasterReceive_12cRegPtr_Cnt_T_str.DLR         67           tgt_12c_SetUpMasterReceive_12cRegPtr_Cnt_T_str.DLR         66           tgt_12c_SetUpMasterReceive_12cRegPtr_Cnt_T_str.DLR         66           tgt_12c_SetUpMasterReceive_12cRegPtr_Cnt_T_str.DLR         66           tgt_12c_SetUpMasterReceive_12cRegPtr_Cnt_T_str.DLR         2309           tgt_12c_SetUpMasterReceive_12cRegPtr_Cnt_T_str.DLR         66           tgt_12c_SetUpMasterReceive_12cRegPtr_Cnt_T_str.DLR         66           tgt_12c_SetUpMasterReceive_12cRegPtr_Cnt_T_str.DLR         1204           tgt_12c_SetUpMasterReceive_12cRegPtr_Cnt_T_str.DLR		
tg		
tg1_2c_SetRecv_12cRegPtr_Cnt_T_str.DDR         2           tg1_2c_SetRecv_12cRegPtr_Cnt_T_str.PD         3           tg1_2c_SetRecv_12cRegPtr_Cnt_T_str.PD         3           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR         55           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.MR         66           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DR         56           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLK         2309           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLK         1204           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CKH         1204           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR         67           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR         67           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DXR         66           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DXR         66           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNDR         3           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PID11         1204           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DND         3           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DND         3           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DND         1           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNT         1           tg1_2c_SetupMasterReceive_12cRegPtr_Cnt_T_s		
tgl_l2c_SelRecv_l2cRegPtr_Cnt_Tstr.PD         3           tgl_l2c_SelRecv_l2cRegPtr_Cnt_Tstr.PSL         3           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.DAR         55           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.DAR         66           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.CNL         2309           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.CNL         2309           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.CNT         87           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.CNT         87           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.DAR         67           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.DAR         67           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.DAR         66           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.DAR         55           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.DAR         5           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.DAR         66           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.DAR         5           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.DAR         66           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.DAR         66           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.DAR         12           tgl_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.DAR         14           tgl_l2c_SetupMasterReceive_l2cRe		
tgt   Zc_SetRecv   ZcRepPtr_Cnt_T_str.PSL         3           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_str.DAR         55           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.DAR         66           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.STR         556           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.CLKL         2309           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.CLKL         1204           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.CKNT         87           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.CKNT         87           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.DRR         67           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.DXR         66           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.DXR         66           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.DXR         66           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.PID12         66           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.PID12         66           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.DID12         66           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.DID1         1           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.DID1         1           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.DID1         2           tgt   Zc_SetupMasterReceive   ZcRepPtr_Cnt_T_str.DID1		
tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.IMR         66           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.IMR         66           tgl. 2c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLKL         2309           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLKH         1204           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CNT         87           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         67           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         67           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         66           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         66           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         66           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         5           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.EMDR         3           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PDID1         1204           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNC         66           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNC         3           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNC         3           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNC         3           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNC         2           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNC         2		
tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.IMR         66           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.STR         556           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLKL         2309           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLKH         1204           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CNT         87           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR         67           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR         67           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         66           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         2309           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.MDR         2309           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         3           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PDR         3           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNL         1204           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNAC         3           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNAC         3           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DN         1           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNC         2           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNC         3           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNC         3 </td <td></td> <td></td>		
tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.CLKL         2309           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.CLKL         2309           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.CLKH         1204           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.DRR         87           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.DRR         67           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.DRR         66           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.MDR         2309           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.MDR         2309           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.DNR         5           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.DNR         3           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.PDI1         1204           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.DNAC         3           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.DNAC         3           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.DN         1           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.DN         1           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.DOT         3           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.DOT         3           tgl.   2c_ SetupMasterReceive   2cRegPtr_Cnt_T_str.DOR         2           tgl.   2c_ SetupMa		
tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T str.CLKL         2309           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T str.CLKH         1204           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T str.CNT         87           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DRR         67           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DXR         66           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T str.MDR         2309           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T str.MDR         2309           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T str.PMDR         3           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T str.PDR         3           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T str.PDI11         1204           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T str.PDI12         66           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DMAC         3           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DMAC         3           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DIN         1           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DIN         2           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DOUT         3           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOUT         3           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOR         2           tgl. 12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOR <t< td=""><td>tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR</td><td></td></t<>	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	
tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLKH         1204           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DTR         87           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DRR         67           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DXR         55           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DXR         66           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DXR         5           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DRN         2309           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.EMDR         3           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DRN         3           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DD11         1204           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DMAC         3           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DMAC         3           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR         1           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR         1           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR         1           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.SET         3           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.SET         3           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DOR         2           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DAR         5	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CNT         87           tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR         67           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR         55           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DXR         66           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.MDR         2309           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PMDR         3           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.BMDR         3           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PMDR         3           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PID11         1204           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PID12         66           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMAC         3           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIR         1           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIR         1           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         2           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOUT         3           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOR         2           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DR         2           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DR         3           tg_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DA         55           tg_12c_S	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DRR         67           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DXR         55           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DXR         66           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.MDR         2309           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.WR         5           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.EMDR         3           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PBC         66           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID11         1204           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DID12         66           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN         1           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN         1           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN         1           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DOUT         3           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CR         1           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CR         1           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CR         1           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN         2           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DR         3           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DR         5	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
tgt_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.MDR         2309           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.IVR         5           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.EMDR         3           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID1         1204           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID11         1204           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID12         66           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DMAC         3           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PIN         1           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN         1           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN         2           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DOUT         3           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DUT         3           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLR         1           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DDR         2           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DDR         2           tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DDR         3           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR         55           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR         55           tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLK         2309	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.MDR       2309         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.IVR       5         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.EMDR       3         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID10       66         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID11       1204         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DID12       66         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DMAC       3         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN       1         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN       1         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN       2         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DUT       3         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.SET       3         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DUT       1         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DDR       2         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DDR       2         tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DDR       2         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR       55         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR       55         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLK       2309         tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLK </td <td></td> <td>66</td>		66
tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.IVR  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.EMDR  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PSC  66  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID11  1204  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID12  66  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DID2  66  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DID4  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DID4  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DID4  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DID8  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DID4  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DID4  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DUT  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CUT  3  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLR  1  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLR  1  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DD  3  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DD  3  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DD  3  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DD  3  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DD  4  tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR  55  tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR  56  tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR  56  tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL  2309  tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL  2309		2309
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC  66  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12  66  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DNAC  1  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DNAC  2  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DNAC  2  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DNAC  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DNAC  55  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.NAR  66  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR  556  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL  2309  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL  1204		5
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC 66  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11 1204  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12 66  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12 66  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC 3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PUN 1  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR 1  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR 2  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DUT 3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DUT 3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DUT 3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DR 1  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DR 2  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD 3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD 3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DAR 55  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR 566  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLK 2309  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLK 2309  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH 1204		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DDR  2  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DDR  2  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DAR  55  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR  55  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR  566  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL  2309  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL  1204		66
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DUT  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DUT  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DUT  1  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DUT  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DDR  2  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DDR  2  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DAR  55  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.JMR  66  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR  556  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL  2309  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL  1204		
tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DMAC  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN  2  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DUT  3  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.SET  3  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLR  1  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.ODR  2  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.ODR  2  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PD  3  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PD  3  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.OAR  55  tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.JMR  66  tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR  556  tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL  2309  tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL  1204		
tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.FUN  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN  2  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DUT  3  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.SET  3  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLR  1  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CLR  1  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.ODR  2  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DD  3  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PD  3  tgt_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PD  3  tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.OAR  55  tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR  66  tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR  556  tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL  2309  tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKH  1204		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN  2  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR  1  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR  2  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL  3  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR  55  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR  66  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR  556  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL  2309  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH  1204		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN 2 tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT 3 tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET 3 tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR 1 tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR 2 tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD 3 tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD 3 tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL 3 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR 55 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR 66 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR 556 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL 2309 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL 1204		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR  2  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL  3  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR  55  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR  66  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR  556  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL  2309  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH  1204		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR  2  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD  3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL  3  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR  55  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR  66  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR  556  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL  2309  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH  1204		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR  2 tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD  3 tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL  3 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR  55 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR  66 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR  556 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL  2309 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH  1204		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR 2 tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD 3 tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL 3 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR 55 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR 66 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR 556 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL 2309 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH 1204		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD 3  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL 3  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR 55  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR 66  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR 556  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL 2309  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH 1204		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL 3 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR 55 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR 66 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR 556 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL 2309 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH 1204		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR 55  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR 66  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR 556  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL 2309  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH 1204		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR 66  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR 556  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL 2309  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH 1204		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL 2309 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH 1204		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH 1204	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	
	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT 87	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR 67	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67

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Name	Input Value		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	5		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	1 2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt Buffer Cnt M u08[0]	36	36	✓ ×
DigColPsInt_Buffer_Cnt_M_u08[1]	55	55	•
DigColPsInt_Buffer_Cnt_M_u08[2]	66	66	
DigColPsInt CurrentSlave Cnt M u08	55	55	<b>✓</b>
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ SENSOR1 SETREG	READ_SENSOR1_SETREG	-
DigColPsInt_PrevReqDataType_Cnt_M_u08	3	3	•
DigColPsInt_SkipRegisterWrite_Cnt_M_Igc	0	0	•
I2c_Send(Length_Cnt_T_u32)	1	1	•
I2c_SetRecv(Length_Cnt_T_u32)	0	0	~
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	0	0	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR	55	55	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR	66	66	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	556	556	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT	87	87	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SAR	55	55	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR	2309	2309	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR	5	5	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12	66	3	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC	1	1	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	-
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	-
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	556	556	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>V</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>V</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	66	66	<b>Y</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>V</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	66	66	<b>V</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	3	3	<b>V</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1	1	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>

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Name	Actual Value	Expected Value	Result
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	3	3	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	3	3	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✓
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✓
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✓
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	✓
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	~
tgt_l2c_SetRecorv_l22 <del>bTeggTR</del> tr_COnt_TT_str.DXR	66	66	✓
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	66	66	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	1204	1204	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	

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Name	Actual Value	Expected Value	Result
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✓

Т				V
Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	~
SetupWriteRegister	1	SetupWriteRegister	1	•
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	~

lame	Input Value
bigColPsInt_Buffer_Cnt_M_u08[0]	66
ligColPsInt_Buffer_Cnt_M_u08[1]	77
bigColPsInt_Buffer_Cnt_M_u08[2]	88
bigColPsInt_CurrentSlave_Cnt_M_u08	11
bigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
ligColPsInt_PrevReqDataType_Cnt_M_u08	0
igColPsInt_SensInitialized_Cnt_M_lgc	1
igColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
tc GetStatus()	123
c GetStatus(I2cRegPtr Cnt T str)	tgt I2c GetStatus I2cRegPtr Cnt T str
c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
ype_Cnt_T_u08	1
cREG1_temp	target_i2cREG1_temp
_ColSensorl2CAddress_Cnt_u08	target_izckeGi_temp 40
rget_i2cREG1_temp.OAR	66
rget i2cREG1 temp.IMR	78
	78
rget_i2cREG1_temp.STR	495
rget_i2cREG1_temp.CLKL	
rget_i2cREG1_temp.CLKH	56 897
rget_i2cREG1_temp.CNT	
rget_i2cREG1_temp.DRR	98
rget_i2cREG1_temp.SAR	66
rget_i2cREG1_temp.DXR	78
rget_i2cREG1_temp.MDR	495
rget_i2cREG1_temp.IVR	66
rget_i2cREG1_temp.EMDR	0
rget_i2cREG1_temp.PSC	78
rget_i2cREG1_temp.PID11	56
rget_i2cREG1_temp.PID12	78
rget_i2cREG1_temp.DMAC	0
rget_i2cREG1_temp.FUN	0
rget_i2cREG1_temp.DIR	0
rget_i2cREG1_temp.DIN	1
rget_i2cREG1_temp.DOUT	0
rget_i2cREG1_temp.SET	0
rget_i2cREG1_temp.CLR	0
rget_i2cREG1_temp.ODR	1
rget_i2cREG1_temp.PD	0
rget_i2cREG1_temp.PSL	0
t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	66
t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	78
t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	78
t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	495
t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	56
t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	897
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	98
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	66
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	78

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DigColPsInt_StartRequest		TAZOI(AL
Name	Input Value	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR	495	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	66	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC	78	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	56	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	78	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0	
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	
yt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	
	495	
t_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL		
t_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	56	
t_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	
t_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	
t_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	
t_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	0	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	78	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	
t_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	
t_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	0	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	0	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	
gt I2c SetRecv I2cRegPtr Cnt T str.IMR	78	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78	
gt I2c SetRecv I2cRegPtr Cnt T str.CLKL	495	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	
gt I2c SetRecv I2cRegPtr Cnt T str.DRR	98	
	66	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	78	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR		
yt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78	
pt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	
pt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	
t_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	1	
pt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78	
	78	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	495	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL		
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	98	

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Name	Input Value		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	66		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	78		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	495		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0		
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0		
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0		
gt I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	1		
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0		
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0		
gt I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	66		
gt I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	78		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56		
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0		
gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	0		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0		
gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	0		
gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0		
gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	1		
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	0		
lame	Actual Value	Expected Value	Res
igColPsInt_Buffer_Cnt_M_u08[0]	32	32	
DigColPsInt_Buffer_Cnt_M_u08[1]	77	77	
DigColPsInt_Buffer_Cnt_M_u08[2]	88	88	
DigColPsInt_CurrentSlave_Cnt_M_u08	40	40	
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG	READ_SENSOR1_SETREG	
DigColPsInt_PrevReqDataType_Cnt_M_u08	1	1	
	0	0	
DigColPsInt_SkipRegisterWrite_Cnt_M_Igc	1	1	
2c_Send(Length_Cnt_T_u32)			
2c_SetRecv(Length_Cnt_T_u32)	0	0	
2c_SetupMasterReceive(DataLength_Cnt_T_u16)	0	0	
2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	66	66	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	78	78	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	78	78	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	495	495	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	56	56	
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	897	897	
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	98	98	
		66	
gt_I2c_GetStatus_I2cRegPtr Cnt T str.SAR	66	78	
	78		
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	78	495	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR	78 495	495	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	78 495 66	66	
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	78 495 66 0	66 0	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC	78 495 66 0 78	66 0 78	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	78 495 66 0 78 56	66 0 78 56	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11 gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	78 495 66 0 78 56 78	66 0 78 56 78	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11 gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12 gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12 gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC	78 495 66 0 78 56 78 0	66 0 78 56 78 0	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	78 495 66 0 78 56 78	66 0 78 56 78	

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Name	Actual Value	Expected Value	Result
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>~</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	0	<b>V</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	~
tgt I2c GetStatus I2cRegPtr Cnt T str.ODR	1	1	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	66	66	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	78	78	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	<b>V</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	56 897	56 897	<b>*</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	Ž
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	66	66	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	78	78	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	<b>V</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	78 0	78 0	<b>*</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	7
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	<b>V</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0 66	0 66	<b>*</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	78	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.NTR	78	78	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	897	897	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	98	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	66	66	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	78	78	<b>*</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	495 66	495 66	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FMDR	0	0	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	78	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	56	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	78	78	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1 0	1	<b>*</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	0	0	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	66	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78	78	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78	78	· ·
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	495 56	495 56	· ·
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897	897	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	98	98	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66	66	<b>~</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	78	78	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	495	495	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66	66	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>V</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	78	78	<b>V</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11 tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	56 78	56 78	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.Pib12  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	0	0	~

 $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.ODR$ 

tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD

tgt\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str.PSL

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**Actual Value Expected Value** tgt\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.FUN tgt\_l2c\_SetupMasterReceive\_l2cRegPtr\_Cnt\_T\_str.DIR tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.DIN tgt\_l2c\_SetupMasterReceive\_l2cRegPtr\_Cnt\_T\_str.DOUT tgt\_l2c\_SetupMasterReceive\_l2cRegPtr\_Cnt\_T\_str.SET tgt\_l2c\_SetupMasterReceive\_l2cRegPtr\_Cnt\_T\_str.CLR tqt I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR tgt\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.PD tgt\_l2c\_SetupMasterReceive\_l2cRegPtr\_Cnt\_T\_str.PSL  $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.OAR$  $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IMR$  $tgt\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str.STR$ tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKL  $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKH$ tgt\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str.CNT tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DRR  $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SAR$ tgt\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str.DXR  $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.MDR$ tgt\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str.IVR  $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.EMDR$ tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSC  $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID11$ tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID12 tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DMAC tgt\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str.FUN tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIR  $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIN$  $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DOUT$  $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SET$ tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR 

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c Send	1	I2c Send	1	<b>~</b>

Test Step 2.8 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	40
DigColPsInt_Buffer_Cnt_M_u08[1]	50
DigColPsInt_Buffer_Cnt_M_u08[2]	60
DigColPsInt_CurrentSlave_Cnt_M_u08	12
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
I2c_GetStatus()	766
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	1
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	55
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44

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DigColPsini_StartRequest		GEO   Cal
Name	Input Value	
target i2cREG1 temp.MDR	566	
target_i2cREG1_temp.IVR	554	
target_i2cREG1_temp.EMDR	1	
target_i2cREG1_temp.PSC	44	
target_i2cREG1_temp.PID11	4466	
target_i2cREG1_temp.PID12	44	
target i2cREG1 temp.DMAC	1	
	1	
target_i2cREG1_temp.FUN		
target_i2cREG1_temp.DIR	2 0	
target_i2cREG1_temp.DIN		
target_i2cREG1_temp.DOUT	1	
target_i2cREG1_temp.SET	1	
target_i2cREG1_temp.CLR	2	
target_i2cREG1_temp.ODR	0	
target_i2cREG1_temp.PD	3	
target_i2cREG1_temp.PSL	3	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	567	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	44	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	4444	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT	129	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR	6	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SAR	567	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	44	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	566	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	554	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	44	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	44	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN	1	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR	2	
	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET	2	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PD	3	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	3	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	567	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	566	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	554	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	2	
	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR		
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	3	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	4466	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	

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Name	Input Value		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554		
tgt I2c SetRecv I2cRegPtr Cnt T str.EMDR	1		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	44		
tgt I2c SetRecv I2cRegPtr Cnt T str.DMAC	1		
	1		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN			
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	2		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	0		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	566		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	129		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	567		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR			
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	44		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	566		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	2		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	0		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	3		
	3		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL			
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	567		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	6		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	4400		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3		
Name	Actual Value	Expected Value	Resul
DigColPsInt_Buffer_Cnt_M_u08[0]	32	32	
DigColPsInt Buffer Cnt M u08[1]	50	50	
DigColPsInt_Buffer_Cnt_M_u08[2]	60	60	
DigColPsInt_Buller_Cnt_M_uvo[2]  DigColPsInt CurrentSlave Cnt M u08	55	55	
DIGOUL SHIT CRITELIONANE CHIT IN THOU	99	99	

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Name	Actual Value	Expected Value	Result
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG	READ_SENSOR1_SETREG	~
DigColPsInt_PrevReqDataType_Cnt_M_u08	1	1	•
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	~
I2c_Send(Length_Cnt_T_u32)	1	1	✓
I2c_SetRecv(Length_Cnt_T_u32)	0	0	~
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	0	0	•
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✓
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC	44	44	<b>✓</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✓
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	

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Name	Actual Value	Expected Value	Result
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	2	2	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	1	1	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	2	2	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	3	3	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	6	6	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	44	44	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	129	129	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~

Τ				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c Send	1	I2c Send	1	-

Test Step 2.9 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	70

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Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[1]	80
DigColPsInt_Buffer_Cnt_M_u08[2]	90
DigColPsInt_CurrentSlave_Cnt_M_u08	45
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt PrevReqDataType Cnt M u08	3
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
I2c_GetStatus()	886
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_l2c_Send_l2cRegPtr_Cnt_T_str
I2c SetRecv(I2cRegPtr Cnt T str)	
_ , , , , , , , , , , , , , , , , , , ,	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	1
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	60
target_i2cREG1_temp.OAR	65
target_i2cREG1_temp.IMR	89
target_i2cREG1_temp.STR	67
target_i2cREG1_temp.CLKL	7
target_i2cREG1_temp.CLKH	577
target_i2cREG1_temp.CNT	88
target_i2cREG1_temp.DRR	23
target_i2cREG1_temp.SAR	65
target_i2cREG1_temp.DXR	89
target_i2cREG1_temp.MDR	7
target_i2cREG1_temp.IVR	44
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	89
target_i2cREG1_temp.PID11	577
target_i2cREG1_temp.PID12	89
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
	2
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	0
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR	65
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	89
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	67
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	7
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	577
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	88
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	23
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SAR	65
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR	89
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	7
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR	44
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	89
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	577
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12	89
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC	2
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN	0
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR	0
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
tgt_l2c_GetStatus_l2cRegPtr_Cnt_1_str.D001 tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET	2 2
	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PD	2
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	0
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	65
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	577
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	88
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23

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Name	Input Value	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	
tgt I2c Send I2cRegPtr Cnt T str.DXR	89	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	2	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	89	
	577	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	89	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12		
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	2	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	1	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	2	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	67	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	577	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	88	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	89	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	89	
	2	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	2	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	2	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	0	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	1	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.FUN	0	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DUT	2	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	2	
	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	
	0	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	l o c	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	65	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	89 67	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	89	

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Name	Input Value		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	89 7		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44		
tgt_12c_SetupMasterTransmit_12cRegPtt_Cnt_T_sir.ivR  tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR	2		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	89		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	577		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	89		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt Buffer Cnt M u08[0]	32	32	
DigColPsInt Buffer Cnt M u08[1]	80	80	<b>~</b>
DigColPsInt_Buffer_Cnt_M_u08[2]	90	90	~
DigColPsInt_CurrentSlave_Cnt_M_u08	60	60	<b>✓</b>
DigColPsInt CurrentStepNo Cnt M enum	READ_SENSOR1_SETREG	READ_SENSOR1_SETREG	~
DigColPsInt PrevReqDataType Cnt M u08	1	1	<b>✓</b>
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	•
I2c_Send(Length_Cnt_T_u32)	1	1	~
I2c_SetRecv(Length_Cnt_T_u32)	0	0	~
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	0	0	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	<b>✓</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	65	65	<b>✓</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	89	89	<b>✓</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	67	67	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT	88	88	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	23	23	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SAR	65	65	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR	89	89	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	7	7	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	44	44	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR	2	2	· ·
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC	89	89	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	577 89	577	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12	2	89	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR	0	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	·
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT	2	2	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	89	89	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	67	67	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	<b>~</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	89	89	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	· ·
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	89	89	· ·
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>

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Name	Actual Value	Expected Value	Result
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>V</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	1 2	1 2	· ·
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	2	2	J
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	0	0	<b>V</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	2	2	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65	65	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	89	89	<b>~</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	67 7	67 7	<b>✓</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	577	577	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	88	88	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	23	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	65	65	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89	89	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7	7	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	44	44	<b>V</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	2	2	<b>~</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	89 577	89 577	Ž
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11 tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89	89	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	2	2	<b>V</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	0	1	<b>~</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	1 2	2	Ž
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	0	0	-
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	65	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	89	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	67	67	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	577	577	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	88	88	<b>V</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	23 65	23 65	~
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.DXR	89	89	-
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7	7	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	44	44	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89	89	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577	577	<b>V</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89	89	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	2	0	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>~</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	2	2	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	2	2	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	0	0	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	65 89	65 89	Ž
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	67	67	<b>V</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	65	65	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	89	89	<b>~</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	7	7	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	44	44	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	2 89	2 89	· ·
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	7
2		•	

 $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLR$ 

tgt\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str.ODR

 $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PD$ 

 $tgt\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str.PSL$ 

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0

1

2

0



DigColPsInt\_StartRequest Actual Value **Expected Value** tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID12 89 89  $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DMAC$ 2 tgt\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str.FUN 0 0  $tgt\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str.DIR$ 0 0  $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIN$ 1 1  $tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DOUT$ 2 2 2 tgt\_l2c\_SetupMasterTransmit\_l2cRegPtr\_Cnt\_T\_str.SET 2

0

1

2

Τ				V
Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	l2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	~

Test Step 2.10 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	3
DigColPsInt_Buffer_Cnt_M_u08[1]	6
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_CurrentSlave_Cnt_M_u08	77
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
2c_GetStatus()	0
2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	1
2cREG1_temp	target_i2cREG1_temp
COlSensorl2CAddress_Cnt_u08	69
arget_i2cREG1_temp.OAR	54
arget i2cREG1 temp.IMR	66
arget i2cREG1 temp.STR	8
arget_i2cREG1_temp.CLKL	554
arget_i2cREG1_temp.CLKH	344
arget_i2cREG1_temp.CNT	123
target i2cREG1 temp.DRR	45
arget i2cREG1 temp.SAR	54
arget i2cREG1 temp.DXR	66
arget_i2cREG1_temp.MDR	554
arget_i2cREG1_temp.lVR	788
arget_i2cREG1_temp.EMDR	3
	66
arget_i2cREG1_temp.PSC	
arget_i2cREG1_temp.PID11	344
arget_i2cREG1_temp.PID12	66
arget_i2cREG1_temp.DMAC	3
arget_i2cREG1_temp.FUN	1
arget_i2cREG1_temp.DIR	3
arget_i2cREG1_temp.DIN	2
arget_i2cREG1_temp.DOUT	3
arget_i2cREG1_temp.SET	3
arget_i2cREG1_temp.CLR	3
arget_i2cREG1_temp.ODR	2
arget_i2cREG1_temp.PD	1
arget_i2cREG1_temp.PSL	2
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	54
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	66
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	8
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	554
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	344
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	123
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	45

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Name	Input Value	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	54	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	66	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	554	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.lVR	788	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	66	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	344	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	66	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	3	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	3	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	1	
	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL		
gt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	
pt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	8	
pt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	554	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	788	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	3	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	
	2	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL		
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554	
ıt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788	
t_12c_SetRecv_12cRegPtr_Cnt_T_str.EMDR	3	
yt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	
yt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	344	
pt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	66	
pt_12c_SetRecv_12cRegPtr_Cnt_T_str.DMAC	3	
t_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	1	
	3	
yt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR		
yt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	
yt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	
yt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54	
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	
	8	
gt_l2c_SetupMasterReceive l2cRegPtr Cnt T str.STR		
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	554	

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Name	Input Value		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	554		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	788		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.EMDR	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344		
tgt I2c SetupMasterReceive I2cReqPtr Cnt T str.PID12	66		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	3		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	1		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	54		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	66		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.Nrk  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	8		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	554		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	344		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	45		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	344		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	2		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT	3		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	3		
tqt I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	3		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	3	3	-
DigColPsInt_Buffer_Cnt_M_u08[1]	6	6	•
DigColPsInt_Buffer_Cnt_M_u08[2]	9	9	-
DigColPsInt_CurrentSlave_Cnt_M_u08	69	69	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_GETDATA	READ_SENSOR1_GETDATA	~
DigColPsInt_PrevReqDataType_Cnt_M_u08	1	1	•
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1	1	•
I2c_SetRecv(Length_Cnt_T_u32)	2	2	•
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	2	2	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	54 66	54 66	¥
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	8	8	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	554	554	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH	344	344	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	123	123	
tgt I2c GetStatus I2cRegPtr Cnt T str.DRR	45	45	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	54	54	-
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR	554	554	-
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	788	788	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	344	344	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	

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Name	Actual Value	Expected Value	Result
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN	2	2	·
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR	2	2	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	1	1	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	54	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	66	66	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	8	8	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554	554	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	344	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	123	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	45	45	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	54	54	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66 554	66 554	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	788	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	3	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	66	66	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	344	344	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	66	66	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	3	3	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	3	3	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	3	3	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54	54	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	66	66	·
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8	8	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	554	554 344	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	123	123	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	45	45	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	54	54	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	66	66	
tgt I2c SetRecv I2cRegPtr Cnt T str.MDR	554	554	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788	788	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	3	3	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	66	66	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	344	344	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	3	3	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	3	3	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	3	3	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	2	2	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	2	1 2	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	54	54	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	66	66	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8	8	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	554	554	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	344	344	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	123	123	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	45	45	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	54	54	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	554	554	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788	788	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	3	3	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	66	66	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344	344	·
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	

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Name	Actual Value	Expected Value	Result
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	3	3	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	2	2	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	3	3	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	3	3	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	2	2	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54	54	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8	8	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554	554	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344	344	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123	123	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45	45	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54	54	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554	554	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788	788	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344	344	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	2	2	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	~

Т				V
Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	~
SetupRead	1	SetupRead	1	<b>✓</b>
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	~
I2c_SetRecv	1	I2c_SetRecv	1	<b>✓</b>

Test Step 2.11 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	11
DigColPsInt_Buffer_Cnt_M_u08[1]	22
DigColPsInt_Buffer_Cnt_M_u08[2]	33
DigColPsInt_CurrentSlave_Cnt_M_u08	65
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
I2c_GetStatus()	65535
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	2
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	33
target_i2cREG1_temp.OAR	3
target_i2cREG1_temp.IMR	100
target_i2cREG1_temp.STR	7788
target_i2cREG1_temp.CLKL	2767
target_i2cREG1_temp.CLKH	556
target_i2cREG1_temp.CNT	564
target_i2cREG1_temp.DRR	88
target_i2cREG1_temp.SAR	3
target_i2cREG1_temp.DXR	100

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Name	Input Value	
target i2cREG1 temp.MDR	2767	
target_i2cREG1_temp.IVR	9	
target_i2cREG1_temp.EMDR	0	
target_i2cREG1_temp.PSC	100	
target_i2cREG1_temp.PID11	556	
target_i2cREG1_temp.PID12	100	
target_i2cREG1_temp.DMAC	2	
target_i2cREG1_temp.FUN	0	
target_i2cREG1_temp.DIR	1	
target_i2cREG1_temp.DIN	3	
	2	
target_i2cREG1_temp.DOUT		
target_i2cREG1_temp.SET	0	
target_i2cREG1_temp.CLR	1	
target_i2cREG1_temp.ODR	3	
target_i2cREG1_temp.PD	0	
target i2cREG1 temp.PSL	3	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	3	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	100	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	7788	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	2767	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	556	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	564	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	88	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	3	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR	100	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR	2767	
	9	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	100	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	556	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	100	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	1	
	3	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN		
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	1	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	3	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	3	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	
	100	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR		
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	7788	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	2767	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	
	2767	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR		
gt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	556	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR		
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	2	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	
	3	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL		
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	3	
	100	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	7788	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR		
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.lMR gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	7788	
gzo_cetricer_zetregr ti_onicstr.onic igt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.sTR igt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL igt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH igt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH igt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	7788 2767	

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Name	Input Value		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3		
	100		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR			
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	9		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	100		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	556		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	100		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	2		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	0		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	1		
tgt I2c SetRecv I2cRegPtr Cnt T str.DIN	3		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	2		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	0		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	1		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	3		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	3		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	100		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	2767		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	556		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	2767		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	100		
	556		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11			
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	100		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3		
	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT			
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	0		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.PSL	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	7788		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	2767		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	100		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	100		
	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3		
Name	Actual Value	Expected Value	Result
		•	Nesult
DigColPsInt_Buffer_Cnt_M_u08[0]	11	11	~
DigColPsInt_Buffer_Cnt_M_u08[1]	22	22	~
DigColPsInt_Buffer_Cnt_M_u08[2]	33	33	•
DigColPsInt_CurrentSlave_Cnt_M_u08	65	65	<b>✓</b>

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Name	Actual Value	Expected Value	Result
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE	INIT_COMPLETE	•
DigColPsInt_PrevReqDataType_Cnt_M_u08	2	2	•
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	3	3	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	100	100	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	556	556	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	564	564	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	88	88	•
tgt I2c GetStatus I2cRegPtr Cnt T str.SAR	3	3	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	100	100	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	2767	2767	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	9	9	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	100	100	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	556	556	
	100	100	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	2	2	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC			
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR	1	1	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT	2	2	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	3	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	100	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	7788	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	556	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	564	•
	88	88	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	3	3	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR			
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	100	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	2767	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	9	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	100	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	556	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	3	3	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100	100	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556	556	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	564	564	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	88	88	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	3	3	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100	100	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767	2767	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9	9	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	100	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556	556	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100	100	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	2	2	
	0	0	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	•
	0 1 3	0 1 3	•

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Name	Actual Value	Expected Value	Result
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3	3	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100	100	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788	7788	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556	556	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564	564	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88	88	•
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.SAR	3	3	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	100	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	2767	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	9	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	100	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556	556	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	100	~
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	2	2	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>~</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	_
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	_
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	_
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	0	0	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	_
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	3	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	100	_
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	_
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	556	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	_
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	88	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3	3	_
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100	100	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767	2767	-
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	100	100	•
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	556	556	-
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	100	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.Pb12	2	2	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	-
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	1	1	-
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	3	3	-
tgt_l2c_SetupMasterTransmit_l2cRegPtt_Cnt_T_str.DinV	2	2	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	0	0	-
tgt_lzc_SetupMasterTransmit_l2cRegPtr_Cnt_1_str.SE1  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	1	1	
	3	3	-
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	0	0	
		3	-
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3	3	

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	~

Test Step 2.12 (Repeat Count = 1)		✓
Name	Input Value	
DigColPsInt_Buffer_Cnt_M_u08[0]	44	
DigColPsInt_Buffer_Cnt_M_u08[1]	55	
DigColPsInt_Buffer_Cnt_M_u08[2]	66	
DigColPsInt_CurrentSlave_Cnt_M_u08	78	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_SETREG	
DigColPsInt_PrevReqDataType_Cnt_M_u08	3	
DigColPsInt_SensInitialized_Cnt_M_lgc	1	
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1	

DigColPsInt\_StartRequest

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DigCoiPSIIIL_StartRequest		
Name	Input Value	
2c_GetStatus()	4000	
c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str	
tc_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str	
c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str	
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str	
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str	
ype_Cnt_T_u08	3	
cREG1_temp	target_i2cREG1_temp	
_ColSensorl2CAddress_Cnt_u08	55	
arget_i2cREG1_temp.OAR	678	
arget_i2cREG1_temp.IMR	45	
arget_i2cREG1_temp.STR	66	
arget_i2cREG1_temp.CLKL	56	
arget_i2cREG1_temp.CLKH	6788	
rget_i2cREG1_temp.CNT	7878	
rget_i2cREG1_temp.DRR	12	
rget_i2cREG1_temp.SAR	678	
arget_i2cREG1_temp.DXR	45	
rget_i2cREG1_temp.MDR	56	
rget_i2cREG1_temp.IVR	778	
arget_i2cREG1_temp.EMDR	1	
arget_i2cREG1_temp.PSC	45	
urget_i2cREG1_temp.PID11	6788	
arget_i2cREG1_temp.PID12	45	
arget_i2cREG1_temp.DMAC	1	
arget_i2cREG1_temp.FUN	1	
arget_i2cREG1_temp.DIR	0	
arget_i2cREG1_temp.DIN	1	
arget_i2cREG1_temp.DOUT	1	
arget_i2cREG1_temp.SET	1	
arget_i2cREG1_temp.CLR	0	
arget_i2cREG1_temp.ODR	1	
arget_i2cREG1_temp.PD	2	
arget i2cREG1 temp.PSL	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	678	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	45	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	66	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	56	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	6788	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	7878	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	12	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	678	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	45	
pt I2c GetStatus I2cRegPtr Cnt T str.MDR	56	
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	778	
yt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	
	45	
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	6788	
yt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	45	
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	1	
yt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC		
t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0	
t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1	
t_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT	1	
t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	1	
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0	
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1	
t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	2	
t_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	1	
t_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	678	
t_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	45	
t_l2c_Send_l2cRegPtr_Cnt_T_str.STR	66	
t_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	56	
t_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	6788	
t_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	7878	
yt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	
t_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	678	
t_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	45	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	56	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	778	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	45	

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Name	Input Value
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	45
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1
tgt I2c SetRecv I2cRegPtr Cnt T str.OAR	678
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	45
	66
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	56
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	6788
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	7878
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	12
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	678
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	45
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	56
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	778
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	45
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	6788
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	45
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	0
	1
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	2
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	1
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	678
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	45
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	56
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	6788
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	7878
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	678
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	45
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	56
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	778
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	1
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	45
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	6788
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	45
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	1
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.FUN	1
	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	1
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	0
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	1
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	678
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	45
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	56
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	6788
	7878
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	12
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	12 678
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	12 678 45
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	12 678 45 56
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	12 678 45

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3			
Name	Input Value		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	45		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	6788		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	45 1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	2		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	1		1
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	44	44	<b>Y</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	55 66	55	<b>V</b>
DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08	78	78	-
DigColPsInt CurrentStepNo Cnt M enum	INIT_SENSOR1_READEXTERR_SETREG	INIT_SENSOR1_READEXTERR_SETREG	J
DigColPsInt_PrevReqDataType_Cnt_M_u08	3	3	-
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1	1	-
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	678	678	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR	45	45	-
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	66	66	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	56	56	-
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT	7878	7878	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR	12	12	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	678	678	· ·
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	45 56	56 56	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR	778	778	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	J
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	45	45	-
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	6788	6788	-
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	45	45	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN	1	1	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	· ·
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	J
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	
tgt I2c GetStatus I2cRegPtr Cnt T str.PD	2	2	,
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	1	1	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	678	678	-
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	45	45	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	66	66	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	56	56	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	6788	6788	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	7878	7878	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	· ·
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SAR tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	678 45	678 45	J
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	56	56	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	778	778	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	1	1	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	45	45	-
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	6788	6788	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	45	45	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>V</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	- V
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	0	0	-
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	1	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	678	678	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	45	45	-

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Name	Actual Value	Expected Value	Result
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	66 56	66 56	<b>'</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	6788	6788	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	7878	7878	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	12	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	678	678	_
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	45	45	<b>~</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	56	56	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	778	778	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	1	1	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	45	45	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	6788	6788	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	45	45	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	0	0	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	1	1	· ·
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	J
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	1	1	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	678	678	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	45	45	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	66	66	-
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	56	56	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	7878	7878	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	12	12	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	678	678	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	45	45	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	56	56	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	778	778	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	1	1	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	45	45	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	6788	6788	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	45	45	<b>V</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.DIN	1	1	
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	1	1	·
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	-
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>~</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	1	1	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	678	678	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	45	45	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	66	66	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	56	56	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	7878	7878	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	12	12	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	678	678	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	45	45	¥
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	56	56	-4
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	778	778 1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	45	45	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	6788	6788	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	45	45	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	_
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	-
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN			
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	1	1	<b>~</b>
		1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1		~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	1	1	· ·
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	1 1 0	1 0	· · · · · · · · · · · · · · · · · · ·

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	(
Name	Input Value
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	78
	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	495
	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	56
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	78
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	0
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	56
tot 12c SetunMasterReceive 12cDooDtr Cnt T str DID12	78
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	0
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	0
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0 0
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	0

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DigColPsint_StartRequest		[GEC]	CHU
Name	Input Value		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	0		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	0		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	0		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.PSL	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	78		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	495		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98 98		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	98		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	1		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	•
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	•
DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08	30 40	30 40	
DigCoir sint_Currentsiave_Crit ivi doo	40	40	•
	INIT NOT INITIALIZED	INIT NOT INITIALIZED	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_NOT_INITIALIZED  1	INIT_NOT_INITIALIZED  1	
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08	1	1	•
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1 0 66 78	1 0	
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	1 0 66 78 78	1 0 66 78 78	
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	1 0 66 78 78 495	1 0 66 78 78 495	
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	1 0 66 78 78 495 56	1 0 66 78 78 495 56	
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT	1 0 66 78 78 495 56 897	1 0 66 78 78 495 56	
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR	1 0 66 78 78 495 56 897 98	1 0 66 78 78 495 56 897 98	
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SAR	1 0 66 78 78 495 56 897	1 0 66 78 78 495 56	
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR	1 0 66 78 78 495 56 897 98	1 0 66 78 78 495 56 897 98	
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR	1 0 66 78 78 495 56 897 98 66 78	1 0 66 78 78 495 56 897 98 66 78	
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DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DID12  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC	1 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 78	1 0 66 78 78 495 56 897 98 66 78 495 66 0 78	
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DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PDC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN	1 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 78	1 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 78	
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DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PBD  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PBD  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PBD11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DINAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DINAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUR	1 0 66 78 78 78 495 56 897 98 66 78 495 66 0 78 56 78 0 0 0 1 0 0 0 1 0 0 66 78	1 0 66 78 78 78 495 56 897 98 66 78 495 66 0 78 56 78 0 0 0 1 0 0 1 0 0 0 1 0 0 66 78	
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DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PDC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PDD11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PDD12  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DR  tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLK  tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLK  tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLK	1 0 666 78 78 495 566 897 98 666 78 495 666 0 0 78 566 78 0 0 0 0 1 0 0 0 0 0 1 1 0 0 0 666 78 78 78 495 566	1 0 66 78 78 78 495 56 897 98 66 78 495 66 0 78 56 78 0 0 0 1 0 0 0 1 0 0 66 78 78 78 495 56	
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PDC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PDC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PDD11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DINAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUR  tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	1 0 666 78 78 495 566 897 98 666 78 78 495 566 897 98 696 78 78 78 78 78 78 78 78 78 78 78 78 78	1 0 66 78 78 78 495 56 897 98 66 78 495 66 0 78 56 78 0 0 0 1 0 0 1 0 0 1 0 0 66 78 78 495 56 897 98	
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PIDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DL  tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DL  tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DL  tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DLR  tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DLR	1 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 78 0 0 0 1 0 0 1 0 0 66 78 78 495 56 897 98	1 0 66 78 78 78 495 56 897 98 66 78 495 66 0 78 56 78 0 0 0 1 0 0 0 1 0 0 0 1 0 0 66 78 78 495 56 897 98	

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Name	Actual Value	Expected Value	Result
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	78	78	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56 78	56 78	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	0	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC tgt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	0	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	1	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	•
tgt I2c Send I2cRegPtr Cnt T str.CLR	0	0	•
tgt I2c Send I2cRegPtr Cnt T str.ODR	1	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	66	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	78	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78	78	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	495	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	56	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	897	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	98	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66	66	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78	78	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495	495	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66	66	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	0	0	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	78	78	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	56	56	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78 0	78 0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	0	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	0	0	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	1	1	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	0	0	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	1	1	•
tgt I2c SetRecv I2cRegPtr Cnt T str.PD	0	0	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	66	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78	78	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78	78	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495	495	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56	56	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	897	897	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98	98	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66	66	<b>→</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78	78	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495	495	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	66	66	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	78	78	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56	56	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	78 0	78 0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	1	1	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	0	0	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	0	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	1	1	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	56	56	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	

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Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	495	495	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	0	0	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	0	0	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	40
DigColPsInt_Buffer_Cnt_M_u08[1]	50
pigColPsInt_Buffer_Cnt_M_u08[2]	60
DigColPsInt CurrentSlave Cnt M u08	55
DigColPsInt CurrentStepNo Cnt M enum	READ COMPLETE
DigColPsInt PrevReqDataType Cnt M u08	2
DigColPsInt_SensInitialized_Cnt_M_lgc	1
bigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
2c GetStatus()	554
2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	tgt_l2c_Send_l2cRegPtr_Cnt_T_str
2c SetRecv(I2cRegPtr Cnt T str)	tgt I2c SetRecv I2cRegPtr Cnt T str
2c SetupMasterReceive(I2cRegPtr Cnt T str)	tgt I2c SetupMasterReceive I2cRegPtr Cnt T str
2c SetupMasterTransmit(I2cRegPtr Cnt T str)	tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str
ype_Cnt_T_u08	tgt_lzc_SetupwasterTransmit_lzcRegPti_Cnt_1_sti
ype_Crit_i_uuo 2cREG1 temp	target i2cREG1 temp
_ColSensorl2CAddress_Cnt_u08	20
	567
arget_i2cREG1_temp.OAR	44
arget_i2cREG1_temp.IMR	444
arget_i2cREG1_temp.STR	
arget_i2cREG1_temp.CLKL	566
arget_i2cREG1_temp.CLKH	4466
arget_i2cREG1_temp.CNT	129
arget_i2cREG1_temp.DRR	6
arget_i2cREG1_temp.SAR	567
arget_i2cREG1_temp.DXR	44
arget_i2cREG1_temp.MDR	566
arget_i2cREG1_temp.IVR	554
arget_i2cREG1_temp.EMDR	1
arget_i2cREG1_temp.PSC	44
arget_i2cREG1_temp.PID11	4466
arget_i2cREG1_temp.PID12	44
arget_i2cREG1_temp.DMAC	1
arget_i2cREG1_temp.FUN	1
arget_i2cREG1_temp.DIR	2
arget_i2cREG1_temp.DIN	0
arget_i2cREG1_temp.DOUT	1
arget_i2cREG1_temp.SET	1
arget_i2cREG1_temp.CLR	2
arget_i2cREG1_temp.ODR	0
arget_i2cREG1_temp.PD	3
arget_i2cREG1_temp.PSL	3
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	567
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	44
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	4444
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	566

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Name	Input Value
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	129
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	6
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SAR	567
tgt I2c GetStatus I2cRegPtr Cnt T str.DXR	44
tgt I2c GetStatus I2cRegPtr Cnt T str.MDR	566
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	554
	1
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC	44
	4466
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	44
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	0
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT	1
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET	1
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR	2
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	4466
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	129
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	567
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	554
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
	1
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	567
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	44
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	566
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	554
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	1
	1
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
	3
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3

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		• "	
Name	Input Value		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	567		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	44		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	6		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	567		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	44		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	566		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	554		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	2		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3		
Name			
	Actual Value	Expected Value	Resu
	Actual Value	Expected Value	Resu
DigColPsInt_Buffer_Cnt_M_u08[0]		·	Resu
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	38	38	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	38 50	38 50	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08	38 50 60	38 50 60	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum	38 50 60 20	38 50 60 20	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08	38 50 60 20 READ_SENSOR1_SETREG	38 50 60 20 READ_SENSOR1_SETREG	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	38 50 60 20 READ_SENSOR1_SETREG 4	38 50 60 20 READ_SENSOR1_SETREG 4	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc I2c_Send(Length_Cnt_T_u32)	38 50 60 20 READ_SENSOR1_SETREG 4 0	38 50 60 20 READ_SENSOR1_SETREG 4 0	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc I2c_Send(Length_Cnt_T_u32) tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	38 50 60 20 READ_SENSOR1_SETREG 4 0 1	38 50 60 20 READ_SENSOR1_SETREG 4 0 1	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc I2c_Send(Length_Cnt_T_u32) tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc I2c_Send(Length_Cnt_T_u32) tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	38 50 60 20 READ_SENSOR1_SETREG 4 0 1	38 50 60 20 READ_SENSOR1_SETREG 4 0 1	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc I2c_Send(Length_Cnt_T_u32) tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.JMR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc I2c_Send(Length_Cnt_T_u32) tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.JMR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc I2c_Send(Length_Cnt_T_u32) tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.JMR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc I2c_Send(Length_Cnt_T_u32) tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129 6	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129 6	
DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  I2c_Send(Length_Cnt_T_u32)  Igt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR  Igt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR  Igt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR  Igt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL  Igt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL  Igt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH  Igt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT  Igt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT  Igt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT  Igt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR  Igt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR  Igt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR  Igt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129 6 567	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129 6 567	
DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  I2c_Send(Length_Cnt_T_u32)  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.JMR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129 6 567 44	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129 6 567 44	
DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_u08  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  I2c_Send(Length_Cnt_T_u32)  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DAR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DAR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DAR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DAR	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129 6 567 44 566	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129 6 567 44 566	
DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  I2c_Send(Length_Cnt_T_u32)  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DAR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DNR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.NVR	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129 6 567 44 566 554	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129 6 567 44 566 554	
DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  12c_Send(Length_Cnt_T_u32)  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.OAR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.JMR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.STR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.CLKL  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.CLKL  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.CLKH  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.CNT  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DRR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DRR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DRR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DXR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DXR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DXR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.MDR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.MDR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DXR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DXR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DXR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DXR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DXR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DXR	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129 6 567 44 566 554	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129 6 567 44 566 554	
DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  I2c_Send(Length_Cnt_T_u32)  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.JIMR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DKR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.BNDR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.BNDR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.BNDR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.BNDR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.BNDR  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129 6 567 44 566 554	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129 6 567 44 566 554	
DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  12c_Send(Length_Cnt_T_u32)  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.OAR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.IMR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.CkL  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.CkL  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.CkL  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.CkH  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.CkH  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DkR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DkR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DkR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DkR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DkR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DkR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.DkR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.MDR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.WR  tgt_12c_GetStatus_12cRegPtr_Cnt_T_str.EMDR	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129 6 567 44 566 554	38 50 60 20 READ_SENSOR1_SETREG 4 0 1 567 44 4444 566 4466 129 6 567 44 566 554	

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Name	Actual Value	Expected Value	Result
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN	1	1	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET	1	1	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR	2	2	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR	0	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	
tgt I2c Send I2cRegPtr Cnt T str.IMR	44	44	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	129	129	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	6	6	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	566	566	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	44	44	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	566	566	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	554	554	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	1	1	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	44	44	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	44	44	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1 2	1 2	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	1	1	
	1	1	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetRecv_l2cRegPtr_Cnt_T str.CLR	2	2	
	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	3	3	
	567	567	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	44	44	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.NR  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	4444	4444	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	566	566	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	4466	4466	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	129	129	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	6	6	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	567	567	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	44	44	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	566	566	
.gsoctopinactor/tocor/c_izortogi ii_Oni_i_sii.iviDit		554	
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str IVR	554		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR tgt l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	554	1	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC			

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Name	Actual Value	Expected Value	Result
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	44	44	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	1	1	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	2	2	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	0	0	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	3	3	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	567	567	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	44	44	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	4444	4444	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	566	566	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	554	554	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	1	1	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	44	44	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	4466	4466	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	0	0	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>

T				V
Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c Send	1	I2c Send	1	<b>✓</b>

Test Step 2.15 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	70
DigColPsInt_Buffer_Cnt_M_u08[1]	80
DigColPsInt_Buffer_Cnt_M_u08[2]	90
DigColPsInt_CurrentSlave_Cnt_M_u08	60
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
I2c_GetStatus()	766
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	3
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	30
target_i2cREG1_temp.OAR	65
target_i2cREG1_temp.IMR	89
target_i2cREG1_temp.STR	67
target_i2cREG1_temp.CLKL	7
target_i2cREG1_temp.CLKH	577
target_i2cREG1_temp.CNT	88
target_i2cREG1_temp.DRR	23

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Name	Input Value	
arget i2cREG1 temp.SAR	65	
arget i2cREG1 temp.DXR	89	
arget_i2cREG1_temp.MDR	7	
	44	
arget_i2cREG1_temp.IVR		
arget_i2cREG1_temp.EMDR	2	
arget_i2cREG1_temp.PSC	89	
arget_i2cREG1_temp.PID11	577	
arget_i2cREG1_temp.PID12	89	
arget_i2cREG1_temp.DMAC	2	
arget_i2cREG1_temp.FUN	0	
arget_i2cREG1_temp.DIR	0	
arget_i2cREG1_temp.DIN	1	
arget_i2cREG1_temp.DOUT	2	
arget_i2cREG1_temp.SET	2	
arget_i2cREG1_temp.CLR	0	
arget i2cREG1 temp.ODR	1	
~	2	
arget_i2cREG1_temp.PD		
arget_i2cREG1_temp.PSL	0	
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	65	
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	89	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	67	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	7	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH	577	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	88	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	23	
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	65	
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	89	
	7	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR		
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	44	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	89	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	577	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12	89	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1	
gt I2c GetStatus I2cRegPtr Cnt T str.DOUT	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PD	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	
	88	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT		
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	
t_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	
t_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	2	
	0	
t_I2c_Send_I2cRegPtr_Cnt_T_str.FUN		
yt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	
yt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
ıt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	
pt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	
	65	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR		
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7	

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Name	Input Value		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	2		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0		
	1		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR			
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.IMR	89		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67		
	7		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL			
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.SAR	65		
	89		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR			
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	7		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	44		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577		
	89		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12			
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	65		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	577		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88		
	23		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	44		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2		
	0		
tot I2c SetupMasterTransmit I2cRegPtr Cnt T str CLR			
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	2		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR			
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	2	Expected Value	Result
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name	2 0 Actual Value	•	Result
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	2	Expected Value 36 80	Result

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Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[2]	90	90	•
DigColPsInt_CurrentSlave_Cnt_M_u08	30	30	•
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG	READ_SENSOR1_SETREG	•
DigColPsInt_PrevReqDataType_Cnt_M_u08	3	3	•
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	•
l2c_Send(Length_Cnt_T_u32)	1	1	•
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR	65	65	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR	89	89	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	67	67	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	7	7	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH	577	577	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	88	88	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	23	23	•
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SAR	65	65	•
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	89	89	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	7	7	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	44	44	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	2	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	89	89	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	577	577	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	89	89	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR	0	0	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN	1	1	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	65	65	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	89	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	67	67	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	7	7	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	577	577	
tgt I2c Send I2cRegPtr Cnt T str.CNT	88	88	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	65	65	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	89	89	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	7	7	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	44	44	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	2	2	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	89	89	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	577	577	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	1	1	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	2	2	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65	65	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89	89	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67	67	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7	7	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577	577	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88	88	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	23	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	65	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	89	89	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7	7	
rgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44	44	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	2	2	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89	89	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577	577	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89	89	
J	**	**	

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Name	Actual Value	Expected Value	Result
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	2	2	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	2	2	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	1	1	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	2	2	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	65	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	89	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67	67	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88	88	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23	23	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65	65	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89	89	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7	7	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44	44	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89	89	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577	577	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	89	89	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	2	2	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	89	89	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	7	7	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	65	65	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	7	7	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	577	577	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	0	0	<b>~</b>

Т				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c Send	1	I2c Send	1	-

Test Step 2.16 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	44

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DigColFsmi_StartRequest	
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[1]	55
DigColPsInt_Buffer_Cnt_M_u08[2]	66
DigColPsInt_CurrentSlave_Cnt_M_u08	55
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_READ
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
2c_GetStatus()	655
2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	tgt_l2c_Send_l2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt I2c SetupMasterReceive I2cRegPtr Cnt T str
2c SetupMasterTransmit(I2cRegPtr Cnt T str)	tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
	3
2cREG1_temp	target i2cREG1 temp
_ColSensorI2CAddress_Cnt_u08	55
arget_i2cREG1_temp.OAR	55
arget_i2cREG1_temp.IMR	66
arget_i2cREG1_temp.STR	556
	2309
arget_i2cREG1_temp.CLKL	
arget_i2cREG1_temp.CLKH	1204
arget_i2cREG1_temp.CNT	87
arget_i2cREG1_temp.DRR	67
arget_i2cREG1_temp.SAR	55
arget_i2cREG1_temp.DXR	66
arget_i2cREG1_temp.MDR	2309
arget_i2cREG1_temp.IVR	5
arget_i2cREG1_temp.EMDR	3
arget_i2cREG1_temp.PSC	66
arget_i2cREG1_temp.PID11	1204
arget_i2cREG1_temp.PID12	66
arget_i2cREG1_temp.DMAC	3
arget i2cREG1 temp.FUN	1
arget i2cREG1 temp.DIR	1
arget_i2cREG1_temp.DIN	2
arget_i2cREG1_temp.DOUT	3
arget_i2cREG1_temp.SET	3
arget_i2cREG1_temp.CLR	1
arget i2cREG1 temp.ODR	2
arget i2cREG1 temp.PD	3
	3
arget_i2cREG1_temp.PSL	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	55
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	66
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	556
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	87
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	67
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	55
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	66
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	5
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	66
t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
t_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12	66
pt_12c_GetStatus_12cRegPtr_Cnt_T_str.PiD12	3
	1
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	
t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	1
t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	2
t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3
t_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR	1.
t_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR	2
t_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PD	3
pt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	3
pt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
yt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
	556
t I2c Send I2cReaPtr Cnt T str STR	555
	2309
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
gt_l2c_Send_l2cRegPtr_Cnt_T_str.STR gt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL gt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH gt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	2309 1204 87

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DigColFSint_Stankequest		1000
Name	Input Value	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	66	
	1204	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PlD11	66	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	3	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC		
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	556	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	55	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	66	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	2309	
	5	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	3	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	66	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	1204	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	
tgt I2c SetRecv I2cRegPtr Cnt T str.ODR	2	
tgt I2c SetRecv I2cRegPtr Cnt T str.PD	3	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	556	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	2309	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	1204	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	87	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	67	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	66	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	2	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	3	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	3	
	1	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	2	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	3	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	
	55	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	33	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	66	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	

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Name	Input Value		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	67		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	5		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	66		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	1204		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	44	44	~
DigColPsInt_Buffer_Cnt_M_u08[1]	55	55	•
DigColPsInt_Buffer_Cnt_M_u08[2]	66	66	~
DigColPsInt_CurrentSlave_Cnt_M_u08	55	55	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_READ	INIT_SENSOR2_CHECKSTAT_READ	~
DigColPsInt_PrevReqDataType_Cnt_M_u08	0	0	~
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1	1	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR	55	55	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR	66	66	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	556	556	<b>V</b>
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>V</b>
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>*</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	87 67	87 67	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR	66	66	-
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR	2309	2309	-
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC	3	3	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT	3	3	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET	3	3	<b>V</b>
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR	1	1	<b>•</b>
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR	2	2	<b>V</b>
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PD	3	3	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	3 55	3 55	<b>*</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	2309	2309	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
	1	66	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	66		
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	3	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3 1 1	1	· ·
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	3	1	~

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Name	Actual Value	Expected Value	Resul
gt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	•
gt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	1	1	•
gt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	2	2	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	•
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	,
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	•
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	3	3	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	•
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	•
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	67	67	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	55	55	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.MDR	2309	2309	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	3	3	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	1204	1204	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	3	3	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1	1	
	1	1	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT			
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	•
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	•
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	66	66	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	
	1	1	

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Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	3	3	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	2	2	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	3	3	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3	3	✓

	T	🗸			
Δ	ctual Function	Count	Expected Function	Count	Result
*1	none*	0	*** No Call Expected ***	0	~

Test Step 2.17 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	66
DigColPsInt_Buffer_Cnt_M_u08[1]	77
DigColPsInt Buffer Cnt M u08[2]	88
	11
DigColPsInt_CurrentSlave_Cnt_M_u08	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADADDRREG_SENDCMD
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_Igc	0
I2c_GetStatus()	123
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	1
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	40
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	78
target_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56
target i2cREG1 temp.CNT	897
target i2cREG1 temp.DRR	98
target i2cREG1 temp.SAR	66
target i2cREG1 temp.DXR	78
target_i2cREG1_temp.MDR	495
target_i2cREG1_temp.IVR	66
target i2cREG1 temp.EMDR	0
target i2cREG1 temp.PSC	78
target i2cREG1 temp.PID11	56
target i2cREG1 temp.PID12	78
	0
target_i2cREG1_temp.DMAC	
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	78
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	78
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT	897
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	495
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.lVR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	56
0	

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DigColPsini_StartRequest		1 1 2 1 2 1 2
Name	Input Value	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	78	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN	1	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT	0	
	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR		
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	78	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	495	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	0	
	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR		
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	66	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	78	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	56	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	
tgt I2c SetRecv I2cRegPtr Cnt T str.SAR	66	
tgt I2c SetRecv I2cRegPtr Cnt T str.DXR	78	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	495	
	66	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR		
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	1	
	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	78	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	78	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	98	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	66	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	78	
	495	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	66	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	0	

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Name	Input Value			
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78			
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	56			
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78 0			
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	0			
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0			
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1			
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	0			
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	0			
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0			
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1			
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	0			
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	0 66			
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	78			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495			
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	66 0			
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	78			
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	56			
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	78			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1			
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	0			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0			
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	0			
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0			
Name	Actual Value	Exped	cted Value	Resul
DigColPsInt_Buffer_Cnt_M_u08[0]	66	66		
DigColPsInt_Buffer_Cnt_M_u08[1]	77	77		•
DigColPsInt_Buffer_Cnt_M_u08[2]	88	88		•
DigColPsInt_CurrentSlave_Cnt_M_u08	11	11		•
DigColPsInt_CurrentStepNo_Cnt_M_enum			ENSOR2 EXTREADADDRREG SEN	•
DigColPsInt_PrevReqDataType_Cnt_M_u08	0	0		•
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0 66	0		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR	78	66 78		
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	78	78		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	495	495		
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	56	56		•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	897	897		•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR				
tot IOs CatCtatus IOsDosDts Cat T ats CAD	98	98		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SAR	66	66		
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	66 78	66 78		•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR	66 78 495	66 78 495		•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR	66 78 495 66	66 78 495 66		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR	66 78 495 66 0	66 78 495 66 0		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC	66 78 495 66 0 78	66 78 495 66 0 78		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	66 78 495 66 0	66 78 495 66 0		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC	66 78 495 66 0 78 56	66 78 495 66 0 78 56		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12	66 78 495 66 0 78 56	66 78 495 66 0 78 56 78		0
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC	66 78 495 66 0 78 56 78	66 78 495 66 0 78 56 78		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN	66 78 495 66 0 78 56 78 0 0	66 78 495 66 0 78 56 78 0		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT	66 78 495 66 0 78 56 78 0 0 0	66 78 495 66 0 78 56 78 0 0 0		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET	66 78 495 66 0 78 56 78 0 0 0	66 78 495 66 0 78 56 78 0 0 0		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DID12  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR	66 78 495 66 0 78 56 78 0 0 0 0	66 78 495 66 0 78 56 78 0 0 0 1		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CDR	66 78 495 66 0 78 56 78 0 0 0 1	66 78 495 66 0 78 56 78 0 0 0 0 1		0
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR	66 78 495 66 0 78 56 78 0 0 0 1 0 0 0	66 78 495 66 0 78 56 78 0 0 0 0 1		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PD  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	66 78 495 66 0 78 56 78 0 0 0 1 0 0 0 1	66 78 495 66 0 78 56 78 0 0 0 0 1 0 0		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUN  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DUT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR	66 78 495 66 0 78 56 78 0 0 0 1 0 0 0	66 78 495 66 0 78 56 78 0 0 0 0 1		

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Name	Actual Value	Expected Value	Result
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	<b>*</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	56 897	56 897	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	98	98	,
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	<b>✓</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	66	66	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	56   78	56 78	<b>*</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12 tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0	0	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	0 66	0	· ·
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	78	66 78	Ž
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.NTR	78	78	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	495	-
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	56	56	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	897	897	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	98	98	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66	66	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78	78	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495	495	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66	66	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	0   78	0 78	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	56	56	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	78	78	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	0	0	<b>V</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	0	0	-
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	66	66	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78	78	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	78	78	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	56	56	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	897	897	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98 66	98	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	78	66 78	Ž
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	495	495	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66	66	-
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	78	78	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	56	56	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	78	78	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>V</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	0	0	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	0	0	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	0	0	<b>V</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	0	0	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	0	0	~

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Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	78	78	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	495	495	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	495	495	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	0	0	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	56	56	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	0	0	<b>~</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	0	0	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~

T				✓
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 2.18 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
DigColPsInt Buffer Cnt M u08[0]	0
DigColPsInt Buffer Cnt M u08[1]	0
DigColPsInt Buffer Cnt M u08[2]	0
DigColPsInt CurrentSlave Cnt M u08	0
DigColPsInt CurrentStepNo Cnt M enum	INIT NOT INITIALIZED
DigColPsInt PrevRegDataType Cnt M u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt SkipRegisterWrite Cnt M Igc	0
I2c GetStatus()	0
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	0
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	0
target_i2cREG1_temp.OAR	0
target_i2cREG1_temp.IMR	0
target_i2cREG1_temp.STR	0
target_i2cREG1_temp.CLKL	0
target_i2cREG1_temp.CLKH	0
target_i2cREG1_temp.CNT	0
target_i2cREG1_temp.DRR	0
target_i2cREG1_temp.SAR	0
target_i2cREG1_temp.DXR	0
target_i2cREG1_temp.MDR	0
target_i2cREG1_temp.IVR	0
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	0
target_i2cREG1_temp.PID11	0
target_i2cREG1_temp.PID12	0
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0

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DigColPsint_StartRequest		- Table 1 (at
Name	Input Value	
target_i2cREG1_temp.CLR	0	
target_i2cREG1_temp.ODR	0	
target_i2cREG1_temp.PD	0	
target_i2cREG1_temp.PSL	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR	0	
	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL		
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	0	
	0	
igt_I2c_Send_I2cRegPtr_Cnt_T_str.STR		
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	0	
tgt I2c Send I2cRegPtr Cnt T str.EMDR	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	0	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	0	
	0	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR		
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	0	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	0	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	0	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	0	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	0	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	0	
igt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	0	
rgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	
	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	
	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC		

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<u> </u>			
Name	Input Value		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	0		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0		
GL_EG_OCIUPINIASICI TIATISTIIL_IZONEGF II_OTIL_I_SII.DIN	0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT			
	0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	0 0 0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0 0 0 0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	0 0 0 0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	0 0 0 0 0	Expected Value	Result
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	0 0 0 0 0 0	Expected Value	Result 🗸
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name	0 0 0 0 0 0 0 0 Actual Value	•	Result
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name DigColPsInt_Buffer_Cnt_M_u08[0]	0 0 0 0 0 0 0 0 <b>Actual Value</b>	0	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	0 0 0 0 0 0 0 <b>Actual Value</b> 0	0	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	0 0 0 0 0 0 0 0 <b>Actual Value</b> 0	0 0 0	~ ~ ~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08	0 0 0 0 0 0 0 0 <b>Actual Value</b> 0 0	0 0 0 0	· · ·
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum	0	0 0 0 0 init_not_initialized	· · · · · · · · · · · · · · · · · · ·
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08	0	0 0 0 0 INIT_NOT_INITIALIZED 0	· · · · · · · · · · · · · · · · · · ·
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0 0 0 0 INIT_NOT_INITIALIZED 0	· · · · · · · · · · · · · · · · · · ·
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR	0	0 0 0 INIT_NOT_INITIALIZED 0 0	· · · · · · · · · · · · · · · · · · ·
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR	0	0 0 0 INIT_NOT_INITIALIZED 0 0 0	· · · · · · · · · · · · · · · · · · ·
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	0	0 0 0 INIT_NOT_INITIALIZED 0 0 0 0 0	· · · · · · · · · · · · · · · · · · ·
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	0	0 0 0 INIT_NOT_INITIALIZED 0 0 0 0 0 0 0	· · · · · · · · · · · · · · · · · · ·
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD  tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	0	0 0 0 INIT_NOT_INITIALIZED 0 0 0 0 0 0 0 0 0	· · · · · · · · · · · · · · · · · · ·
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	0	0 0 0 0 INIT_NOT_INITIALIZED 0 0 0 0 0 0 0 0 0 0 0	· · · · · · · · · · · · · · · · · · ·
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT	0	0 0 0 0 INIT_NOT_INITIALIZED 0 0 0 0 0 0 0 0 0 0 0 0 0 0	· · · · · · · · · · · · · · · · · · ·

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N	A -4:1 V-I:	From a stand Walter	D14
Name	Actual Value	Expected Value	Result
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR	0	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FMDR	0	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	0	0	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	0	0	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	0	0	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC	0	0	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN	0	0	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET	0	0	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR	0	0	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>V</b>
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PD	0	0	· ·
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	0	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	0	0	- 4
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	0	0	J
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	0	0	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	0	0	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	0	0	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	0	0	<b>V</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	0	0	-
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	0	0	Ž
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	0	0	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	0	0	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	0	0	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	0	0	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	0	0	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	0	0	<b>J</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	0	0	_
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	0	0	<b>V</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	0	0	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	0	0	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	0	0	~

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Name	Actual Value	Expected Value	Result
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	0	0	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	0	0	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	0	0	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.lVR	0	0	·
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	0	0	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	0	0	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0	0	<b>~</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	·
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	0	0	·
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	0	0	·
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	0	0	·
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	·
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0	0	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>~</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>~</b>

T				V
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 2.19 (Repeat Count = 1)		
Name	Input Value	
DigColPsInt_Buffer_Cnt_M_u08[0]	255	
DigColPsInt_Buffer_Cnt_M_u08[1]	255	
DigColPsInt_Buffer_Cnt_M_u08[2]	255	
DigColPsInt_CurrentSlave_Cnt_M_u08	127	
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE	
DigColPsInt_PrevReqDataType_Cnt_M_u08	5	
DigColPsInt_SensInitialized_Cnt_M_lgc	1	
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1	
I2c_GetStatus()	65535	
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str	
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str	
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str	
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str	
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str	
Type_Cnt_T_u08	5	
i2cREG1_temp	target_i2cREG1_temp	
k_ColSensorl2CAddress_Cnt_u08	127	
target_i2cREG1_temp.OAR	1023	
target_i2cREG1_temp.IMR	255	
target_i2cREG1_temp.STR	32767	

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DigColPsini_StartRequest	[ WACT
Name	Input Value
arget_i2cREG1_temp.CLKL	65535
arget i2cREG1 temp.CLKH	65535
arget_i2cREG1_temp.CNT	65535
arget_i2cREG1_temp.DRR	255
arget_i2cREG1_temp.SAR	1023
arget_i2cREG1_temp.DXR	255
arget_i2cREG1_temp.MDR	65535
	4095
arget_i2cREG1_temp.IVR	3
arget_i2cREG1_temp.EMDR	
arget_i2cREG1_temp.PSC	255
arget_i2cREG1_temp.PID11	65535
arget_i2cREG1_temp.PID12	255
arget_i2cREG1_temp.DMAC	3
arget_i2cREG1_temp.FUN	1
arget_i2cREG1_temp.DIR	3
arget_i2cREG1_temp.DIN	3
arget_i2cREG1_temp.DOUT	3
arget_i2cREG1_temp.SET	3
arget_i2cREG1_temp.CLR	3
arget_i2cREG1_temp.ODR	3
arget_i2cREG1_temp.PD	3
arget_i2cREG1_temp.PSL	3
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	1023
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	255
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	32767
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	65535
t_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	65535
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	65535
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	255
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	1023
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	255
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	65535
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	4095
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	255
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	65535
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	255
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN	1
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR	3
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	3
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	3
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	3
pt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3
pt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023
pt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	255
yt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	32767
yt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535
t_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	65535
t_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	65535
	255
tt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	1023
t_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	
t_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	255
yt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	65535
t_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	4095
yt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
t_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	255
t_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	65535
t_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	255
t_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
t_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
t_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
yt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
t_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
yt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
gt_l2c_send_l2cRegPtr_Cnt_T_str.CLR	3
	3
yt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3 3
	1.5
gt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	1023

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DigColFSini_Stankequest		
Name	Input Value	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	255	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	32767	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	65535	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	65535	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	65535	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	255	
	1023	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	255	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR		
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	65535	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	4095	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	3	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	255	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	65535	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	255	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	3	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
pt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	
pt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	
yt_12c_SetRecv_12cRegPtr_Cnt_T_str.DOUT	3	
	3	
yt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET		
yt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	
pt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	3	
pt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	
pt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
t_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	1023	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	255	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	32767	
pt I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	65535	
yt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	65535	
yt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	65535	
t_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	255	
yt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	1023	
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	255	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	65535	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	4095	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	3	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	255	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	65535	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	255	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	
gt I2c SetupMasterReceive I2cRegPtr Cnt T str.DIN	3	
pt I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	3	
t_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	
pt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	
t_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	1023	
ıt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	255	
t_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	32767	
t_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	65535	
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	65535	
t I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT		
	65535	
t_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	255	
t_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	1023	
t_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	255	
t_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	65535	
t_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	4095	
t_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	3	
t_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	255	
t_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	65535	
t_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	255	
t_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	3	
t_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	
t_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	
t_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	
pt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	

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Name	Input Value		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL Name	3 Actual Value	Expected Value	Resul
DigColPsInt_Buffer_Cnt_M_u08[0]	255	255	Resul
DigColPsInt_Buffer_Cnt_M_u08[1]	255	255	
DigColPsInt_Buffer_Cnt_M_u08[2]	255	255	
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE	READ_COMPLETE	
	5	5	
DigColPsInt_PrevReqDataType_Cnt_M_u08	1	1	
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc			
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	1023	1023	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	255	255	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	32767	32767	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH	65535	65535	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT	65535	65535	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	255	255	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	1023	1023	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	255	255	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	65535	65535	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	4095	4095	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	255	255	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	65535	65535	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12	255	255	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC	3	3	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN	1	1	
tgt I2c GetStatus I2cRegPtr Cnt T str.DIR	3	3	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN	3	3	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT	3	3	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR	3	3	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR	3	3	
	3	3	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL			
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023	1023	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	255	255	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	32767	32767	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	65535	65535	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	65535	65535	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	255	255	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	1023	1023	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	255	255	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	65535	65535	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	4095	4095	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	· · · · · · · · · · · · · · · · · · ·
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	255	255	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	65535	65535	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	255	255	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	3	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1	1	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	3	3	
tgt I2c Send I2cRegPtr Cnt T str.DIN	3	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	3	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	3	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	3	3	
	3	3	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR			
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3	3	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	1023	1023	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	255	255	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	32767	32767	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	65535	65535	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	65535	65535	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	65535	65535	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	255	255	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	1023	1023	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	255	255	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	65535	65535	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	4095	4095	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	3	3	
-55-00.0000.0g. a_Ont_1_00.EMD/\			
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	255	255	

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Name	Actual Value	Expected Value	Result
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	255	255	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	3	3	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	1	1	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	3	3	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	3	3	<b>~</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	3	3	<b>→</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	3	3	<b>-</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>-</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	1023	1023	<b>-</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	255	255	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	32767	32767	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	65535	65535	<b>-</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	255	255	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	1023	1023	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	255	255	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	65535	65535	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	4095	4095	<b>-</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	3	3	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	255	255	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	65535	65535	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	255	255	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1	1	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	3	3	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	•
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	3	3	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	1023	1023	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	255	255	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	32767	32767	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	65535	65535	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	255	255	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	1023	1023	•
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	255	255	•
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	65535	65535	-
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	4095	4095	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	255	255	•
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	65535	65535	•
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	255	255	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	3	3	-
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	1	1	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	3	3	-
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	3	3	•
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	3	3	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	3	3	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	3	3	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	3	3	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	3	3	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3	3	· ·

T				V
Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	~



#### **Test Case 3: Path Test**

Description

Test Vector Description:

TS3.1"((DigColPsInt\_SensInitialized\_Cnt\_M\_lgc == TRUE) && (DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum >= INIT\_COMPLETE))=True ((Status\_Cnt\_T\_u16 & l2C\_BUSBUSY) == 0U)=True ((Type\_Cnt\_T\_u08 == D\_ANGLEDATA\_CNT\_U08) && (DigColPsInt\_PrevReqDataType\_Cnt\_M\_u08 == D\_ANGLEDATA\_CNT\_U08))=False ((Type\_Cnt\_T\_u08 > D\_NONE\_CNT\_U08) && (Type\_Cnt\_T\_u08 <= D\_STATUSREG\_CNT\_U08))=False" (TS3.2"((DigColPsInt\_SensInitialized\_Cnt\_M\_lgc == TRUE) && (DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum >= INIT\_COMPLETE))=True ((Status\_Cnt\_T\_u16 & l2C\_BUSBUSY) == 0U)=True ((Type\_Cnt\_T\_u08 == D\_ANGLEDATA\_CNT\_U08)) && (DigColPsInt\_PrevReqDataType\_Cnt\_M\_u08 == D\_ANGLEDATA\_CNT\_U08))=False ((Type\_Cnt\_T\_u08 > D\_NONE\_CNT\_U08) && (Type\_Cnt\_T\_u08 <= D\_STATUSREG\_CNT\_U08))=True" (TS3.3"((DigColPsInt\_SensInitialized\_Cnt\_M\_lgc == TRUE) && (DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum >= INIT\_COMPLETE))=True ((Type\_Cnt\_T\_u08 == D\_ANGLEDATA\_CNT\_U08)) && (DigColPsInt\_PrevReqDataType\_Cnt\_M\_u08 == D\_ANGLEDATA\_CNT\_U08))=True" (TS3.4"((DigColPsInt\_SensInitialized\_Cnt\_M\_lgc == TRUE) && (DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum >= INIT\_COMPLETE))=True ((Status\_Cnt\_T\_u16 & l2C\_BUSBUSY) == 0U)=False" (DigColPsInt\_SensInitialized\_Cnt\_M\_lgc == TRUE) && (DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum >= INIT\_COMPLETE))=True ((Status\_Cnt\_T\_u16 & l2C\_BUSBUSY) == 0U)=False" (DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum >= INIT\_COMPLETE))=False (Status\_Cnt\_T\_u16 & l2C\_BUSBUSY) == 0U)=False" (DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum >= INIT\_COMPLETE))=False

Test Step 3.1 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_CurrentSlave_Cnt_M_u08	40
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_Igc	0
I2c_GetStatus()	123
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	0
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	10
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	78
target_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56
target_i2cREG1_temp.CNT	897
target_i2cREG1_temp.DRR	98
target_i2cREG1_temp.SAR	66
target_i2cREG1_temp.DXR	78
target_i2cREG1_temp.MDR	495
target_i2cREG1_temp.IVR	66
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	78
target_i2cREG1_temp.PID11	56
target_i2cREG1_temp.PID12	78
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	56

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DigColPsini_StartRequest		1 1 2 1 2 1 2
Name	Input Value	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	78	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN	1	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT	0	
	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR		
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	78	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	495	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	0	
	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR		
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	66	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	78	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	56	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	
tgt I2c SetRecv I2cRegPtr Cnt T str.SAR	66	
tgt I2c SetRecv I2cRegPtr Cnt T str.DXR	78	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	495	
	66	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR		
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	1	
	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	78	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	78	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	98	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	66	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	78	
	495	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	66	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	0	

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tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.PSC	Input Value		
	78		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	56		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	0		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	495 56		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	897		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	98		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	78		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	0		
		Expected Value	Result
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]	0 Actual Value	10	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]	0 Actual Value 10 20	10 20	Ž
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]	0 Actual Value 10 20 30	10 20 30	*
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08	0 Actual Value 10 20 30 10	10 20 30 10	• • • • • • • • • • • • • • • • • • •
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum	0 Actual Value 10 20 30 10 INIT_COMPLETE	10 20 30 10 INIT_COMPLETE	*
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08	0 Actual Value 10 20 30 10 INIT_COMPLETE 0	10 20 30 10 INIT_COMPLETE 0	• • • • • • • • • • • • • • • • • • •
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0	10 20 30 10 INIT_COMPLETE 0	• • • • • • • • • • • • • • • • • • •
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08	0 Actual Value 10 20 30 10 INIT_COMPLETE 0	10 20 30 10 INIT_COMPLETE 0	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66	10 20 30 10 INIT_COMPLETE 0 0	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_u08  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78	10 20 30 10 INIT_COMPLETE 0 0 66	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_u08  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78	10 20 30 10 INIT_COMPLETE 0 0 66 78	
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_u08  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.OAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.STR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897	10 20 30 10 INIT_COMPLETE 0 0 66 78 78	0
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_u08  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.OAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.STR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CNT  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897	
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.OAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.STR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CNT  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98	
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.OAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.STR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CNT  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78	
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.OAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.STR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CNT  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.NDR	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_u08  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.NDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.NDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.NDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_u08  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_igc  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.BMR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 495 56 897 98 66 78 495 66 0 78	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.NR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.NR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56	
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_T_str.OAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.OAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.STR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKH  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.MDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.MDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.EMDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.EMDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PID11  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PID11  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PID11	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 495 56 897 98 66 78 495 66 0 78	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.NR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.NR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 78	10 20 30 10 INIT_COMPLETE 0 0 66 78 495 56 897 98 66 78 495 66 0 78 56 78	
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.OAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.STR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CNT  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.MDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.BNDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.EMDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.EMDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDC  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PID11  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PID12  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DMAC	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 78	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 78	
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.OAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.ENR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKH  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.MDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.MDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.EMDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.EMDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDC  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDC  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PID11  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PID12  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DMAC  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.FUN	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 495 66 0 78	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 78	
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.OAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.EMR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.EMDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.EMDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.EMDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.EMDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PID11  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PID12  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DMAC  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 495 66 0 78	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 78	
tgt_!2c_SetupMasterTransmit_i2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.OAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.STR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CkL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CkL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CkH  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DXR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DNR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDD11  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PID11  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DMAC  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIR	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 78 0 0 0 1	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 495 60 0 1	
tgt_!2c_SetupMasterTransmit_i2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_SkipRegisterWrite_Cnt_M_log  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.OAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKH  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.MDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.MDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PSC  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PSC  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PID11  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIAC  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUT  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUT  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUT  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUT  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLR	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 495 66 0 0 0 0 1 0 0 0 0	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 78 0 0 0 0 0	
tgt_!2c_SetupMasterTransmit_i2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_SkipRegisterWrite_Cnt_M_log  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.OAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKH  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDD1  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PD11  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN1  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUT	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 495 66 0 0 1 0 0 1 1 0 0 0 1	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 78 0 0 0 1	
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_SkipRegisterWrite_Cnt_M_log  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.OAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDD11  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PID11  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUT  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUR	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 78 0 0 0 1 0 0 1 0 1 0 0 1	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 70 0 0 0 1 0 0 1	
tgt_!2c_SetupMasterTransmit_i2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_SkipRegisterWrite_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_T_str.OAR tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.AR tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CkI tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CkI tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DkR tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DkR tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DkR tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DkR tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PiD11 tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PiD11 tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.Din1 tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.Din2 tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.Din3 tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.Din4 tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.Din5 tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.Din6 tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DOUT	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 78 0 0 0 1 0 0 1 0 0 0 0 1	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 70 0 0 0 1 0 0 0 1	
tgt_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL  Name  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_PrevReqDataType_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.OAR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.ARR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CLKL  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.CNT  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DRR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.MDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDR  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDD1  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.PDD1  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DNAC  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DNAC  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DIN  tgt_!2c_GetStatus_!2cRegPtr_Cnt_T_str.DUT	0 Actual Value 10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 78 0 0 0 1 0 0 1 0 1 0 0 1	10 20 30 10 INIT_COMPLETE 0 0 66 78 78 495 56 897 98 66 78 495 66 0 78 56 70 0 0 0 1 0 0 1	

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Name	Actual Value	Expected Value	Result
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	56	56	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	897	897	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	98	98	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66 78	66 78	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	495	495	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.MDR tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	66	66	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	0	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	78	78	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	78	78	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	0	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	0	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	66	
tgt I2c SetRecv I2cRegPtr Cnt T str.IMR	78	78	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	78	78	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	495	
tgt I2c SetRecv I2cRegPtr Cnt T str.CLKH	56	56	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	897	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	98	98	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66	66	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78	78	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	495	495	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	66	66	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	78	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	56	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78	78	
tgt I2c SetRecv I2cRegPtr Cnt T str.DMAC	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	
tgt I2c SetRecv I2cRegPtr Cnt T str.DIN	1	1	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	66	66	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78	78	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	78	78	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495	495	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56	56	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897	897	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98	98	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66	66	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78	78	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495	495	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66	66	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78	78	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56	56	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78	78	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	1	1	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	0	0	
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	1	1	- I • •
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	0	0	

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Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	-
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	78	78	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	495	495	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	56	56	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	897	897	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	66	66	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	78	78	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	495	495	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	66	66	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	0	0	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	78	78	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	56	56	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	78	78	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	0	0	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0	0	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>~</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~

Т				V
Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	-

Name         Input Value           DigColPsInt_Buffer_Cnt_M_u08[0]         40           DigColPsInt_Buffer_Cnt_M_u08[1]         50           DigColPsInt_Buffer_Cnt_M_u08[2]         60           DigColPsInt_CurrentSlave_Cnt_M_u08         55           DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_COMPLETE           DigColPsInt_PrevReqDataType_Cnt_M_u08         2           DigColPsInt_SensInitialized_Cnt_M_lgc         1           DigColPsInt_SkipRegisterWrite_Cnt_M_lgc         1           12c_GetStatus()         554           12c_GetStatus(l2cRegPtr_Cnt_T_str)         tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str           12c_Send(l2cRegPtr_Cnt_T_str)         tgt_l2c_Send_l2cRegPtr_Cnt_T_str           12c_SetRecv(l2cRegPtr_Cnt_T_str)         tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str           12c_SetPRecv(l2cRegPtr_Cnt_T_str)         tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str           12c_SetupMasterReceive(l2cRegPtr_Cnt_T_str)         tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str	Test Step 3.2 (Repeat Count = 1)	<b>✓</b>
DigCoPisht   Buffer_Cnt_M_u08[1]   50     DigCoPisht   Buffer_Cnt_M_u08[2]   60     DigCoPisht   Buffer_Cnt_M_u08[2]   60     DigCoPisht   CurrentSierve_Cnt_M_u08   55     DigCoPisht_CurrentSierve_Cnt_M_u08   55     DigCoPisht_CurrentSierve_Cnt_M_u08   2     DigCoPisht_Sensitialized_Cnt_M_u08   2     DigCoPisht_Sensitialized_Cnt_M_u08   2     DigCoPisht_Sensitialized_Cnt_M_u08   2     DigCoPisht_Sensitialized_Cnt_M_u08   1     Liz_CoEstiatus(CategoPir_Cnt_T_str)   1     Liz_Coestiatus(CategoPir_Cnt_		Input Value
DigCoPisin   Buffer_Cnt_M u08 1		
DigCoIPsint Buffer_Cnt_M_u08[2]         60           DigCoIPsint_CurrentSiave_Cnt_M_u08         55           DigCoIPsint_PrevRecDataType_Cnt_M_u08         2           DigCoIPsint_Sensinitalized_Cnt_M_lgc         1           DigCoIPsint_ShipRegisterWrite_Cnt_M lgc         1           Lize_GetStatus()         554           Lize_GetStatus()         554           Lize_GetStatus()CRegPtr_Cnt_T_str)         tg_Lize_GetStatus_J2cRegPtr_Cnt_T_str           Lize_GetStatus()CRegPtr_Cnt_T_str)         tg_Lize_GetStatus_J2cRegPtr_Cnt_T_str           Lize_SetupMasterReceive(IzeRegPtr_Cnt_T_str)         tg_Lize_Send_IzeRegPtr_Cnt_T_str           Lize_SetupMasterTransmit(IzeRegPtr_Cnt_T_str)         tg_Lize_SetupMasterTransmit(IzeRegPtr_Cnt_T_str)           <		50
DigCoPaint_CurrentSiave_Cnt_M_u08         55           DigCoPaint_CurrentSiave_Cnt_M_enum         INT_COMPLETE           DigCoPaint_SereReDataType_Cnt_M_u08         2           DigCoPaint_Seinshidaized_Cnt_M_lgc         1           DigCoPaint_Seinshidaized_Cnt_M_lgc         1           L2c_GetSlatus()         554           L2c_GetSlatus()         554           L2c_Send(JcRegPtr_Cnt_T_str)         Ig_L2c_Send_L2cRegPtr_Cnt_T_str           L2c_Send(JcRegPtr_Cnt_T_str)         Ig_L2c_Send_L2cRegPtr_Cnt_T_str           L2c_SetMeylasterReceive(JcRegPtr_Cnt_T_str)         Ig_L2c_SetupMasterReceive_L2cRegPtr_Cnt_T_str           L2c_SetupMasterReceive(JcRegPtr_Cnt_T_str)         Ig_L2c_SetupMasterTransmit(JcRegPtr_Cnt_T_str           L2c_SetupMasterTransmit(JcRegPtr_Cnt_T_str)         Ig_L2c_SetupMasterTransmit(JcRegPtr_Cnt_T_str           Type_Cnt_T_u08         5           L2c_REG1_temp         target_L2cReG1_temp           L2c_REG1_temp         44           Larget_L2cReG1_temp_DAR         44           Larget_L2cReG1_temp_CLKL         446           Larget_L2cReG1_temp_CLKL         446           Larget_L2cReG1_temp_DRR         6           Larget_L2cReG1_temp_DRR         6           Larget_L2cReG1_temp_DRR         6           Larget_L2cReG1_temp_DMR         44		60
DigColPsint_CurrentStepNo_Cnt_M_enum         INIT_COMPLETE           DigColPsint_PrevRepDataType_Cnt_M_u08         2           DigColPsint_SkipRegisterWrite_Cnt_M_u0c         1           DigColPsint_SkipRegisterWrite_Cnt_M_u0c         1           Use_GetStatus()         554           Use_GetStatus()         554           Use_GetStatus()         Use_Loc GetStatus _ LocRegPtr_Cnt_T_str           Use_Send(UzeRegPtr_Cnt_T_str)         Use_LocRegPtr_Cnt_T_str           Use_Send(UzeRegPtr_Cnt_T_str)         Use_Send_UzeRegPtr_Cnt_T_str           Use_Send(UzeRegPtr_Cnt_T_str)         Use_Send_UzeRegPtr_Cnt_T_str           Use_Send(UzeRegPtr_Cnt_T_str)         Use_Send_UzeRegPtr_Cnt_T_str           Use_Send(UzeRegPtr_Cnt_T_str)         Use_Send_UzeRegPtr_Cnt_T_str           Use_Send(UzeRegPtr_Cnt_T_str)         Use_Send_UzeRegPtr_Cnt_T_str           Use_Send(UzeRegPtr_Cnt_T_str)         Use_Send_UzeRegPtr_Cnt_T_str           Use_Send(UzeRegPtr_Cnt_T_str)         Use_Low_UzeRegPtr_Cnt_T_str           Use_Send(UzeRegPtr_Cnt_T_str)         Use_Low_UzeRegPtr_Cnt_T_str           Use_Send(UzeRegPtr_Cnt_T_str)         Use_Low_UzeRegPtr_Cnt_T_str           Use_Send(UzeRegPtr_Cnt_T_str)         Use_Low_UzeRegPtr_Cnt_T_str           Use_Send(UzeRegPtr_Cnt_T_str)         Use_Low_UzeRegPtr_Cnt_T_str           Use_Send(UzeRegPtr_Cnt_T_str)		
DigCoPIsht_PrevReqDataType_CnLM_u0s         1           DigCoPIsht_Sensihitalized_Cnt_M_lgc         1           12c_GetStatus()         554           12c_GetStatus()         554           12c_GetStatus()2RegPtr_Cnt_T_str)         tgt_12c_GetStatus()2RegPtr_Cnt_T_str           12c_Send()2RegPtr_Cnt_T_str)         tgt_12c_Send()2RegPtr_Cnt_T_str           12c_SetUpMasterReceive()2RegPtr_Cnt_T_str)         tgt_12c_SetUpMasterReceive()2RegPtr_Cnt_T_str           12c_SetUpMasterReceive()2RegPtr_Cnt_T_str)         tgt_12c_SetUpMasterReceive()2RegPtr_Cnt_T_str           12c_SetUpMasterTransmit()2RegPtr_Cnt_T_str         tgt_12c_SetUpMasterTransmit()2RegPtr_Cnt_T_str           12c_SetEGT_Lemp_DXR		INIT COMPLETE
DigCoIPsint_SkintPkintsed_Cnt_M.lgc         1           DigCoIPsint_SkintPkeipsiterVinte_Cnt_M.lgc         1           12c_GeIStatus(12cRegPtr_Cnt_T_str)         554           12c_GeIStatus(12cRegPtr_Cnt_T_str)         tgt_12c_GeIStatus_12cRegPtr_Cnt_T_str           12c_Sent(12cRegPtr_Cnt_T_str)         tgt_12c_Sent_Excep_12cRegPtr_Cnt_T_str           12c_SetLev(12cRegPtr_Cnt_T_str)         tgt_12c_SetLev(12cRegPtr_Cnt_T_str           12c_SetLev(12cRegPtr_Cnt_T_str)         tgt_1		
DigColPsint_SkipRegisterWrite_Cnt_M_lgc         1           12c_GelStatus()         554           12c_GelStatus()         554           12c_GelStatus(2cRegPtr_Cnt_T_str)         tgt_12c_Send_12cRegPtr_Cnt_T str           12c_Send(12cRegPtr_Cnt_T_str)         tgt_12c_Send_12cRegPtr_Cnt_T str           12c_SetUpMasterReceive(12cRegPtr_Cnt_T_str)         tgt_12c_SetUpMasterPransmit_12cRegPtr_Cnt_T str           12c_SetUpMasterReceive(12cRegPtr_Cnt_T_str)         tgt_12c_SetUpMasterPransmit_12cRegPtr_Cnt_T str           12c_SetUpMasterTransmit_(12cRegPtr_Cnt_T_str)         tgt_12c_SetUpMasterPransmit_12cRegPtr_Cnt_T_str           12c_SetUpMasterTransmit_(12cRegPtr_Cnt_T_str)         tgt_12c_SetUpMasterPransmit_12cRegPtr_Cnt_T_str           12c_SetUpMasterTransmit_(12cRegPtr_Cnt_T_str)         tgt_12c_SetUpMasterPransmit_12cRegPtr_Cnt_T_str           12c_SetUpMasterTransmit_12cRegPtr_Cnt_T_str         tgt_12c_SetUpMasterPransmit_12cRegPtr_Cnt_T_str           12c_SetUpMasterTransmit_12cRegPtr_Cnt_T_str         tgt_12c_SetUpMasterTransmit_12cRegPtr_Cnt_T_str           12c_SetUpMasterTransmit_12cRegPtr_Cnt_T_str         tgt_12c_SetUpMasterTransmit_12cRegPtr_Cnt_T_str           12c_SetUpMasterTransmit_12cRegPtr_Cnt_T_str         tgt_12c_SetUpMasterTransmit_12cRegPtr_Cnt_T_str           12c_SetUpMasterTransmit_12cRegPtr_Cnt_T_str         tgt_12c_SetUpMasterTransmit_12cRegPtr_Cnt_T_str           12c_SetUpMasterTransmit_12cRegPtr_Cnt_T_str         tgt_12c_SetUpMasterTransmit_1	DigColPsInt SensInitialized Cnt M Igc	1
2c_GetStatus ZcRegPtr_Cnt_T_str)		1
12c_Send(12cRegPtr_Cnt_T_str)         tgt_12c_Send_12cRegPtr_Cnt_T_str           12c_SetRew(12cRegPtr_Cnt_T_str)         tgt_12c_SetRew(12cRegPtr_Cnt_T_str           12c_SetUpMasterReceive(12cRegPtr_Cnt_T_str)         tgt_12c_SetupMasterTransmit(12cRegPtr_Cnt_T_str           12c_SetupMasterTransmit(12cRegPtr_Cnt_T_str)         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str           12c_SetupMasterTransmit(12cRegPtr_Cnt_T_str)         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str           12c_SetupMasterTransmit(12cRegPtr_Cnt_T_str)         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str           12c_SetupMasterTransmit(12cRegPtr_Cnt_T_str)         tgt_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str           12c_SetupMasterTransmit(12cRegPtr_Cnt_T_str)         tgt_12c_Set_1emp           12c_Set_1_temp         tgt_12c_Set_1emp           12c_Set_1_temp         44           12c_Set_1_temp_DAR         44           12c_Set_1_temp_DAR         6           12c_Set_1_temp_DAR         44           12c_Set_1_temp_DAR         44           12c_Set_1_temp_DAR         55           12c_Set_1_temp_DAR         44           12c_Set_1_temp_DAR         44           12c_Set_1_temp_DAR         44           12c_Set_1_temp_DAR         44           12c_Set_1_temp_DAR         44           12c_Set_1_temp_DAR         44	I2c_GetStatus()	554
12c_SetRecv(!2cRegPtr_Cnt_Tstr)         tgt_!2c_SetRecv_!2cRegPtr_Cnt_Tstr           12c_SetupMasterReceive(!2cRegPtr_Cnt_Tstr)         tgt_!2c_SetupMasterReceive(!2cRegPtr_Cnt_Tstr)           12c_SetupMasterTransmit(!2cRegPtr_Cnt_Tstr)         tgt_!2c_SetupMasterTransmit(!2cRegPtr_Cnt_Tstr           Type_Cnt_T_u08         5           12cREG1_temp         target_!2cREG1_temp           k_ColSensorl/2cAddress_Cnt_u08         20           target_!2cREG1_temp_IMR         44           target_!2cREG1_temp_STR         4444           target_!2cREG1_temp_CLKL         566           target_!2cREG1_temp_CLKH         4466           target_!2cREG1_temp_DRR         6           target_!2cREG1_temp_DRR         44           target_!2cREG1_temp_DRR         44           target_!2cREG1_temp_DRR         6           target_!2cREG1_temp_DRR         44           target_!2cREG1_temp_DRDR         44           target_	I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
12c_SetupMasterReceive(12cRegPtr_Cnt_T_str)         tgl_2c_SetupMasterReceive[12cRegPtr_Cnt_T_str]           12c_SetupMasterTransmit(12cRegPtr_Cnt_T_str)         tgl_12c_SetupMasterTransmit[12cRegPtr_Cnt_T_str]           Type_Cnt_T_u08         5           12c_SetupMasterTransmit[12cRegPtr_Cnt_T_str]         5           12c_REG1_temp         4           12c_SetSe1_temp_OAR         567           12c_SetSe1_temp_LNR         444           12c_SetSe1_temp_CLKL         566           12c_SetSe1_temp_CLKH         4466           12c_SetSe1_temp_DLR         6           12c_SetSe1_temp_DRR         6           12c_SetSe1_temp_DRR         44           12c_SetSe1_temp_DXR         44           12c_SetSe1_temp_PRC         44           12c_SetSe1_temp_PRC         44           12c_SetSe1_temp_PRC         44           12c_SetSe1_temp_DID12         44           12c_SetSe1_temp_DID12         44           12c_SetSe1_temp_DINA         1<	I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_l2c_Send_l2cRegPtr_Cnt_T_str
i2c_SetupMasterTransmit(i2cRegPtr_Cnt_T_str)         tgt_i2c_SetupMasterTransmit_i2cRegPtr_Cnt_T_str           Type_Cnt_T_u08         5           i2cREG1_temp         target_i2cREG1_temp           k_ColSensori2cAddress_Cnt_u08         20           target_i2cREG1_temp_DAR         44           target_i2cREG1_temp_BIMR         444           target_i2cREG1_temp_CTLKI         566           target_i2cREG1_temp_CLKH         4466           target_i2cREG1_temp_DRR         6           target_i2cREG1_temp_DRR         6           target_i2cREG1_temp_DXR         44           target_i2cREG1_temp_DXR         44           target_i2cREG1_temp_DXR         567           target_i2cREG1_temp_DXR         44           target_i2cREG1_temp_DXR         44           target_i2cREG1_temp_DXR         566           target_i2cREG1_temp_PXR         566           target_i2cREG1_temp_DXR         44           target_i2cREG1_temp_PXR         564           target_i2cREG1_temp_PXR         44           target_i2cREG1_temp_PXC         44           target_i2cREG1_temp_PXD         446           target_i2cREG1_temp_DINAC         1           target_i2cREG1_temp_DMAC         1           target_i2cREG1_temp_DIN	I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08         5           i2cREG1_temp         target_i2cREG1_temp           k_Colsensorl2CAddress_Cnt_u08         20           target_i2cREG1_temp_OAR         567           target_i2cREG1_temp_IMR         44           target_i2cREG1_temp_CIK         566           target_i2cREG1_temp_CLK         466           target_i2cREG1_temp_CLKH         446           target_i2cREG1_temp_DCR         129           target_i2cREG1_temp_DRR         6           target_i2cREG1_temp_DAR         44           target_i2cREG1_temp_DAR         44           target_i2cREG1_temp_DAR         44           target_i2cREG1_temp_DAR         566           target_i2cREG1_temp_DAR         44           target_i2cREG1_temp_DAR         44           target_i2cREG1_temp_PDR         44           target_i2cREG1_	I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
i2cREG1_temp         target_i2cREG1_temp           k_ColSensorl2CAddress_Cnt_u08         20           target_i2cREG1_temp_OAR         567           target_i2cREG1_temp_IMR         44           target_i2cREG1_temp_STR         44444           target_i2cREG1_temp_CLKL         566           target_i2cREG1_temp_CLKH         4466           target_i2cREG1_temp_DRR         6           target_i2cREG1_temp_DRR         6           target_i2cREG1_temp_DAR         44           target_i2cREG1_temp_DAR         44           target_i2cREG1_temp_MDR         566           target_i2cREG1_temp_MDR         566           target_i2cREG1_temp_MDR         44           target_i2cREG1_temp_EMDR         1           target_i2cREG1_temp_EMDR         44           target_i2cREG1_temp_PDC         44           target_i2cREG1_temp_PDMC         4466           target_i2cREG1_temp_PDMAC         44           target_i2cREG1_temp_PDMAC         1           target_i2cREG1_temp_FUN         1           target_i2cREG1_temp_FUN         2           target_i2cREG1_temp_DIR         2           target_i2cREG1_temp_DIN         0           target_i2cREG1_temp_DOUT         1	I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
k_ColSensorl2CAddress_Cnt_u08         20           target_i2cREG1_temp.OAR         567           target_i2cREG1_temp.IMR         44           target_i2cREG1_temp.STR         4444           target_i2cREG1_temp.CLKL         566           target_i2cREG1_temp.CLKH         4466           target_i2cREG1_temp.DRT         6           target_i2cREG1_temp.DRR         6           target_i2cREG1_temp.DXR         44           target_i2cREG1_temp.DXR         44           target_i2cREG1_temp.MDR         566           target_i2cREG1_temp.MDR         566           target_i2cREG1_temp.MDR         44           target_i2cREG1_temp.BMDR         1           target_i2cREG1_temp.PBDR         44           target_i2cREG1_temp.PBD11         4466           target_i2cREG1_temp.PID12         44           target_i2cREG1_temp.PID102         44           target_i2cREG1_temp.DMAC         1           target_i2cREG1_temp.FUN         1           target_i2cREG1_temp.FUN         2           target_i2cREG1_temp.DIN         0           target_i2cREG1_temp.DIN         0	Type_Cnt_T_u08	5
target_izcREG1_temp.OAR         567           target_izcREG1_temp.IMR         44           target_izcREG1_temp.CTR         4444           target_izcREG1_temp.CLKL         566           target_izcREG1_temp.CLKH         4466           target_izcREG1_temp.CNT         129           target_izcREG1_temp.DRR         6           target_izcREG1_temp.DXR         44           target_izcREG1_temp.DXR         44           target_izcREG1_temp.DNR         566           target_izcREG1_temp.NVR         554           target_izcREG1_temp.EMDR         1           target_izcREG1_temp.PSC         44           target_izcREG1_temp.PID11         4466           target_izcREG1_temp.PID12         44           target_izcREG1_temp.PID12         44           target_izcREG1_temp.DINAC         1           target_izcREG1_temp.FUN         1           target_izcREG1_temp.FUN         1           target_izcREG1_temp.FUN         2           target_izcREG1_temp.DIR         2           target_izcREG1_temp.DIR         0           target_izcREG1_temp.DOUT         1	i2cREG1_temp	target_i2cREG1_temp
target_i2cREG1_temp.IMR         44           target_i2cREG1_temp.STR         4444           target_i2cREG1_temp.CLKL         566           target_i2cREG1_temp.CLKH         4466           target_i2cREG1_temp.CNT         129           target_i2cREG1_temp.DRR         6           target_i2cREG1_temp.DRR         44           target_i2cREG1_temp.DXR         44           target_i2cREG1_temp.MDR         566           target_i2cREG1_temp.IVR         554           target_i2cREG1_temp.EMDR         1           target_i2cREG1_temp.PDSC         44           target_i2cREG1_temp.PID11         4466           target_i2cREG1_temp.PID12         44           target_i2cREG1_temp.DIMAC         1           target_i2cREG1_temp.DMAC         1           target_i2cREG1_temp.FUN         1           target_i2cREG1_temp.FUN         2           target_i2cREG1_temp.DIR         2           target_i2cREG1_temp.DIN         0           target_i2cREG1_temp.DOUT         1	k_ColSensorl2CAddress_Cnt_u08	20
target_i2cREG1_temp.STR         4444           target_i2cREG1_temp.CLKL         566           target_i2cREG1_temp.CLKH         4466           target_i2cREG1_temp.DNT         129           target_i2cREG1_temp.DRR         6           target_i2cREG1_temp.DXR         44           target_i2cREG1_temp.DXR         44           target_i2cREG1_temp.MDR         566           target_i2cREG1_temp.EMDR         1           target_i2cREG1_temp.EMDR         4           target_i2cREG1_temp.PSC         44           target_i2cREG1_temp.PID11         4466           target_i2cREG1_temp.PID12         44           target_i2cREG1_temp.DMAC         1           target_i2cREG1_temp.FUN         1           target_i2cREG1_temp.FUN         1           target_i2cREG1_temp.DIR         2           target_i2cREG1_temp.DIN         0           target_i2cREG1_temp.DIN         0           target_i2cREG1_temp.DOUT         1	target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.CLKL         566           target_i2cREG1_temp.CLKH         4466           target_i2cREG1_temp.CNT         129           target_i2cREG1_temp.DRR         6           target_i2cREG1_temp.SAR         567           target_i2cREG1_temp.DXR         44           target_i2cREG1_temp.MDR         566           target_i2cREG1_temp.EMDR         1           target_i2cREG1_temp.PSC         44           target_i2cREG1_temp.PSC         44           target_i2cREG1_temp.PID11         4466           target_i2cREG1_temp.DMAC         1           target_i2cREG1_temp.DMAC         1           target_i2cREG1_temp.DIN         1           target_i2cREG1_temp.DIN         0           target_i2cREG1_temp.DIN         0           target_i2cREG1_temp.DOUT         1	target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.CLKH         4466           target_i2cREG1_temp.DRR         6           target_i2cREG1_temp.DRR         567           target_i2cREG1_temp.DXR         44           target_i2cREG1_temp.MDR         566           target_i2cREG1_temp.IVR         554           target_i2cREG1_temp.EMDR         1           target_i2cREG1_temp.PSC         44           target_i2cREG1_temp.PID11         4466           target_i2cREG1_temp.DMAC         4           target_i2cREG1_temp.DMAC         1           target_i2cREG1_temp.FUN         1           target_i2cREG1_temp.DIR         2           target_i2cREG1_temp.DIR         2           target_i2cREG1_temp.DIN         0           target_i2cREG1_temp.DOUT         1	target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CNT         129           target_i2cREG1_temp.DRR         6           target_i2cREG1_temp.SAR         567           target_i2cREG1_temp.DXR         44           target_i2cREG1_temp.MDR         566           target_i2cREG1_temp.IVR         554           target_i2cREG1_temp.EMDR         1           target_i2cREG1_temp.PSC         44           target_i2cREG1_temp.PID11         4466           target_i2cREG1_temp.DMAC         1           target_i2cREG1_temp.FUN         1           target_i2cREG1_temp.FUN         1           target_i2cREG1_temp.DIR         2           target_i2cREG1_temp.DIR         2           target_i2cREG1_temp.DIN         0           target_i2cREG1_temp.DOUT         1	target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.DRR         6           target_i2cREG1_temp.SAR         567           target_i2cREG1_temp.DXR         44           target_i2cREG1_temp.MDR         566           target_i2cREG1_temp.IVR         554           target_i2cREG1_temp.EMDR         1           target_i2cREG1_temp.PSC         44           target_i2cREG1_temp.PID11         4466           target_i2cREG1_temp.PID12         44           target_i2cREG1_temp.DMAC         1           target_i2cREG1_temp.FUN         1           target_i2cREG1_temp.DIR         2           target_i2cREG1_temp.DIR         2           target_i2cREG1_temp.DIN         0           target_i2cREG1_temp.DOUT         1	target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.SAR       567         target_i2cREG1_temp.DXR       44         target_i2cREG1_temp.MDR       566         target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       44         target_i2cREG1_temp.PID11       4466         target_i2cREG1_temp.PID12       44         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1         target_i2cREG1_temp.DIR       2         target_i2cREG1_temp.DIR       2         target_i2cREG1_temp.DIN       0         target_i2cREG1_temp.DOUT       1	target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DXR       44         target_i2cREG1_temp.MDR       566         target_i2cREG1_temp.IVR       554         target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       44         target_i2cREG1_temp.PID11       4466         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1         target_i2cREG1_temp.DIR       2         target_i2cREG1_temp.DIR       0         target_i2cREG1_temp.DOUT       1	target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.MDR       566         target_i2cREG1_temp.IVR       554         target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       44         target_i2cREG1_temp.PID11       4466         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1         target_i2cREG1_temp.DIR       2         target_i2cREG1_temp.DIR       0         target_i2cREG1_temp.DOUT       1	target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.IVR       554         target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       44         target_i2cREG1_temp.PID11       4466         target_i2cREG1_temp.PID12       44         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1         target_i2cREG1_temp.DIR       2         target_i2cREG1_temp.DIN       0         target_i2cREG1_temp.DOUT       1	target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       44         target_i2cREG1_temp.PID11       4466         target_i2cREG1_temp.PID12       44         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1         target_i2cREG1_temp.DIR       2         target_i2cREG1_temp.DIN       0         target_i2cREG1_temp.DOUT       1	target_i2cREG1_temp.MDR	566
target_i2cREG1_temp.PSC       44         target_i2cREG1_temp.PID11       4466         target_i2cREG1_temp.PID12       44         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1         target_i2cREG1_temp.DIR       2         target_i2cREG1_temp.DIN       0         target_i2cREG1_temp.DOUT       1	target_i2cREG1_temp.IVR	554
target_i2cREG1_temp.PID11       4466         target_i2cREG1_temp.PID12       44         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1         target_i2cREG1_temp.DIR       2         target_i2cREG1_temp.DIN       0         target_i2cREG1_temp.DOUT       1	target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PID12       44         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1         target_i2cREG1_temp.DIR       2         target_i2cREG1_temp.DIN       0         target_i2cREG1_temp.DOUT       1	target_i2cREG1_temp.PSC	44
target_i2cREG1_temp.DMAC         1           target_i2cREG1_temp.FUN         1           target_i2cREG1_temp.DIR         2           target_i2cREG1_temp.DIN         0           target_i2cREG1_temp.DOUT         1	target_i2cREG1_temp.PID11	4466
target_i2cREG1_temp.FUN 1 target_i2cREG1_temp.DIR 2 target_i2cREG1_temp.DIN 0 target_i2cREG1_temp.DOUT 1	target_i2cREG1_temp.PID12	44
target_i2cREG1_temp.DIR 2 target_i2cREG1_temp.DIN 0 target_i2cREG1_temp.DOUT 1	target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.DIN 0 target_i2cREG1_temp.DOUT 1	target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DOUT 1	target_i2cREG1_temp.DIR	2
0.2 · · · 2 p · · ·	target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.SET 1	target_i2cREG1_temp.DOUT	
	target_i2cREG1_temp.SET	1

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Name	Input Value	
target_i2cREG1_temp.CLR	2	
target i2cREG1 temp.ODR	0	
target_i2cREG1_temp.PD	3	
target_i2cREG1_temp.PSL	3	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR	567	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	44	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	4444	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	566	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT	129	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	6	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	567	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	44	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	566	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	554	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	44	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	4466	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	44	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	
	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	2	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	1	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR	2	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR	0	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	4444	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	
	4466	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	129	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT		
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	6	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	
gt I2c Send I2cRegPtr Cnt T str.PID12	44	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	
	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN		
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	2	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	0	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	3	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	567	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	44	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	129	
	6	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR		
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	566	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	554	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	1	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	
	1	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN		
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	2	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	

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Name	Input Value		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	1		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	1		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0		
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3		
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	3 567		
tgt_l2c_SetupMasterReceive_l2cRegPtt_Cnt_T_str.lMR	44		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	566		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	567		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	44 566		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.lVR	554		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	4466		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	1		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	2		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	1		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.SET	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	567		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	4444 566		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	4466		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	44		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	44		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	34	34	•
DigColPsInt_Buffer_Cnt_M_u08[1]	50	50	•
DigColPsInt_Buffer_Cnt_M_u08[2]	60	60	•
DigColPsInt_CurrentSlave_Cnt_M_u08	20	20	•
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG	READ_SENSOR1_SETREG	•
DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	5 0	5	
l2c_Send(Length_Cnt_T_u32)	1	1	
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR	44	44	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	4444	4444	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT	129	129	<b> </b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	•

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Name	Actual Value	Expected Value	Result
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SAR	567	567	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR	44	44	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR	1	1	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC	44	44	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	4466	4466	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID12	44	44	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DMAC	1	1	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN	0	0	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT	1	1	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.SET	1	1	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR	2	2	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR	0	0	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	3	3	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	567	567	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	129	129	•
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	6	6	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	2	2	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	1	1	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	1	1	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	2	2	
	0	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	3	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	3	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	567	567	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR			
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	44	44	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	4444	4444	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	566	566	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	129	129	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	6	6	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	567	567	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	44	44	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	566	566	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	554	554	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	1	1	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	1	1	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	1	1	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	2	2	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	0	0	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	1	1	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	1	1	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	2	2	•
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	3	3	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	44	44	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	
	566	566	
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL			

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Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	Result
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	_
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.SAR	567	567	<b>✓</b>
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.DXR	44	44	•
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	<b>✓</b>
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.IVR	554	554	_
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.EMDR	1	1	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	44	44	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	4466	4466	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	44	44	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	1	1	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	0	0	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>

Τ			V	
Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	~
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	~

Test Step 3.3 (Repeat Count = 1)		<b>✓</b>
Name	Input Value	
DigColPsInt_Buffer_Cnt_M_u08[0]	3	
DigColPsInt_Buffer_Cnt_M_u08[1]	6	
DigColPsInt_Buffer_Cnt_M_u08[2]	9	
DigColPsInt_CurrentSlave_Cnt_M_u08	77	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE	
DigColPsInt_PrevReqDataType_Cnt_M_u08	1	
DigColPsInt_SensInitialized_Cnt_M_lgc	1	
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1	
I2c_GetStatus()	0	
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str	
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str	
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str	
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str	
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str	
Type_Cnt_T_u08	1	

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DigColPsInt_StartRequest		TAZCICAG
Name	Input Value	
i2cREG1_temp	target_i2cREG1_temp	
k_ColSensorl2CAddress_Cnt_u08	69	
arget_i2cREG1_temp.OAR	54	
arget_i2cREG1_temp.IMR	66	
arget_i2cREG1_temp.STR	8	
arget_i2cREG1_temp.CLKL	554	
arget_i2cREG1_temp.CLKH	344	
arget_i2cREG1_temp.CNT	123	
arget_i2cREG1_temp.DRR	45	
arget_i2cREG1_temp.SAR	54	
arget_i2cREG1_temp.DXR	66	
arget_i2cREG1_temp.MDR	554	
arget_i2cREG1_temp.IVR	788 3	
arget_i2cREG1_temp.EMDR arget_i2cREG1_temp.PSC	66	
arget_i2cREG1_temp.PID11	344	
arget_i2cREG1_temp.PID12	66	
arget_i2cREG1_temp.DMAC	3	
arget_i2cREG1_temp.FUN	1	
arget i2cREG1 temp.DIR	3	
arget_i2cREG1_temp.DIN	2	
arget_i2cREG1_temp.DOUT	3	
arget_i2cREG1_temp.SET	3	
arget_i2cREG1_temp.CLR	3	
arget_i2cREG1_temp.ODR	2	
arget_i2cREG1_temp.PD	1	
arget_i2cREG1_temp.PSL	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	54	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	66	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	8	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	554	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH	344	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT	123	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR	45	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	54	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	66	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	554	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	788	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR	3	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSC	66	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	344	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	66	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	3	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	2	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3	
gt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	3 2	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PD	1	
gt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	2	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	66	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	3	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	2	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	
gt_ize_ochd_izertegr ti_ont_1_str.boo1	0	

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<u> </u>	
Name	Input Value
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
tgt I2c Send I2cRegPtr Cnt T str.ODR	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
tgt I2c Send I2cRegPtr Cnt T str.PSL	2
tgt I2c SetRecv I2cRegPtr Cnt T str.OAR	54
tgt I2c SetRecv I2cRegPtr Cnt T str.IMR	66
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	8
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	344
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	45
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	54
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	3
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	3
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	2
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	1
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	2
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	54
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	3
	3 66
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	66
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	66 344 66
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	66 344 66 3
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	66 344 66 3 1
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	66 344 66 3

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Name	Input Value		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	2		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	2		
Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	3	3	ixesuit
DigColPsInt_Buffer_Cnt_M_u08[1]	6	6	~
DigColPsInt_Buffer_Cnt_M_u08[2]	9	9	~
DigColPsInt_CurrentSlave_Cnt_M_u08	69	69	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_GETDATA	READ_SENSOR1_GETDATA	~
DigColPsInt_PrevReqDataType_Cnt_M_u08	1	1	~
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1	1	~
I2c_SetRecv(Length_Cnt_T_u32)	2 2	2	<b>V</b>
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)  tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	54	54	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	_
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	8	8	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	554	554	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	344	344	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	123	123	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	45	45	<b>V</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	54	54 66	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR	554	554	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	788	788	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	344	344	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIR	3	3 2	<b>*</b>
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DIN tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT	3	3	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PD	1	1	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	54	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	· ·
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	554	554	<b>*</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	344	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	123	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	45	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	54	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	554	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	788	<b>*</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	3	3	<b>V</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	66 344	66 344	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	-
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	3	3	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>*</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	1	1	<b>*</b>
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54	54	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8	8	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554	554	<b>V</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344	344	<b>V</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123 45	123 45	V
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR		10	

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Name	Actual Value	Expected Value	Result
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54	54	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>v</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	554	554	<b>~</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788	788	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	3	3	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	66	66	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344 66	344 66	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	3	3	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	1	1	_
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	·
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	3	3	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	<b>~</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	_
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>~</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54	54	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	8	8	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	554	554	<b>→</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	344	344	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	123	123	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45	45	~
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.SAR	54	54	<b>✓</b>
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.DXR	66	66	~
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.MDR	554	554	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788	788	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344	344	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✓
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✓
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	✓
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54	54	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8	8	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554	554	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344	344	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123	123	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45	45	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54	54	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554	554	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788	788	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344	344	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✓
$tgt\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DOUT$	3	3	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>✓</b>





T			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	~
SetupRead	1	SetupRead	1	<b>✓</b>
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	•
I2c SetRecv	1	I2c SetRecv	1	<b>✓</b>

Test Step 3.4 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	11
DigColPsInt_Buffer_Cnt_M_u08[1]	22
DigColPsInt_Buffer_Cnt_M_u08[2]	33
DigColPsInt_CurrentSlave_Cnt_M_u08	65
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
I2c_GetStatus()	65535
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	2
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	33
target_i2cREG1_temp.OAR	3
target_i2cREG1_temp.IMR	100
target_i2cREG1_temp.STR	7788
target_i2cREG1_temp.CLKL	2767
target_i2cREG1_temp.CLKH	556
target_i2cREG1_temp.CNT	564
target_i2cREG1_temp.DRR	88
target_i2cREG1_temp.SAR	3
target_i2cREG1_temp.DXR	100
target_i2cREG1_temp.MDR	2767
target_i2cREG1_temp.IVR	9
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	100
target_i2cREG1_temp.PID11	556
target_i2cREG1_temp.PID12	100
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	3
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	3
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	100
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	7788
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	556
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	564
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	88
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	100
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	2767
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	9
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	100
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	556
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	100
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	3

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DigColFSint_StartRequest		71000
Name	Input Value	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DOUT	2	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLR	1	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.ODR	3	
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PD	0	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	100	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	7788	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	2767	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	556	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	564	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	88	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	100	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	2767	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	9	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	
	556	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	100	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	2	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC		
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	2	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	1	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	3	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	2767	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	9	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	2	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	
	1	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	
	2	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET		
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	100	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	7788	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	3	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556	
tat I2c SetupMasterReceive I2cReaPtr Cnt T str PID12	100	
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12 tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	

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Name	Input Value		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	2		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	0		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	3		
tgt I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	0		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	556 564		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	88		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	100		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556 100		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	2		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	0 3		
tgt_izc_setupiwasterriansmit_izckegrti_cnt_i_str.rsc			
Namo	Actual Value	Evpected Value	Pocult
Name DiaColPsInt Buffer Cnt M u08[0]	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	Actual Value 11 22	Expected Value  11 22	
	11	11	-
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	11 22	11 22	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum	11 22 33 65 INIT_COMPLETE	11 22 33 65 INIT_COMPLETE	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08	11 22 33 65 INIT_COMPLETE 2	11 22 33 65 INIT_COMPLETE 2	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	11 22 33 65 INIT_COMPLETE 2 0	11 22 33 65 INIT_COMPLETE 2	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_CurrentStepCol_M_u08 DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR	11 22 33 65 INIT_COMPLETE 2 0 3	11 22 33 65 INIT_COMPLETE 2 0 3	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_CurrentStepNo_Cnt_M_u08 DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR	11 22 33 65 INIT_COMPLETE 2 0 3 100	11 22 33 65 INIT_COMPLETE 2 0 3	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_CurrentStepNo_Cnt_M_u08 DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.JMR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	11 22 33 65 INIT_COMPLETE 2 0 3 100	11 22 33 65 INIT_COMPLETE 2 0 3	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788 2767	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788 2767	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.JMR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788 2767 556	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788 2767 556	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788 2767 556 564	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788 2767 556 564	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788 2767 556 564 88 3 100	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788 2767 556 564 88 3 100	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.JMR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DDR	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788 2767 556 564 88 3 100 2767	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788 2767 556 564 88 3 100 2767	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DNR	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788 2767 556 564 88 3 100 2767 9	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788 2767 556 564 88 3 100 2767 9	
DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_SkipRegisterWrite_Cnt_M_u08  DigColPsInt_SkipRegisterWrite_Cnt_M_lgc  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.OAR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKL  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CLKH  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.CNT  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DRR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.DXR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.MDR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR  tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788 2767 556 564 88 3 100 2767 9 0	11 22 33 65 INIT_COMPLETE 2 0 3 100 7788 2767 556 564 88 3 100 2767 9	
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Name	Actual Value	Expected Value	Resul
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	3	•
gt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	100	•
gt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	2767	•
gt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	9	•
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	100	
igt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556 100	556 100	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	2	2	
gt_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC gt_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0	0	
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	1	1	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	
gt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	3	3	•
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	100	100	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	2767	2767	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	556	556	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564	564	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88	88	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3	3	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100	100	•
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	2767	2767	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9	9	•
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	0	0	•
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	100	100	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556	556	•
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100	100	
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	
igt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0	0	
gt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	
gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR gt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	3	3	
gt I2c SetRecv I2cRegPtr Cnt T str.PD	0	0	
gt_l2c_SetRecv_l2cRegPtr_Ont_1_str.PSL	3	3	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	3	3	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100	100	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	7788	7788	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	556	556	
gt I2c SetupMasterReceive I2cRegPtr Cnt T str.CNT	564	564	
gt I2c SetupMasterReceive I2cRegPtr Cnt T str.DRR	88	88	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3	3	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	100	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	2767	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	9	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	100	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556	556	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	100	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	0	0	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	1	1	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	•
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	•
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	•
gt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	
gt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	3	3	
gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	3	3	•
gt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	100	100	•
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
gt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	556	

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Name	Actual Value	Expected Value	Result
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	564	564	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	88	88	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100	100	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	2767	2767	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	100	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556	556	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	100	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	•
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	2	2	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	3	3	•
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c GetStatus	1	I2c GetStatus	1	<b>✓</b>

Test Step 3.5 (Repeat Count = 1)	🗸
Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	44
DigColPsInt_Buffer_Cnt_M_u08[1]	55
DigColPsInt_Buffer_Cnt_M_u08[2]	66
DigColPsInt_CurrentSlave_Cnt_M_u08	55
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_READ
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1.
I2c_GetStatus()	655
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	3
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	55
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	55

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Name	Input Value
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	66
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.STR	556
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
tgt I2c GetStatus I2cRegPtr Cnt T str.CLKH	1204
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	87
	67
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	55
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IVR	5
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	66
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PID11	1204
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	2
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PD	3
	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	66
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	556
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	2309
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	1204
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	87
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	2309
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	5
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	1204
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
	3
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	1
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	2
	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3

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DigColPsInt\_StartRequest

		• "	
Name	Input Value		_
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	55		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	66		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	2309		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	5		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	3		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	66		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	1204		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	66		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	3		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	1		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	3		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	2		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3		
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	556		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	1204		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	1		
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN			
tgt I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	2 3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	3		
	1		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3		
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3		
		Expected Value	Descri
Name	Actual Value	Expected Value	Resul
DigColPsInt_Buffer_Cnt_M_u08[0]	44	44	,
DigColPoint_Buffer_Cnt_M_u08[1]	55	55	
DigColPoint_Buffer_Cnt_M_u08[2]	66	66	
DigColPoint_CurrentSlave_Cnt_M_u08	INIT SENSORS CHECKSTAT DE	55	
DigColPoint_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_RE		
DigColPsInt_PrevReqDataType_Cnt_M_u08	0	0	
DigColPsInt_SkipRegisterWrite_Cnt_M_Igc		1	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	•
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.IMR	66	66	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	1
tot 12c GetStatus 12cRecPtr Cnt T etr SAR	55	55	

55

66

5

3

66

1204

2309

55

66

5

3

66

1204

2309

tgt\_I2c\_GetStatus\_I2cRegPtr\_Cnt\_T\_str.SAR

tgt\_I2c\_GetStatus\_I2cRegPtr\_Cnt\_T\_str.DXR

tgt\_I2c\_GetStatus\_I2cRegPtr\_Cnt\_T\_str.MDR

tgt\_I2c\_GetStatus\_I2cRegPtr\_Cnt\_T\_str.IVR

tgt\_I2c\_GetStatus\_I2cRegPtr\_Cnt\_T\_str.EMDR

tgt\_I2c\_GetStatus\_I2cRegPtr\_Cnt\_T\_str.PSC

 $tgt\_l2c\_GetStatus\_l2cRegPtr\_Cnt\_T\_str.PID11$ 

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Name	Actual Value	Expected Value	Result
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>V</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3 1	<b>*</b>
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	
tgt 12c GetStatus 12cRegPtr Cnt T str.DIN	2	2	~
tgt I2c GetStatus I2cRegPtr Cnt T str.DOUT		3	,
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	•
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	~
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PD	3	3	~
tgt_l2c_GetStatus_l2cRegPtr_Cnt_T_str.PSL	3	3	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.STR	556	556	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>V</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	87	87 67	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	67 55	55	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	
tgt I2c Send I2cRegPtr Cnt T str.MDR	2309	2309	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	66	66	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>~</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	66	66	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DIN		2	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	3	3	<b>V</b>
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.SET	1	3	· ·
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	1 2	~
tgt_l2c_Send_l2cRegPtr_Cnt_T_str.PD	3	3	~
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>✓</b>
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	556	556	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	66	66	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR		3	
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	66	66	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	-
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	1	1	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	1	1	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	2	2	~
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	3	3	<b>*</b>
tgt_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	55		
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	66	55 66	- J
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.NTR	556	556	_
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>V</b>
	1204	1204	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH			~
	87	87	_
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH		87 67	-
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	87		~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	87 67	67	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	87 67 55 66 2309	67 55 66 2309	· · · · · · · · · · · · · · · · · · ·
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	87 67 55 66	67 55 66	~

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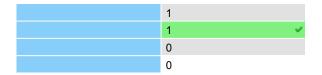
Name	Actual Value	Expected Value	Result
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	66	66	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1	1	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	3	3	~
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
tgt_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	2	2	✓
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✓
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✓
tgt_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	3	3	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	•



DigColPsInt
DigColPsInt
DigColPsInt\_GetCustData

100 % 100 %



D:\Synergy_Work_Area\C1xx_DigColPs
D:\Synergy_Work_Area\C1xx_DigColPs\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
TI TMS 570 PLS UDE (Default)
Unit Test
\$(PROJECTROOT)\DigColPs\src\Sa_DigColPsInt.c
-D_DATA_ACCESS= -Dconst= -DSTATIC= -Dinline= -I\$(PROJECTROOT)\DigColPs\utp\contract -I\$(PROJECTROOT)\DigColPs\utp\contract -I\$(PROJECTROOT)\DigColPs\utp\contract\Sa_DigColPs -I\$(PROJECTROOT)\DigColPs\include -I\$(PROJECTROOT)\StdDef\include -I\$(PROJECTROOT)\StdDef\include -I\$(PROJECTROOT)\StdDef\include\TMS570_HerculesRegs -I\$(Compiler Install Path)\include



```
Name of Tester-Priti Mangalekar
Code File(s) Under TestSa_DigGoPIshtLc
Code File(s) Version: 7
Module Design Document DigCoPIsht_MDD.docx
Module Design Document DigCoPIsht_MDD.docx
Module Design Document Version:8
Data Dictionary Version:9
Unit Test Plan Version:9
Unit T
```

Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	<pre>\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj</pre>
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	<pre>\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd</pre>
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	\$(Compiler Install Path)\include
Time Unit	Cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy Work Area\Clxx DigColPs\UnitTestEnv\config\UDE TMS570 DEBUG.WSP



#### Test Vector Description:

TS1.1DigColPsInt\_I2CHwCustData\_Uls\_M\_u16=>Min TS1.2DigColPsInt\_I2CHwCustData\_Uls\_M\_u16=>Max TS1.3DigColPsInt\_I2CHwCustData\_Uls\_M\_u16=Pos

			V
DigColPsInt_I2CHwCustData_Uls_M_u16	0		
DigColPsInt_GetCustData()	0	0	~

			<b>✓</b>
DigColPsInt_I2CHwCustData_Uls_M_u16	511		
DigColPsInt_GetCustData()	511	511	~

			<b>✓</b>
DigColPsInt_I2CHwCustData_Uls_M_u16	124		
DigColPsInt_GetCustData()	124	124	✓

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DigColPsInt\_Init

 Project
 DigColPsInt

 Module
 DigColPsInt

 Test Object
 DigColPsInt\_Init

### Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

#### **Statistics**

Total Testcases	1
Successful	1
Failed	0
Not Executed	0

#### **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\C1xx_DigColPs
Configuration File	D:\Synergy_Work_Area\C1xx_DigColPs\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\DigColPs\src\Sa_DigColPsInt.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -DSTATIC= -Dinline= -I\$(PROJECTROOT)\DigColPs\utp\contract -I\$(PROJECTROOT)\DigColPs\utp\contract -I\$(PROJECTROOT)\DigColPs\include -I\$(PROJECTROOT)\StdDef\include

Comments/Description/Spe	ecification
Name	Text



Module 'DigColPsInt' 

Name of Tester:Priti Mangalekar Code File(s) Under Test:Sa\_DigColPsInt.c Code File(s) Version:7

Module Design Document:DigColPsInt\_MDD.docx Module Design Document Version:8

Data Dictionary Version:9 Unit Test Plan Version:2

Ontil Test Fiall Version:2
Optimization Level:Level 2
Compiler (CodeGen) Version:TMS470\_4.9.5
Model Type:Excel Macro
Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.30
Total FLASH Used (Bytes):N/A
Total RAM Used (Bytes):N/A

Total CALS Used (Bytes):N/A Special Test Requirements: Test Date:10/13/2014 Comments:

NOTE 1: In """DigColPsInt\_StartRequest""" function, path """(Type\_Cnt\_T\_u08 > D\_NONE\_CNT\_U08) = TRUE && (Type\_Cnt\_T\_u08 <= D\_STATUSREG\_CNT\_U08) = FALSE""" cannot be covered because range of """Type\_Cnt\_T\_u08""" is '0-5' and value of """D\_STATUSREG\_CNT\_U08""" is '34'.

NOTE2: In function ""DigColPsInt\_GetData"",""DigColPsInt\_StartRequest"" and ""DigColPsInt\_InterruptNotification"" values for """12c\_SetRecv(Length\_Cnt\_T\_u32)""", """12c\_SetStatus(Status\_Cnt\_T\_u16)""", """12c\_SetUpMasterReceive(DataLength\_Cnt\_T\_u16)""" and 12c\_SetupMasterTransmit(DataLength\_Cnt\_T\_u16) are ignored in few vectors as they

are taking garbage value when they are not updated with expected value in particular vector.

NOTE3: The return value of """"DigColPsInt\_GetData""" function is going out of range, anomaly """6156""" is raised for the same.

NOTE4:Range of DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum is considered as 0 to 36, as enum DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum is of type CommStepType which is of 37 elements.

NOTE5:In function ""DigColPsInt\_InterruptNotification"", path ""Case I2C\_RECV\_OVERRUN: True"" cannot be covered because range of ""Flags\_Cnt\_T\_b16"" is 0 to 64 given in MDD.

NOTE6:In function ""DigColPsInt\_InterruptNotification"", output variable ""DigColPsInt\_AttempOccurForCustDatRead\_Cnt\_M\_u08"" is going out

of range.'

Attributes	
Name	Value
Compiler Install Path	<pre>\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5</pre>
Float Precision	9
InitObjDir	<pre>\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj</pre>
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	<pre>\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd</pre>
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	\$(Compiler Install Path)\include
Time Unit	Cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\Clxx_DigColPs\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP



### Test Case 1: Boundary Test

Description

Test Vector Description:

TS1.1GetSystemTime\_mS\_u32=min TS1.2GetSystemTime\_mS\_u32=max TS1.3GetSystemTime\_mS\_u32=mid TS1.4All min TS1.5All max

Test Step 1.1 (Repeat Count = 1)			<b>✓</b>		
Name	Input Value				
GetSystemTime mS u32(CurrentTime)	target GetSystemTime mS u3:	2 CurrentTime			
I2c_Enable(I2cRegPtr_Cnt_T_str)	target_l2c_Enable_l2cRegPtr_0	_			
I2c_EnableNotification(I2cRegPtr_Cnt_T_str)	target I2c EnableNotification I2				
I2c_Init(I2cRegPtr_Cnt_T_str)	target I2c Init I2cRegPtr Cnt	target_I2c_Init_I2cRegPtr_Cnt_T_str			
I2c_SetCount(I2cRegPtr_Cnt_T_str)		target_I2c_SetCount_I2cRegPtr_Cnt_T_str			
i2cREG1_temp		target_i2cREG1_temp			
target_GetSystemTime_mS_u32_CurrentTime	0				
target_i2cREG1_temp.OAR	23				
target_i2cREG1_temp.IMR		10			
target i2cREG1 temp.STR					
target_i2cREG1_temp.CLKL	666	1000			
target_i2cREG1_temp.CLKH	7587				
target_i2cREG1_temp.CNT	356				
·	98				
target_i2cREG1_temp.DRR					
target_i2cREG1_temp.SAR	876				
target_i2cREG1_temp.DXR	98				
target_i2cREG1_temp.MDR	764				
target_i2cREG1_temp.IVR	736				
target_i2cREG1_temp.EMDR	1				
target_i2cREG1_temp.PSC	33				
target_i2cREG1_temp.PID11	7				
target_i2cREG1_temp.PID12	12				
target_i2cREG1_temp.DMAC	1				
target_i2cREG1_temp.FUN	1				
target_i2cREG1_temp.DIR	1				
target_i2cREG1_temp.DIN	1				
target_i2cREG1_temp.DOUT	1				
target_i2cREG1_temp.SET	0				
target_i2cREG1_temp.CLR	0				
target_i2cREG1_temp.ODR	1				
target_i2cREG1_temp.PD	0				
	0				
target_i2cREG1_temp.PSL	1				
target_i2cREG1_temp.PSL	1	Expected Value	Result		
target_i2cREG1_temp.PSL  Name	1 Actual Value	Expected Value	Result		
target_i2cREG1_temp.PSL  Name  DigColPsInt_I2CHwCustData_Uls_M_u16	1 Actual Value 511	511			
target_i2cREG1_temp.PSL  Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32	Actual Value 511 0	511 0			
target_i2cREG1_temp.PSL  Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)	1 Actual Value 511 0 63	511 0 63	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \		
target_i2cREG1_temp.PSL  Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)	1 Actual Value 511 0 63 2	511 0 63 2	· · · · · · · · · · · · · · · · · · ·		
target_i2cREG1_temp.PSL  Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR	1 Actual Value 511 0 63 2 23	511 0 63 2 23	· · · · · · · · · · · · · · · · · · ·		
target_i2cREG1_temp.PSL  Name  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR	1 Actual Value 511 0 63 2 23 10	511 0 63 2 23 10	· · · · · · · · · · · · · · · · · · ·		
target_i2cREG1_temp.PSL  Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR	1 Actual Value 511 0 63 2 23 10 1000	511 0 63 2 23 10	**************************************		
target_i2cREG1_temp.PSL  Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL	1 Actual Value 511 0 63 2 23 10 1000 666	511 0 63 2 23 10 1000 666	**************************************		
target_i2cREG1_temp.PSL  Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL	1 Actual Value 511 0 63 2 2 23 10 1000 666 7587	511 0 63 2 23 10 1000 666 7587	**************************************		
target_i2cREG1_temp.PSL  Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKH  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKH	1 Actual Value 511 0 63 2 2 23 10 1000 666 7587 356	511 0 63 2 23 10 1000 666 7587 356	**************************************		
target_i2cREG1_temp.PSL  Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKH  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT	1 Actual Value 511 0 63 2 2 23 10 1000 666 7587 356 98	511 0 63 2 23 10 1000 666 7587 356 98	**************************************		
target_i2cREG1_temp.PSL  Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKH  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.SAR	1 Actual Value 511 0 63 2 2 23 10 1000 666 7587 356 98 876	511 0 63 2 23 10 1000 666 7587 356 98 876	**************************************		
target_i2cREG1_temp.PSL  Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.SAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR	1 Actual Value 511 0 63 2 2 23 10 1000 666 7587 356 98 876 98	511 0 63 2 23 10 1000 666 7587 356 98 876 98	**************************************		
target_i2cREG1_temp.PSL  Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.SAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.MDR	1 Actual Value 511 0 63 2 2 23 10 1000 666 7587 356 98 876	511 0 63 2 23 10 1000 666 7587 356 98 876	**************************************		
target_i2cREG1_temp.PSL  Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.SAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR	1 Actual Value 511 0 63 2 2 23 10 1000 666 7587 356 98 876 98	511 0 63 2 23 10 1000 666 7587 356 98 876 98	**************************************		
target_i2cREG1_temp.PSL  Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.SAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.MDR	1 Actual Value 511 0 63 2 2 23 10 1000 666 7587 356 98 876 98 764	511 0 63 2 23 10 1000 666 7587 356 98 876 98 764	**************************************		
target_i2cREG1_temp.PSL  Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.MDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.JVR	1 Actual Value 511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736	511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736	· · · · · · · · · · · · · · · · · · ·		
target_i2cREG1_temp.PSL  Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.MDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.MDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IVR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.EMDR	1 Actual Value 511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736	511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736	· · · · · · · · · · · · · · · · · · ·		
target_i2cREG1_temp.PSL  Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.MDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IVR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.EMDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.EMDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.EMDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.EMDR	1 Actual Value 511 0 63 2 23 10 1000 666 7587 356 98 876 98 876 98 764 736 1	511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736 1 33	· · · · · · · · · · · · · · · · · · ·		
target_i2cREG1_temp.PSL  Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IVR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.EMDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.EMDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PSC  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID11	1 Actual Value 511 0 63 2 23 10 1000 666 7587 356 98 876 98 876 98 764 736 1 33 7	511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736 1 33 7	· · · · · · · · · · · · · · · · · · ·		
target_i2cREG1_temp.PSL  Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CKH  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.MDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IVR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.EMDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PSC  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID11  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID11	1 Actual Value 511 0 63 2 23 10 1000 666 7587 356 98 876 98 876 98 10 1 33 7	511 0 63 2 23 10 1000 666 7587 356 98 876 98 8764 736 1 33 7	· · · · · · · · · · · · · · · · · · ·		
target_i2cREG1_temp.PSL  Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.MDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.WR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PSC  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PSC  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID11  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DMAC	1 Actual Value 511 0 63 2 23 10 1000 666 7587 356 98 876 98 876 1 33 7	511 0 63 2 23 10 1000 666 7587 356 98 876 98 876 1 33 7 12			
target_i2cREG1_temp.PSL  Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.MDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IVR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.EMDR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID11  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID12  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DMAC  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DMAC  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.FUN	1 Actual Value 511 0 63 2 23 10 1000 666 7587 356 98 876 98 876 1 33 7 12 1	511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736 1 33 7 12 1			
target_i2cREG1_temp.PSL  Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.OAR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.IMR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.CLKL  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.CLKL  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.CLKL  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.CNT  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DRR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DRR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DRR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DXR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DXR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DNR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.ENDR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.PID11  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.PID12  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.PID12  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.PUN  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.PUN  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.PUN  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.PUN  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DIR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DIR	1 Actual Value 511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736 1 33 7 12 1 1	511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736 1 33 7 12 1 1			
target_i2cREG1_temp.PSL  Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.OAR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.OAR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.CLKL  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.CLKL  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.CLKL  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.CNT  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DRR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DRR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DRR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DRR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DRR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DRR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.PIDR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.PID11  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.PID12  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DMAC  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.PUN  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.PUN  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DIR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DIR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DIR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DIN  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DIN	1 Actual Value 511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736 1 33 7 12 1 1 1	511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736 1 33 7 12 1 1			
target_i2cREG1_temp.PSL  Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.OAR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.IMR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.CLKL  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.CLKL  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.CLKL  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.CNT  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DRR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DRR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DRR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DRR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DRR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DRR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.PID11  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.PID11  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.PID12  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DMAC  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DUN  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DUN  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DIR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DIN  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DUN  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DUN  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DUT  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DUT	1  Actual Value  511  0  63  2  23  10  1000  666  7587  356  98  876  98  764  736  1  33  7  12  1  1  1  1  1  0	511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736 1 33 7 12 1 1 1 1	**************************************		
target_i2cREG1_temp.PSL  Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.OAR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.OAR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.STR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.CLKL  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.CLKL  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.CNT  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DRR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DRR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DRR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DRR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DRR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DRR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.PIDR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.PID11  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.PID12  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.PID12  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DIN  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DIR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DIR  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DIN  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DUT  target_i2c_EnableNotification_i2cRegPtr_Cnt_T_str.DUT	1 Actual Value 511 0 63 2 23 10 1000 6666 7587 356 98 876 98 764 736 1 1 33 7 12 1 1 1 1 1 0 0 0	511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736 1 33 7 12 1 1 1 1 1 0 0			
Name  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitialTime_mS_M_u32  I2c_EnableNotification(Flags_Cnt_T_b32)  I2c_SetCount(Count_Cnt_T_u16)  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID11  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID11  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID12  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DNAC  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DNAC  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DIR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DIR  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DIN  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUN  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUN  target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DUN	1  Actual Value  511  0  63  2  23  10  1000  666  7587  356  98  876  98  764  736  1  33  7  12  1  1  1  1  1  0	511 0 63 2 23 10 1000 666 7587 356 98 876 98 764 736 1 33 7 12 1 1 1 1	**************************************		

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Name	Actual Value	Expected Value	Result
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PSL	1	1	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.OAR	23	23	•
target_l2c_Enable_l2cRegPtr_Cnt_T_str.IMR	10	10	- V
target_l2c_Enable_l2cRegPtr_Cnt_T_str.STR target_l2c Enable_l2cRegPtr_Cnt_T str.CLKL	666	666	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLKH	7587	7587	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CNT	356	356	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DRR	98	98	•
target_I2c_Enable_I2cRegPtr_Cnt_T_str.SAR	876	876	-
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DXR	98	98	<b>✓</b>
target_I2c_Enable_I2cRegPtr_Cnt_T_str.MDR	764	764	<b>✓</b>
target_I2c_Enable_I2cRegPtr_Cnt_T_str.IVR	736	736	•
target_I2c_Enable_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PSC	33	33	•
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PID11	7	7	<b>~</b>
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PID12	12	12	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DMAC	1	1	- V
target_l2c_Enable_l2cRegPtr_Cnt_T_str.FUN	1	1	
target_l2c_Enable_l2cRegPtr_Cnt_T_str.DIR target_l2c_Enable_l2cRegPtr_Cnt_T_str.DIN	1	1	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DOUT	1	1	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.SET	0	0	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLR	0	0	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PD	0	0	-
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PSL	1	1	<b>✓</b>
target_I2c_Init_I2cRegPtr_Cnt_T_str.OAR	23	23	-
target_I2c_Init_I2cRegPtr_Cnt_T_str.IMR	10	10	•
target_I2c_Init_I2cRegPtr_Cnt_T_str.STR	1000	1000	-
target_I2c_Init_I2cRegPtr_Cnt_T_str.CLKL	666	666	<b>✓</b>
target_I2c_Init_I2cRegPtr_Cnt_T_str.CLKH	7587	7587	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.CNT	356	356	<b>✓</b>
target_I2c_Init_I2cRegPtr_Cnt_T_str.DRR	98	98	•
target_I2c_Init_I2cRegPtr_Cnt_T_str.SAR	876	876	
target_I2c_Init_I2cRegPtr_Cnt_T_str.DXR	98 764	98 764	- V
target_l2c_Init_l2cRegPtr_Cnt_T_str.MDR target_l2c_Init_l2cRegPtr_Cnt_T_str.IVR	736	736	
target_l2c_init_l2cRegPtr_Cnt_T_str.EMDR	1	1	
target I2c Init I2cReqPtr Cnt T str.PSC	33	33	
target_I2c_Init_I2cRegPtr_Cnt_T_str.PID11	7	7	•
target_I2c_Init_I2cRegPtr_Cnt_T_str.PID12	12	12	-
target_I2c_Init_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>✓</b>
target_I2c_Init_I2cRegPtr_Cnt_T_str.FUN	1	1	-
target_I2c_Init_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_Init_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>→</b>
target_I2c_Init_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_Init_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
target_I2c_Init_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.PD	0	0	<b>~</b>
target_l2c_Init_l2cRegPtr_Cnt_T_str.PSL	1	23	<b>→</b>
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.OAR	23 10	10	
target_l2c_SetCount_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetCount_l2cRegPtr_Cnt_T_str.STR	1000	1000	
target_l2c_SetCount_l2cRegPtr_Cnt_T_str.CLKL	666	666	
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLKH	7587	7587	
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CNT	356	356	
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DRR	98	98	
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.SAR	876	876	_
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DXR	98	98	<b>✓</b>
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.MDR	764	764	-
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.IVR	736	736	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.EMDR	1	1	-
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PSC	33	33	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PID11	7	7	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PID12	12	12	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLR	0	0	· · · · · · · · · · · · · · · · · · ·

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Name	Actual Value	Expected Value	Result
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.ODR	1	1	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
target I2c SetCount I2cRegPtr Cnt T str.PSL	1	1	<b>✓</b>

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c_Init	1	I2c_Init	1	~
I2c_SetCount	1	I2c_SetCount	1	~
I2c_EnableNotification	1	I2c_EnableNotification	1	~
I2c_Enable	1	I2c_Enable	1	•
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	•

Test Step 1.2 (Repeat Count = 1)			<b>✓</b>		
Name	Input Value				
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u	32_CurrentTime			
I2c_Enable(I2cRegPtr_Cnt_T_str)	target_I2c_Enable_I2cRegPtr_	_Cnt_T_str			
I2c_EnableNotification(I2cRegPtr_Cnt_T_str)	target_I2c_EnableNotification_	_I2cRegPtr_Cnt_T_str			
I2c_Init(I2cRegPtr_Cnt_T_str)	target_I2c_Init_I2cRegPtr_Cnt	target_I2c_Init_I2cRegPtr_Cnt_T_str			
I2c_SetCount(I2cRegPtr_Cnt_T_str)	target_I2c_SetCount_I2cRegF	target_I2c_SetCount_I2cRegPtr_Cnt_T_str			
i2cREG1_temp	target_i2cREG1_temp				
target_GetSystemTime_mS_u32_CurrentTime	4294967295				
target_i2cREG1_temp.OAR	456				
target_i2cREG1_temp.IMR	66				
target_i2cREG1_temp.STR	56				
target_i2cREG1_temp.CLKL	4555				
target_i2cREG1_temp.CLKH	987				
target_i2cREG1_temp.CNT	87				
target_i2cREG1_temp.DRR	54				
target_i2cREG1_temp.SAR	1000				
target_i2cREG1_temp.DXR	45				
target_i2cREG1_temp.MDR	98				
target_i2cREG1_temp.IVR	332				
target_i2cREG1_temp.EMDR	2				
target_i2cREG1_temp.PSC	4				
target_i2cREG1_temp.PID11	7788				
target i2cREG1 temp.PID12	34				
target i2cREG1 temp.DMAC	2				
target_i2cREG1_temp.FUN	0				
target_i2cREG1_temp.DIR	2				
target_i2cREG1_temp.DIN	2				
target_i2cREG1_temp.DOUT	3				
target_i2cREG1_temp.SET	3				
target_i2cREG1_temp.CLR	3				
target_i2cREG1_temp.ODR	2				
target_i2cREG1_temp.PD	1				
target_i2cREG1_temp.PSL	0				
Name	Actual Value	Expected Value	Result		
DigColPsInt_I2CHwCustData_Uls_M_u16	511	511	<b>✓</b>		
DigColPsInt_InitialTime_mS_M_u32	4294967295	4294967295	<b>→</b>		
I2c_EnableNotification(Flags_Cnt_T_b32)	63	63			
I2c_SetCount(Count_Cnt_T_u16)	2	2	•		
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR	456	456	_		
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>		
target I2c EnableNotification I2cRegPtr Cnt T str.STR	56	56			
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL	4555	4555	•		
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKH	987	987			
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>→</b>		
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR	54	54			
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.SAR	1000	1000			
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR	45	45			
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.MDR	98	98			
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.IVR	332	332			
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.EMDR	2	2	<u> </u>		
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PSC	4	4			
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID11	7788	7788			
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID12	34	34	-		
	2	2			
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DMAC		0			
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.FUN	0 2	2			
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DIR					
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DIN	2	2			

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Name	Actual Value	Expected Value	Result
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.SET	3	3	<u> </u>
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLR	3	3	•
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PD	1	1	•
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>
target_l2c_Enable_l2cRegPtr_Cnt_T_str.OAR	456	456	•
target_l2c_Enable_l2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target_I2c_Enable_I2cRegPtr_Cnt_T_str.STR	56	56	<b>✓</b>
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLKL	4555	4555	<b>✓</b>
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLKH	987	987	<b>✓</b>
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DRR	54	54	•
target_I2c_Enable_I2cRegPtr_Cnt_T_str.SAR	1000	1000	_
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DXR	45	45	•
target_l2c_Enable_l2cRegPtr_Cnt_T_str.MDR	98	98	
target_l2c_Enable_l2cRegPtr_Cnt_T_str.IVR	332	332	
	2	2	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.EMDR			
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PSC	4	4	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PID11	7788	7788	-
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PID12	34	34	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DMAC	2	2	-
target_I2c_Enable_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DIR	2	2	•
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DOUT	3	3	-
target_I2c_Enable_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLR	3	3	-
target_I2c_Enable_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PD	1	1	
	0	0	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PSL		i i	
target_I2c_Init_I2cRegPtr_Cnt_T_str.OAR	456	456	
target_I2c_Init_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.STR	56	56	~
target_l2c_Init_l2cRegPtr_Cnt_T_str.CLKL	4555	4555	•
target_l2c_Init_l2cRegPtr_Cnt_T_str.CLKH	987	987	✓
target_l2c_Init_l2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_Init_I2cRegPtr_Cnt_T_str.DRR	54	54	<b>✓</b>
target_I2c_Init_I2cRegPtr_Cnt_T_str.SAR	1000	1000	<b>✓</b>
target_I2c_Init_I2cRegPtr_Cnt_T_str.DXR	45	45	<b>✓</b>
target_I2c_Init_I2cRegPtr_Cnt_T_str.MDR	98	98	•
target_I2c_Init_I2cRegPtr_Cnt_T_str.IVR	332	332	_
target_I2c_Init_I2cRegPtr_Cnt_T_str.EMDR	2	2	
target_l2c_Init_l2cRegPtr_Cnt_T_str.PSC	4	4	
target_l2c_Init_l2cRegPtr_Cnt_T_str.PID11	7788	7788	
target_I2c_Init_I2cRegPtr_Cnt_T_str.PID12	34	34	
target_I2c_Init_I2cRegPtr_Cnt_T_str.DMAC	2	2	
target_I2c_Init_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>~</b>
target_I2c_Init_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
target_l2c_Init_l2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_Init_I2cRegPtr_Cnt_T_str.SET	3	3	✓
target_I2c_Init_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>✓</b>
target_I2c_Init_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_Init_I2cRegPtr_Cnt_T_str.PD	1	1	<b>✓</b>
target_I2c_Init_I2cRegPtr_Cnt_T_str.PSL	0	0	
target_l2c_SetCount_l2cRegPtr_Cnt_T_str.OAR	456	456	
-			
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.IMR	66	66	· ·
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.STR	56	56	<b>✓</b>
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLKL	4555	4555	<b>→</b>
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLKH	987	987	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DRR	54	54	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.SAR	1000	1000	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DXR	45	45	<b>✓</b>
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.MDR	98	98	-
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.IVR	332	332	
target_l2c_SetCount_l2cRegPtr_Cnt_T_str.EMDR	2	2	
· · · · · · · · · · · · · · · · · · ·	4	4	
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PSC	7788	7788	
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PID11			· ·
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PID12	34	34	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.FUN	0	0	





Name	Actual Value	Expected Value	Result
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DIR	2	2	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DIN	2	2	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DOUT	3	3	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.SET	3	3	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLR	3	3	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.ODR	2	2	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PSL	0	0	✓

Τ				V
Actual Function	Count	Expected Function	Count	Result
I2c_Init	1	I2c_Init	1	~
I2c_SetCount	1	I2c_SetCount	1	~
I2c_EnableNotification	1	I2c_EnableNotification	1	~
I2c_Enable	1	I2c_Enable	1	<b>✓</b>
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	~

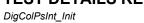
Name	Input Value				
GetSystemTime_mS_u32(CurrentTime)	· · · · · · · · · · · · · · · · · · ·	target_GetSystemTime_mS_u32_CurrentTime			
I2c_Enable(I2cRegPtr_Cnt_T_str)	target_I2c_Enable_I2cRegPtr_Cnt_T_str				
I2c EnableNotification(I2cRegPtr Cnt T str)		target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str			
I2c_Init(I2cRegPtr_Cnt_T_str)	target_I2c_Init_I2cRegPtr_Cnt_	-			
I2c_SetCount(I2cRegPtr_Cnt_T_str)	target_I2c_SetCount_I2cRegPt				
i2cREG1_temp	target_i2cREG1_temp				
target_GetSystemTime_mS_u32_CurrentTime	1457865				
target_i2cREG1_temp.OAR	66				
target_i2cREG1_temp.IMR	125				
target i2cREG1 temp.STR	44				
target_i2cREG1_temp.CLKL	566				
target_i2cREG1_temp.CLKH	3298				
target_i2cREG1_temp.CNT	455				
target_i2cREG1_temp.DRR	6				
target_i2cREG1_temp.SAR	123				
target_i2cREG1_temp.DXR	7				
target_i2cREG1_temp.MDR	2				
target_i2cREG1_temp.IVR	66				
target_i2cREG1_temp.EMDR	3				
target_i2cREG1_temp.PSC	75				
target_i2cREG1_temp.PID11	5444				
target_i2cREG1_temp.PID12	76				
target i2cREG1 temp.DMAC	0				
target_i2cREG1_temp.FUN	1				
target_i2cREG1_temp.DIR	0				
target i2cREG1 temp.DIN	3				
target_i2cREG1_temp.DOUT	2				
target_i2cREG1_temp.SET	1				
target_i2cREG1_temp.CLR	2				
target_i2cREG1_temp.ODR	3				
target_i2cREG1_temp.PD	2				
target_i2cREG1_temp.PSL	3				
Name	Actual Value	Expected Value	Resu		
	511	511	Resu		
DigColPsInt_I2CHwCustData_Uls_M_u16					
DigColPsInt_InitialTime_mS_M_u32	1457865	1457865			
I2c_EnableNotification(Flags_Cnt_T_b32)	63	63			
I2c_SetCount(Count_Cnt_T_u16)					
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR	66	66			
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR	125	125			
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR	44 566	44 566			
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL	111	1			
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKH	3298	3298			
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.CNT	455 6	455			
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.DRR		6			
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.SAR	123	123			
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.DXR	7	7			
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.MDR	2	2			
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IVR	66	66			
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.EMDR	3 75	3 75			
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PSC					





Name	Actual Value	Expected Value	Result
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID12	76	76	~
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.DMAC	0	0	<b>V</b>
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.FUN	0	0	· ·
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.DIR target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.DIN	3	3	
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.PSL	3	3	~
target_l2c_Enable_l2cRegPtr_Cnt_T_str.OAR	66	66	· ·
target_l2c_Enable_l2cRegPtr_Cnt_T_str.IMR target_l2c_Enable_l2cRegPtr_Cnt_T_str.STR	125 44	125 44	~
target_12c_Enable_12cRegPtr_Cnt_T_str.CLKL	566	566	-
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLKH	3298	3298	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CNT	455	455	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_l2c_Enable_l2cRegPtr_Cnt_T_str.SAR	123	123	~
target_l2c_Enable_l2cRegPtr_Cnt_T_str.DXR	7	7	~
target_l2c_Enable_l2cRegPtr_Cnt_T_str.MDR target_l2c_Enable_l2cRegPtr_Cnt_T_str.IVR	2 66	2 66	<b>V</b>
target_I2c_Enable_I2cRegPtr_Cnt_T_str.IVR target_I2c_Enable_I2cRegPtr_Cnt_T_str.EMDR	3	3	J
target_12c_Enable_12cRegPtr_Cnt_T_str.PSC	75	75	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PID11	5444	5444	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PID12	76	76	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_l2c_Enable_l2cRegPtr_Cnt_T_str.DIR	0	0	~
target_l2c_Enable_l2cRegPtr_Cnt_T_str.DIN	3	3	<b>Y</b>
target_l2c_Enable_l2cRegPtr_Cnt_T_str.DOUT	1	1	-
target_l2c_Enable_l2cRegPtr_Cnt_T_str.SET target_l2c_Enable_l2cRegPtr_Cnt_T_str.CLR	2	2	J
target_12c_Enable_12cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_l2c_Init_l2cRegPtr_Cnt_T_str.IMR	125	125	~
target_l2c_Init_l2cRegPtr_Cnt_T_str.STR	44	44	<b>V</b>
target_l2c_Init_l2cRegPtr_Cnt_T_str.CLKL	566 3298	566 3298	~
target_l2c_Init_l2cRegPtr_Cnt_T_str.CLKH target_l2c_Init_l2cRegPtr_Cnt_T_str.CNT	455	455	
target_l2c_Init_l2cRegPtr_Cnt_T_str.DRR	6	6	-
target_I2c_Init_I2cRegPtr_Cnt_T_str.SAR	123	123	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.DXR	7	7	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.MDR	2	2	~
target_l2c_Init_l2cRegPtr_Cnt_T_str.IVR	66	66	~
target_l2c_Init_l2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_l2c_Init_l2cRegPtr_Cnt_T_str.PSC	75 5444	75 5444	
target_l2c_Init_l2cRegPtr_Cnt_T_str.PID11 target_l2c_Init_l2cRegPtr_Cnt_T_str.PID12	76	76	J
target_12c_Init_12cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>~</b>
target_l2c_Init_l2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_l2c_Init_l2cRegPtr_Cnt_T_str.SET	1	1	~
target_l2c_Init_l2cRegPtr_Cnt_T_str.CLR	2	2	~
target_l2c_Init_l2cRegPtr_Cnt_T_str.ODR	3 2	3 2	~
target_l2c_Init_l2cRegPtr_Cnt_T_str.PD target_l2c_Init_l2cRegPtr_Cnt_T_str.PSL	3	3	J
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.IMR	125	125	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.STR	44	44	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLKH	3298	3298	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CNT	455	455	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_l2c_SetCount_l2cRegPtr_Cnt_T_str.SAR	123	123	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DXR	7 2	7 2	
target_l2c_SetCount_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetCount_l2cRegPtr_Cnt_T_str.IVR	66	66	- V
target_I2c_SetCount_I2cRegPti_Cnt_T_str.tvk target_I2c_SetCount_I2cRegPtr_Cnt_T_str.EMDR	3	3	-
0. =	-	-	

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Name	Actual Value	Expected Value	Result
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PSC	75	75	<b>✓</b>
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PID11	5444	5444	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PID12	76	76	<b>✓</b>
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DIN	3	3	<b>✓</b>
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>✓</b>
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PSL	3	3	~

T				V
Actual Function	Count	Expected Function	Count	Result
I2c_Init	1	I2c_Init	1	~
I2c_SetCount	1	I2c_SetCount	1	<b>✓</b>
I2c_EnableNotification	1	I2c_EnableNotification	1	~
I2c_Enable	1	I2c_Enable	1	<b>✓</b>
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	•

Test Step 1.4 (Repeat Count = 1)	Inmut V-I		
Name	Input Value	20. O	
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u		
I2c_Enable(I2cRegPtr_Cnt_T_str)	target_l2c_Enable_l2cRegPtr_		
I2c_EnableNotification(I2cRegPtr_Cnt_T_str)	target_l2c_EnableNotification_		
I2c_Init(I2cRegPtr_Cnt_T_str)	target_l2c_Init_l2cRegPtr_Cnt		
I2c_SetCount(I2cRegPtr_Cnt_T_str)	target_l2c_SetCount_l2cRegP	tr_Cnt_T_str	
i2cREG1_temp	target_i2cREG1_temp		
target_GetSystemTime_mS_u32_CurrentTime	0		
target_i2cREG1_temp.OAR	0		
target_i2cREG1_temp.IMR	0		
target_i2cREG1_temp.STR	0		
target_i2cREG1_temp.CLKL	0		
target_i2cREG1_temp.CLKH	0		
target_i2cREG1_temp.CNT	0		
target_i2cREG1_temp.DRR	0		
target_i2cREG1_temp.SAR	0		
target_i2cREG1_temp.DXR	0		
target_i2cREG1_temp.MDR	0		
target_i2cREG1_temp.IVR	0		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	0		
target_i2cREG1_temp.PID11	0		
target_i2cREG1_temp.PID12	0		
target_i2cREG1_temp.DMAC	0		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	0		
target_i2cREG1_temp.DOUT	0		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Resul
DigColPsInt_I2CHwCustData_Uls_M_u16	511	511	•
DigColPsInt_InitialTime_mS_M_u32	0	0	
I2c_EnableNotification(Flags_Cnt_T_b32)	63	63	
I2c_SetCount(Count_Cnt_T_u16)	2	2	
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR	0	0	
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR	0	0	
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR	0	0	
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL	0	0	
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKH	0	0	
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT	0	0	
•	0	0	
target 12c EnableNotification 12cRegPtr Cnt T str DPP			
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.DRR target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.SAR	0	0	

0

0

target\_I2c\_EnableNotification\_I2cRegPtr\_Cnt\_T\_str.DXR





N	A street Webse	From a set of Walter	D14
Name	Actual Value	Expected Value 0	Result
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.MDR target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IVR	0	0	J
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PSC	0	0	~
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID11	0	0	~
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID12	0	0	~
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.DIR	0	0	~
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.DIN target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.DOUT	0	0	
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.SET	0	0	
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.OAR	0	0	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.IMR	0	0	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.STR	0	0	~
target_l2c_Enable_l2cRegPtr_Cnt_T_str.CLKL	0	0	~
target_l2c_Enable_l2cRegPtr_Cnt_T_str.CLKH	0	0	· ·
target_l2c_Enable_l2cRegPtr_Cnt_T_str.CNT target_l2c_Enable_l2cRegPtr_Cnt_T_str.DRR	0	0	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DRR target_I2c_Enable_I2cRegPtr_Cnt_T_str.SAR	0	0	-
target_l2c_Enable_l2cRegPtr_Cnt_T_str.DXR	0	0	<b>V</b>
target_I2c_Enable_I2cRegPtr_Cnt_T_str.MDR	0	0	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.IVR	0	0	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PSC	0	0	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PID11	0	0	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PID12	0	0	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_l2c_Enable_l2cRegPtr_Cnt_T_str.DIR	0	0	
target_l2c_Enable_l2cRegPtr_Cnt_T_str.DIN target_l2c_Enable_l2cRegPtr_Cnt_T_str.DOUT	0	0	J
target_l2c_Enable_l2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLR	0	0	-
target_I2c_Enable_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.OAR	0	0	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.IMR	0	0	~
target_l2c_Init_l2cRegPtr_Cnt_T_str.STR	0	0	~
target_l2c_Init_l2cRegPtr_Cnt_T_str.CLKL	0	0	· ·
target_l2c_Init_l2cRegPtr_Cnt_T_str.CLKH target_l2c_Init_l2cRegPtr_Cnt_T_str.CNT	0	0	-
target_I2c_Init_I2cRegPtr_Cnt_T_str.DRR	0	0	J
target_l2c_Init_l2cRegPtr_Cnt_T_str.SAR	0	0	~
target I2c Init I2cRegPtr Cnt T str.DXR	0	0	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.MDR	0	0	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.IVR	0	0	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.PSC	0	0	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.PID11	0	0	~
target_l2c_Init_l2cRegPtr_Cnt_T_str.PID12	0	0	<b>-</b>
target_l2c_Init_l2cRegPtr_Cnt_T_str.DMAC	0	0	· ·
target_l2c_Init_l2cRegPtr_Cnt_T_str.FUN target_l2c_Init_l2cRegPtr_Cnt_T_str.DIR	0	0	
target_I2c_Init_I2cRegPtr_Cnt_T_str.DIN	0	0	
target_12c_Init_12cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_l2c_Init_l2cRegPtr_Cnt_T_str.CLR	0	0	<b>~</b>
target_l2c_Init_l2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_Init_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
target_I2c_Init_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_l2c_SetCount_l2cRegPtr_Cnt_T_str.OAR	0	0	<b>~</b>
target_l2c_SetCount_l2cRegPtr_Cnt_T_str.IMR	0	0	<b>Y</b>
target_l2c_SetCount_l2cRegPtr_Cnt_T_str.STR	0	0	V
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLKL	0	0	
target_l2c_SetCount_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetCount_l2cRegPtr_Cnt_T_str.CNT	0	0	9
target_12c_SetCount_12cRegPtr_Cnt_T_str.DRR	0	0	<b>V</b>
0			

DigColPsInt\_Init





Name	Actual Value	Expected Value	Result
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.SAR	0	0	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DXR	0	0	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.MDR	0	0	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.IVR	0	0	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.EMDR	0	0	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PSC	0	0	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PID11	0	0	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PID12	0	0	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DMAC	0	0	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.FUN	0	0	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DIR	0	0	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DIN	0	0	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DOUT	0	0	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.SET	0	0	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLR	0	0	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.ODR	0	0	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PD	0	0	✓
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PSL	0	0	✓

T				V
Actual Function	Count	Expected Function	Count	Result
I2c_Init	1	I2c_Init	1	~
I2c_SetCount	1	I2c_SetCount	1	<b>✓</b>
I2c_EnableNotification	1	I2c_EnableNotification	1	~
I2c_Enable	1	I2c_Enable	1	•
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	<b>✓</b>

Name	Input Value		
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_	u32 CurrentTime	
I2c Enable(I2cReqPtr Cnt T str)	target I2c Enable I2cRegPti		
I2c_EnableNotification(I2cRegPtr_Cnt_T_str)	target_I2c_EnableNotification		
I2c_Init(I2cRegPtr_Cnt_T_str)	target_I2c_Init_I2cRegPtr_Cr		
I2c_SetCount(I2cRegPtr_Cnt_T_str)	target_I2c_SetCount_I2cReg		
i2cREG1 temp	target_i2cREG1_temp	0	
target_GetSystemTime_mS_u32_CurrentTime	4294967295		
target i2cREG1 temp.OAR	1023		
target_i2cREG1_temp.IMR	255		
target_i2cREG1_temp.STR	32767		
target_i2cREG1_temp.CLKL	65535		
target_i2cREG1_temp.CLKH	65535		
target_i2cREG1_temp.CNT	65535		
target_i2cREG1_temp.DRR	255		
target_i2cREG1_temp.SAR	1023		
target_i2cREG1_temp.DXR	255		
target_i2cREG1_temp.MDR	65535		
target_i2cREG1_temp.IVR	4095		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	255		
target_i2cREG1_temp.PID11	65535		
target_i2cREG1_temp.PID12	255		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	3		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	3		
target_i2cREG1_temp.ODR	3		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Resul
DigColPsInt_I2CHwCustData_Uls_M_u16	511	511	•
DigColPsInt_InitialTime_mS_M_u32	4294967295	4294967295	•
I2c_EnableNotification(Flags_Cnt_T_b32)	63	63	•
I2c_SetCount(Count_Cnt_T_u16)	2	2	•
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR	1023	1023	•
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR	255	255	
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR	32767	32767	•
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	





Name	Actual Value	Expected Value	Result
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	~
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT	65535	65535	~
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR	255	255	~
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.SAR	1023	1023	<b>✓</b>
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR	255	255	<b>Y</b>
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.MDR	65535	65535	<b>~</b>
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.IVR	4095	4095	
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.EMDR	3	3	<u> </u>
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.PSC	255	255	
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.PID11	65535	65535	<u> </u>
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.PID12	255	255	
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.DMAC	3	3	<b>V</b>
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>V</b>
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DIN	3	3	
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.DOUT	3	3	
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.SET	3	3 3	
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.CLR	3		
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.ODR	3	3	
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.PD	3	3	
target_l2c_EnableNotification_l2cRegPtr_Cnt_T_str.PSL	3	3	
target_l2c_Enable_l2cRegPtr_Cnt_T_str.OAR	1023	1023	
target_l2c_Enable_l2cRegPtr_Cnt_T_str.IMR	255	255	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.STR	32767	32767	Ž
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	
target_l2c_Enable_l2cRegPtr_Cnt_T_str.CLKH	65535	65535	
target_l2c_Enable_l2cRegPtr_Cnt_T_str.CNT	65535	65535	
target_l2c_Enable_l2cRegPtr_Cnt_T_str.DRR	255	255	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.SAR	1023	1023	
target_l2c_Enable_l2cRegPtr_Cnt_T_str.DXR	255	255	
target_l2c_Enable_l2cRegPtr_Cnt_T_str.MDR	65535	65535	
target_l2c_Enable_l2cRegPtr_Cnt_T_str.IVR	4095	4095	
target_l2c_Enable_l2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PSC	255	255 65535	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PID11	65535 255	255	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PID12	3	3	
target_l2c_Enable_l2cRegPtr_Cnt_T_str.DMAC	1	1	
target_l2c_Enable_l2cRegPtr_Cnt_T_str.FUN target_l2c_Enable_l2cRegPtr_Cnt_T_str.DIR	3	3	
	3	3	-
target_l2c_Enable_l2cRegPtr_Cnt_T_str.DIN target_l2c_Enable_l2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLR	3	3	
target_I2C_Enable_I2cRegPtr_Cnt_T_str.ODR	3	3	-
target_l2c_Enable_l2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>*</b>
target_l2c_Init_l2cRegPtr_Cnt_T_str.OAR	1023	1023	
target_l2c_Init_l2cRegPtr_Cnt_T_str.IMR	255	255	·
target_l2c_Init_l2cRegPtr_Cnt_T_str.STR	32767	32767	
target_l2c_Init_l2cRegPtr_Cnt_T_str.CLKL	65535	65535	_
target_l2c_Init_l2cRegPtr_Cnt_T_str.CLKH	65535	65535	
target_l2c_Init_l2cRegPtr_Cnt_T_str.CNT	65535	65535	
target_I2c_Init_I2cRegPtr_Cnt_T_str.DRR	255	255	
target_l2c_Init_l2cRegPtr_Cnt_T_str.SAR	1023	1023	<b>*</b>
target_l2c_Init_l2cRegPtr_Cnt_T_str.DXR	255	255	
target_l2c_Init_l2cRegPtr_Cnt_T_str.MDR	65535	65535	
target_l2c_Init_l2cRegPtr_Cnt_T_str.IVR	4095	4095	
target I2c Init I2cRegPtr Cnt T str.EMDR	3	3	·
target_l2c_Init_l2cRegPtr_Cnt_T_str.PSC	255	255	
target_l2c_Init_l2cRegPtr_Cnt_T_str.PID11	65535	65535	·
target_l2c_Init_l2cRegPtr_Cnt_T_str.PID12	255	255	
target_l2c_Init_l2cRegPtr_Cnt_T_str.DMAC	3	3	<b>*</b>
target_l2c_Init_l2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_Init_I2cRegPtr_Cnt_T_str.DIR	3	3	
target_I2c_Init_I2cRegPtr_Cnt_T_str.DIN	3	3	
target_I2c_Init_I2cRegPtr_Cnt_T_str.DOUT	3	3	_
target_I2c_Init_I2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_Init_I2cRegPtr_Cnt_T_str.CLR	3	3	-
target_l2c_Init_l2cRegPtr_Cnt_T_str.ODR	3	3	
target_I2c_Init_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_Init_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.OAR	1023	1023	
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.IMR	255	255	
tangor_i=o_ootoodini_i=ortogr ti_ont_i_out.iiviit			

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Name	Actual Value	Expected Value	Result
target I2c SetCount I2cReqPtr Cnt T str.STR	32767	32767	Result
8			
target_l2c_SetCount_l2cRegPtr_Cnt_T_str.CLKL	65535	65535	
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CNT	65535	65535	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DRR	255	255	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.SAR	1023	1023	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DXR	255	255	<b>✓</b>
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.MDR	65535	65535	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.IVR	4095	4095	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PSC	255	255	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PID11	65535	65535	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PID12	255	255	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.ODR	3	3	•
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_l2c_SetCount_l2cRegPtr_Cnt_T_str.PSL	3	3	•

Т				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c_Init	1	I2c_Init	1	~
I2c_SetCount	1	I2c_SetCount	1	~
I2c_EnableNotification	1	I2c_EnableNotification	1	-
I2c_Enable	1	I2c_Enable	1	~
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	~

Source File(s) File

**Compiler Options** 

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SetupRead			Razorcat
Project			
Module			
Test Object			
Instrumentation: Test Obje	ct Only		
Statement (C0) Coverage			
Branch (C1) Coverage			
Statistics			
Total Testcases			
Successful	•		
Failed			
Not Executed			
Module Properties			
Project Root Directory			
Configuration File			
Target Environment			
Kind of Test			
Linker Options			

Comments/Description/Spec	cification
Name	Text





Attributes	
Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	\$(Compiler Install Path)\include
Time Unit	Cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\Clxx_DigColPs\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

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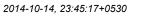
SetupRead

	Case 1		

Description

Test Step 1.1 (Repeat Count = 1)			V
Name	Input Value		
	0.0		
	<u> </u>		
	α		
	0		
	0		
Name	Actual Value	Expected Value	Result
Name	Actual Value	Expected Value	<b>✓</b>
Name	Actual Value	Expected Value	•
Name	Actual Value	Expected Value	•
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a	Actual Value	Expected Value	
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SetupRead





Name	Actual Value	Expected Value	Result
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Actual Function	Count	Expected Function	Count	Result
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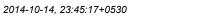
SetupRead

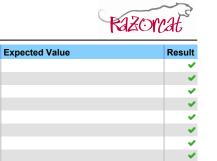
Test Step 1.2 (Repeat Count = 1)			V
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Name	Actual Value	Expected Value Res	
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SetupRead

Name

**Actual Value** 





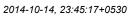
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T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
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Test Step 1.3 (Repeat Count = 1)			<b>✓</b>
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Name	Actual Value	Expected Value	Result
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SetupRead

Name

**Actual Value** 





**Expected Value** 

Actual Function	Count	Expected Function		Count	Result
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Test Step 1.4 (Repeat Count = 1)	✓
Name	Input Value

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Actual Function	Count	Expected Function	Count	t Result
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Test Step 1.5 (Repeat Count = 1)			V
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Name		Expected Value	*
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Actual Function	Count	Expected Function	Count	Result
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Test Step 1.6 (Repeat Count = 1)			✓.
Name	Input Value		
Name	Actual Value	Expected Value	Result
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			<b>✓</b>

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Actual Function	Count	Expected Function	Count	Result
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Test Step 1.7 (Repeat Count = 1)	✓
Name	Input Value

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SetupRead Name Input Value Actual Value **Expected Value** Result Name 

SetupRead

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Name	Actual Value	Expected Value	Result
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Actual Function	Count	Expected Function	Count	Result
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				<b>✓</b>

Test Step 1.8 (Repeat Count = 1)			
Name	Input Value		
Name	Actual Value	Expected Value	Result
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Name	Actual Value	Expected Value	Result
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Actual Function	Count	Expected Function	Count	Result
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DigColPsInt\_InterruptNotification

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of range.'

DigColPsInt\_InterruptNotification



Module 'DigColPsInt'

Name of Tester:Priti Mangalekar
Code File(s) Under Test:Sa\_DigColPsInt.c
Code File(s) Version:7
Module Design Document:DigColPsInt\_MDD.docx
Module Design Document Version:8
Data Dictionary Version:9
Unit Test Plan Version:2
Optimization Level:Level 2
Compiler (CodeGen) Version:TMS470\_4.9.5
Model Type:Excel Macro
Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.30
Total FLASH Used (Bytes):N/A
Total FLASH Used (Bytes):N/A
Total CALS Used (Bytes):N/A
Total Total Endough Test Requirements:
Test Date:10/13/2014
Comments:

NOTE 1: In """DigColPsInt\_StartRequest"" function, path """(Type\_Cnt\_T\_u08 > D\_NONE\_CNT\_u08) = TRUE && (Type\_Cnt\_T\_u08 <= D\_STATUSREG\_CNT\_u08) = FALSE"" cannot be covered because range of """Type\_Cnt\_T\_u08" is '0-5' and value of """D\_STATUSREG\_CNT\_U08) = TRUE Type\_Cnt\_T\_u08 <= D\_STATUSREG\_CNT\_u08 = True Type\_Cnt\_T\_u08 =

Attributes	
Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	<pre>\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd</pre>
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	\$(Compiler Install Path)\include
Time Unit	Cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\Clxx_DigColPs\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP



#### **Test Case 1: Metrics Test**

DigColPsInt\_InterruptNotification

Description

Test Vector Description:

TS1.1"Shortest Execution Path switch ((i2cIntFlags)Flags\_Cnt\_T\_b16)=>Default" TS1.2"Longest Execution Path switch case INIT\_SENSOR2\_EXTREADCTRLREG\_READ:True ((DigColPsInt\_Buffer\_Cnt\_M\_u08[1] & 0x01U) == 0x01U )=True ((DigColPsInt\_ColCustDatFound\_Cnt\_M\_lgc == TRUE) && (DigColPsInt\_ColCustDatFound\_Cnt\_M\_lgc == TRUE) && (DigColPsInt\_AttempOccurForCustDatRead\_Cnt\_M\_u08 > D\_MAXATTEMPTSFORCUSTDATREAD\_CNT\_U08 )=False"

Test Step 1.1 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2
DigColPsInt_Buffer_Cnt_M_u08[0]	22
DigColPsInt_Buffer_Cnt_M_u08[1]	44
DigColPsInt_Buffer_Cnt_M_u08[2]	55
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	495
DigColPsInt_CurrentSlave_Cnt_M_u08	100
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	7
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	5
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SkipRegisterWrite_Cnt_M_Igc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	897
DigColPsInt_TransactionCnt_Cnt_M_u08	20
Flags_Cnt_T_b16	64
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str) I2c SetRecv(I2cRegPtr Cnt T str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
l2c SetStatus(l2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str target_l2c SetStatus_l2cRegPtr_Cnt_T_str
_ , , , , , , , , , , , , , , , , , , ,	target_l2c_Setstatus_l2ckegPti_Cfit_1_str  target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
l2c_SetupMasterReceive(l2cRegPtr_Cnt_T_str) l2c_SetupMasterTransmit(l2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	14
k_SpurSensorl2CAddress_Cnt_u08	20
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	66
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR	78
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR	495
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	56 78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_I_str.FUN target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DUT	0
target_ize_Genotopoonu_izer\egr ti_Ont_1_Str.DO01	V

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DigColPsInt\_InterruptNotification

DigColPSint_Interruptivotilication		
Name	Input Value	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	
arget I2c GenStopCond I2cRegPtr Cnt T str.PD	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	
arget I2c Send I2cRegPtr Cnt T str.CLKL	495	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	
arget I2c Send I2cRegPtr Cnt T str.DRR	98	
· ·		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	
	78	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	66	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	78	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	
arget I2c SetRecv I2cRegPtr Cnt T str.FUN	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	
arget I2c SetRecv I2cRegPtr Cnt T str.DIN	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.D0UT	0	
	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	66	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	78	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	78	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	495	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	56	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	897	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	98	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	66	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	78	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	495	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	66	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	78	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	56	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	78	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	
	0	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	

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Name	Input Value
target I2c SetStatus I2cRegPtr Cnt T str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR target_I2c SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66 78
target I2c SetupMasterReceive I2cRegPtr Cnt T str.STR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	495 66
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	1 0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	495 56
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	897
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	56 78
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR target_I2c SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_1_str.PD target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.lMR	78
target_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56
target_i2cREG1_temp.CNT	897
target_i2cREG1_temp.DRR	98
target_i2cREG1_temp.DVP	66
target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR	78 495
target i2cREG1_temp.IVR	66
target i2cREG1 temp.EMDR	0
target_i2cREG1_temp.PSC	78
target_i2cREG1_temp.PID11	56
target i2cREG1 temp.PID12	78
target_i2cREG1_temp.DMAC	0

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Name	Input Value		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	0		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2	2	~
DigColPsInt_Buffer_Cnt_M_u08[0]	22	22	<b>~</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	44	44	
DigColPsInt_Buffer_Cnt_M_u08[2]	55	55	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	<b>V</b>
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	<b>V</b>
DigColPsInt_ColCustDatFound_Cnt_M_Igc	0	0	<b>*</b>
DigColPsInt_ColSnsrData_Cnt_M_u16	495 100	100	
DigColPsInt_CurrentSlave_Cnt_M_u08		1.	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ 7	INIT_SENSOR1_READERROR_READ 7	
DigColPsInt_I2CHwCustData_Uls_M_u16	5	5	
DigColPoint_I2CHwincompleteCustData_Uls_M_u16	1	1	
DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt NackOccured Cnt M_lgc	1	1	
	1	1	
DigColPsInt_RecvOverrunError_Cnt_M_Igc DigColPsInt_RecvdDataType Cnt M u08	1	1	-
DigColPsInt_RecvobataType_Cit_w_u06  DigColPsInt_SpurCustDatFound Cnt M lgc	1	1	
DigColPsInt_SpurSnsrData_Cnt_M_u16	897	897	
DigColPsInt_TransactionCnt_Cnt_M_u08	20	20	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	66	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	78	78	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	78	78	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	495	495	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	56	56	·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	897	897	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	98	98	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	66	66	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	78	78	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	78	78	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	56	56	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	78	78	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	<b>V</b>
target 12c Send 12cRegPtr Cnt T str MDR	495	495	-

495

66

0

78

56

78

0

0

0

495

66

0

78

56

78

0

0

0

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.MDR

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IVR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.EMDR

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSC

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID11

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID12

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DMAC target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.FUN

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIR

 $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIN$ 

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Name	Actual Value	Expected Value	Result
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	0	0	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	·
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	66	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	78	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	78	78	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	56	<b>V</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	897	897	· ·
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	98	98 66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78	78	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495	495	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66	66	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	78	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	66	66	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	78	78	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR	78	78	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL	495	495	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	56	56	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	897 98	98 98	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	78	78	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	495	495	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	78	78	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	78	78	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN	1	1	
target I2c SetStatus I2cRegPtr Cnt T str.DOUT	0	0	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78	78	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78	78	<b>~</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	495 56	495 56	<b>V</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	897	897	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98	98	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78	78	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78	78	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78 0	78 0	· ·
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	0	0	
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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~

Τ				
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	•

Test Step 1.2 (Repeat Count = 1)		
Name	Input Value	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	0	
DigColPsInt_Buffer_Cnt_M_u08[0]	123	
DigColPsInt_Buffer_Cnt_M_u08[1]	145	
DigColPsInt_Buffer_Cnt_M_u08[2]	200	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	
DigColPsInt_ColSnsrData_Cnt_M_u16	2767	
DigColPsInt_CurrentSlave_Cnt_M_u08	45	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_READ	
DigColPsInt_I2CHwCustData_Uls_M_u16	76	
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	77	
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	
DigColPsInt_NackOccured_Cnt_M_lgc	0	
DigColPsInt_PrevReqDataType_Cnt_M_u08	2	
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	
DigColPsInt_RecvdDataType_Cnt_M_u08	2	
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	
DigColPsInt_SpurSnsrData_Cnt_M_u16	564	
DigColPsInt_TransactionCnt_Cnt_M_u08	130	
Flags_Cnt_T_b16	32	
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str	
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str	
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str	
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str	
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str	
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str	
T_DataRegisters_Cnt_u08[0]	0	
T_DataRegisters_Cnt_u08[1]	32	

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Name	Input Value	
T_DataRegisters_Cnt_u08[2]	30	
T_DataRegisters_Cnt_u08[3]	36	
T_DataRegisters_Cnt_u08[4]	38	
T_DataRegisters_Cnt_u08[5]	34	
T_DataRegisters_Cnt_u08[6]	10	
T_DataRegisters_Cnt_u08[7]	12	
T_DataRegisters_Cnt_u08[8]	14	
i2cREG1_temp	target_i2cREG1_temp	
k ColSensorl2CAddress Cnt u08	7	
k_SpurSensorl2CAddress_Cnt_u08	123	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100	
target I2c GenStopCond I2cRegPtr Cnt T str.STR	7788	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767	
	9	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	
target I2c Send I2cRegPtr Cnt T str.CNT	564	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	
target I2c Send I2cRegPtr Cnt T str.MDR	2767	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	
	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR target_I2c Send_I2cRegPtr_Cnt_T_str.PSC	100	
· · ·		
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	88	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	100	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	2767	
	9	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	· · · · · · · · · · · · · · · · · · ·	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	

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Name	Input Value
	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3
target I2c SetRecv I2cRegPtr Cnt T str.DOUT	2
	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target I2c SetStatus I2cRegPtr Cnt T str.OAR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100
target I2c SetStatus I2cRegPtr Cnt T str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CNT	564
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100
target I2c SetupMasterReceive I2cReqPtr Cnt T str.PID11	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PiDI2	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	1
target I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	3
	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	2767
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	9

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Name target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR			
target 12c SetunMasterTransmit 12cDeaDtr Cnt T atr EMDD	Input Value		
targot_izo_oetupiviastei rransiliit_izoneynti_ont_l_Str.EMDK	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target i2cREG1 temp.OAR	3		
target i2cREG1 temp.IMR	100		
target_i2cREG1_temp.STR	7788		
target_i2cREG1_temp.CLKL	2767		
target_i2cREG1_temp.CLKH	556		
target i2cREG1 temp.CNT	564		
target i2cREG1 temp.DRR	88		
	3		
target_i2cREG1_temp.SAR	100		
target_i2cREG1_temp.DXR			
target_i2cREG1_temp.MDR	2767		
target_i2cREG1_temp.IVR	9		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	100		
target_i2cREG1_temp.PID11	556		
target_i2cREG1_temp.PID12	100		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	3		
	0		
target_i2cREG1_temp.ODR			
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL	0 3	Expected Value	Result
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name	0	Expected Value	Result
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	0 3 Actual Value 1	1	Result
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0]	0 3 Actual Value 1 12	1 12	Result
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	0 3 Actual Value 1 12 145	1 12 145	~
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]	0 3 Actual Value 1 12 145 200	1 12 145 200	Result
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc	0 3 Actual Value 1 12 145 200 0	1 12 145 200 0	***
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0 3 Actual Value 1 12 145 200 0	1 12 145 200 0	~
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc	0 3 Actual Value 1 12 145 200 0 0 0 0	1 12 145 200 0 0	
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16	0 3 Actual Value 1 12 145 200 0 0 0 0	1 12 145 200 0 0 0 2767	
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08	0 3  Actual Value 1 12 145 200 0 0 0 2767 7	1 12 145 200 0 0 0 2767	
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum	0 3  Actual Value 1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET	1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET	0
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16	0 3  Actual Value 1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76	1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76	0
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target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_I2CHvCustData_Uls_M_u16 DigColPsInt_I2CHvCustData_Uls_M_u16 DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I3CHwIncompleteCustData_Uls_M_u16 DigColPsInt_I3CHwIncompleteCustData_Uls_M_u16 DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvdDataType_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.JMR	0 3  Actual Value 1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0 0 0 2 1 564 130 1 1 1 3 100	1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0 0 0 2 1 564 130 1 1 1 3 100	
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SpurCustData_Type_Cnt_M_u08 DigColPsInt_SpurCustDataFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	0 3  Actual Value 1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0 0 0 2 1 564 130 1 1 1 3 100 7788	1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0 0 0 2 1 564 130 1 1 1 3 100 7788	
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustDatA_Uls_M_u16  DigColPsInt_I2CHwCustDatA_Uls_M_u16  DigColPsInt_I2CHwCustDatA_Uls_M_u16  DigColPsInt_I3CHwCustDatA_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)  I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	0 3  Actual Value  1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0 0 0 0 2 1 1 564 130 1 1 1 3 100 7788 2767 556	1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0 0 0 1 1 1 3 100 7788 2767 556	
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustDatA_UIs_M_u16  DigColPsInt_I2CHwCustDatA_UIs_M_u16  DigColPsInt_I2CHwCustDatA_UIs_M_u16  DigColPsInt_I3CHwIncompleteCustData_UIs_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)  I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	0 3  Actual Value 1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0 0 0 0 2 1 1 564 130 1 1 1 3 100 7788 2767 556 564	1 12 145 200 0 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0 0 0 1 1 1 3 100 7788 2767 556 564	
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_I3cHailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  Izc_Send(Length_Cnt_T_u32)  Izc_SetupMasterTransmit(DataLength_Cnt_T_u16)  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.JMR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	0 3  Actual Value 1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0 0 0 0 2 1 1 564 130 1 1 1 3 100 7788 2767 556 564 88	1 12 145 200 0 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0 0 0 1 1 1 3 100 7788 2767 556 564 88	
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)  I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	0 3  Actual Value 1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0 0 0 0 2 1 1 564 130 1 1 1 3 100 7788 2767 556 564 88 3	1 12 145 200 0 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0 0 0 1 1 1 3 100 7788 2767 556 564 88 3	
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_RecvOpercustDatFound_Cnt_M_lgc  DigColPsInt_RecvOpercustDatFound_Cnt_M_	0 3  Actual Value 1 12 145 200 0 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0 0 0 0 2 1 1 564 130 1 1 1 1 3 100 7788 2767 556 564 88 3 100	1 12 145 200 0 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0 0 0 1 1 1 3 100 7788 2767 556 564 88 3 100	
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)  I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	0 3  Actual Value 1 12 145 200 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0 0 0 0 2 1 1 564 130 1 1 1 3 100 7788 2767 556 564 88 3	1 12 145 200 0 0 0 0 2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0 0 0 1 1 1 3 100 7788 2767 556 564 88 3	

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9	9	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100	100	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556	556	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100	100	<b>~</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC	2	2	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>V</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	0	0	
target I2c SetStatus I2cRegPtr Cnt T str.CLR	1	1	<b>*</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100	100	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788	7788	✓
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	2767	2767	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556	556	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564	564	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88	88	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3	3	<b>✓</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	100	100	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	2767	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	9	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	100	✓
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	556	556	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	100	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>V</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	0	0	<b>~</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	3	3	<u> </u>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	100	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7788 2767	7788 2767	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	556 564	556 564	-
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	88	88	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100	100	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	2767	2767	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	100	100	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556	556	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	100	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c Send	1	I2c Send	1	<b>✓</b>

#### **Test Case 2: Boundary Test**

#### Description

```
Test Vector Description:
```

```
TS2.1Flags_Cnt_T_b16 = min
TS2.2Flags_Cnt_T_b16 = max
TS2.3Flags_Cnt_T_b16 = mid
TS2.4DigColPsInt_CurrentStepNo_Cnt_M_enum = min
TS2.5DigColPsInt_CurrentStepNo_Cnt_M_enum = max
TS2.6DigColPsInt_CurrentStepNo_Cnt_M_enum = mid
TS2.7k_SpurSensorl2CAddress_Cnt_u08 = min
TS2.7k_SpurSensorl2CAddress_Cnt_u08 = min
TS2.8k_SpurSensorl2CAddress_Cnt_u08 = mid
TS2.9k_SpurSensorl2CAddress_Cnt_u08 = mid
TS2.10DigColPsInt_Buffer_Cnt_M_u08[3] = min
TS2.11DigColPsInt_Buffer_Cnt_M_u08[3] = min
TS2.11DigColPsInt_Buffer_Cnt_M_u08[3] = mid
TS2.13DigColPsInt_InitFailedOnce_Cnt_M_lgc = min
TS2.14DigColPsInt_InitFailedOnce_Cnt_M_lgc = max
TS2.15DigColPsInt_SkipRegisterWrite_Cnt_M_lgc = min
TS2.16DigColPsInt_SkipRegisterWrite_Cnt_M_lgc = max
TS2.17DigColPsInt_SkipRegisterWrite_Cnt_M_lgc = min
TS2.18DigColPsInt_PrevReqDataType_Cnt_M_u08 = min
TS2.18DigColPsInt_PrevReqDataType_Cnt_M_u08 = min
TS2.21DigColPsInt_PrevReqDataType_Cnt_M_u08 = min
TS2.21DigColPsInt_TransactionCnt_Cnt_M_u08 = min
TS2.22DigColPsInt_TransactionCnt_Cnt_M_u08 = min
TS2.22DigColPsInt_TransactionCnt_Cnt_M_u08 = min
TS2.22BigColPsInt_TransactionCnt_Cnt_M_u08 = min
TS2.22bigColPsInt_TransactionCnt_Cnt_M_u08 = min
TS2.22bigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 = min
TS2.22bigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 = min
TS2.22DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 = min
TS2.23DigColPsInt_ColCustDatFound_Cnt_M_lgc = min
TS2.3DigColPsInt_OclCustDatFound_Cnt_M_lgc = min
TS2.3DigColPsInt_OclCustDatFound_Cnt_M_lgc = min
TS2.3DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 = min
TS2.3DigColPsInt_SpurCustDatFound_Cnt_M_lgc = min
TS2.35DigColPsInt_SpurCustDatFound_Cnt_M_lgc = min
```

Test Step 2.1 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	1
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12

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Digoon ant_interruptivatioation		
Name	Input Value	
T_DataRegisters_Cnt_u08[8]	14	
i2cREG1_temp	target_i2cREG1_temp	
k_ColSensorl2CAddress_Cnt_u08	9	
k_SpurSensorI2CAddress_Cnt_u08	10	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	
target I2c GenStopCond I2cRegPtr Cnt T str.STR	556	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	
target I2c GenStopCond I2cRegPtr Cnt T str.CLKH	1204	
target I2c GenStopCond I2cRegPtr Cnt T str.CNT	87	
target I2c GenStopCond I2cRegPtr Cnt T str.DRR	67	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	
	1204	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	66	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12		
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204 66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	66	
target_i2c_SetRecv_i2cRegPtr_Cnt_T_str.MDR	2309	
	5	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR		
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	

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Name	Input Value
	· ·
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target I2c SetStatus I2cRegPtr Cnt T str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target I2c SetStatus I2cRegPtr Cnt T str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target I2c SetStatus I2cRegPtr Cnt T str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target I2c SetStatus I2cRegPtr Cnt T str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	1
target 120 Octupinaster Fransillit IZCNegrti Olit i Str.FUN	

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DigCoPsint_AttempOccurForCustDatRead_Cnt_M_u088	DigColPsini_interruptiNotification			MACITAL
	Name	Input Value		
Supple     Desire     Desire   Desire     Desire     Desire     Desire     Desire     Desire   Desire     Desire     Desire     Desire     Desire     Desire   Desire     Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire   Desire				
Septemble   Description   Septemble   Se				
Target_10_5_SANQANSANT Transmit_Color_ColTart_COL_R  Target_10_SANQANSANT Transmit_Color_ColTart_ColR  Target_10_SSANQANSANT Transmit_Color_ColTart_ColR  Target_10_SSANQANSANT Transmit_Color_ColTart_ColR  Target_10_SSANQANT Transmit_Color_ColTart_ColR  Target_10_SSANQANT Transmit_Color_ColTart_ColR  Target_10_SSANQANT Transmit_Color_ColTarget_10  Target_10_SSANQANT Transmit_ColTarget_10  T				
signal Lies Selectivities Transmit Delegis Cort. T. st. PD. 3  ***Selection Cort. Cort. Selection Cort. Selec				
Image:   Companies   Compani	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
	target_i2cREG1_temp.OAR	55		
Image:	· · - · · · · · · · · · · · · · · · · ·			
Imput   Impu				
Simple   DRIFED   Name O.NT				
Sept   1968EG   1989 DRR				
Basel   Liberge   James   Ja				
Marget  ZOREGI   Semp DAR   2000				
Integral (200FGC)   Inte		66		
Integral_CAPERSI_Impn_PDFC	target_i2cREG1_temp.MDR	2309		
Image: Laper   Laper	target_i2cREG1_temp.IVR			
Image   L2RES   Image   DOT				
Image: Laper Col.   Image Double   September   Septe				
Image: LageREG1_temp CIR	target_i2cREG1_temp.DIN	2		
Images   LageREG1   Image   CIR	target_i2cREG1_temp.DOUT	3		
Larget_L2REG1_Lamp_ODR				
Larget_2/2REG1_temp.PD   3   3   3   3   3   3   3   3   3				
Name				
Name				
DigCoPsint_AttempOccurForCustDaiRead_Cnt_M_u088			Expected Value	Result
DigColPsint Buffer_Cnt_M_u08[0]			The second secon	Kesuit
DigCoPisht Buffer, Cnt, M_ u08[1]   20   20   20   20   20   20   20   2				•
DigCoPsint_BusbusySeqEror_Cnt_M_lgc         1         1         1           DigCoPsint_CntGraitOccurred_Cnt_M_lgc         1         1         1           DigCoPsint_CoutSubaroun_Cnt_M_u16         2309         2309         2309           DigCoPsint_CourtentStape_Cnt_M_u08         123         123         123           DigCoPsint_CurrentStape_Cnt_M_u08         123         123         123           DigCoPsint_CourtentStape_Cnt_M_u08         1NT_COMPLETE         NNT_COMPLETE         NNT_COMPLETE           DigCoPsint_LizCHwicostplate_Uis_M_u16         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         2         2         2         2         2         2 <td></td> <td>20</td> <td>20</td> <td>-</td>		20	20	-
DigColPsint_CndFailOccurred_Cnt_M_lgc         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         2         2         2         2	DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	•
DigCoPsint_ColCustDatFound_Cnt_M_lgc	DigColPsInt_BusBusySeqError_Cnt_M_lgc			•
DigCoPsint_CorsnstData_Cnt_M_u16				
DigColPsint_CurrentSlave_Cnt_M_u08				
DigColPsInt_CurrentStepNo_Cnt_M_enum         INIT_COMPLETE         INIT_COMPLETE           DigColPsInt_I2CHwCounsIdata_Uis_M_u16         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         2         1         1				
DigColPsint_I2CHwCustData_Uis_M_u16         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         2         2	·			
DigColPsInt_InitFailedOnce_Cnt_M_lgc				-
DigColPsInt_NackOccured_Cnt_M_lgc	DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	2	2	<b>✓</b>
DigColPsint_RecvOverrunError_Cnt_M_lgc	DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	<b>✓</b>
DigColPsint_RecvdDataType_Cnt_M_u08	DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_SpurCustDatFound_Cnt_M_u1ge				<b>→</b>
DigColPsInt_SpurSnsrData_Cnt_M_u16				
DigColPsInt_TransactionCnt_Cnt_M_u08				
12c_SetStatus(Status_Cnt_T_u16)				
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR       55       55         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR       66       66         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR       556       556         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL       2309       2309         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH       1204       1204         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT       87       87         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR       67       67         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR       67       67         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR       66       66         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR       66       66         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR       2309       2309         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR       3       3         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR       3       3         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PDD1       1204       1204         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12       66       66         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID42       66       66         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC       3       3         targ				
target_12c_GenStopCond_12cRegPtr_Cntstr.STR       556       556         target_12c_GenStopCond_12cRegPtr_Cntstr.CLKL       2309       2309         target_12c_GenStopCond_12cRegPtr_Cntstr.CLKH       1204       1204         target_12c_GenStopCond_12cRegPtr_Cntstr.CNT       87       87         target_12c_GenStopCond_12cRegPtr_Cntstr.DRR       67       67         target_12c_GenStopCond_12cRegPtr_Cntstr.SAR       55       55         target_12c_GenStopCond_12cRegPtr_Cntstr.DXR       66       66         target_12c_GenStopCond_12cRegPtr_Cntstr.MDR       2309       2309         target_12c_GenStopCond_12cRegPtr_Cntstr.MDR       5       5         target_12c_GenStopCond_12cRegPtr_Cntstr.WDR       5       5         target_12c_GenStopCond_12cRegPtr_Cntstr.EMDR       3       3         target_12c_GenStopCond_12cRegPtr_Cntstr.PIDDR       3       3         target_12c_GenStopCond_12cRegPtr_Cntstr.PID11       1204       1204         target_12c_GenStopCond_12cRegPtr_Cntstr.PID12       66       66         target_12c_GenStopCond_12cRegPtr_Cntstr.DMAC       3       3         target_12c_GenStopCond_12cRegPtr_Cntstr.DMAC       3       3         target_12c_GenStopCond_12cRegPtr_Cntstr.DMAC       3       3         target_12c_GenStopCond_12cR				-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL       2309       2309         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH       1204       1204         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT       87       87         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR       67       67         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR       55       55         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR       66       66         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR       2309       2309         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR       5       5         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC       66       66         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11       1204       1204         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12       66       66         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR       1       1	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target   2c GenStopCond   12cRegPtr Cnt_T str.CLKH       1204       1204         target   2c GenStopCond   12cRegPtr Cnt_T str.CNT       87       87         target   2c GenStopCond   12cRegPtr Cnt_T str.DRR       67       67         target   2c GenStopCond   12cRegPtr Cnt_T str.DRR       55       55         target   12c GenStopCond   12cRegPtr_Cnt_T str.DXR       66       66         target   12c GenStopCond   12cRegPtr_Cnt_T str.MDR       2309       2309         target   12c GenStopCond   12cRegPtr_Cnt_T str.IVR       5       5         target   12c GenStopCond   12cRegPtr_Cnt_T str.EMDR       3       3         target   12c GenStopCond   12cRegPtr_Cnt_T str.PSC       66       66         target   12c GenStopCond   12cRegPtr_Cnt_T str.PID11       1204       1204         target   12c GenStopCond   12cRegPtr_Cnt_T str.PID12       66       66         target   12c GenStopCond   12cRegPtr_Cnt_T str.PIDAC       3       3         target   12c GenStopCond   12cRegPtr_Cnt_T str.PUN       1       1         target   12c GenStopCond   12cRegPtr_Cnt_T str.PUN       1       1         target   12c GenStopCond   12cRegPtr_Cnt_T str.PUN       1       1         target   12c GenStopCond   12cRegPtr_Cnt_T str.DIR       1       1	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT       87       87         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR       67       67         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR       55       55         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR       66       66         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR       2309       2309         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR       5       5         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC       66       66         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11       1204       1204         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12       66       66         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR       1       1	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL			<b>✓</b>
target   2c GenStopCond   12cRegPtr Cnt T str.DRR       67       67         target   12c GenStopCond   12cRegPtr Cnt T str.DRR       55       55         target   12c GenStopCond   12cRegPtr Cnt T str.DXR       66       66         target   12c GenStopCond   12cRegPtr Cnt T str.MDR       2309       2309         target   12c GenStopCond   12cRegPtr Cnt T str.IVR       5       5         target   12c GenStopCond   12cRegPtr Cnt T str.EMDR       3       3         target   12c GenStopCond   12cRegPtr Cnt T str.PSC       66       66         target   12c GenStopCond   12cRegPtr Cnt T str.PID11       1204       1204         target   12c GenStopCond   12cRegPtr Cnt T str.PID12       66       66         target   12c GenStopCond   12cRegPtr Cnt T str.PIDAC       3       3         target   12c GenStopCond   12cRegPtr Cnt T str.PUN       1       1         target   12c GenStopCond   12cRegPtr Cnt T str.PUN       1       1         target   12c GenStopCond   12cRegPtr Cnt T str.PUN       1       1				
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR       55       55         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR       66       66         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR       2309       2309         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR       5       5         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC       66       66         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11       1204       1204         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12       66       66         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR       1       1				
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR       66       66       66         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR       2309       2309         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR       5       5         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC       66       66         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11       1204       1204         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12       66       66         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR       1       1				
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR       2309       2309         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR       5       5         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR       3       3         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC       66       66         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11       1204       1204         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12       66       66         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC       3       3         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FUN       1       1         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR       1       1				
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR       5       5         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC       66       66         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11       1204       1204         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12       66       66         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR       1       1				
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC       66       66         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11       1204       1204         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12       66       66         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR       1       1				
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11 1204 1204 1204 target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12 66 66 starget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC 3 3 3 starget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1			5	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC 3 3 3 4 4 arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN 1 1 1 1 4 arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	5 3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	5 3 66	3 66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR 1	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11 target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	5 3 66 1204 66	3 66 1204 66	•
	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11 target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12 target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	5 3 66 1204 66 3	3 66 1204 66 3	
	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11 target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12 target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	5 3 66 1204 66 3	3 66 1204 66 3	

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Name	Actual Value	Expected Value	Resul
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1 2	1 2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	66 2309	66 2309	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target I2c Send I2cRegPtr Cnt T str.PSC	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1 2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	
target I2c SetRecv I2cRegPtr Cnt T str.DMAC	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3 55	3 55	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR	66	66	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR	556	556	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	,
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204 66	1204 66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12 target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✓
target I2c SetStatus I2cRegPtr Cnt T str.ODR	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.STR	556	556	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SAR	55	55	<u> </u>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	
target I2c SetupMasterReceive I2cReqPtr Cnt T str.PID11	1204	1204	· ·
	66	66	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC			
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR			
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	2	2	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	3	3	<b>~</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>~</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	556	556	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>~</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✓
$target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DOUT$	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✓

Т				V
Actual Function	Count	Expected Function	Count	Result
I2c_SetStatus	1	I2c_SetStatus	1	~

Test Step 2.2 (Repeat Count = 1)		✓
Name	Input Value	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2	
DigColPsInt_Buffer_Cnt_M_u08[0]	22	
DigColPsInt_Buffer_Cnt_M_u08[1]	44	
DigColPsInt_Buffer_Cnt_M_u08[2]	55	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	

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Name	Input Value
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	495
DigColPsInt_CurrentSlave_Cnt_M_u08	100
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	7
DigColPsInt I2CHwIncompleteCustData Uls M u16	5
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
	1
DigColPoInt_NackOccured_Cnt_M_lgc	2
DigColPsInt_PrevReqDataType_Cnt_M_u08	
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SkipRegisterWrite_Cnt_M_Igc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	897
DigColPsInt_TransactionCnt_Cnt_M_u08	20
Flags_Cnt_T_b16	64
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
	36
T_DataRegisters_Cnt_u08[3]	
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	14
k_SpurSensorI2CAddress_Cnt_u08	20
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	56
	897
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	0
	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	78

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		( 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1
Name	Input Value	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	78	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0 78	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	78 56	
target I2c SetRecv I2cRegPtr Cnt T str.PID12	78	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	Ō	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	78	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	78	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	495	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	56	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	897	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	98	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	78	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	495	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	78	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11 target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	56 78	
	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	
target I2c SetStatus I2cRegPtr_Cnt_T_str.PUN target I2c SetStatus I2cRegPtr Cnt T str.DIR	0	
target I2c SetStatus I2cRegPtr_Cnt_T_str.DIN	1	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	0	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66	

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Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID12	78		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIR	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	0		
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	78		
	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	495		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL			
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	56		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	897		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	98		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD			
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	0		
target_i2cREG1_temp.OAR	66		
target_i2cREG1_temp.IMR	78		
target_i2cREG1_temp.STR	78		
target_i2cREG1_temp.CLKL	495		
target_i2cREG1_temp.CLKH	56		
target_i2cREG1_temp.CNT	897		
target_i2cREG1_temp.DRR	98		
target_i2cREG1_temp.SAR	66		
target_i2cREG1_temp.DXR	78		
target_i2cREG1_temp.MDR	495		
target_i2cREG1_temp.IVR	66		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	78		
target_i2cREG1_temp.PID11	56		
target i2cREG1 temp.PID12	78		
target_i2cREG1_temp.DMAC	0		
target i2cREG1 temp.FUN	0		
target i2cREG1_temp.DIR	0		
target i2cREG1 temp.DIN	1		
	0		
target_i2cREG1_temp.DOUT	0		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR			
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Resul
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2	2	•
DigColPsInt_Buffer_Cnt_M_u08[0]	22	22	•
DigColPsInt_Buffer_Cnt_M_u08[1]	44	44	•
DigColPsInt_Buffer_Cnt_M_u08[2]	55	55	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	•
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	

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DigColPsInt\_ColSnsrData\_Cnt\_M\_u16

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Name	Actual Value	Expected Value	Result
DigColPsInt_CurrentSlave_Cnt_M_u08	100	100	•
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ	INIT_SENSOR1_READERROR_READ	<b>✓</b>
DigColPsInt_I2CHwCustData_Uls_M_u16	7	7	•

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Name		Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC		78	78	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11		56	56	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12		78	78	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC		0	0	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN		0	0	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR		0	0	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN		1	1	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT		0	0	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET		0	0	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR		0	0	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR		1	1	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD		0	0	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL		0	0	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR		66	66	✓
target_12c_6e5e111000000000000000000000000000000000	It 0 ti	Re <b>78</b> _I2cRegPtr_	708 tRecv_	tRecvuptNotificat=

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	•

T				V
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 2.3 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	15
DigColPsInt_Buffer_Cnt_M_u08[2]	16
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	566
DigColPsInt_CurrentSlave_Cnt_M_u08	110
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	7
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	8
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	129
DigColPsInt_TransactionCnt_Cnt_M_u08	30
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
l2c_Send(l2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c SetRecv(I2cRegPtr Cnt T str)	target I2c SetRecv I2cRegPtr Cnt T str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c SetupMasterTransmit(I2cRegPtr Cnt T str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T DataRegisters Cnt u08[2]	30
T DataRegisters Cnt u08[3]	36
T DataRegisters Cnt u08[4]	38
T DataRegisters Cnt u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T DataRegisters Cnt u08[7]	10
	14
T_DataRegisters_Cnt_u08[8]	
2cREG1_temp	target_i2cREG1_temp
<_ColSensorI2CAddress_Cnt_u08	19
<_SpurSensorI2CAddress_Cnt_u08	30
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567

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Name	Input Value	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	4444 566	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	4466	
	129	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	6	
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	567	
target I2c Send I2cRegPtr Cnt T str.DXR	44	
target I2c Send I2cRegPtr Cnt T str.MDR	566	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	567	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129 6	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR		
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	567 44	
target_l2c_SetRecv_l2cRegPtr_Cnt_1_str.DXR target_l2c SetRecv_l2cRegPtr_Cnt_T_str.MDR	566	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.lVR	554	
target I2c SetRecv I2cRegPtr Cnt T str.EMDR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	
target I2c SetRecv I2cRegPtr Cnt T str.PID11	4466	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	

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Name	Input Value
	6
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target I2c SetStatus I2cRegPtr Cnt T str.PSC	44
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DXR	44
	566
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
	1
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	129
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	6
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	1
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target i2cREG1 temp.CLKL	566



Name	Input Value		
target_i2cREG1_temp.CLKH	4466		
target_i2cREG1_temp.CNT	129		
target_i2cREG1_temp.DRR target_i2cREG1_temp.SAR	6 567		
target i2cREG1_temp.DXR	44		
target i2cREG1 temp.MDR	566		
target_i2cREG1_temp.IVR	554		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	44		
target_i2cREG1_temp.PID11	4466		
target_i2cREG1_temp.PID12	44		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR	2		
target i2cREG1 temp.DIN	0		
target i2cREG1 temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3	1	1
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3 10	3 10	· ·
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	15	15	
DigColPsInt_Buffer_Cnt_M_u08[2]	16	16	
DigColPsInt BusBusySeqError Cnt M Igc	0	0	-
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	-
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	566	566	~
DigColPsInt_CurrentSlave_Cnt_M_u08	110	110	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_SETREG	INIT_SENSOR1_READEXTERR_SETREG	~
DigColPsInt_I2CHwCustData_Uls_M_u16	7	7	~
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	8	8	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	· ·
DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	
DigColPsInt_RecvdDataType_Cnt_M_u08	2	2	-
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	-
DigColPsInt_SpurSnsrData_Cnt_M_u16	129	129	-
DigColPsInt_TransactionCnt_Cnt_M_u08	30	30	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566	566	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	129	129	<b>*</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR	6	6	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	567	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	44	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	566	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	44	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	2	2	\ \ \ \ \ \ \
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN	0	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	~
	44	44	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR			<b> </b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	566 4466	566 4466	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	7

2014-10-14, 23:42:41+0530



Imaged   Dis. Seried   Jack Press   Jack P	Name	Actual Value	Expected Value	Result
Langer (Lie, Server) (Lie, Ser				~
Laged 102 Seed Edicagnic Out 1 at INCR  102 (102 Seed Edicagnic Out 1 at INCR  103 (102 Seed 126 Seed 126 Seed Out 126 Seed 126 S				~
Sept   120   Sept   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   200   20				<b>✓</b>
Hangel, D.S., Send, Distrigating, D.C.   Jan 1901 Hangel, D.S., Send, Distrigating, Co.   Jan 1901 Hangel, D.S., Send, Distrigating, Co.   Jan 1901 Hangel, D.S., Send, Distrigating, Co.   Jan 1900 Hangel, D.S., Send, Libridgating, Co.   Jan 1900 Hangel, D.S., Sender, Libridgating, Co.   Jan				~
Hange, Die, Sone, Definging, Dutt Jan Pilot 1 Hange, Die, Sone, Definging, Dutt Jan Die Dutt. 1 Hange, Die, Sone, Definging, Dutt Jan Die Dutt. 1 Hange, Die, Sone, Definging, Dutt Jan Die Dutt. 1 Hange, Die, Sone, Definging, Dutt Jan Die Dutt. 1 Hange, Die, Sone, Definging, Dutt Jan Die Dutt. 1 Hange, Die, Sone, Definging, Dutt Jan Die Dutt. 1 Hange, Die, Sone, Definging, Dutt Jan Die Dutt. 1 Hange, Die, Sone, Definging, Dutt Jan Die Dutt. 1 Hange, Die, Sone, Definging, Dutt Jan Die Dutt. 1 Hange, Die, Sone, Definging, Dutt Jan Die Dutt. 1 Hange, Die, Sone, Definging, Dutt Jan Die Dutt. 1 Hange, Die, Sone, Definging, Dutt Jan Die Dutt. 1 Hange, Die, Sone, Definging, Dutt Jan Die Dutt. 1 Hange, Die, Sone, Definging, Dutt Jan Die Dutt. 1 Hange, Die, Sone, Definging, Dutt Jan Die Dutt. 1 Hange, Die, Sone, Definging, Dutt Jan Die Dutt. 1 Hange, Die, Sone, Definging, Dutt Jan Die Dutt. 1 Hange, Die, Sone, Definging, Dutt Jan Die Dutt. 1 Hange, Die, Sone, Definging, Dutt Jan Die Dutt. 1 Hange, Die, Sone, Definging, Dutt Jan Die Dutt. 1 Hange, Die, Sone, Definging, Dutt Jan Die Dutt. 1 Hange, Die, Sone, Definging, Dutt Jan Die Dutt. 1 Hange, Die, Sone, Definging, Dutt Jan Die Dutt. 1 Hange, Die, Sone, Definging, Dutt Jan Die Dutt. 1 Hange, Die, Sone, Definging, Dutt Jan Die Dutt. 1 Hange, Die, Sone, Definging, Dutt Jan Die Dutt. 1 Hange, Die, Sone, Definging, Dutt Jan Die Dutt. 1 Hange, Die, Sone, Definging, Dutt Jan Die Dutt. 1 Hange, Die, Sone, Definging, Dutt Jan Die Dutt. 1 Hange, Die, Sone, Definging, Dutt Jan Die Dutt. 1 Hange, Die, Sone, Definging, Dutt Jan Die Dutt. 1 Hange, Die, Sone, Definging, Dutt Jan Die Dutt. 1 Hange, Die, Sone, Definging, Dutt Jan Die Dutt. 1 Hange, Die, Sone, Definging, Dutt Jan Di	target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR			<b>✓</b>
Mapper   Dec. Service   Control   March   Ma	target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	~
Target July Served	target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11			~
Laged 12.5 and 120 Pept Port T. HETUN 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	<b>✓</b>
	target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
	target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
	target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>~</b>
Langer 12.5 Send CartheyPro CRT 1 at SET   1   1   1   1   1   1   1   1   1	target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	✓
Larget ID. Series (2018)   Cont.   Taricum   2	target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
Langer 12.5 Send (2016)PIF CRIT_1 SENDOR   10   10   10   10   10   10   10   10	target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
September   Color	target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
Septemble   Decemble	target I2c Send I2cRegPtr Cnt T str.ODR	0	0	<b>✓</b>
		3	3	<b>✓</b>
Insert   D.S. Selfsen, D.R. Regift   CHT_1 to DAR   14			3	~
Integral   22, Selfeco   22Regiffer   CH_T_str   MR				<b>✓</b>
Impact   12.8. Selfecor   28.RepPir CHT_INF CHT	· · · · · - · · - · · · · · · · · · · · · · · · · · · · ·			
Imprel 125 SePrice   Jackspric Cot   1 st CULK   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566   566				<b>✓</b>
Singer  Lie, Selfeco, UzReaght, Colt.   List CNT   129   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   120   1				
Image:   125   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   126   1				
Image   125 SetReory   ZeckegePtr   Cett   Tat DRR   6   8   9   9   9   9   9   9   9   9   9				
Images   126, Selfect   Dishelphi Colt   1 st DNR				-
Integral Lib. Selfecy   Zickep Pt Coll   List DNR   44   44   44   44   44   44   44				
target_Lize_Selfecv_LizeRepPir_Cnt_T_str_NDR         556           larget_Lize_Selfecv_LizeRepPir_Cnt_T_str_NDR         554           target_Lize_Selfecv_LizeRepPir_Cnt_T_str_NDR         1           target_Lize_Selfecv_LizeRepPir_Cnt_T_str_NDR         1           target_Lize_Selfecv_LizeRepPir_Cnt_T_str_NDDID1         446           target_Lize_Selfecv_LizeRepPir_Cnt_T_str_NDDID1         446           target_Lize_Selfecv_LizeRepPir_Cnt_T_str_NDDID1         44           target_Lize_Selfecv_LizeRepPir_Cnt_T_str_NDDID1         44           target_Lize_Selfecv_LizeRepPir_Cnt_T_str_NDDID1         1           target_Lize_Selfecv_LizeRepPir_Cnt_T_str_NDDID1         1           target_Lize_Selfecv_LizeRepPir_Cnt_T_str_NDDID1         0           target_Lize_Selfecv_LizeRepPir_Cnt_T_str_NDDID1         0           target_Lize_Selfecv_LizeRepPir_Cnt_T_str_NDDID1         1           target_Lize_Selfecv_LizeRepPir_Cnt_T_str_NDDID1         1           target_Lize_Selfecv_LizeRepPir_Cnt_T_str_NDDID1         1           target_Lize_Selfecv_LizeRepPir_Cnt_T_str_NDDID1         0           target_Lize_Selfecv_LizeRepPir_Cnt_T_str_NDDID1         0           target_Lize_Selfecv_LizeRepPir_Cnt_T_str_NDDID1         0           target_Lize_Selfecv_LizeRepPir_Cnt_T_str_NDDID1         0           target_Lize_Selfecv_LizeRepPir_Cnt_T_str_NDDID1         3 </td <td></td> <td></td> <td></td> <td>-</td>				-
Integral Los Selfkeov   Jocksepht Cont   T. str. DRI				
target L2s. SerReov J2cRepPr Cnt T_str ENDR 1 target L2s. SerReov J2cRepPr Cnt T_str ENDR 4 44 44 1 target L2s. SerReov J2cRepPr Cnt T_str PDC 44 1 target L2s. SerReov J2cRepPr Cnt T_str PDC 44 1 target L2s. SerReov J2cRepPr Cnt T_str PDC 44 1 target L2s. SerReov J2cRepPr Cnt T_str PDC 44 1 target L2s. SerReov J2cRepPr Cnt T_str DDC 41 1 target L2s. SerReov J2cRepPr Cnt T_str DDC 41 1 target L2s. SerReov J2cRepPr Cnt T_str DDC 41 1 target L2s. SerReov J2cRepPr Cnt T_str DDC 41 1 target L2s. SerReov J2cRepPr Cnt T_str DDC 42 2 target L2s. SerReov J2cRepPr Cnt T_str DDC 42 2 target L2s. SerReov J2cRepPr Cnt T_str DDC 42 1 target L2s. SerReov J2cRepPr Cnt T_str DDC 41 1 target L2s. SerReov J2cRepPr Cnt T_str DDC 41 1 target L2s. SerReov J2cRepPr Cnt T_str DDC 41 1 target L2s. SerReov J2cRepPr Cnt T_str DDC 41 1 target L2s. SerReov J2cRepPr Cnt T_str DDC 51 1 target L2s. SerReov J2cRepPr Cnt T_str DDC 51 2 target L2s. SerReov J2cRepPr Cnt T_str DDC 51 3 3 3 3 4 target L2s. SerReov J2cRepPr Cnt T_str DDC 51 3 3 3 3 4 target L2s. SerReov J2cRepPr Cnt T_str DDC 53 3 3 3 4 target L2s. SerReov J2cRepPr Cnt T_str DDC 53 3 3 3 4 target L2s. SerReov J2cRepPr Cnt T_str DDC 54 567 567 567 567 567 567 567 567 567 567				~
Bargel L2e SelReov   22RepPt CntT   str PSC	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target   Ze_SetReov_ ZeRegPtv_CntstrD1012	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>✓</b>
target 122_ SelRecv_122RegPtr_CntT_str.PID12         44           darget 122_ SelRecv_122RegPtr_CntT_str.DMAC         1         1           target 122_ SelRecv_122RegPtr_CntT_str.DMN         1         1           target 122_ SelRecv_122RegPtr_CntT_str.DIN         0         0           target 122_ SelRecv_122RegPtr_CntT_str.DINN         0         0           target 122_ SelRecv_122RegPtr_CntT_str.DOUT         1         1           target 122_ SelRecv_122RegPtr_CntT_str.DOUT         1         1           target 122_ SelRecv_122RegPtr_CntT_str.DOOR         0         0           target 122_ SelRecv_122RegPtr_CntT_str.DOOR         0         0           target 122_ SelRecv_122RegPtr_CntT_str.DOR         3         3           target 122_ SelRecv_122RegPtr_CntT_str.DR         3         3           target 122_ SelRecv_122RegPtr_CntT_str.DR         3         3           target 122_ SelRecv_122RegPtr_CntT_str.DR         44         44           target 122_ SelRecv_122RegPtr_CntT_str.DR	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	✓
	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	<b>~</b>
Integel Lip SetRevy   ZeRegPtr Cnt_T str FUN	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	✓
target_12c_SetRecv_12cRegPtr_Cnt_T str.DIR	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	✓
	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_12e_SetRecv_12cRegPtr_Cnt_T_str.DOUT 1	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	✓
target   2c, SetRecy   2cRepPtr Cnt, T, str SET	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	✓
target_12c_SetRecv_12cRegPtr_Cnt_T_str.ORR         2           target_12c_SetRecv_12cRegPtr_Cnt_T_str.ORR         0           1 target_12c_SetRecv_12cRegPtr_Cnt_T_str.DR         3           1 target_12c_SetRecv_12cRegPtr_Cnt_T_str.DR         3           1 target_12c_SetRecv_12cRegPtr_Cnt_T_str.DR         567           1 target_12c_SetStatus_12cRegPtr_Cnt_T_str.OAR         567           1 target_12c_SetStatus_12cRegPtr_Cnt_T_str.STR         444           4 target_12c_SetStatus_12cRegPtr_Cnt_T_str.STR         4444           4 target_12c_SetStatus_12cRegPtr_Cnt_T_str.CtKL         566           566         566           4 target_12c_SetStatus_12cRegPtr_Cnt_T_str.CtKL         4466           4 target_12c_SetStatus_12cRegPtr_Cnt_T_str.DRT         6           6 c_starget_12c_SetStatus_12cRegPtr_Cnt_T_str.DRT         6           6 c_starget_12c_SetStatus_12cRegPtr_Cnt_T_str.DAT         44           4 target_12c_SetStatus_12cRegPtr_Cnt_T_str.DAT         1           4 target_12c_	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
target_12c_SelRecv_12cRegPtr_Cnt_T_str.ORR	target I2c SetRecv I2cRegPtr Cnt T str.SET	1	1	✓
target   I2c, SetRecv   I2cRegPtr_Cnt_Tstr.ODR		2	2	<b>✓</b>
target_l2c_SelRecv_l2cRegPtr_Cnt_Tstr.PD         3         3           target_l2c_SelRecv_l2cRegPtr_Cnt_Tstr.PSL         3         3           target_l2c_SelStatus_l2cRegPtr_Cnt_Tstr.PSL         3         3           target_l2c_SelStatus_l2cRegPtr_Cnt_Tstr.DNA         567         557           target_l2c_SelStatus_l2cRegPtr_Cnt_Tstr.DNR         444         44           target_l2c_SelStatus_l2cRegPtr_Cnt_Tstr.Str.SNR         4444         444           target_l2c_SelStatus_l2cRegPtr_Cnt_Tstr.CLKL         566         566           target_l2c_SelStatus_l2cRegPtr_Cnt_Tstr.CLKH         4466         4466           target_l2c_SelStatus_l2cRegPtr_Cnt_Tstr.CLKH         4466         4466           target_l2c_SelStatus_l2cRegPtr_Cnt_Tstr.CNT         129         129           target_l2c_SelStatus_l2cRegPtr_Cnt_Tstr.CNT         6         6           target_l2c_SelStatus_l2cRegPtr_Cnt_Tstr.DNR         44         44           target_l2c_SelStatus_l2cRegPtr_Cnt_Tstr.DNR         566         566           target_l2c_SelStatus_l2cRegPtr_Cnt_Tstr.DNR         566         566           target_l2c_SelStatus_l2cRegPtr_Cnt_Tstr.DNR         554         44           target_l2c_SelStatus_l2cRegPtr_Cnt_Tstr.DNC         1         1           target_l2c_SelStatus_l2cRegPtr_Cnt_Tstr.DNAC         1         1			0	<b>✓</b>
target_ 2c_SetRacv_ 2cRegPtr_Cnt_Tstr.PSL   3   3   3   target_ 2c_SetStatus_ 2cRegPtr_Cnt_Tstr.DAR   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567   567				_
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR         567         567           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR         44         44           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR         444         444           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL         566         566           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH         4466         4466           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRT         129         129           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR         6         6           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR         6         6           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR         44         44           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR         44         44           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR         566         566           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR         1         1           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR         1         1           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIT         446         44           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIT         446         44           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN         1         1           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN         0				<b>✓</b>
target_12c_SetStatus_12cRegPtr_Cnt_T_str.IMR         44         44           target_12c_SetStatus_12cRegPtr_Cnt_T_str.STR         4444         4444           target_12c_SetStatus_12cRegPtr_Cnt_T_str.CLKL         566         566           target_12c_SetStatus_12cRegPtr_Cnt_T_str.CLKH         4466         4466           target_12c_SetStatus_12cRegPtr_Cnt_T_str.CNT         129         129           target_12c_SetStatus_12cRegPtr_Cnt_T_str.DRR         6         6           target_12c_SetStatus_12cRegPtr_Cnt_T_str.DXR         44         44           target_12c_SetStatus_12cRegPtr_Cnt_T_str.DXR         44         44           target_12c_SetStatus_12cRegPtr_Cnt_T_str.DXR         44         44           target_12c_SetStatus_12cRegPtr_Cnt_T_str.DXR         566         566           target_12c_SetStatus_12cRegPtr_Cnt_T_str.DXR         554         554           target_12c_SetStatus_12cRegPtr_Cnt_T_str.DXR         44         44           target_12c_SetStatus_12cRegPtr_Cnt_T_str.PDT1         4466         446           target_12c_SetStatus_12cRegPtr_Cnt_T_str.DID11         4466         4486           target_12c_SetStatus_12cRegPtr_Cnt_T_str.DIN         1         1           target_12c_SetStatus_12cRegPtr_Cnt_T_str.DIN         1         1           target_12c_SetStatus_12cRegPtr_Cnt_T_str.DIN         0 </td <td></td> <td></td> <td>i i</td> <td>_</td>			i i	_
target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.CLKL         566         566           target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.CLKL         566         566           target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.CLKL         4466         4466           target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.CNT         129         129           target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DRR         6         6           target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DXR         44         44           target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DXR         44         44           target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DXR         44         44           target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DXR         566         566           target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DXR         56         566           target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DNR         56         566           target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DND         1         1           target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DND         1         1           target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DNAC         1         1           target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DIN         1         1           target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DIN         0         0           target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DN         0         0				_
target_12c_SetStatus_12cRegPtr_Cnt_T_str.CLKL         566         566           target_12c_SetStatus_12cRegPtr_Cnt_T_str.CLKH         4466         4466           target_12c_SetStatus_12cRegPtr_Cnt_T_str.CNT         129         129           target_12c_SetStatus_12cRegPtr_Cnt_T_str.DRR         6         6           target_12c_SetStatus_12cRegPtr_Cnt_T_str.DRR         6         6           target_12c_SetStatus_12cRegPtr_Cnt_T_str.DXR         44         44           target_12c_SetStatus_12cRegPtr_Cnt_T_str.DXR         44         44           target_12c_SetStatus_12cRegPtr_Cnt_T_str.DXR         566         566           target_12c_SetStatus_12cRegPtr_Cnt_T_str.DXR         554         554           target_12c_SetStatus_12cRegPtr_Cnt_T_str.DRR         1         1           target_12c_SetStatus_12cRegPtr_Cnt_T_str.PID12         44         44           target_12c_SetStatus_12cRegPtr_Cnt_T_str.PID12         44         44           target_12c_SetStatus_12cRegPtr_Cnt_T_str.DMAC         1         1           target_12c_SetStatus_12cRegPtr_Cnt_T_str.DIN         1         1           target_12c_SetStatus_12cRegPtr_Cnt_T_str.DIN         2         2           target_12c_SetStatus_12cRegPtr_Cnt_T_str.DUT         1         1           target_12c_SetStatus_12cRegPtr_Cnt_T_str.DUT         1         1				
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH         4466         4466           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT         129         129           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR         6         6           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR         44         44           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR         44         44           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DNR         566         566           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DNR         554         554           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR         1         1           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR         1         1           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11         4466         4466           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DID12         44         44           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DNAC         1         1           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN         1         1           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN         0         0           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOT         1         1           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOT         1         1           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOR         0				•
target_!2e_SetStatus_!2eRegPtr_Cnt_T_str.CNT         129         129           target_!2e_SetStatus_!2eRegPtr_Cnt_T_str.DRR         6         6           target_!2e_SetStatus_!2eRegPtr_Cnt_T_str.SAR         567         567           target_!2e_SetStatus_!2eRegPtr_Cnt_T_str.DXR         44         44           target_!2e_SetStatus_!2eRegPtr_Cnt_T_str.MDR         566         566           target_!2e_SetStatus_!2eRegPtr_Cnt_T_str.EMDR         554         554           target_!2e_SetStatus_!2eRegPtr_Cnt_T_str.EMDR         1         1           target_!2e_SetStatus_!2eRegPtr_Cnt_T_str.PSC         44         44           target_!2e_SetStatus_!2eRegPtr_Cnt_T_str.PID11         4466         4466           target_!2e_SetStatus_!2eRegPtr_Cnt_T_str.PID12         44         44           target_!2e_SetStatus_!2eRegPtr_Cnt_T_str.DMAC         1         1           target_!2e_SetStatus_!2eRegPtr_Cnt_T_str.DIN         1         1           target_!2e_SetStatus_!2eRegPtr_Cnt_T_str.DIN         0         0           target_!2e_SetStatus_!2eRegPtr_Cnt_T_str.DIN         0         0           target_!2e_SetStatus_!2eRegPtr_Cnt_T_str.SET         1         1           target_!2e_SetStatus_!2eRegPtr_Cnt_T_str.DR         0         0           target_!2e_SetStatus_!2eRegPtr_Cnt_T_str.DR         0         0 <td></td> <td></td> <td></td> <td>. 4</td>				. 4
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR         6         6           target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR         567         567           target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR         44         44           target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR         566         566           target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR         554         554           target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR         1         1           target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11         4466         446           target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12         44         44           target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC         1         1           target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN         1         1           target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR         2         2           target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR         2         2           target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT         1         1           target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT         1         1           target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CDR         2         2           target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DDR         0         0           target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DAR         3         3				
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR       567       567         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR       44       44         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMR       566       566         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.NVR       554       554         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR       1       1         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC       44       44         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PiD11       4466       446         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PiD12       44       44         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC       1       1         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN       1       1         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN       2       2         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN       0       0         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT       1       1         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DDUT       1       1         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DDR       0       0         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DDR       0       0         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DDR       3       3         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DAR       567				
target_12c_SetStatus_12cRegPtr_Cnt_T_str.DXR				<b>Y</b>
target_l2c_SetStatus_l2cRegPtr_CntT_str.MDR       566       566         target_l2c_SetStatus_l2cRegPtr_CntT_str.IVR       554       554         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.BMDR       1       1         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PDC       44       44         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11       4466       4466         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12       44       44         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC       1       1         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN       1       1         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR       2       2         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN       0       0         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DUT       1       1         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DUT       1       1         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET       1       1         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR       2       2         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DDR       0       0         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DAR       3       3         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DAR       567       567         target_l2c_SetUpMasterReceive_l2cRegPtr_Cnt_T_str.DAR <td< td=""><td></td><td></td><td></td><td></td></td<>				
target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.IVR       554       554         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.EMDR       1       1         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.PSC       44       44         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.PID11       4466       4466         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.PID12       44       44         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DMAC       1       1         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DN       1       1         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DIR       2       2         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DIN       0       0         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DOUT       1       1         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DOUT       1       1         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.CLR       2       2         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.ODR       0       0         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.ODR       0       0         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DOR       3       3         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.OAR       567       567         target_!2c_SetUpMasterReceive_!2cRegPtr_Cnt_T_str.STR       444       444         target_!2c_SetUpMasterReceive_!2cRegPtr_Cnt_T_str.STR <td></td> <td></td> <td></td> <td><b>Y</b></td>				<b>Y</b>
target_!2c_SetStatus_!2cRegPtr_Cntstr.EMDR       1       1         target_!2c_SetStatus_!2cRegPtr_Cntstr.PSC       44       44         target_!2c_SetStatus_!2cRegPtr_Cntstr.PID11       4466       4466         target_!2c_SetStatus_!2cRegPtr_Cntstr.PID12       44       44         target_!2c_SetStatus_!2cRegPtr_Cntstr.DMAC       1       1         target_!2c_SetStatus_!2cRegPtr_Cntstr.DMAC       1       1         target_!2c_SetStatus_!2cRegPtr_Cntstr.FUN       1       1         target_!2c_SetStatus_!2cRegPtr_Cntstr.DIR       2       2         target_!2c_SetStatus_!2cRegPtr_Cntstr.DIN       0       0         target_!2c_SetStatus_!2cRegPtr_Cntstr.DOUT       1       1         target_!2c_SetStatus_!2cRegPtr_Cntstr.DOUT       1       1         target_!2c_SetStatus_!2cRegPtr_Cntstr.DET       1       1         target_!2c_SetStatus_!2cRegPtr_Cntstr.DDR       0       0         target_!2c_SetStatus_!2cRegPtr_Cntstr.DDR       0       0         target_!2c_SetStatus_!2cRegPtr_Cntstr.PD       3       3         target_!2c_SetStatus_!2cRegPtr_Cntstr.DD       3       3         target_!2c_Setstatus_!2cRegPtr_Cntstr.DAR       567       567         target_!2c_SetupMasterReceive_!2cRegPtr_Cntstr.IMR       44       44 </td <td></td> <td></td> <td></td> <td><b>~</b></td>				<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11       44       44         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12       44       4466         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12       44       44         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC       1       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DN       1       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR       2       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN       0       0         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT       1       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DET       1       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR       2       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DDR       0       0         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DDR       0       0         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DD       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DD       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DAR       3       3         target_I2c_Setstatus_I2cRegPtr_Cnt_T_str.OAR       567       567         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DAR       444       444         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR			~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11       4466       4466         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12       44       44         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC       1       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR       2       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN       0       0         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT       1       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET       1       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR       2       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR       2       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DDR       0       0         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DD       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DAR       567       567         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR       444       44         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL       566       566				~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12       44       44         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIMC       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN       0         0       0         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT       1         1       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET       1         1       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR       2         2       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR       0         0       0         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DD       3         3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD       3         3       3         4       3         4       44         4       44         4       44         4       44         4       444         4       444         4       444         4       444         4       444         4       444         4       444         4	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44		~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC       1       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DUT       0       0         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT       1       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET       1       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR       2       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR       0       0         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DD       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DAR       567       567         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR       44       44         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR       4444       444         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL       566       566	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN       0         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR       0         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DD       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR       567         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR       44         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR       4444         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR       4444         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL       566	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN       0         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR       0         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DD       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DAR       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR       567         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR       44         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR       4444         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL       566	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR       2       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN       0       0         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT       1       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET       1       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR       2       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR       0       0         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR       567       567         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR       44       44         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR       4444       444         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR       4444       444         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL       566       566		1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN       0       0         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT       1       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET       1       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR       2       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR       0       0         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL       3       3         target_I2c_SetUpMasterReceive_I2cRegPtr_Cnt_T_str.OAR       567       567         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR       44       44         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR       4444       444         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL       566       566	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR       0         0       0         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD       3         3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL       3         3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR       567         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR       44         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR       4444         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL       566		0	0	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET       1       1         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR       2       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR       0       0         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR       567       567         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR       44       44         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR       4444       444         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL       566       566				~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR       2       2         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR       0       0         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR       567       567         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR       44       44         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR       4444       444         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL       566       566				
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR       0       0         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR       567       567         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR       44       44         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR       4444       4444         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL       566       566				~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD       3       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR       567       567         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR       44       44         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR       4444       4444         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL       566       566				
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR       567       567         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR       44       44         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR       4444       4444         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL       566       566				-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR 567 567 target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR 44 44 444 444 4444 4444 4444 4444 44				
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR 44 44 444 444 4444 4444 4444 4444 44				
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR 4444 4444 4444 4444 4444 4444 4444 4				
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL 566 566				
				<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH 4466 4466 4466				<b>~</b>
	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>✓</b>

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	✓
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3	3	<b>✓</b>

T				V
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 2.4 (Repeat Count = 1)	🗸
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	4
DigColPsInt_Buffer_Cnt_M_u08[0]	28
DigColPsInt_Buffer_Cnt_M_u08[1]	56
DigColPsInt_Buffer_Cnt_M_u08[2]	100
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	7
DigColPsInt_CurrentSlave_Cnt_M_u08	120
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_NOT_INITIALIZED
DigColPsInt_I2CHwCustData_Uls_M_u16	10
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	11
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	4
DigColPsInt_RecvOverrunError_Cnt_M_Igc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1

DigColPsInt InterruptNotification

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Input Value DigColPsInt\_SpurCustDatFound\_Cnt\_M\_lgc 88 DigColPsInt\_SpurSnsrData\_Cnt\_M\_u16 DigColPsInt TransactionCnt Cnt M u08 40 Flags\_Cnt\_T\_b16 2 I2c GenStopCond(I2cRegPtr Cnt T str) target I2c GenStopCond I2cRegPtr Cnt T str I2c\_Send(I2cRegPtr\_Cnt\_T\_str) target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str I2c SetRecv(I2cRegPtr Cnt T str) target I2c SetRecv I2cRegPtr Cnt T str I2c\_SetStatus(I2cRegPtr\_Cnt\_T\_str) target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str I2c\_SetupMasterReceive(I2cRegPtr\_Cnt\_T\_str) target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str I2c\_SetupMasterTransmit(I2cRegPtr\_Cnt\_T\_str) T\_DataRegisters\_Cnt\_u08[0] T\_DataRegisters\_Cnt\_u08[1] 32 T\_DataRegisters\_Cnt\_u08[2] 30 T\_DataRegisters\_Cnt\_u08[3] 36 T\_DataRegisters\_Cnt\_u08[4] 38 34 T DataRegisters Cnt u08[5] T\_DataRegisters\_Cnt\_u08[6] 10 T\_DataRegisters\_Cnt\_u08[7] 12 T\_DataRegisters\_Cnt\_u08[8] 14 i2cREG1\_temp target\_i2cREG1\_temp k\_ColSensorl2CAddress\_Cnt\_u08 24 k\_SpurSensorI2CAddress\_Cnt\_u08 40  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.OAR$ 65 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.IMR 89 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.STR 67  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKL$ 7 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKH 577 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CNT 88 target I2c GenStopCond I2cRegPtr Cnt T str.DRR 23 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.SAR 65 target I2c GenStopCond I2cRegPtr Cnt T str.DXR 89 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.MDR 7 target I2c GenStopCond I2cRegPtr Cnt T str.IVR 44 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.EMDR 2  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PSC$ 89 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PID11 577  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PID12$ 89 2  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DMAC$ target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.FUN 0 0  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DIR$ target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DIN 1 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DOUT 2 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.SET 2 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLR 0  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.ODR$ 1 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PD 2 target I2c GenStopCond I2cRegPtr Cnt T str.PSL 0 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.OAR 65 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IMR 89 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.STR 67 target I2c Send I2cRegPtr Cnt T str.CLKL 7 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKH 577 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CNT 88 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DRR 23 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SAR 65 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DXR 89 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.MDR 44 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IVR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.EMDR 2 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSC 89 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID11 577 89 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID12 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DMAC 2 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.FUN 0 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIR 0 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIN 1 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DOUT 2 target I2c Send I2cRegPtr Cnt T str.SET 2 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLR n target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.ODR 1 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PD 2 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSL 0  $target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.OAR$ 65

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Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89
target I2c SetRecv I2cRegPtr Cnt T str.PID11	577
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89
	2
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67
target I2c SetStatus I2cRegPtr Cnt T str.CLKL	7
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577
	88
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	577
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CNT	88
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89
	577
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2
	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2

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Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
target_i2cREG1_temp.OAR	65		
target_i2cREG1_temp.IMR	89		
target_i2cREG1_temp.STR	67		
target_i2cREG1_temp.CLKL	7		
target_i2cREG1_temp.CLKH	577		
target_i2cREG1_temp.CNT	88		
target_i2cREG1_temp.DRR	23		
target_i2cREG1_temp.SAR	65		
target_i2cREG1_temp.DXR	89		
target_i2cREG1_temp.MDR	7		
target_i2cREG1_temp.IVR	44		
target_i2cREG1_temp.EMDR	2		
target_i2cREG1_temp.PSC	89		
target_i2cREG1_temp.PID11	577		
target_i2cREG1_temp.PID12	89		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	2		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result

target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	4	4	~
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	56	56	~
DigColPsInt_Buffer_Cnt_M_u08[2]	100	100	<b>✓</b>
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	•
DigColPsInt_ColCustDatFound_Cnt_M_Igc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	7	7	•
DigColPsInt_CurrentSlave_Cnt_M_u08	40	40	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_SETREG	INIT_SENSOR2_READERROR_SETREG	<b>✓</b>
DigColPsInt_I2CHwCustData_Uls_M_u16	10	10	~
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	11	11	<b>✓</b>
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1	1	~
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	~
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	<b>✓</b>
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	88	88	<b>✓</b>
DigColPsInt_TransactionCnt_Cnt_M_u08	40	40	~
I2c_Send(Length_Cnt_T_u32)	1	1	<b>✓</b>
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65	65	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89	89	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	577	577	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88	88	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23	23	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65	65	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	89	89	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44	44	

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Name	Actual Value	Expected Value	Result
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0 65	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	65 89	89	
target I2c SetStatus I2cRegPtr Cnt T str.STR	67	67	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7	7	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577	577	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	88	88	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23	23	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65	65	<b>✓</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	89	89	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	7 44	7 44	<b>*</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FWDR	2	2	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.PSC	89	89	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	577	577	·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89	89	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>•</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	<b>~</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	0	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.PSL	0	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	65	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	89	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67	67	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577	577	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23	23	<b>Y</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65	65	<b>~</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	89 7	89 7	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	44	44	•
target I2c SetupMasterReceive I2cRegPtr Cnt T str.EMDR	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89	89	·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577	577	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	<u> </u>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2 2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	1	1	-
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65 89	65 89	· ·
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	7	7	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2 2	2 2	Ž
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	4	4	<u> </u>

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InterruptNotification

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~

T			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
I2c_GenStopCond	1	I2c_GenStopCond	1	~
SetupWriteRegister	1	SetupWriteRegister	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	<b>✓</b>

Test Step 2.5 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	5
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	554
DigColPsInt_CurrentSlave_Cnt_M_u08	5
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE
DigColPsInt_I2CHwCustData_Uls_M_u16	13
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	14
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	123
DigColPsInt_TransactionCnt_Cnt_M_u08	50
Flags_Cnt_T_b16	1
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
_DataRegisters_Cnt_u08[0]	0
Γ_DataRegisters_Cnt_u08[1]	32
Γ_DataRegisters_Cnt_u08[2]	30
Γ_DataRegisters_Cnt_u08[3]	36
Γ_DataRegisters_Cnt_u08[4]	38
_DataRegisters_Cnt_u08[5]	34
_DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
_DataRegisters_Cnt_u08[8]	14
2cREG1_temp	target_i2cREG1_temp
_ColSensorl2CAddress_Cnt_u08	29
_SpurSensorI2CAddress_Cnt_u08	50
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	54
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788
arget I2c GenStopCond I2cRegPtr Cnt T str.EMDR	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
arget I2c GenStopCond I2cRegPtr Cnt T str.DMAC	3

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Name	Input Value	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	
	8	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	
target I2c Send I2cRegPtr Cnt T str.PID11	344	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	
	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554	
	344	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	
target I2c SetRecv I2cRegPtr Cnt T str.CLR	3	
· · ·		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR	8	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	123	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	788	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344	

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Name	Input Value
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1.
target I2c SetupMasterTransmit I2cReqPtr Cnt T str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	2
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	1
	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	
target_i2cREG1_temp.OAR	54
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	8
target i2cREG1 temp.CLKL	554
target_i2cREG1_temp.CLKH	344
target_i2cREG1_temp.CNT	123
target_i2cREG1_temp.DRR	45
target i2cREG1 temp.SAR	54
target_i2cREG1_temp.DXR	66
	554
target_i2cREG1_temp.MDR	
target_i2cREG1_temp.IVR	788
target_i2cREG1_temp.EMDR	3

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Name	Input Value		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	344		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	3		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	3		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	2		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	5	5	~
DigColPsInt Buffer Cnt M u08[0]	123	123	<b>✓</b>

target_izertzer_temp.obit	-		
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	2		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	5	5	~
DigColPsInt_Buffer_Cnt_M_u08[0]	123	123	~
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	~
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	✓
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✓
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	✓
DigColPsInt_ColSnsrData_Cnt_M_u16	554	554	✓
DigColPsInt_CurrentSlave_Cnt_M_u08	5	5	✓
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE	READ_COMPLETE	✓
DigColPsInt_I2CHwCustData_Uls_M_u16	13	13	✓
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	14	14	✓
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✓
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✓
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✓
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	✓
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✓
DigColPsInt_SpurSnsrData_Cnt_M_u16	123	123	✓
DigColPsInt_TransactionCnt_Cnt_M_u08	50	50	✓
I2c_SetStatus(Status_Cnt_T_u16)	7	7	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54	54	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8	8	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554	554	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344	344	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123	123	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45	45	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	54	54	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554	554	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788	788	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344	344	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	1	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	2	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	54	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.IMR	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8	8	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554	554	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	344	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	123	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	45	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	54	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	554	
target I2c Send I2cRegPtr Cnt T str.IVR	788	788	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	344	344	
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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	3	3	<b>Y</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	Ž
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	3	3 2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	·
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54	54	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	8	8	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554	554	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344 123	344 123	<i>y</i>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	45	45	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54	54	·
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554	554	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788	788	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344	344	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	<i>y</i>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	3	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	<b>*</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54	54	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8	8	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554	554	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344	344	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	123	123	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45	45	<b>Y</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54	54	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66 554	66 554	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	788	788	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344	344	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	3	3	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	· ·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	2	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL	2	2	
target_I2c_Setotatus_I2cRegPti_Cnt_T_str.OAR	54	54	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8	8	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554	554	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344	344	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123	123	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45	45	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54	54	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554	554	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788	788	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	~

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344	344	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54	54	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8	8	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554	554	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344	344	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123	123	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45	45	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54	54	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554	554	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788	788	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344	344	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✓
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>✓</b>

Τ				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c_SetStatus	1	I2c_SetStatus	1	~

Test Step 2.6 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	6
DigColPsInt_Buffer_Cnt_M_u08[0]	100
DigColPsInt_Buffer_Cnt_M_u08[1]	200
DigColPsInt_Buffer_Cnt_M_u08[2]	250
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	7846
DigColPsInt_CurrentSlave_Cnt_M_u08	10
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READEXTERR_SETREG
DigColPsInt_I2CHwCustData_UIs_M_u16	16
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	17
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	98
DigColPsInt_TransactionCnt_Cnt_M_u08	60
Flags_Cnt_T_b16	1
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str

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Name	Input Value
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	34
k_SpurSensorl2CAddress_Cnt_u08	60
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR	10
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR	10
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR	7846
target I2c GenStopCond I2cRegPtr Cnt T str.IVR	55
target I2c GenStopCond I2cRegPtr Cnt T str.EMDR	1
target I2c GenStopCond I2cRegPtr Cnt T str.PSC	10
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11	8974
	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1 1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223
	7846
target I2c SetRecv I2cRegPtr Cnt T str.CLKL	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974 98

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Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10
target I2c SetStatus I2cRegPtr Cnt T str.STR	1223
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846
target_12c_SetStatus_12cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target I2c SetStatus I2cRegPtr Cnt T str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1.
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98

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Name	Input Value		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	12		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	10		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	10		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	7846		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	55		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	2		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1		
target_i2cREG1_temp.OAR	10		
target_i2cREG1_temp.IMR	10		
target i2cREG1 temp.STR	1223		
target_i2cREG1_temp.CLKL	7846		
target i2cREG1 temp.CLKH	8974		
target i2cREG1 temp.CNT	98		
target i2cREG1 temp.DRR	12		
target i2cREG1 temp.SAR	10		
target i2cREG1 temp.DXR	10		
target i2cREG1 temp.MDR	7846		
target i2cREG1 temp.IVR	55		
target i2cREG1 temp.EMDR	1		
target_i2cREG1_temp.PSC	10		
target i2cREG1 temp.PID11	8974		
target i2cREG1 temp.PID12	10		
target i2cREG1 temp.DMAC	1		
target i2cREG1 temp.FUN	1		
target i2cREG1 temp.DIR	2		
target i2cREG1 temp.DIN	1		
	1		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET target_i2cREG1_temp.CLR	2		
target i2cREG1_temp.ODR	1		
target i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	1		
		Form a set of Markon	D 11
Name DigColPoint AttempOccurForCustDatPead Cnt M u08	Actual Value	Expected Value	Result
LUGI OIPEIDI ATTAMOLICCUIFLORI HETI INTRANCI ('nt M LUIX	16	16	

target_i2cREG1_temp.PSL 1				
Name	Actual Value	Expected Value	Result	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	6	6	~	
DigColPsInt_Buffer_Cnt_M_u08[0]	100	100	~	
DigColPsInt_Buffer_Cnt_M_u08[1]	200	200	~	
DigColPsInt_Buffer_Cnt_M_u08[2]	250	250	✓	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	<b>✓</b>	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✓	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✓	
DigColPsInt_ColSnsrData_Cnt_M_u16	7846	7846	✓	
DigColPsInt_CurrentSlave_Cnt_M_u08	10	10	<b>✓</b>	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE	INIT_COMPLETE	✓	
DigColPsInt_I2CHwCustData_Uls_M_u16	16	16	✓	
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	17	17	✓	
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1	1	✓	
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	<b>✓</b>	
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✓	
DigColPsInt_RecvdDataType_Cnt_M_u08	5	5	<b>✓</b>	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~	
DigColPsInt_SpurSnsrData_Cnt_M_u16	98	98	~	
DigColPsInt_TransactionCnt_Cnt_M_u08	60	60	✓	
I2c_SetStatus(Status_Cnt_T_u16)	7	7	✓	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10	10	✓	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10	10	✓	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223	1223	✓	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✓	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✓	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98	98	<b>✓</b>	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12	12	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10	10	<b>✓</b>	

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12	12	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	10	10	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.DXR	10	10	-
target I2c SetStatus I2cRegPtr Cnt T str.MDR	7846	7846	
target I2c SetStatus I2cRegPtr Cnt T str.IVR	55	55	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	10	10	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974	8974	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10	10	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target I2c SetStatus I2cRegPtr Cnt T str.DIR	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1	1	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	10	10	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223	1223	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CNT	98	98	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12	12	~
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SAR	10	10	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10	10	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846	7846	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55	55	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10	10	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	8974	8974	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	10	10	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223	1223	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98	98	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10	10	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846	7846	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55	55	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974	8974	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	1	1	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	_



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Actual Function	Count	Expected Function	Count	Result
I2c_SetStatus	1	I2c_SetStatus	1	•

Test Step 2.7 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	7
DigColPsInt_Buffer_Cnt_M_u08[0]	1
DigColPsInt_Buffer_Cnt_M_u08[1]	5
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt ColSnsrData Cnt M u16	0 847
DigColPsInt_CurrentSlave_Cnt_M_u08	15
DigColPsInt CurrentStepNo Cnt M enum	INIT SENSOR1 DUMMY READ
DigColPsInt_I2CHwCustData_Uls_M_u16	19
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	20
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	487
DigColPsInt_TransactionCnt_Cnt_M_u08	70
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str) I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
2c_SetStatus( 2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	39
k_SpurSensorI2CAddress_Cnt_u08	0 34
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	24
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR	455
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	987
target I2c GenStopCond I2cRegPtr Cnt T str.CNT	487
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3 3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT	2 2
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR	3
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2

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Name	Input Value	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	
target I2c Send I2cRegPtr Cnt T str.OAR	34	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	
target I2c Send I2cRegPtr Cnt T str.DOUT	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	34	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	24	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	455	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	847	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	987	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	487	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	34	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	34	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	24	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	847	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	56	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	
target I2c SetRecv I2cRegPtr Cnt T str.PSC	24	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	987	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	24	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	34	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	24	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	455	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	847	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	987	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	487	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	34	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	34	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	24	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	847	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	56	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	24	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	987	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	24	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	
g		

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Name	Input Value
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	455
	847
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	987
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	24
	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24
	455
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	24
	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	2
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2
target_i2cREG1_temp.OAR	34
target_i2cREG1_temp.IMR	24
target i2cREG1 temp.STR	455
target i2cREG1 temp.CLKL	847
° =	
target_i2cREG1_temp.CLKH	987
target_i2cREG1_temp.CNT	487
target_i2cREG1_temp.DRR	34
target_i2cREG1_temp.SAR	34
target_i2cREG1_temp.DXR	24
target_i2cREG1_temp.MDR	847
target_i2cREG1_temp.IVR	56
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	24
target_i2cREG1_temp.PID11	987
target i2cREG1 temp.PID12	24
	2
target_i2cREG1_temp.DMAC	
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	3
target_i2cREG1_temp.DIN	3
target_i2cREG1_temp.DOUT	2

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Separate   Control   Separate	Name	Input Value		
	target_i2cREG1_temp.SET	•		
Separate   Action   Separate   Se	target_i2cREG1_temp.CLR	3		
Name	target_i2cREG1_temp.ODR	3		
Actual Value	target_i2cREG1_temp.PD	2		
Digital Part   District   Distr	target_i2cREG1_temp.PSL	2		
DOCUMENT   BARRY_COLM_MORT    3   3   3   4	Name		•	Result
DigocParls   Jame Cr.   M.   Judit				~
Digital File   Diefe   Cit   M   USB				
Digital Fland Standard Section Co. M. Mgs				
Digitable   Digi				
Digotheric Cooksetherium C.M. M. 196				
DigicoPartin Consensata Crit M. 1915   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   947   9				
DigicoPlania CurrentStaws Crist M, warm				
Dispositive  Commission   Dispositive  Com				
DigicaPellus   District control   District Contro				~
Digitable     Digitable     Digitable   Digitable   Digitable   Digitable   Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable       Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable   Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable   Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable     Digitable				~
Disposition   NanoScience   Crit M   190   0   0   0   0   0   0   0   0   0		20	20	•
Disposition  Reconstruction Cort, M, Igo	DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
Digitar   Revolutionary   Re	DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigiciDarini, Spaciastalariound, Crit, M. Igis  DigiciDarini, Spaciastalariound, Crit, M. Igis  DigiciDarini, Transaction Crit, Crit, M. Igis  DigiciDarini, Transaction Crit, Crit, M. Igis  DigiciDarini, Transaction Crit, M. Igis  DigiciDarini, D. Igis  DigiciDar	DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DipoCharlant Sauranational Cost M, Juli6				
DipicalPaint, TransactionCrit, Crit, My USB   70   70				
282. Setuplester   10   1   12   2   2   3   3   3   4   4   4   4   4   4   4				
222 SetUpMasterTrainmitDatable Ingth, Crit_Tuifo  3   3   3   4   4   4   4   4   4   4				
Langet I.P.C. GenStopCond, IzeRegPT Cnt, T. str. MRR				
taget_12c_GenStopCond_12cRegPt_Cnt_T_str.STR         455         455           target_12c_GenStopCond_12cRegPt_Cnt_T_str.STR         455         455           target_12c_GenStopCond_12cRegPt_Cnt_T_str.CtxH         847         847           target_12c_GenStopCond_12cRegPt_Cnt_T_str.CtxH         897         957           value_12c_GenStopCond_12cRegPt_Cnt_T_str.DtxH         487         487           target_12c_GenStopCond_12cRegPt_Cnt_T_str.DtxR         34         34           target_12c_GenStopCond_12cRegPt_Cnt_T_str.DtxR         34         34           target_12c_GenStopCond_12cRegPt_Cnt_T_str.DtxR         24         24           target_12c_GenStopCond_12cRegPt_Cnt_T_str.DtxR         24         24           target_12c_GenStopCond_12cRegPt_Cnt_T_str.DtxR         24         24           target_12c_GenStopCond_12cRegPt_Cnt_T_str.DtxR         25         26           target_12c_GenStopCond_12cRegPt_Cnt_T_str.DtxR         26         26           target_12c_GenStopCond_12cRegPt_Cnt_T_str.DtxR         27         27           target_12c_GenStopCond_12cRegPt_Cnt_T_str.DtxR         28         28           target_12c_GenStopCond_12cRegPt_Cnt_T_str.DtxR         29         29           target_12c_GenStopCond_12cRegPt_Cnt_T_str.DtxR         20         20           target_12c_GenStopCond_12cRegPt_Cnt_T_str.DtxR <td></td> <td></td> <td></td> <td></td>				
Integel   2c. GenStopCond   ZeRegPP_Cnt_T.str.CLK .   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847   847				
target IZe, GenStopCond, IZeRegPT, Cnt T, str.CNT         487         487         487           target, IZe, GenStopCond, IZeRegPT, Cnt T, str.DRR         34         34         34           target, IZe, GenStopCond, IZeRegPT, Cnt T, str.DRR         34         34         34           target, IZe, GenStopCond, IZeRegPT, Cnt T, str.DRR         34         34         34           target, IZe, GenStopCond, IZeRegPT, Cnt T, str.MDR         847         847         847           target, IZe, GenStopCond, IZeRegPT, Cnt T, str.MDR         847         847         847           target, IZe, GenStopCond, IZeRegPT, Cnt T, str.PDRT         56         59         94           target, IZe, GenStopCond, IZeRegPT, Cnt T, str.PDRT         56         59         94           target, IZe, GenStopCond, IZeRegPT, Cnt T, str.PDRT         987         987         987         987           target, IZe, GenStopCond, IZeRegPT, Cnt T, str.DMAC         2         2         2         4           target, IZe, GenStopCond, IZeRegPT, Cnt T, str.DMR         3         3         3         9           target, IZe, GenStopCond, IZeRegPT, Cnt T, str.DMR         3         3         3         9           target, IZe, GenStopCond, IZeRegPT, Cnt T, str.DMR         3         3         3         3         9				
target_12c_GenStopCond_12cRepPtr_Cnt_T_str.DRR         34         34           target_12c_GenStopCond_12cRepPtr_Cnt_T_str.DRR         34         34           target_12c_GenStopCond_12cRepPtr_Cnt_T_str.DRR         34         34           target_12c_GenStopCond_12cRepPtr_Cnt_T_str.DRR         24         24           target_12c_GenStopCond_12cRepPtr_Cnt_T_str.DRR         847         847           target_12c_GenStopCond_12cRepPtr_Cnt_T_str.DRR         56         56           target_12c_GenStopCond_12cRepPtr_Cnt_T_str.DRR         2         2           target_12c_GenStopCond_12cRepPtr_Cnt_T_str.DRDR         2         2           target_12c_GenStopCond_12cRepPtr_Cnt_T_str.DDT1         987         987           target_12c_GenStopCond_12cRepPtr_Cnt_T_str.DDT1         24         24           target_12c_GenStopCond_12cRepPtr_Cnt_T_str.DDT2         24         24           target_12c_GenStopCond_12cRepPtr_Cnt_T_str.DDT3         3         3           target_12c_GenStopCond_12cRepPtr_Cnt_T_str.DDT3         3         3           target_12c_GenStopCond_12cRepPtr_Cnt_T_str.DDT3         3         3           target_12c_GenStopCond_12cRepPtr_Cnt_T_str.DDT3         2         2           target_12c_GenStopCond_12cRepPtr_Cnt_T_str.DDT3         3         3           target_12c_GenStopCond_12cRepPtr_Cnt_T_str.DDT3				
target_IZe_GenStopCond_IZeRegPtr_Cnt_T_str.SAR         34         34           target_IZe_GenStopCond_IZeRegPtr_Cnt_T_str.SAR         34         34           target_IZe_GenStopCond_IZeRegPtr_Cnt_T_str.MDR         847         847           target_IZe_GenStopCond_IZeRegPtr_Cnt_T_str.MDR         847         847           target_IZe_GenStopCond_IZeRegPtr_Cnt_T_str.MDR         56         56           target_IZe_GenStopCond_IZeRegPtr_Cnt_T_str.MDR         2         2           target_IZe_GenStopCond_IZeRegPtr_Cnt_T_str.PID11         987         987           target_IZe_GenStopCond_IZeRegPtr_Cnt_T_str.PID12         24         24           target_IZe_GenStopCond_IZeRegPtr_Cnt_T_str.PID14         987         987           target_IZe_GenStopCond_IZeRegPtr_Cnt_T_str.PID15         24         24           target_IZe_GenStopCond_IZeRegPtr_Cnt_T_str.DMC         2         2           target_IZe_GenStopCond_IZeRegPtr_Cnt_T_str.DMT         3         3           target_IZe_GenStopCond_IZeRegPtr_Cnt_T_str.DMT         3         3           target_IZe_GenStopCond_IZeRegPtr_Cnt_T_str.DMT         2         2           target_IZe_GenStopCond_IZeRegPtr_Cnt_T_str.CDMT         3         3           target_IZe_GenStopCond_IZeRegPtr_Cnt_T_str.DMT         3         3           target_IZe_GenStopCond_IZeRegPtr_Cnt_T_str.DMT				
target_Ize_GenSlopCond_IzeRegPtr_Cnt_T_str.DNR         34         34         34           target_Ize_GenSlopCond_IzeRegPtr_Cnt_T_str.DNR         847         847         847           target_Ize_GenSlopCond_IzeRegPtr_Cnt_T_str.DNR         847         847         947           target_Ize_GenSlopCond_IzeRegPtr_Cnt_T_str.DNR         56         56         56         95           target_Ize_GenSlopCond_IzeRegPtr_Cnt_T_str.DNR         2         2         2         1           target_Ize_GenSlopCond_IzeRegPtr_Cnt_T_str.DID11         887         987         987         987           target_Ize_GenSlopCond_IzeRegPtr_Cnt_T_str.DID12         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24         24				~
Institute   Ze_GenStopCond   ZeRegPtr_Cnt_T_str MDR		34	34	~
target   12c   GenStopCond   12cRegPtr   Cnt   T   str   ENDR   2	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	24	24	~
target_Ize_GenStopCond_IzeRegPtr_Cnt_T_str-ENDR         2         2           target_Ize_GenStopCond_IzeRegPtr_Cnt_T_str-PID11         987         987           target_Ize_GenStopCond_IzeRegPtr_Cnt_T_str-ID111         987         987           target_Ize_GenStopCond_IzeRegPtr_Cnt_T_str-ID12         24         24           target_Ize_GenStopCond_IzeRegPtr_Cnt_T_str-DMAC         2         2           target_Ize_GenStopCond_IzeRegPtr_Cnt_T_str-DMR         3         3           target_Ize_GenStopCond_IzeRegPtr_Cnt_T_str-DMR         3         3           target_Ize_GenStopCond_IzeRegPtr_Cnt_T_str-DMT         3         3           target_Ize_GenStopCond_IzeRegPtr_Cnt_T_str-DUT         2         2           target_Ize_GenStopCond_IzeRegPtr_Cnt_T_str-DUT         2         2           target_Ize_GenStopCond_IzeRegPtr_Cnt_T_str-DUT         2         2           target_Ize_GenStopCond_IzeRegPtr_Cnt_T_str-DUT         3         3           target_Ize_GenStopCond_IzeRegPtr_Cnt_T_str-DDR         3         3           target_Ize_GenStopCond_IzeRegPtr_Cnt_T_str-Dtr-D         2         2           target_Ize_GenStopCond_IzeRegPtr_Cnt_T_str-Dtr-D         2         2           target_Ize_Send_IzeRegPtr_Cnt_T_str-Dtr-D         2         2           target_Ize_Send_IzeRegPtr_Cnt_T_str-D         2         <	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	847	847	~
target_I2e_GenStopCond_I2cRegPtr_Cnt_T_str.PDC1         24         24           target_I2e_GenStopCond_I2cRegPtr_Cnt_T_str.PD111         987         987           target_I2e_GenStopCond_I2cRegPtr_Cnt_T_str.PD12         24         24           target_I2e_GenStopCond_I2cRegPtr_Cnt_T_str.PD12         24         24           target_I2e_GenStopCond_I2cRegPtr_Cnt_T_str.DNAC         2         2           target_I2e_GenStopCond_I2cRegPtr_Cnt_T_str.DIR         3         3           target_I2e_GenStopCond_I2cRegPtr_Cnt_T_str.DIN         3         3           target_I2e_GenStopCond_I2cRegPtr_Cnt_T_str.DUT         2         2           target_I2e_GenStopCond_I2cRegPtr_Cnt_T_str.DUT         2         2           target_I2e_GenStopCond_I2cRegPtr_Cnt_T_str.DUT         2         2           target_I2e_GenStopCond_I2cRegPtr_Cnt_T_str.DOR         3         3           target_I2e_GenStopCond_I2cRegPtr_Cnt_T_str.DOR         3         3           target_I2e_GenStopCond_I2cRegPtr_Cnt_T_str.DR         2         2           target_I2e_GenStopCond_I2cRegPtr_Cnt_T_str.DR         3         3           target_I2e_GenStopCond_I2cRegPtr_Cnt_T_str.DR         3         4           target_I2e_GenStopCond_I2cRegPtr_Cnt_T_str.DR         3         4           target_I2e_Send_I2cRegPtr_Cnt_T_str.DAR         34 <t< td=""><td>target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR</td><td>56</td><td>56</td><td>~</td></t<>	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	56	56	~
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.PID11         987         987           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.PID12         24         24           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DMC         2         2           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DMC         0         0           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DIN         3         3           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DIN         3         3           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DIN         3         3           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DOUT         2         2           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DOUT         2         2           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CdR         3         3           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DODR         3         3           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DD         2         2           target_12c_Send_12cRegPtr_Cnt_T_str.DAR         34         34           target_12c_Send_12cRegPtr_Cnt_T_str.MR         44         44           target_12c_Send_12cRegPtr_Cnt_T_str.MR         24         44           target_12c_Send_12cRegPtr_Cnt_T_str.DR         455         455           target_12c_Send_12cRegPtr_Cnt_T_str.CNT         487         487	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2		
target   2c GenStopCond   2cRegPtr_Cnt_T_str.PID12				
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DMAC   2				
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN         0         0           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN         3         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN         3         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DUT         2         2         2           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR         3         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DDR         3         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DDR         3         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DDR         2         2         2           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DR         3         3         4           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DR         2         2         2           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DR         3         3         4           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DR         3         3         4           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DR         3         4         4           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DR         3         4         4           target_l2c_Send_l2cRegPtr_Cnt_T_str.DR         4         4				
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR         3         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN         3         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DUT         2         2         4           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DUT         2         2         4           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DDR         3         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DDR         3         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DDR         3         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DDR         2         2         2           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DAR         34         34         34         34         34         34         34         34         34         34         34         34         34         34         34         34         34         34         34         34         34         34         34         34         34         34         34         34         34         34         34         34         34         34         34         34         34         34         34         34         34         34 <td< td=""><td></td><td></td><td></td><td></td></td<>				
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN         3         3           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DUT         2         2           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DUT         2         2           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DLR         3         3           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DDR         3         3           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DDR         3         3           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DDR         2         2           target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR         34         34           target_I2c_Send_I2cRegPtr_Cnt_T_str.DAR         34         34           target_I2c_Send_I2cRegPtr_Cnt_T_str.DAR         24         24           target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL         847         847           target_I2c_Send_I2cRegPtr_Cnt_T_str.DLK         987         987           target_I2c_Send_I2cRegPtr_Cnt_T_str.DAR         34         34           targ				
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT         2         2         2           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET         2         2         2           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DR         3         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DDR         3         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DD         2         2         2           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DR         34         34         34           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR         34         34         34           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR         34         34         34           target_l2c_Gend_l2cRegPtr_Cnt_T_str.DAR         34         34         34           target_l2c_Send_l2cRegPtr_Cnt_T_str.DLK         455         455         455           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL         847         847         847           target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR         34         34         34           target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR         34         34         34           target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR         34         34         34           target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR         34		-	•	•
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.SET         2         2           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CDR         3         3           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DDR         3         3           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DD         2         2           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.PSL         2         2           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DAR         34         34           target_12c_Send_12cRegPtr_Cnt_T_str.DAR         34         34           target_12c_Send_12cRegPtr_Cnt_T_str.DAR         34         34           target_12c_Send_12cRegPtr_Cnt_T_str.DAR         455         455           target_12c_Send_12cRegPtr_Cnt_T_str.CKH         847         847           target_12c_Send_12cRegPtr_Cnt_T_str.CKH         987         987           target_12c_Send_12cRegPtr_Cnt_T_str.CKT         487         487           target_12c_Send_12cRegPtr_Cnt_T_str.DAR         34         34           target_12c_S				-
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD         2         2           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL         2         2           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DAR         34         34           target_l2c_Send_l2cRegPtr_Cnt_T_str.MR         24         24           target_l2c_Send_l2cRegPtr_Cnt_T_str.STR         455         455           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL         847         847           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH         987         487           target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR         34         487           target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR         34         34           target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR         34         34           target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR         34         34           target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR         34         34           target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR         24         24           target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR         847         847           target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR         24         24           target_l2c_Send				<b>✓</b>
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DDR         3         3         vtarget_12c_GenStopCond_12cRegPtr_Cnt_T_str.PD         2         2         vtarget_12c_GenStopCond_12cRegPtr_Cnt_T_str.PSL         2         2         vtarget_12c_GenStopCond_12cRegPtr_Cnt_T_str.PSL         2         2         vtarget_12c_Send_12cRegPtr_Cnt_T_str.DAR         34         34         vtarget_12c_Send_12cRegPtr_Cnt_T_str.MIMR         24         24         vtarget_12c_Send_12cRegPtr_Cnt_T_str.STR         455         455         455         455         455         455         455         455         455         455         455         455         455         457         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487				~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL         2         2         vtarget_l2c_Send_l2cRegPtr_Cnt_T_str.OAR         34         34         34         vtarget_l2c_Send_l2cRegPtr_Cnt_T_str.IMR         24         24         vtarget_l2c_Send_l2cRegPtr_Cnt_T_str.IMR         24         45         455         455         vtarget_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL         847         847         vtarget_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH         847         847         vtarget_l2c_Send_l2cRegPtr_Cnt_T_str.CNT         487         487         vtarget_l2c_Send_l2cRegPtr_Cnt_T_str.DNT         487         487         vtarget_l2c_Send_l2cRegPtr_Cnt_T_str.DNT         487         487         vtarget_l2c_Send_l2cRegPtr_Cnt_T_str.DNT         34         34         34         487         vtarget_l2c_Send_l2cRegPtr_Cnt_T_str.DNT         24         34         34         487         vtarget_l2c_Send_l2cRegPtr_Cnt_T_str.DNT         24         24         24         24         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487         487	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR         34         34         ✓           target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR         24         24         ✓           target_l2c_Send_l2cRegPtr_Cnt_T_str.STR         455         455         ✓           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL         847         847         ✓           target_l2c_Send_l2cRegPtr_Cnt_T_str.CKH         987         987         ✓           target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT         487         487         ✓           target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR         34         34         ✓           target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR         34         34         ✓           target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR         24         24         ✓           target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR         847         847         ✓           target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR         847         847         ✓           target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR         2         2         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.BDDR         2         2         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.DD1         987         987         ✓           target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC         2         2         ✓	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR         24         24           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL         845         455           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL         847         847           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH         987         987           target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT         487         487           target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR         34         34           target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR         34         34           target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR         24         24           target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR         847         847           target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR         847         847           target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR         847         847           target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR         2         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR         2         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11         987         987           target_l2c_Send_l2cRegPtr_Cnt_T_str.DID42         24         24           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIMAC         2         2           target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN         3         3           target_l2c_Send_l2cRegPtr_Cnt_T_	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_l2c_Send_l2cRegPt_Cnt_T_str.STR       455       455         target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL       847       847         v       target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH       987       987         target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT       487       487         target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR       34       34         target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR       34       34         target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR       34       34         target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR       24       24         target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR       847       847         target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR       56       56         target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR       2       2         target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11       987       987         target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12       24       24         target_l2c_Send_l2cRegPtr_Cnt_T_str.DIMAC       2       2         target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN       0       0         target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN       3       3         target_l2c	target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34		~
target_!2c_Send_!2cRegPtr_Cntstr.CLKL       847       847         target_!2c_Send_!2cRegPtr_Cntstr.CLKH       987       987         target_!2c_Send_!2cRegPtr_Cntstr.CNT       487       487         target_!2c_Send_!2cRegPtr_Cntstr.DRR       34       34         target_!2c_Send_!2cRegPtr_Cntstr.DRR       34       34         target_!2c_Send_!2cRegPtr_Cntstr.DXR       24       24         target_!2c_Send_!2cRegPtr_Cntstr.MDR       847       847         target_!2c_Send_!2cRegPtr_Cntstr.INR       56       56         target_!2c_Send_!2cRegPtr_Cntstr.EMDR       2       2         target_!2c_Send_!2cRegPtr_Cntstr.PSC       24       24         target_!2c_Send_!2cRegPtr_Cntstr.PID11       987       987         target_!2c_Send_!2cRegPtr_Cntstr.PID12       24       24         target_!2c_Send_!2cRegPtr_Cntstr.DMAC       2       2         target_!2c_Send_!2cRegPtr_Cntstr.DMAC       2       2         target_!2c_Send_!2cRegPtr_Cntstr.DIR       3       3         target_!2c_Send_!2cRegPtr_Cntstr.DIR       3       3         target_!2c_Send_!2cRegPtr_Cntstr.DIR       3       3         target_!2c_Send_!2cRegPtr_Cntstr.DIN       3       3         target_!2c_Send_!2cRegPtr_Cntstr.DIN	target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24	24	~
target_!2c_Send_!2cRegPtr_Cnt_T_str.CLKH       987       987         target_!2c_Send_!2cRegPtr_Cnt_T_str.CNT       487       487         target_!2c_Send_!2cRegPtr_Cnt_T_str.DRR       34       34         target_!2c_Send_!2cRegPtr_Cnt_T_str.SAR       34       34         target_!2c_Send_!2cRegPtr_Cnt_T_str.DXR       24       24         target_!2c_Send_!2cRegPtr_Cnt_T_str.DXR       847       847         target_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR       56       56         target_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR       2       2         target_!2c_Send_!2cRegPtr_Cnt_T_str.PSC       24       24         target_!2c_Send_!2cRegPtr_Cnt_T_str.PID11       987       987         target_!2c_Send_!2cRegPtr_Cnt_T_str.DID2       24       24         target_!2c_Send_!2cRegPtr_Cnt_T_str.DID4       2       2         target_!2c_Send_!2cRegPtr_Cnt_T_str.DIAC       2       2         target_!2c_Send_!2cRegPtr_Cnt_T_str.FUN       0       0         target_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.DOUT       2       2				~
target_12c_Send_12cRegPtr_Cnt_T_str.CNT       487       487         target_12c_Send_12cRegPtr_Cnt_T_str.DRR       34       34         target_12c_Send_12cRegPtr_Cnt_T_str.SAR       34       34         target_12c_Send_12cRegPtr_Cnt_T_str.DXR       24       24         target_12c_Send_12cRegPtr_Cnt_T_str.MDR       847       847         target_12c_Send_12cRegPtr_Cnt_T_str.IVR       56       56         target_12c_Send_12cRegPtr_Cnt_T_str.EMDR       2       2         target_12c_Send_12cRegPtr_Cnt_T_str.PSC       24       24         target_12c_Send_12cRegPtr_Cnt_T_str.PID11       987       987         target_12c_Send_12cRegPtr_Cnt_T_str.PID12       24       24         target_12c_Send_12cRegPtr_Cnt_T_str.DMAC       2       2         target_12c_Send_12cRegPtr_Cnt_T_str.DMAC       2       2         target_12c_Send_12cRegPtr_Cnt_T_str.DIN       0       0         target_12c_Send_12cRegPtr_Cnt_T_str.DIN       3       3         target_12c_Send_12cRegPtr_Cnt_T_str.DIN       3       3         target_12c_Send_12cRegPtr_Cnt_T_str.DIN       3       3         target_12c_Send_12cRegPtr_Cnt_T_str.DIN       3       3         target_12c_Send_12cRegPtr_Cnt_T_str.DOUT       2       2				~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR       34       34       4         target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR       34       34       4         target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR       24       24       4         target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR       847       847       4         target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR       56       56       4         target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR       2       2       4         target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC       24       24       4         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11       987       987       4         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12       24       24       4         target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC       2       2       4         target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC       2       2       4         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       0       0       4         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       3       3       4         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       3       3       4         target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT       2       2       4				~
target_12c_Send_12cRegPtr_Cnt_T_str.SAR       34       34       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.DXR       24       24       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.MDR       847       847       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.IVR       56       56       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.EMDR       2       24       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.PSC       24       24       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.PID11       987       987       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.PID12       24       24       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.DMAC       2       2       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.DMAC       2       2       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.FUN       0       0       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.DIR       3       3       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.DIN       3       3       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.DOUT       2       2       ✓				~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR       24       24       ✓         target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR       847       847       ✓         target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR       56       56       ✓         target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR       2       2       ✓         target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC       24       24       ✓         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11       987       987       ✓         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12       24       24       ✓         target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC       2       2       ✓         target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN       0       0       ✓         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR       3       3       ✓         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       3       3       ✓         target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT       2       2       ✓				
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR       847         target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR       56         target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR       2         target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC       24         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11       987         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12       24         target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC       2         target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN       0         0       0         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT       2				
target_12c_Send_12cRegPtr_Cnt_T_str.IVR       56       56       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.EMDR       2       24       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.PSC       24       24       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.PID11       987       987       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.PID12       24       24       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.DMAC       2       2       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.FUN       0       0       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.DIR       3       3       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.DIN       3       3       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.DOUT       2       2       ✓				
target_12c_Send_12cRegPtr_CntT_str.EMDR       2       2         target_12c_Send_12cRegPtr_CntT_str.PSC       24       24         target_12c_Send_12cRegPtr_CntT_str.PID11       987       987         target_12c_Send_12cRegPtr_Cnt_T_str.PID12       24       24         target_12c_Send_12cRegPtr_Cnt_T_str.DMAC       2       2         target_12c_Send_12cRegPtr_Cnt_T_str.FUN       0       0         target_12c_Send_12cRegPtr_Cnt_T_str.DIR       3       3         target_12c_Send_12cRegPtr_Cnt_T_str.DIN       3       3         target_12c_Send_12cRegPtr_Cnt_T_str.DOUT       2       2				
target_12c_Send_12cRegPtr_Cntstr.PSC       24       24       ✓         target_12c_Send_12cRegPtr_Cntstr.PID11       987       987       ✓         target_12c_Send_12cRegPtr_Cntstr.PID12       24       24       ✓         target_12c_Send_12cRegPtr_Cntstr.DMAC       2       2       ✓         target_12c_Send_12cRegPtr_Cntstr.FUN       0       0       ✓         target_12c_Send_12cRegPtr_Cntstr.DIR       3       3       ✓         target_12c_Send_12cRegPtr_Cntstr.DIN       3       3       ✓         target_12c_Send_12cRegPtr_Cntstr.DOUT       2       2       ✓				<b>V</b>
target_12c_Send_12cRegPtr_Cntstr.PID11       987       987         target_12c_Send_12cRegPtr_Cntstr.PID12       24       24         target_12c_Send_12cRegPtr_Cntstr.DMAC       2       2         target_12c_Send_12cRegPtr_Cntstr.FUN       0       0         target_12c_Send_12cRegPtr_Cntstr.DIR       3       3         target_12c_Send_12cRegPtr_Cnt_T_str.DIN       3       3         target_12c_Send_12cRegPtr_Cnt_T_str.DOUT       2       2				~
target_12c_Send_12cRegPtr_Cnt_T_str.PID12       24       24       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.DMAC       2       2       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.FUN       0       0       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.DIR       3       3       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.DIN       3       3       ✓         target_12c_Send_12cRegPtr_Cnt_T_str.DOUT       2       2       ✓				<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN       0       0       ✓         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR       3       3       ✓         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       3       3       ✓         target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT       2       2       ✓	target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24	24	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR 3 3 3 \$\frac{1}{2}\$ target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN 3 \$\frac{1}{2}\$ target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT 2 2 \$\frac{1}{2}\$	target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN 3 3 4 4 arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT 2 2 2	target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN			~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT 2 2				
0 0				~
target_izc_benu_izckegrtr_cnt_i_str.ben 2				· ·
	talget_izt_oeliu_izthegrii_ciit_i_sti.oe i			

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3 3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	2	2	
target_12c_Send_12cRegPtr_Cnt_T_str.PSL	2	2	
target I2c SetRecv I2cRegPtr Cnt T str.OAR	34	34	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	24	24	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	455	455	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	847	847	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	987	987	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	487	487	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	34	34 34	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	34 24	24	
target_i2c_SetRecv_i2cRegPtr_Cnt_T_str.MDR	847	847	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	56	56	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	24	24	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	987	987	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	24	24	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	3 2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2 2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	34	34	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	24	24	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	455	455	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	847	847	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	987	987	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	487	487	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR	34	34 34	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	24	24	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.MDR	847	847	
target I2c SetStatus I2cRegPtr Cnt T str.IVR	56	56	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	24	24	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	987	987	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	24	24	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3 2	3 2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	
target I2c SetStatus I2cRegPtr Cnt T str.CLR	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	34	34	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	24	24	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	455	455	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	847	847	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	987	987	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	487	487	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	34	34	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	34 24	34 24	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.bbR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	847	847	
target_i2c_SetupMasterReceive_i2cRegPtr_Cnt_T_str.IVR	56	56	
target_i2c_SetupMasterReceive_i2cRegPtr_Cnt_T_str.EMDR	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	24	24	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	987	987	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	24	24	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	•
		10	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	3	3	•

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34	34	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24	24	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455	455	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847	847	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987	987	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487	487	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34	34	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34	34	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24	24	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847	847	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56	56	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24	24	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987	987	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24	24	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>✓</b>

Τ				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteData	1	SetupWriteData	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c_Send	1	I2c_Send	1	-

Test Step 2.8 (Repeat Count = 1)	🗸
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8
DigColPsInt_Buffer_Cnt_M_u08[0]	28
DigColPsInt_Buffer_Cnt_M_u08[1]	56
DigColPsInt_Buffer_Cnt_M_u08[2]	100
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	20
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	22
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	23
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	80
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32

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DigColPsini_interruptivotilication		(MAC)(M)
Name	Input Value	
「_DataRegisters_Cnt_u08[2]	30	
_DataRegisters_Cnt_u08[3]	36	
_DataRegisters_Cnt_u08[4]	38	
「_DataRegisters_Cnt_u08[5]	34	
「_DataRegisters_Cnt_u08[6]	10	
「_DataRegisters_Cnt_u08[7]	12	
「_DataRegisters_Cnt_u08[8]	14	
2cREG1_temp	target_i2cREG1_temp	
_ColSensorl2CAddress_Cnt_u08	44	
C_SpurSensorI2CAddress_Cnt_u08	127	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	
arget I2c GenStopCond I2cRegPtr Cnt T str.STR	556	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	
	55	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR		
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.STR	556	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	2309	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	
arget I2c Send I2cRegPtr Cnt T str.DRR	67	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	
arget I2c Send I2cRegPtr Cnt T str.MDR	2309	
arget I2c Send I2cRegPtr Cnt T str.IVR	5	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	
	2309	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_l2c_setRecv_l2cRegPtr_Cnt_T_str.MDR  arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR  arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	5 3	

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Name	Input Value
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	1204
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target I2c SetRecv I2cRegPtr Cnt T str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
	1
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target I2c SetupMasterReceive I2cReqPtr Cnt T str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	5
J	



	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	3 3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET target_I2c SetupMasterTransmit_I2cRegPtr_Cnt_T str.CLR	1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	2		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	55		
target i2cREG1 temp.IMR	66		
target_i2cREG1_temp.STR	556		
target_i2cREG1_temp.CLKL	2309		
target_i2cREG1_temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CDR	2		
target_i2cREG1_temp.ODR	3		
target_i2cREG1_temp.PD			
target_i2cREG1_temp.PSL	3	Evnected Value	Posult
target_i2cREG1_temp.PSL  Name	3 Actual Value	Expected Value	Result
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3	Expected Value 8 12	Result
target_i2cREG1_temp.PSL  Name	3 Actual Value 8	8	•
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]	3 Actual Value 8 12	8 12	Ž
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]	3 Actual Value 8 12 56	8 12 56	~
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]	3 Actual Value 8 12 56 100	8 12 56 100	~
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc	3 Actual Value 8 12 56 100 1	8 12 56 100 1	***
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc	3 Actual Value 8 12 56 100 1	8 12 56 100 1	0
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc	3 Actual Value 8 12 56 100 1 1 1 1 1	8 12 56 100 1 1	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16	3 Actual Value 8 12 56 100 1 1 1 1 2309	8 12 56 100 1 1 1 2309	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08	3 Actual Value 8 12 56 100 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22	8 12 56 100 1 1 1 2309	0
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum	3 Actual Value 8 12 56 100 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23	8 12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23	0
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_I12CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc	3 Actual Value 8 12 56 100 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1	8 12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_I12CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc	3 Actual Value 8 12 56 100 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1	8 12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_I12CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc	3 Actual Value 8 12 56 100 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1	8 12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_I12CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvdDataType_Cnt_M_u08	3 Actual Value 8 12 56 100 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1	8 12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_I12CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvdDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc	3 Actual Value 8 12 56 100 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 2 1	8 12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 2 1	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I12CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvdDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16	3 Actual Value 8 12 56 100 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 2 1 87	8 12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 2 1 87	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I12CHwCustData_Uls_M_u16  DigColPsInt_I1itFailedOnce_Cnt_M_lgc  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08	3 Actual Value 8 12 56 100 1 1 1 2309 127 IINIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 2 1 87 80	8 12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 2 1 87 80	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I3CHWCustData_Uls_M_u16  DigColPsInt_I12CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)	3 Actual Value 8 12 56 100 1 1 1 2309 127 IINIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 2 1 87 80 1	8 12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 2 1 87 80 1	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I3CHwCustData_Uls_M_u16  DigColPsInt_I3CHwCustData_Uls_M_u16  DigColPsInt_I3CHwCustData_Uls_M_u16  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)  I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3 Actual Value 8 12 56 100 1 1 1 2309 127 IINIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 2 1 87 80 1 1 1	8 12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 2 1 87 80 1 1	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I3CHwIncompleteCustData_Uls_M_u16  DigColPsInt_I3CHwIncompleteCustData_Uls_M_u16  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvdDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)  I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	3 Actual Value 8 12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 2 1 87 80 1 1 1 1 55	8 12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 2 1 87 80 1 1 1 55	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_u16  DigColPsInt_CurrentStave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I3CHwCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_u08  DigColPsInt_SpurCustData_Cnt_M_u08  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)  I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	3 Actual Value 8 12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 2 1 1 5 6 6 6	8 12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 2	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u08  DigColPsInt_CurrentStave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_I3CHwCustData_Uls_M_u16  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvdDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_u08  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)  I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.JMR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.JMR	3 Actual Value 8 12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 1 55 66 556	8 12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 1 2 1 55 66 556	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I3CHwCustData_Uls_M_u16  DigColPsInt_I3CHwIncompleteCustData_Uls_M_u16  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_u16  DigColPsInt_SpurCustDatFound_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)  I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.JKR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	3 Actual Value 8 12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 1 55 66 556 2309	8 12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 1 55 66 556 2309	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_I2cHwIncompleteCustData_Uls_M_u16  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)  I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	3 Actual Value 8 12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 1 55 66 556	8 12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 1 2 1 55 66 556 2309 1204	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDeataType_Cnt_M_u08  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  Izc_Send(Length_Cnt_T_u32)  Izc_SetupMasterTransmit(DataLength_Cnt_T_u16)  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	3 Actual Value 8 12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 1 1 55 66 556 2309 1204	8 12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 1 55 66 556 2309	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_I2cHwIncompleteCustData_Uls_M_u16  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)  I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	3 Actual Value 8 12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 1 1 5 66 556 2309 1204 87	8 12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 1 55 66 556 2309 1204 87	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDetatType_Cnt_M_u08  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)  I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	3 Actual Value 8 12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 1 1 5 66 556 2309 1204 87 67	8 12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 1 55 66 556 2309 1204 87 67	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CorrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I3cHialiedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)  I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	3 Actual Value 8 12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 1 1 5 66 556 2309 1204 87 67 55	8 12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 1 55 66 556 2309 1204 87 67 55	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_u06  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  I2c_Send(Length_Cnt_T_u32)  I2c_SetupMasterTransmit(Datal_ength_Cnt_T_u16)  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR	3 Actual Value 8 12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 1 5 6 66 556 2309 1204 87 67 55 66	8 12 56 100 1 1 1 1 2309 127 INIT_SENSOR2_EXTREADCTRLREG_SET 22 23 1 1 1 1 1 55 66 556 2309 1204 87 67 55 66	

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Name	Actual Value	Expected Value	Result
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC	66	66	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC	66	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	
target I2c GenStopCond I2cRegPtr Cnt T str.DIN	2	2	<b>→</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	67	67	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	3 66	3 66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	1204	1204	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11 target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	66	66	
target_12c_Send_12cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	<u> </u>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>→</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>~</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	55	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	3	3 66	· ·
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	66 1204	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_I_str.PID11 target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	1204 66	
target_I2c_SetRecv_I2cRegPtr_Cnt_1_str.PID12 target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.FUN	1	1	
target I2c SetRecv I2cRegPtr Cnt T str.DIR	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	<u> </u>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>V</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	1	1	<b>Y</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR	1 2	2	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	3	3	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.SET	3	3	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>Y</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309 5	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR target_I2c SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2C_SetupMasterReceive_I2CRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>V</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	55	55	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	556	556	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	2	2	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3 1	3	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	2	2	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	
	1-	i -	

Т				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c Send	1	I2c Send	1	<b>✓</b>



Test Step 2.9 (Repeat Count = 1)	<b>→</b>
Name	Input Value
DigColPsInt AttempOccurForCustDatRead Cnt M u08	9
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt Buffer Cnt M u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	495
DigColPsInt_CurrentSlave_Cnt_M_u08	25
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	25
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	26
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	897
DigColPsInt_TransactionCnt_Cnt_M_u08	90
Flags_Cnt_T_b16	2
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	49
k_SpurSensorI2CAddress_Cnt_u08	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	66 78
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR	495
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0
~	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	56
	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12 target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0
target I2c GenStopCond I2cRegPtr Cnt T str.FUN	0
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR	0
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN	1
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DUT	0
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET	0
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLR	0
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR	1
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DD	0
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	66
target_l2c_Send_l2cRegPtr_Cnt_1_str.UAR target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	78
target_l2c_Send_l2cRegPtr_Cnt_T_str.NRR target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	78
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	495
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	56
targot_120_0011d_120110g1 tt_O11t_1_Stt.OLINT1	VV

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Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	1
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	66
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	78
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	78
target_12c_SetRecv_12cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	0
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
target_12c_SetRecv_12cRegPtr_Cnt_T_str.PSL	0
target I2c SetStatus I2cRegPtr Cnt T str.OAR	66
target I2c SetStatus I2cRegPtr Cnt T str.IMR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	78
target I2c SetStatus I2cRegPtr Cnt T str.CLKL	495
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	56
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	0
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	0
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0
toract IOs CatCtatus IOsDasDts Cat T ats DOI	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66
	66 78 78

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Name	Input Value
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKH	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
target I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56
	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	0
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	78
target_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56
target_i2cREG1_temp.CNT	897
target i2cREG1 temp.DRR	98
·	66
target_i2cREG1_temp.SAR	
target_i2cREG1_temp.DXR	78
target_i2cREG1_temp.MDR	495
target_i2cREG1_temp.IVR	66
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	78
target_i2cREG1_temp.PID11	56
target_i2cREG1_temp.PID12	78
target_i2cREG1_temp.DMAC	0
	0
target_i2cREG1_temp.FUN	
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.SET target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.CLR	
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR	0 1
target_i2cREG1_temp.CLR	0

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Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	9	9	<b>*</b>
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	•
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	•
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	Ž
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	
DigColPsInt_CilicatDatFound Cnt M Igc	0	0	
DigColPsInt_ColSnsrData_Cnt_M_u16	495	495	
DigColPsInt_CurrentSlave_Cnt_M_u08	100	100	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_SETREG		
DigColPsInt_I2CHwCustData_Uls_M_u16	25	25	
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	26	26	•
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	-
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	•
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	-
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	•
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	-
DigColPsInt_SpurSnsrData_Cnt_M_u16	897	897	•
DigColPsInt_TransactionCnt_Cnt_M_u08	90	90	<b> </b>
I2c_Send(Length_Cnt_T_u32)	1	1	•
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	78	78	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	897	897	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	98	98	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	66	66	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR	78	78 495	Ĭ
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR	495 66	66	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR	0	0	j
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.PSC	78	78	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	56	56	j
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	78	78	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0	0	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target I2c GenStopCond I2cRegPtr Cnt T str.DIR	0	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	0	0	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	897	897	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0 78	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	78 56	78 56	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11 target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PiD12 target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	78	-

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Name	Actual Value	Expected Value	Result
target_I2c_S&tReev_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	98	

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PD$ 

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSL$ 

DigColPsInt\_InterruptNotification



Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✓
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	1	1	<b>✓</b>

Τ				V
Actual Function	Count	Expected Function	Count	Result
I2c_GenStopCond	1	I2c_GenStopCond	1	~
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c Send	1	I2c Send	1	<b>✓</b>

0

0

Name	Input Value
DigColPsInt AttempOccurForCustDatRead Cnt M u08	10
DigColPsInt Buffer Cnt M u08[0]	0
DigColPsInt Buffer Cnt M u08[1]	0
DigColPsInt_Buffer_Cnt_M_u08[2]	0
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1.
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	566
DigColPsInt_CurrentSlave_Cnt_M_u08	30
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	28
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	29
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1.
DigColPsInt_PrevReqDataType_Cnt_M_u08	4
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1.
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	129
DigColPsInt_TransactionCnt_Cnt_M_u08	100
Flags_Cnt_T_b16	32
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
Γ_DataRegisters_Cnt_u08[0]	0
Γ_DataRegisters_Cnt_u08[1]	32
Γ_DataRegisters_Cnt_u08[2]	30
「_DataRegisters_Cnt_u08[3]	36
Γ_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10

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Digeon sint_interruptive interaction		
Name	Input Value	
T_DataRegisters_Cnt_u08[7]	12	
T_DataRegisters_Cnt_u08[8]	14	
i2cREG1_temp	target_i2cREG1_temp	
k_ColSensorl2CAddress_Cnt_u08	54	
k_SpurSensorI2CAddress_Cnt_u08	120	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6 567	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	44	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR	554	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FMDR	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	
target I2c GenStopCond I2cRegPtr Cnt T str.PID11	4466	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	
target I2c GenStopCond I2cRegPtr Cnt T str.FUN	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	567	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1 44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	4466	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11 target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	2	
target I2c Send I2cRegPtr Cnt T str.DIN	0	
target I2c Send I2cRegPtr Cnt T str.DOUT	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	

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target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DUT  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DDR  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DD  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD  target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DAR  target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MR  target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR  target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT  target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR  target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR  target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR  target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	Input Value  0  1  1  2  0  3  3  567  44  4444  566  4466  129  6  567
target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DOUT target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.SET target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLR target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.ODR target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PD target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PSL target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.OAR target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.MR target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.STR target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.CLKL target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.CLKL target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.CLKL target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.CNT target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DRR target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DRR target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.SAR target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DXR	1 1 2 0 3 3 567 44 4444 566 4466 129
target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DOUT target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.SET target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLR target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.ODR target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PD target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PSL target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.OAR target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.IMR target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.STR target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.CLKL target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.CLKL target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.CLKL target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.CNT target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DRR target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DRR target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.SAR target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DXR	1 1 2 0 3 3 567 44 4444 566 4466 129
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD target_l2c_SetSecv_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	1 2 0 3 3 567 44 4444 566 4466 129 6
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	2 0 3 3 567 44 4444 566 4466 129
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	0 3 3 567 44 4444 566 4466 129
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	3 567 44 4444 566 4466 129
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	3 567 44 4444 566 4466 129
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	3 567 44 4444 566 4466 129
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	567 44 4444 566 4466 129
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	44 4444 566 4466 129
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	4444 566 4466 129
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	566 4466 129 6
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	4466 129 6
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	4466 129 6
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	129 6
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	6
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	567
0 = = = = = = =	
0 = = = = = = =	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566
0 =	
	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44
0 = = = 0 = ==	4466
0 0	
	44
0 = = 0 = ==	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
312 121111112 1 13 121 2 211	0
0 = = = 0 = ==	
0 0	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
	3
0 0	
·	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444
	566
	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SAR	567
	44
0 = = 1 = 0 = ==	566
	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSC	44
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	4466
0 = = 1 = 0 = ==	
0	44
	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
	0
0 = = 1 = 0 = ==	1
0	
0 1 - 0	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
0 = = 1 = 0 = ==	3
	3
0	
	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
	566
	4466
	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
	44
0 = = 1 = 0 = ==	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
	44
0 = = 1 = 0 = ==	4466
	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1

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Name	Immut Value		
Name target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	3		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	567		
target_i2cREG1_temp.IMR	44		
target_i2cREG1_temp.STR	4444		
target_i2cREG1_temp.CLKL	566		
target_i2cREG1_temp.CLKH	4466 129		
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	6		
target_i2cREG1_temp.SAR	567		
target_i2cREG1_temp.DXR	44		
target_i2cREG1_temp.MDR	566		
target_i2cREG1_temp.IVR	554		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11	44 4466		
target i2cREG1_temp.PID11	44		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	2		
target_i2cREG1_temp.DIN	0		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	10	10	<b> </b>
- 19 - 21 - 21 - 21 - 21 - 21 - 21 - 21			
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	36 0	36 0	~
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	36 0 0	36 0 0	~
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc	36 0	36 0	~
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	36 0 0 1	36 0 0 1	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc	36 0 0 1 1	36 0 0 1 1	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08	36 0 0 1 1 1 1 566 120	36 0 0 1 1 1 1 566 120	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
DigCoIPsInt_Buffer_Cnt_M_u08[0] DigCoIPsInt_Buffer_Cnt_M_u08[1] DigCoIPsInt_Buffer_Cnt_M_u08[2] DigCoIPsInt_BusBusySeqError_Cnt_M_lgc DigCoIPsInt_CmdFailOccurred_Cnt_M_lgc DigCoIPsInt_ColCustDatFound_Cnt_M_lgc DigCoIPsInt_ColSnsrData_Cnt_M_u16 DigCoIPsInt_CurrentSlave_Cnt_M_u08 DigCoIPsInt_CurrentStepNo_Cnt_M_enum	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG	· · · · · · · · · · · · · · · · · · ·
DigCoIPsInt_Buffer_Cnt_M_u08[0] DigCoIPsInt_Buffer_Cnt_M_u08[1] DigCoIPsInt_Buffer_Cnt_M_u08[2] DigCoIPsInt_BusBusySeqError_Cnt_M_lgc DigCoIPsInt_CmdFailOccurred_Cnt_M_lgc DigCoIPsInt_ColCustDatFound_Cnt_M_lgc DigCoIPsInt_ColSnsrData_Cnt_M_u16 DigCoIPsInt_CurrentSlave_Cnt_M_u08 DigCoIPsInt_CurrentStepNo_Cnt_M_enum DigCoIPsInt_I2CHwCustData_UIs_M_u16	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28	***************************************
DigCoIPsInt_Buffer_Cnt_M_u08[0] DigCoIPsInt_Buffer_Cnt_M_u08[1] DigCoIPsInt_Buffer_Cnt_M_u08[2] DigCoIPsInt_BusBusySeqError_Cnt_M_lgc DigCoIPsInt_CmdFailOccurred_Cnt_M_lgc DigCoIPsInt_ColCustDatFound_Cnt_M_lgc DigCoIPsInt_ColCustDatFound_Cnt_M_lgc DigCoIPsInt_ColSnsrData_Cnt_M_u16 DigCoIPsInt_CurrentSlave_Cnt_M_u08 DigCoIPsInt_CurrentStepNo_Cnt_M_enum DigCoIPsInt_I2CHwCustData_UIs_M_u16 DigCoIPsInt_I2CHwIncompleteCustData_UIs_M_u16	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29	***************************************
DigCoIPsInt_Buffer_Cnt_M_u08[0] DigCoIPsInt_Buffer_Cnt_M_u08[1] DigCoIPsInt_Buffer_Cnt_M_u08[2] DigCoIPsInt_BusBusySeqError_Cnt_M_lgc DigCoIPsInt_CmdFailOccurred_Cnt_M_lgc DigCoIPsInt_ColCustDatFound_Cnt_M_lgc DigCoIPsInt_ColSnsrData_Cnt_M_u16 DigCoIPsInt_CurrentSlave_Cnt_M_u08 DigCoIPsInt_CurrentStepNo_Cnt_M_enum DigCoIPsInt_I2CHwCustData_UIs_M_u16	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28	· · · · · · · · · · · · · · · · · · ·
DigCoIPsInt_Buffer_Cnt_M_u08[0] DigCoIPsInt_Buffer_Cnt_M_u08[1] DigCoIPsInt_Buffer_Cnt_M_u08[2] DigCoIPsInt_BusBusySeqError_Cnt_M_lgc DigCoIPsInt_CmdFailOccurred_Cnt_M_lgc DigCoIPsInt_ColCustDatFound_Cnt_M_lgc DigCoIPsInt_ColSnsrData_Cnt_M_u16 DigCoIPsInt_CurrentSlave_Cnt_M_u08 DigCoIPsInt_CurrentStepNo_Cnt_M_enum DigCoIPsInt_I2CHwCustData_UIs_M_u16 DigCoIPsInt_I2CHwIncompleteCustData_UIs_M_u16 DigCoIPsInt_I2CHwIncompleteCustData_UIs_M_u16 DigCoIPsInt_I3CHwIncompleteCustData_UIs_M_u16 DigCoIPsInt_InitFailedOnce_Cnt_M_lgc	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0	· · · · · · · · · · · · · · · · · · ·
DigCoIPsInt_Buffer_Cnt_M_u08[0] DigCoIPsInt_Buffer_Cnt_M_u08[1] DigCoIPsInt_Buffer_Cnt_M_u08[2] DigCoIPsInt_BusBusySeqError_Cnt_M_lgc DigCoIPsInt_CmdFailOccurred_Cnt_M_lgc DigCoIPsInt_ColCustDatFound_Cnt_M_lgc DigCoIPsInt_ColSnsrData_Cnt_M_u16 DigCoIPsInt_CurrentSlave_Cnt_M_u08 DigCoIPsInt_CurrentStepNo_Cnt_M_enum DigCoIPsInt_I2CHwCustData_UIs_M_u16 DigCoIPsInt_I2CHwIncompleteCustData_UIs_M_u16 DigCoIPsInt_I2CHwIncompleteCustData_UIs_M_u16 DigCoIPsInt_InitFailedOnce_Cnt_M_lgc DigCoIPsInt_NackOccured_Cnt_M_lgc DigCoIPsInt_RecvOverrunError_Cnt_M_lgc DigCoIPsInt_RecvOverrunError_Cnt_M_lgc DigCoIPsInt_RecvdDataType_Cnt_M_u08	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 4	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1	
DigCoIPsInt_Buffer_Cnt_M_u08[0] DigCoIPsInt_Buffer_Cnt_M_u08[1] DigCoIPsInt_Buffer_Cnt_M_u08[2] DigCoIPsInt_BusBusySeqError_Cnt_M_lgc DigCoIPsInt_CmdFailOccurred_Cnt_M_lgc DigCoIPsInt_ColCustDatFound_Cnt_M_lgc DigCoIPsInt_ColSnsrData_Cnt_M_u16 DigCoIPsInt_CurrentSlave_Cnt_M_u08 DigCoIPsInt_CurrentStepNo_Cnt_M_enum DigCoIPsInt_I2CHwCustData_UIs_M_u16 DigCoIPsInt_I2CHwIncompleteCustData_UIs_M_u16 DigCoIPsInt_I1EfailedOnce_Cnt_M_lgc DigCoIPsInt_NackOccured_Cnt_M_lgc DigCoIPsInt_RecvOverrunError_Cnt_M_lgc DigCoIPsInt_RecvdDataType_Cnt_M_u08 DigCoIPsInt_RecvdDataType_Cnt_M_u08 DigCoIPsInt_SpurCustDatFound_Cnt_M_lgc	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 4 1	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 4 1	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u16 DigColPsInt_L2CHwCustData_Uls_M_u16 DigColPsInt_l2CHwCustData_Uls_M_u16 DigColPsInt_l1ErailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvdDataType_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDataTound_Cnt_M_lgc	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 4 1 129	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 4 1 1	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_enum DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_12CHwCustData_UIs_M_u16 DigColPsInt_l12CHwCustData_UIs_M_u16 DigColPsInt_lnitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 4 1 129 100	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 4 1 129 100	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_l2CHwCustData_Uls_M_u16 DigColPsInt_litFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32)	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 4 1 129	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 4 1 1	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_enum DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_12CHwCustData_UIs_M_u16 DigColPsInt_l12CHwCustData_UIs_M_u16 DigColPsInt_lnitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 4 1 129 100 1	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 4 1 129 100 1	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_litFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvdDataType_Cnt_M_u08 DigColPsInt_RecvdDataType_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 4 1 129 100 1	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 4 1 129 100 1	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CrHwCustData_Uls_M_u16 DigColPsInt_I2CrHwIncompleteCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_str.OAR	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 567 44 4444	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 567 44 4444	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 567 44 4444 566	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 1 4 1 129 100 1 1 1 5667 44 4444 566	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_linitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_u08 DigColPsInt_RecvdDataType_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 567 44 4444 566 4466	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 567 44 4444 566 4466	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_linitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvDustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 567 44 4444 566 4466 129	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 1 4 1 1129 100 1 1 1 567 44 4444 566 4466 129	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_linitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_u08 DigColPsInt_RecvdDataType_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 567 44 4444 566 4466	36 0 0 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 567 44 4444 566 4466	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_lizItFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvdDataType_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 567 44 4444 566 4466 129 6	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 1 567 44 4444 566 4466 129 6	
DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_u08  I2C_Send(Length_Cnt_T_u32)  I2C_SetupMasterTransmit(DataLength_Cnt_T_u16)  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	36 0 0 1 1 1 1 5666 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 1 29 100 1 1 1 567 44 4444 566 4466 129 6 567	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 1 567 44 4444 566 4466 129 6 567	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_l2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_l1EralledOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Lengtn_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.UKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 1 129 100 1 1 1 567 44 4444 566 4466 129 6 567 44 566 554	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 1 567 44 4444 566 4466 129 6 567 44 566 554	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_litFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Lengtn_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CKH target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 567 44 4444 566 4466 129 6 567 44 566 554	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 567 44 4444 566 4466 129 6 567 44 566 554	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.JMR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.JKR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRDR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRDR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRDR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRDR	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 567 44 4444 566 4466 129 6 567 44 566 554 1	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 567 44 4444 566 4466 129 6 567 44 566 554 1 44	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I3EHdOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvdDataType_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_SpurSnsrData_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.URR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DDR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DDR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DDR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DDR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DDR	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 1 566 4444 4444 566 6 567 44 566 554 1 44 4466	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 1 567 44 4444 4566 4466 129 6 5567 44 566 554 1 44 4466	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_12CHwCustData_Uls_M_u16 DigColPsInt_12CHwUcustData_Uls_M_u16 DigColPsInt_l2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_l2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_u08 DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_12c_GenStopCond_12cRegPtr_Cnt_T_str.OAR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CkL target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CkL target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CkL target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRDR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.PIDD1 target_12c_GenStopCond_12cRegPtr_Cnt_T_str.PIDD11 target_12c_GenStopCond_12cRegPtr_Cnt_T_str.PIDD12	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 567 44 4444 566 4466 129 6 567 44 566 554 1	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 567 44 4444 566 4466 129 6 567 44 566 554 1 44	
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I3EHdOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvdDataType_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_SpurSnsrData_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.URR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DDR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DDR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DDR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DDR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DDR	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 1 567 44 4444 566 4466 129 6 5567 44 566 554 1 44 4466 44	36 0 0 1 1 1 1 566 120 INIT_SENSOR2_READERROR_SETREG 28 29 0 1 1 1 4 1 129 100 1 1 1 567 44 44444 566 4466 129 6 5567 44 566 554 1 44 4466 44	

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	0	Ž
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	· ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	566 4466	566 4466	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	129	129	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	· · ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11 target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	4466	4466 44	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PMAC	1	1	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	· · ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567 44	· ·
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	44 566	566	
target I2c SetRecv I2cRegPtr Cnt T str.IVR	554	554	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	· · · · · · · · · · · · · · · · · · ·
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR	4444 566	4444 566	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	✓
			-
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11	44 4466	44 4466	· ·

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	566	566	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	554	554	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	4466	4466	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	1	1	<b>V</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1	1	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	2	2	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	1	1	<b>V</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	1	1	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	2	2	<b>V</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	567	567	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	44	44	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	4444	4444	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	566	566	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	4466	4466	
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT	129	129	-
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	6	6	-
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	567	567	-
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	44	44	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	· ·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	1	1	· ·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	4466	4466	· ·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>V</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	•
	1	1	

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c Send	1	I2c Send	1	

Test Step 2.11 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2

2014-10-14, 23:42:41+0530



DigCoPaint_Buffer_Cnt_M_u08[0]   255     DigCoPaint_Buffer_Cnt_M_u08[1]   255     DigCoPaint_Buffer_Cnt_M_u08[2]   255     DigCoPaint_Buffer_Cnt_M_u08[2]   255     DigCoPaint_Buffer_Cnt_M_u08[2]   255     DigCoPaint_Cndisub/sequer_Cnt_M_lige   0     DigCoPaint_Cndisub/sequer_Cnt_M_lige   0     DigCoPaint_Cndisub/sequer_Cnt_M_lige   0     DigCoPaint_Cndisub/sequer_Cnt_M_u08   35     DigCoPaint_Cndisub/sequer_Cnt_M_u08   35     DigCoPaint_Cndisub/sequer_Cnt_M_u08   35     DigCoPaint_Cndisub/sequer_Cnt_M_u08   35     DigCoPaint_Cndisub/sequer_Cnt_M_u08   35     DigCoPaint_Cndisub/sequer_Cnt_M_u08   35     DigCoPaint_Cndisub/sequer_Cnt_M_u08   31     DigCoPaint_Cndisub/sequer_Cnt_M_u08   31     DigCoPaint_Cndisub/sequer_Cnt_M_u08   32     DigCoPaint_Cndisub/sequer_Cnt_M_u08   32     DigCoPaint_Cndisub/sequer_Cnt_M_u08   30     DigCoPaint_PrevRepolataType_Cnt_M_u08   30     DigCoPaint_PrevRepolataType_Cnt_M_u08   30     DigCoPaint_RecordolataType_Cnt_M_u08   30     DigCoPaint_Sequer_Cnt_M_u08   30     DigCoPaint_Sequer_Cnt_M_u08   30     DigCoPaint_Sequer_Cnt_M_u08   30     DigCoPaint_Sequer_Cnt_M_u08   30     DigCoPaint_Sequer_Cnt_M_u08   30     DigCoPaint_TransactionCnt_Cnt_M_u08   30     DigCoPaint_TransactionCnt_Cnt_N_u08   30     DigCoPaint_TransactionCnt_Cnt_N_u08   30     DigCoPaint_TransactionCnt_Cnt_N_u08   30     DigCoPaint_TransactionCnt_Cnt_N_u08   30     DigCoPaint_TransactionCnt_Cnt_N_u08   30     DigCoPaint_TransactionCnt_Cnt	
DigCoPaint_Buffer_Cnt_M_u08(1) DigCoPaint_Buffer_Cnt_M_u08(2) DigCoPaint_Buffer_Cnt_M_u08(2) DigCoPaint_Buffer_Cnt_M_u08(2) DigCoPaint_Buffer_Cnt_M_u08 DigCoPaint_Cont_M_u08 DigCoPaint_Cont_Subar_Cnt_M_u19 DigCoPaint_Cont_Subar_Cnt_M_u18 7 DigCoPaint_Lore_Cont_Subar_U18 DigCoPaint_DigCort_Cont_M_u18 DigCoPaint_DigCort_Cont_M_u18 DigCoPaint_DigCort_Cont_M_u18 DigCoPaint_DigCort_Cont_M_u18 DigCoPaint_Subar_Cnt_M_u18 DigCoPaint_Subar_Cn	
GCOIPSINL_SpurCustDatFound_Cnt_M_gc   GCOIPSINL_SpurSnsrbata_Cnt_M_u16   88     GCOIPSINL_SpurSnsrbata_Cnt_M_u18   110     ags_Cnt_T_b18   32     ags_Cnt_T_b18   32     arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str)   target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str     c_Send(l2cRegPtr_Cnt_T_str)   target_l2c_Send_l2cRegPtr_Cnt_T_str     c_Selfstatus(l2cRegPtr_Cnt_T_str)   target_l2c_Selfstatus_l2cRegPtr_Cnt_T_str     c_Selfstatus(l2cRegPtr_Cnt_T_str)   target_l2c_Selfstatus_l2cRegPtr_Cnt_T_str     c_Selfstatus(l2cRegPtr_Cnt_T_str)   target_l2c_Selfstatus_l2cRegPtr_Cnt_T_str     c_Selfstatus(l2cRegPtr_Cnt_T_str)   target_l2c_Selfstatus_l2cRegPtr_Cnt_T_str     c_Selfstatus(l2cRegPtr_Cnt_T_str)   target_l2c_Selfstatus_l2cRegPtr_Cnt_T_str     c_Selfstatus(l2cRegPtr_Cnt_T_str)   target_l2c_Selfstatus_l2cRegPtr_Cnt_T_str     c_SeltupMasterTransmit(l2cRegPtr_Cnt_T_str)   target_l2c_Selfstatus_l2cRegPtr_Cnt_T_str     c_Selfstatus_l2cRegPtr_Cnt_T_str   target_l2c_Selfstatus_l2cRegPtr_Cnt_T_str     c_Selfstatus_l2cRegPtr_Cnt_T_str   target_l2c_Selfstatus_l2cRegPtr_Cnt_T_str     c_Selfstatus_l2cRegPtr_Cnt_T_str   target_l2c_Selfstatus_l2cRegPtr_Cnt_T_str     c_Selfstatus_l2cRegPtr_Cnt_T_str   target_l2c_Selfstatus_l2cRegPtr_Cnt_T_str     c_Selfstatus_l2cRegPtr_Cnt_T_str   target_l2c_Selfstatus_l2cRegPtr_Cnt_T_str     c_Selfstatus_l2cRegPtr_Cnt_T_str   target_l2c_Selfstatus_l2cRegPtr_Cnt_T_str   target_l2c_Selfstatus_l2cRegP	
ags_Cnt_T_b16	
E. GenStopCond(!2cRegPtr_Cnt_T_str)	
C_Self(2CRegPtr_Cnt_T_str)	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str     target_l2c_SetStatus_l(2cRegPtr_Cnt_T_str     target_l2c_SetStatus_l2cRegPtr_Cnt_T_str     target_l2c_SetStatus_l2cRegPtr_Cnt_T_str     target_l2c_SetStatus_l2cRegPtr_Cnt_T_str     target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str     target_l2c_SetupMasterReceiv_l2cRegPtr	
2c. SelStatus(I2CRegPtr_Cnt_T_str)         target_I2c_SelStatus_I2CRegPtr_Cnt_T_str           2c. SetupMasterReceive(I2CRegPtr_Cnt_T_str)         target_I2c_SetupMasterReceive_I2CRegPtr_Cnt_T_str           2c. SetupMasterTransmit(I2CRegPtr_Cnt_T_str)         target_I2c_SetupMasterTransmit_I2CRegPtr_Cnt_T_str           2c. SetupMasterTransmit(I2CRegPtr_Cnt_T_str)         target_I2c_SetupMasterTransmit_I2CRegPtr_Cnt_T_str           2c. SetupMasterTransmit(I2CRegPtr_Cnt_T_str         atraget_I2c_SetupMasterTransmit_I2CRegPtr_Cnt_T_str           2c. SetupMasterTransmit(I2CRegPtr_Cnt_T_str         atraget_I2c_SetupMasterTransmit_I2CRegPtr_Cnt_T_str           2c. DataRegisters_Cnt_u08[1]         30           2c. DataRegisters_Cnt_u08[3]         36           2c. DataRegisters_Cnt_u08[5]         34           2c. DataRegisters_Cnt_u08[6]         10           2c. DataRegisters_Cnt_u08[7]         12           2c. DataRegisters_Cnt_u08[8]         14           2c. DataRegisters_Cnt_u08[8]         14           3c. DataRegisters_Cnt_u08[8]         59           3c. DataRegisters_Cnt_u08[8]         59           3c. DataRegisters_Cnt_u08[8]         65           3c. DataRegisters_Cnt_u08[8]         65           3c. DataRegisters_Cnt_u08[8]         65           3c. DataRegisters_Cnt_u08[8]         65           3c. DataRegisters_Cnt_u08[8]	
2c. SetupMasterReceive(I2cRegPtr_Cnt_T_str)         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str           2c. SetupMasterTransmit(I2cRegPtr_Cnt_T_str)         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str           2c. SetupMasterTransmit(I2cRegPtr_Cnt_T_str         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str           2c. DataRegisters_Cnt_u08[0]         0           DataRegisters_Cnt_u08[2]         30           DataRegisters_Cnt_u08[3]         36           DataRegisters_Cnt_u08[4]         38           _DataRegisters_Cnt_u08[5]         34           _DataRegisters_Cnt_u08[6]         10           _DataRegisters_Cnt_u08[7]         12           _DataRegisters_Cnt_u08[8]         14           ccREG1_temp         target_I2c_REG1_temp           _ColSensorI2CAddress_Cnt_u08         59           _SpurSensorI2CAddress_Cnt_u08         59           _SpurSensorI2CAddress_Cnt_u08         5           _gret_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.NAR         89           _gret_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR         67           _gret_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT         88           _gret_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT         88           _gret_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR         23           _gret_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DNR         7	
c_SetupMasterTransmit(l2cRegPt_Cnt_T_str)         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str           DataRegisters_Cnt_u08[0]         0           DataRegisters_Cnt_u08[1]         32           DataRegisters_Cnt_u08[2]         30           DataRegisters_Cnt_u08[3]         36           DataRegisters_Cnt_u08[4]         38           DataRegisters_Cnt_u08[5]         34           DataRegisters_Cnt_u08[6]         10           DataRegisters_Cnt_u08[7]         12           DataRegisters_Cnt_u08[8]         14           REEG1_temp         target_l2cREG1_temp           ColSensorl2CAddress_Cnt_u08         59           SpurSensorl2CAddress_Cnt_u08         5           SpurSensorl2CAddress_Cnt_u08         5           rget_l2c_GenStopCond_l2cRegPtr_Cnt_T str.OAR         65           rget_l2c_GenStopCond_l2cRegPtr_Cnt_T str.STR         67           rget_l2c_GenStopCond_l2cRegPtr_Cnt_T str.STR         67           rget_l2c_GenStopCond_l2cRegPtr_Cnt_T str.CLKL         7           rget_l2c_GenStopCond_l2cRegPtr_Cnt_T str.CLKH         577           rget_l2c_GenStopCond_l2cRegPtr_Cnt_T str.DRR         23           rget_l2c_GenStopCond_l2cRegPtr_Cnt_T str.DRR         23           rget_l2c_GenStopCond_l2cRegPtr_Cnt_T str.DNR         7           rget	
DataRegisters_Cnt_u08[0]   0   0   0   0   0   0   0   0   0	
DataRegisters Cnt_u08[1] 32  DataRegisters Cnt_u08[2] 30  DataRegisters Cnt_u08[3] 36  DataRegisters Cnt_u08[4] 38  DataRegisters Cnt_u08[5] 34  DataRegisters Cnt_u08[6] 10  DataRegisters Cnt_u08[6] 10  DataRegisters Cnt_u08[6] 10  DataRegisters Cnt_u08[6] 14  CataRegisters Cnt_u08[7] 12  DataRegisters Cnt_u08[8] 14  CREG1_temp  ColSensorl2CAddress_Cnt_u08 59  SpurSensorl2CAddress_Cnt_u08 59  SpurSensorl2CAddress_Cnt_u08 59  SpurSensorl2CAddress_Cnt_u08 59  SpurSensorl2CAddress_Cnt_u08 65  rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR 65  rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR 67  rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR 67  rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL 77  rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL 77  rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CKL 77  rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DKR 88  rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DKR 88  rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DKR 88  rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DKR 88  rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DKR 89  rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMR 99  rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC 99  rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC 90  rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC 90  rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC 90  rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC 90  rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC 90  rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC 90  rget_l2c_GenStopCond_l2	
DataRegisters Cnt_u08[2]   30     DataRegisters Cnt_u08[3]   36     DataRegisters Cnt_u08[4]   38     DataRegisters Cnt_u08[5]   34     DataRegisters Cnt_u08[6]   10     DataRegisters Cnt_u08[7]   12     DataRegisters Cnt_u08[7]   12     DataRegisters Cnt_u08[8]   14     CREG1_temp   target_i2cREG1_temp     ColSensori2CAddress_Cnt_u08   59     SpurSensori2CAddress_Cnt_u08   59     SpurSensori2CAddress_Cnt_u08   55     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.OAR   65     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.STR   67     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.CLKL   7     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.CLKL   7     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.CLKL   7     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.CLKL   577     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DRR   23     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DRR   23     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DRR   23     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DRR   23     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DRR   39     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DAR   39     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DAR   39     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DAR   39     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DAR   44     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DAR   2     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_s	
DataRegisters Cnt_u08[3]   36     DataRegisters_Cnt_u08[4]   38     DataRegisters_Cnt_u08[5]   34     DataRegisters_Cnt_u08[6]   10     DataRegisters_Cnt_u08[7]   12     DataRegisters_Cnt_u08[7]   12     DataRegisters_Cnt_u08[8]   14     CREG1_temp   target_i2cREG1_temp     ColSensori2CAddress_Cnt_u08   59     SpurSensori2CAddress_Cnt_u08   55     SpurSensori2CAddress_Cnt_u08   65     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.OAR   65     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.CIKL   7     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.CIKL   7     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.CIKL   7     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DAR   23     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DAR   23     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DAR   23     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DAR   23     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DAR   38     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DAR   39     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DAR   39     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DAR   39     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DAR   39     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DAR   39     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DAR   44     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DAR   2     riget_i2c_GenStopCond	
DataRegisters_Cnt_u08[4]   38     DataRegisters_Cnt_u08[5]   34     DataRegisters_Cnt_u08[6]   10     DataRegisters_Cnt_u08[7]   12     DataRegisters_Cnt_u08[7]   12     DataRegisters_Cnt_u08[8]   14     CREG1_temp   target_i2cREG1_temp     ColSensorl2CAddress_Cnt_u08   59     SpurSensorl2CAddress_Cnt_u08   59     SpurSensorl2CAddress_Cnt_u08   65     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.OAR   65     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.NR   89     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.STR   67     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.CLKL   7     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DLKL   577     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DR   23     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DR   23     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DR   23     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DR   65     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DR   89     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DR   7     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DR   7     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DR   44     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.IVR   44     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.IVR   44     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.IVR   44     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.PSC   89     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.PSC   89     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.PID11   577     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.PID12   89     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.PID12   89     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.PID12   89     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.PID12   89     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.PID12   89     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.PID12   89     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.PID12   80     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.PID12   80     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.PID12   80     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.PID12   80     riget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.PID12   80     riget_i2c_GenStopCond_i2	
DataRegisters_Cnt_u08[5]   34     DataRegisters_Cnt_u08[6]   10     DataRegisters_Cnt_u08[7]   12     DataRegisters_Cnt_u08[7]   14     CREG1_temp   target_izcREG1_temp     ColSensorIzCAddress_Cnt_u08   59     SpurSensorIzCAddress_Cnt_u08   59     SpurSensorIzCAddress_Cnt_u08   5     riget_izc_GenStopCond_izcRegPtr_Cnt_T_str.OAR   65     riget_izc_GenStopCond_izcRegPtr_Cnt_T_str.MR   89     riget_izc_GenStopCond_izcRegPtr_Cnt_T_str.STR   67     riget_izc_GenStopCond_izcRegPtr_Cnt_T_str.CLKL   7     riget_izc_GenStopCond_izcRegPtr_Cnt_T_str.CLKL   7     riget_izc_GenStopCond_izcRegPtr_Cnt_T_str.DKR   577     riget_izc_GenStopCond_izcRegPtr_Cnt_T_str.DKR   23     riget_izc_GenStopCond_izcRegPtr_Cnt_T_str.DKR   23     riget_izc_GenStopCond_izcRegPtr_Cnt_T_str.DKR   89     riget_izc_GenStopCond_izcRegPtr_Cnt_T_str.DXR   89     riget_izc_GenStopCond_izcRegPtr_Cnt_T_str.DXR   89     riget_izc_GenStopCond_izcRegPtr_Cnt_T_str.DXR   89     riget_izc_GenStopCond_izcRegPtr_Cnt_T_str.DXR   7     riget_izc_GenStopCond_izcRegPtr_Cnt_T_str.IVR   44     riget_izc_GenStopCond_izcRegPtr_Cnt_T_str.IVR   44     riget_izc_GenStopCond_izcRegPtr_Cnt_T_str.PSC   89     riget_izc_GenStopCond_izcRegPtr_Cnt_T_str.PID11   577     riget_izc_GenStopCond_izcRegPtr_Cnt_T_str.PID12   89     riget_izc_GenStopCond_izcRegPtr_Cnt_T_str.PID12   80     riget_izc_GenStopCond_iz	
DataRegisters_Cnt_u08[7]   12	
DataRegisters Cnt_u08 8  14   target_i2cREG1_temp   target_i2cREG1_temp	
target_i2cREG1_temp	
SpurSensorl2CAddress_Cnt_u08	
SpurSensorI2CAddress_Cnt_u08   5     arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR   65     arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR   89     arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR   67     arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL   7     arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL   7     arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT   88     arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DNR   23     arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DNR   25     arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DNR   89     arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DNR   89     arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DNR   7     arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR   44     arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR   2     arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC   89     arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11   577     arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12   89     arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC   2     arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC   2     arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC   2     arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DINAC   2     arget_	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DAR  arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR  arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR  arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL  arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL  arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH  arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT  arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR  arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR  arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR  arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DAR  arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DAR  arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DAR  arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.NDR  arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.NDR  arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PIDT  arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11  arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12  arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC  arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC  arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR	
urget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.IMR       89         urget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.STR       67         urget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.CLKL       7         urget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.CLKH       577         urget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.CNT       88         urget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DRR       23         urget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DXR       65         urget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DXR       89         urget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.MDR       7         urget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.IVR       44         urget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.EMDR       2         urget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.PSC       89         urget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.PID11       577         urget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.PID12       89         urget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DMAC       2         urget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DMAC       2         urget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DIR       0	
arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.STR       67         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL       7         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKH       577         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.CNT       88         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR       23         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR       65         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR       89         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.MDR       7         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.IVR       44         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.EMDR       2         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.PSC       89         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.PID11       577         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.PID12       89         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.DMAC       2         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.DMAC       2         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.DIR       0	
arget_ 2c_GenStopCond_ 2cRegPtr_Cnt_T_str.CLKL   7	
arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKH       577         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.CNT       88         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR       23         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.SAR       65         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR       89         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.MDR       7         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.IVR       44         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.EMDR       2         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.PSC       89         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.PID11       577         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.PID12       89         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.DMAC       2         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.DMAC       2         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.FUN       0         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.DIR       0	
arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.CNT       88         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR       23         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.SAR       65         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR       89         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.MDR       7         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.IVR       44         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.EMDR       2         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.PSC       89         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.PID11       577         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.PID12       89         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.DMAC       2         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.DMAC       2         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.FUN       0         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.DIR       0	
arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR       23         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.SAR       65         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR       89         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.MDR       7         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.IVR       44         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.EMDR       2         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.PSC       89         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.PID11       577         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.PID12       89         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.DMAC       2         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.DMAC       2         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.DIR       0	
trget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.SAR       65         trget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DXR       89         trget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.MDR       7         trget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.IVR       44         trget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.EMDR       2         trget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.PSC       89         trget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.PID11       577         trget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.PID12       89         trget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DMAC       2         trget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DMAC       2         trget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.FUN       0         trget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DIR       0	
arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR       89         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.MDR       7         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.IVR       44         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.EMDR       2         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.PSC       89         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.PID11       577         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.PID12       89         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.DMAC       2         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.DMAC       2         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.FUN       0         arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.DIR       0	
Irrget_ 2c_GenStopCond_ 2cRegPtr_Cnt_T_str.MDR   7	
1	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR     2       arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC     89       arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11     577       arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12     89       arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC     2       arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FUN     0       arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR     0	
### ### ### ### ### ### ### ### ### #	
rrget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.PID11       577         rrget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.PID12       89         rrget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DMAC       2         rrget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.FUN       0         rrget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DIR       0	
rget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.PID12         89           rget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DMAC         2           rget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.FUN         0           rget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DIR         0	
rget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DMAC         2           rget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.FUN         0           rget_!2c_GenStopCond_!2cRegPtr_Cnt_T_str.DIR         0	
rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FUN 0 rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR 0	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR 0	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN 1	
rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT 2	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET 2	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR 0	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD 2	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL 0	
rget_l2c_Send_l2cRegPtr_Cnt_T_str.OAR 65	
rget_l2c_Send_l2cRegPtr_Cnt_T_str.IMR 89	
rget_l2c_Send_l2cRegPtr_Cnt_T_str.STR 67	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL 7	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH 577	
rget_l2c_Send_l2cRegPtr_Cnt_T_str.CNT 88	
sirget_ 2c_Send_ 2cRegPtr_Cnt_T_str.SAR         65           sirget_ 2c_Send_ 2cRegPtr_Cnt_T_str.DXR         89	

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Name	Input Value	
	7	
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR		
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	
	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN		
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	
	65	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	89 7	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	
	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN		
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	
target I2c SetRecv I2cRegPtr Cnt T str.ODR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	88	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	
target I2c SetStatus I2cRegPtr Cnt T str.PSC	89	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	577	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	
	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR		
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23	

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Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89   7		
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR target_l2c SetupMasterReceive_l2cRegPtr_Cnt_T str.IVR	44		
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_I_str.IVR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2		
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	65   89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.NR  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	7		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH	577		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	88		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89		
$target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.MDR$	7		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
target_i2cREG1_temp.OAR	65		
target_i2cREG1_temp.IMR	89		
target_i2cREG1_temp.STR	67		
target_i2cREG1_temp.CLKL	7		
target_i2cREG1_temp.CLKH	577		
target_i2cREG1_temp.CNT	88		
target_i2cREG1_temp.DRR	23		
target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR	65 89		
target_IZCREG1_temp.IDXR target_i2cREG1_temp.MDR	7		
target i2cREG1 temp.IVR	44		
target_i2cREG1_temp.EMDR	2		
target i2cREG1 temp.PSC	89		
target_i2cREG1_temp.PID11	577		
target_i2cREG1_temp.PID12	89		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL  Name	Actual Value	Exported Value	Descrit
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2	Expected Value	Result
DigColPsInt_AttempoccurrorcusiDatxead_Cnt_w_u08  DigColPsInt_Buffer_Cnt_M_u08[0]	38	38	
DigColPsInt_Buffer_Cnt_M_u08[1]	255	255	-
DigColPsInt_Buffer_Cnt_M_u08[2]	255	255	<b>~</b>

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Name	Actual Value	Expected Value	Result
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	<b>V</b>
DigColPsInt_ColSnsrData_Cnt_M_u16	7	7	~
DigColPsInt_CurrentSlave_Cnt_M_u08	INIT CENCORA DEADEVIERD CETRES	35	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_SETREG	INIT_SENSOR1_READEXTERR_SETREG 31	-
DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	31 32	32	-
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt RecvOverrunError Cnt M Igc	0	0	-
DigColPsInt_RecvdDataType_Cnt_M_u08	5	5	•
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	88	88	<b>~</b>
DigColPsInt_TransactionCnt_Cnt_M_u08	110	110	~
I2c_Send(Length_Cnt_T_u32)	1	1	•
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65	65	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	577	577	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23	23	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577	577	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89	89	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	2	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0	0	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	2	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2 2	2	
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	0	0	<b>V</b>
	1	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_1_str.PD target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65	65	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89	89	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7	7	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577	577	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88	88	~
<u> </u>			

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	23	✓
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	65	65	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89	89	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7	7	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44	44	✓
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	2	2	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89	89	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577	577	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89	89	✓
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	2	2	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	✓
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	2	2	✓
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	2	2	✓
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	0	0	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	✓
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	2	2	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	✓
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR	65	65	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89	89	

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~

T				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c_Send	1	I2c_Send	1	•

Test Step 2.12 (Repeat Count = 1)	Invest Value
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	4
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	554
DigColPsInt_CurrentSlave_Cnt_M_u08	40
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	34
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	35
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	123
DigColPsInt_TransactionCnt_Cnt_M_u08	120
Flags_Cnt_T_b16	32
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Γ_DataRegisters_Cnt_u08[0]	0
Γ_DataRegisters_Cnt_u08[1]	32
Γ_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
Γ_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
Γ_DataRegisters_Cnt_u08[6]	10
Γ_DataRegisters_Cnt_u08[7]	12
Γ_DataRegisters_Cnt_u08[8]	14
2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	64
k SpurSensorI2CAddress Cnt u08	10

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Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	54
target I2c GenStopCond I2cRegPtr Cnt T str.DXR	66
target I2c GenStopCond I2cRegPtr Cnt T str.MDR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target I2c Send I2cRegPtr Cnt T str.STR	8
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target 12a CatDony 12aDonDtr Cat T atr DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	'
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3 2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3 2 3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3 2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3 2 3

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Name	Input Value	
arget I2c SetRecv I2cRegPtr Cnt T str.PD	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	
arget I2c SetStatus I2cRegPtr Cnt T str.STR	8	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	123	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	788	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788	
arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	
arget I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	1	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54	
arget I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	66	
	8	
arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL		
	554	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	
arget I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	3	
arget I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	1	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PUN arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	
aruot 120 Octubinasterriaristilit 120Neufti Olit I Sti.DIK		
	2	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	
	2 3 3	



Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2		
target_i2cREG1_temp.OAR	54		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	8		
target_i2cREG1_temp.CLKL	554		
target_i2cREG1_temp.CLKH	344		
target_i2cREG1_temp.CNT	123		
target_i2cREG1_temp.DRR	45		
target_i2cREG1_temp.SAR	54		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	554		
target_i2cREG1_temp.IVR	788		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	344		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	3		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	3		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	2		
Name	Actual Value	Expected Value	Result

target_i2cREG1_temp.PSL	2		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	4	4	~
DigColPsInt_Buffer_Cnt_M_u08[0]	38	38	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	~
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	<b>✓</b>
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	~
DigColPsInt_CmdFailOccurred_Cnt_M_Igc	1	1	<b>✓</b>
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	554	554	<b>✓</b>
DigColPsInt_CurrentSlave_Cnt_M_u08	40	40	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READEXTERR_SETREG	INIT_SENSOR2_READEXTERR_SETREG	<b>✓</b>
DigColPsInt_I2CHwCustData_Uls_M_u16	34	34	~
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	35	35	•
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	~
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt_RecvOverrunError_Cnt_M_Igc	1	1	~
DigColPsInt_RecvdDataType_Cnt_M_u08	1	1	<b>✓</b>
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	123	123	<b>✓</b>
DigColPsInt_TransactionCnt_Cnt_M_u08	120	120	~
I2c_Send(Length_Cnt_T_u32)	1	1	<b>✓</b>
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54	54	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8	8	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554	554	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344	344	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123	123	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45	45	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	54	54	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554	554	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788	788	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344	344	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	~

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	1	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	2 54	2 54	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8	8	
target I2c Send I2cRegPtr Cnt T str.CLKL	554	554	· •
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	344	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	123	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	45	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	54	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	554	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	788	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344	344	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>Y</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>Y</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2 3	2	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	3	3 3	
	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	
target I2c Send I2cRegPtr Cnt T str.PD	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54	54	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8	8	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554	554	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344	344	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123	123	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45	45	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54	54	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554	554	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788	788	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344	344	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>Y</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	1	1	<b>*</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	3	3	· ·
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_I_str.ODR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.PSL	2	2	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.OAR	54	54	
target I2c SetStatus I2cRegPtr Cnt T str.IMR	66	66	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8	8	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.CLKL	554	554	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344	344	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	123	123	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45	45	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54	54	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	66	66	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR	554	554	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	788	788	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344	344	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	1	1	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR	3	3	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54	54	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8	8	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554	554	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344	344	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123	123	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45	45	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54	54	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554	554	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788	788	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344	344	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54	54	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8	8	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554	554	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344	344	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123	123	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45	45	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54	54	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554	554	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788	788	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344	344	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	~
		·	-

T				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c Sand	1	12c Sand	1	

Test Step 2.13 (Repeat Count = 1)		<b>✓</b>
Name	Input Value	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	6	
DigColPsInt_Buffer_Cnt_M_u08[0]	123	
DigColPsInt_Buffer_Cnt_M_u08[1]	145	
DigColPsInt_Buffer_Cnt_M_u08[2]	200	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	

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DigColPsini_interruptivotilication		
Name	Input Value	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	
DigColPsInt_ColSnsrData_Cnt_M_u16	2767	
DigColPsInt_CurrentSlave_Cnt_M_u08	45	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ	
DigColPsInt_I2CHwCustData_Uls_M_u16	37	
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	38	
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	
DigColPsInt_NackOccured_Cnt_M_lgc	0	
DigColPsInt_PrevReqDataType_Cnt_M_u08	2	
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	
DigColPsInt_RecvdDataType_Cnt_M_u08	2	
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	
DigColPsInt_SpurSnsrData_Cnt_M_u16	564	
DigColPsInt_TransactionCnt_Cnt_M_u08	130	
lags_Cnt_T_b16	32	
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str	
2c_Send(I2cRegPtr_Cnt_T_str)	target I2c Send I2cRegPtr Cnt T str	
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target I2c SetRecv I2cRegPtr Cnt T str	
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str	
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str	
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str	
_DataRegisters_Cnt_u08[0]	0	
_DataRegisters_Cnt_u08[1]	32	
_DataRegisters_Cnt_u08[2]	30	
_DataRegisters_Cnt_u08[3]	36	
_DataRegisters_Cnt_u08[4]	38	
_DataRegisters_Cnt_u08[5]	34	
_DataRegisters_Cnt_u08[6]	10	
_DataRegisters_Cnt_u08[7]	12	
_DataRegisters_Cnt_u08[8]	14	
2cREG1_temp	target_i2cREG1_temp	
_ColSensorl2CAddress_Cnt_u08	69	
SpurSensorI2CAddress Cnt u08	123	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	7788	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556	
	564	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT		
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	
	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT		
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	
irget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	
irget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	
	100	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	

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DigColPsint_interruptivotincation		
Name	Input Value	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
arget I2c Send I2cRegPtr Cnt T str.ODR	3	
arget I2c Send I2cRegPtr Cnt T str.PD	0	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
arget I2c SetRecv I2cRegPtr Cnt T str.OAR	3	
arget I2c SetRecv I2cRegPtr Cnt T str.IMR	100	
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767	
arget_12c_SetRecv_12cRegPtr_Cnt_T_str.CLKH	556	
	564	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788	
target I2c SetStatus I2cRegPtr Cnt T str.CLKL	2767	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564	
target I2c SetStatus I2cRegPtr Cnt T str.DRR	88	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100	
arget I2c SetStatus I2cRegPtr Cnt T str.MDR	2767	
arget I2c SetStatus I2cRegPtr Cnt T str.IVR	9	
·		
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100	
rarget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	
rarget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88	
	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR		
rarget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	
rarget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	

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		<u> </u>	
Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3 2		
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	100 2767		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_1_str.MDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	9		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	3		
target_i2cREG1_temp.IMR	100		
target_i2cREG1_temp.STR	7788		
target_i2cREG1_temp.CLKL	2767		
target_i2cREG1_temp.CLKH	556		
target_i2cREG1_temp.CNT	564		
target_i2cREG1_temp.DRR	88		
target_i2cREG1_temp.SAR	3		
target_i2cREG1_temp.DXR	100		
target_i2cREG1_temp.MDR	2767		
target_i2cREG1_temp.IVR	9		
target_i2cREG1_temp.EMDR	100		
target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11	100 556		
target_i2cREG1_temp.PID12	100		
target i2cREG1 temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	3		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	6	6	~
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	~
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	•
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	~

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	6	6	~
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	~
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	~
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	•
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt_ColSnsrData_Cnt_M_u16	2767	2767	~
DigColPsInt_CurrentSlave_Cnt_M_u08	45	45	~

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Name	Actual Value	Expected Value	Result
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16	INIT_SENSOR1_READERROR_SETREG 37	INIT_SENSOR1_READERROR_SETREG 37	<b>*</b>
DigColPsInt_I2CHwCustData_Uis_M_u16	38	38	_
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	•
DigColPsInt_NackOccured_Cnt_M_Igc	0	0	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_RecvdDataType_Cnt_M_u08	2	2	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	564	564	<b>Y</b>
DigColPsInt_TransactionCnt_Cnt_M_u08 I2c Send(Length Cnt T u32)	130	130	-
l2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100	100	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	7788	7788	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556	556	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564	564	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88	88	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3 100	3 100	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767	2767	2
target I2c GenStopCond I2cRegPtr Cnt T str.IVR	9	9	<b>V</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100	100	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556	556	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100	100	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	3	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	100	_
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	7788 2767	7788 2767	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	556	
target I2c Send I2cRegPtr Cnt T str.CNT	564	564	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	88	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	100	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	2767	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	9	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100 556	100 556	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11 target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	100	100	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	Ž
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	3	3	-
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	100	100	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	7788	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	2767	2767	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556	556	<b>~</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	564	564	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	88	88	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	3	3	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100 2767	100 2767	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9	9	J
targot_120_00t1100v_120110gi ti_Oiit_1_5tt.1VI1	·	•	

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Name	Actual Value	Expected Value	Result
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	0	0	<b>V</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	100 556	100 556	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.PID12	100	100	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100	100	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788	7788	<b>V</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL	2767	2767 556	<b>V</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH	556 564	564	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR	88	88	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.SAR	3	3	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	100	100	
target I2c SetStatus I2cRegPtr Cnt T str.MDR	2767	2767	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9	9	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>~</b>
target I2c SetStatus I2cRegPtr Cnt T str.PSC	100	100	_
target I2c SetStatus I2cRegPtr Cnt T str.PID11	556	556	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100	100	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100	100	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	7788	7788	¥
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	556	556	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	564 88	564 88	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	3	3	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DXR	100	100	~
target I2c SetupMasterReceive I2cRegPtr Cnt T str.MDR	2767	2767	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	9	-
target I2c SetupMasterReceive I2cRegPtr Cnt T str.EMDR	0	0	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSC	100	100	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556	556	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	100	<b>~</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	100	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	556	556	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	88	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	3	3	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	100	100	

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767	2767	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	100	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556	556	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	100	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~

T				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c_Send	1	I2c_Send	1	~

Test Step 2.14 (Repeat Count = 1)	v v v v v v v v v v v v v v v v v v v
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8
DigColPsInt Buffer Cnt M u08[0]	100
DigColPsInt_Buffer_Cnt_M_u08[1]	200
DigColPsInt_Buffer_Cnt_M_u08[2]	250
DigColPsInt BusBusySeqError Cnt M Igc	1
DigColPsInt CmdFailOccurred Cnt M Igc	1
DigColPsInt ColCustDatFound Cnt M Igc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	7846
DigColPsInt_CurrentSlave_Cnt_M_u08	10
DigColPsInt CurrentStepNo Cnt M enum	INIT SENSOR2 CHECKSTAT READ
DigColPsInt I2CHwCustData Uls M u16	40
DigColPsInt I2CHwIncompleteCustData UIs M u16	41
DigColPsInt InitFailedOnce Cnt M Igc	1
DigColPsInt NackOccured Cnt M Igc	1
DigColPsInt PrevReqDataType Cnt M u08	3
DigColPsInt RecvOverrunError Cnt M Igc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt SkipRegisterWrite Cnt M Igc	0
DigColPsInt SpurCustDatFound Cnt M Igc	1
DigColPsInt SpurSnsrData Cnt M u16	98
DigColPsInt TransactionCnt Cnt M u08	12
Flags_Cnt_T_b16	32
I2c GenStopCond(I2cRegPtr Cnt T str)	target I2c GenStopCond I2cRegPtr Cnt T str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c SetRecv(I2cRegPtr Cnt T str)	target I2c SetRecv I2cRegPtr Cnt T str
I2c SetStatus(I2cRegPtr Cnt T str)	target I2c SetStatus I2cRegPtr Cnt T str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
I2c SetupMasterTransmit(I2cRegPtr Cnt T str)	target I2c SetupMasterTransmit I2cRegPtr Cnt T str
T DataRegisters Cnt u08[0]	0
T DataRegisters Cnt u08[1]	32
T DataRegisters Cnt u08[2]	30
T DataRegisters Cnt u08[3]	36
T DataRegisters Cnt u08[4]	38
T DataRegisters Cnt u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T DataRegisters Cnt u08[7]	12
T DataRegisters Cnt u08[8]	14
i2cREG1_temp	target i2cREG1 temp
k ColSensorI2CAddress Cnt u08	74
k SpurSensorI2CAddress Cnt u08	100
target I2c GenStopCond I2cRegPtr Cnt T str.OAR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223
target I2c GenStopCond I2cRegPtr Cnt T str.CLKL	7846
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974
0 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	

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Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR	12
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	10
target I2c GenStopCond I2cRegPtr Cnt T str.PID11	8974
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1
target I2c GenStopCond I2cRegPtr Cnt T str.PSL	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10
target I2c Send I2cRegPtr Cnt T str.IMR	10
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	1223
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98
target I2c Send I2cRegPtr Cnt T str.DRR	12
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974
	10
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
	2
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10
	1223
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10
target I2c SetRecv I2cRegPtr Cnt T str.DXR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	1223

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Name	Input Value
	7846
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7846
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKH	8974
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55
	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	1223
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1
target i2cREG1 temp.OAR	10
	1.0

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Name	Input Value		
target_i2cREG1_temp.IMR	10		
target_i2cREG1_temp.STR	1223		
target_i2cREG1_temp.CLKL	7846		
target_i2cREG1_temp.CLKH	8974		
target_i2cREG1_temp.CNT	98		
target_i2cREG1_temp.DRR	12		
target_i2cREG1_temp.SAR	10		
target_i2cREG1_temp.DXR	10		
target_i2cREG1_temp.MDR	7846		
target_i2cREG1_temp.IVR	55		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	10		
target_i2cREG1_temp.PID11	8974		
target_i2cREG1_temp.PID12	10		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	2		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	1		
Name	Actual Value	Expected Value	Resul
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8	8	•
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	•
DigColPsInt Buffer Cnt M u08[1]	3	3	

<u> </u>			
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	1		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8	8	~
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	~
DigColPsInt_Buffer_Cnt_M_u08[1]	3	3	~
DigColPsInt_Buffer_Cnt_M_u08[2]	7	7	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	7846	7846	~
DigColPsInt_CurrentSlave_Cnt_M_u08	74	74	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADADDRREG_SEN	INIT_SENSOR1_EXTREADADDRREG_SEN	~
DigColPsInt_I2CHwCustData_Uls_M_u16	40	40	~
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	41	41	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	~
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	98	98	~
DigColPsInt_TransactionCnt_Cnt_M_u08	12	12	~
I2c_Send(Length_Cnt_T_u32)	3	3	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10	10	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR	1223	1223	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT	98	98	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR	12	12	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR	10	10	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR	10	10	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR	7846	7846	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	55	55	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	8974	8974	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR			<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	10	-

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Name	Actual Value	Expected Value	Result
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	1223	1223	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98	98	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10	10	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	10 7846	<i>y</i>
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846 55	55	
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	1	1	_
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	10	10	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974	8974	_
target I2c Send I2cRegPtr Cnt T str.PID12	10	10	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	·
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10	10	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10	10	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223	1223	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98	98	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	12	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10	10	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10	10	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846	7846	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55	55	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10	10	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974	8974	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10	10	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10	10	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	1223	1223	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	98	98	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12	12	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	10	10	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	10	10	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7846	7846	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	55	55	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	10	10	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974	8974	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10	10	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL		1	<b>✓</b>

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10	10	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	10	10	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223	1223	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98	98	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12	12	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10	10	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10	10	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846	7846	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55	55	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10	10	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	8974	8974	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	10	10	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10	10	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10	10	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223	1223	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98	98	<b>-</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10	10	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10	10	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846	7846	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55	55	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10	10	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974	8974	<b>-</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10	10	<b>-</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	•

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupWriteData	1	SetupWriteData	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c_Send	1	I2c_Send	1	•

Test Step 2.15 (Repeat Count = 1)		✓
Name	Input Value	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	10	
DigColPsInt_Buffer_Cnt_M_u08[0]	1	
DigColPsInt_Buffer_Cnt_M_u08[1]	5	
DigColPsInt_Buffer_Cnt_M_u08[2]	9	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	
DigColPsInt_ColSnsrData_Cnt_M_u16	847	
DigColPsInt_CurrentSlave_Cnt_M_u08	20	
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_GETDATA	
DigColPsInt_I2CHwCustData_Uls_M_u16	43	

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Name	Input Value
0igColPsInt_I2CHwIncompleteCustData_UIs_M_u16	44
igColPsInt_InitFailedOnce_Cnt_M_Igc	1
ligColPsInt_NackOccured_Cnt_M_lgc	0
igColPsInt_PrevReqDataType_Cnt_M_u08	4
higColPsInt_RecvOverrunError_Cnt_M_lgc	0
igColPsInt_RecvdDataType_Cnt_M_u08	4
igColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
igColPsInt_SpurCustDatFound_Cnt_M_lgc	0
igColPsInt_SpurSnsrData_Cnt_M_u16	487
igColPsInt_TransactionCnt_Cnt_M_u08	13
lags_Cnt_T_b16	32
cc GenStopCond(I2cRegPtr Cnt T str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
2c Send(I2cRegPtr Cnt T str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
_DataRegisters_Cnt_u08[0]	0
_DataRegisters_Cnt_u08[1]	32
	30
_DataRegisters_Cnt_u08[2]	
_DataRegisters_Cnt_u08[3]	36
_DataRegisters_Cnt_u08[4]	38
_DataRegisters_Cnt_u08[5]	34
_DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
_DataRegisters_Cnt_u08[8]	14
tcREG1_temp	target_i2cREG1_temp
_ColSensorl2CAddress_Cnt_u08	79
_SpurSensorI2CAddress_Cnt_u08	110
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	34
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	24
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	455
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	847
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	987
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	487
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	34
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	34
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	24
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	847
arget I2c GenStopCond I2cRegPtr Cnt T str.IVR	56
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2
arget I2c GenStopCond I2cRegPtr Cnt T str.PSC	24
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	987
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	24
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
urget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3
rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2
irget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3
irget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2
rget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24
rget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847
rrget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34
rget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24
rget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847
rget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56
rget_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	2
	2 24
rget_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
rget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
grant 12a Sand 12aBaaBtr Cnt T atr DIB	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	

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Name	Input Value	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	
	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	34	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	24	
	455	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR		
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	847	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	987	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	487	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	34	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	34	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	24	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	847	
	56	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	24	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	987	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	24	
target I2c SetRecv I2cRegPtr Cnt T str.DMAC	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	34	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	24	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	455	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	847	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	987	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	487	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	34	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	34	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	24	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	847	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	56	
target I2c SetStatus I2cRegPtr Cnt T str.EMDR	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	24	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	987	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	24	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	
target I2c SetStatus I2cRegPtr Cnt T str.SET	2	
	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR		
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	34	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	24	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	455	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	847	
	987	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	487	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	34	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	34	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	24	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	847	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	56	
	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	24	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	987	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	24	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	
0		

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Name	Input Value		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIR	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	847		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	987		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	34 34		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	987		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	24		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2		
target_i2cREG1_temp.OAR	34		
target_i2cREG1_temp.IMR	24		
target_i2cREG1_temp.STR	455		
target_i2cREG1_temp.CLKL	847		
target_i2cREG1_temp.CLKH	987 487		
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	34		
target i2cREG1_temp.SAR	34		
target_i2cREG1_temp.DXR	24		
target i2cREG1 temp.MDR	847		
target i2cREG1 temp.IVR	56		
target_i2cREG1_temp.EMDR	2		
target i2cREG1 temp.PSC	24		
target_i2cREG1_temp.PID11	987		
target_i2cREG1_temp.PID12	24		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	3		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.CLR	3		
target_i2cREG1_temp.ODR	3		
target_i2cREG1_temp.PD	2		
target_i2cREG1_temp.PSL	2	1	
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	10	10	~
DigColPsInt_Buffer_Cnt_M_u08[0]	38	38	<b>V</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	5	5	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[2]	9	9	<b>V</b>
DigColPsInt_BusBusySeqError_Cnt_M_Igc	0	0	<b>*</b>
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	Ž
DigColPsInt_ColCustDatFound_Cnt_M_Igc DigColPsInt_ColSnsrData_Cnt_M_u16	261	261	<b>V</b>
DigColPsInt_ColsnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08	110	110	
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ SENSOR2 SETREG	READ_SENSOR2_SETREG	-
DigColPsInt_I2CHwCustData_Uls_M_u16	43	43	-
DigColPsInt I2CHwlncompleteCustData Uls M u16	44	44	-
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	-
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	<b>✓</b>

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Name	Actual Value	Expected Value	Result
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	•
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	<b>✓</b>
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	· ·
DigColPsInt_SpurSnsrData_Cnt_M_u16	487	487	
DigColPsInt_TransactionCnt_Cnt_M_u08	13	13	
I2c_Send(Length_Cnt_T_u32)	1	1	
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	34	34	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR	24	24	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.NR	455	455	<u> </u>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	847	847	
target I2c GenStopCond I2cRegPtr Cnt T str.CLKH	987	987	<b>✓</b>
target I2c GenStopCond I2cRegPtr Cnt T str.CNT	487	487	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	34	34	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	34	34	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	24	24	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	847	847	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	56	56	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	2	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	24	24	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	987	987	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	24	24	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	3	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	3	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	2	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>v</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	2	2	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	34	34	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	24 455	24 455	
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	847	847	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987	987	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487	487	·
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34	34	
target I2c Send I2cRegPtr Cnt T str.SAR	34	34	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24	24	~
target I2c Send I2cRegPtr Cnt T str.MDR	847	847	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56	56	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24	24	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987	987	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24	24	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>✓</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	34	34	<b>~</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	24	24	<b>•</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	455	455	<u> </u>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	847	847	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	987 487	987 487	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	34	34	
	34	34	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	24	24	
target_l2c_SetRecv_l2cRegPtr_Cnt_1_str.DXR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	847	847	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	56	56	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	24	24	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	987	987	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	24	24	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
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Name	Actual Value	Expected Value	Resul
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	0	0	·
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3 2	3 2	
target I2c SetRecv I2cRegPtr Cnt T str.SET	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	34	34	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	24	24	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	455	455	,
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	847	987	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	987 487	487	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR	34	34	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	34	34	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	24	24	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	847	847	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	56	56	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	24	24	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	987	987	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	24	24	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3 3	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	34	34	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	24	24	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	455	455	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	847	847	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	987	987	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	487	487	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	34 34	34 34	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DXR	24	24	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	847	847	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	56	56	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	24	24	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	987	987	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	24	24	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT target_I2c SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2 2	2 2	
target I2c SetupMasterReceive I2cRegPtr_Cnt_T_str.SET	3	3	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	34	34	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24	24	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	455	455	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	847	847	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987	987	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487	487	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34	34	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34	34	·
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	24	24	•
PROPERTY OF SATURAGE FOR PROPERTY CONTRACTOR OF THE PROPERTY O	847	847	•
	56		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	56	56	
	56 2 24	2 24	

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24	24	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	~

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Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c_Send	1	l2c_Send	1	~

Name	Input Value
	1
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	10
DigColPsInt_Buffer_Cnt_M_u08[0]	20
DigColPsInt_Buffer_Cnt_M_u08[1]	30
DigColPsInt_Buffer_Cnt_M_u08[2]	1
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	30
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_GETDATA
DigColPsInt_I2CHwCustData_Uls_M_u16	46
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	47
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	14
Flags_Cnt_T_b16	32
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Γ_DataRegisters_Cnt_u08[0]	0
Γ_DataRegisters_Cnt_u08[1]	32
Γ_DataRegisters_Cnt_u08[2]	30
Γ_DataRegisters_Cnt_u08[3]	36
Γ_DataRegisters_Cnt_u08[4]	38
Γ_DataRegisters_Cnt_u08[5]	34
Γ_DataRegisters_Cnt_u08[6]	10
Γ_DataRegisters_Cnt_u08[7]	12
Γ_DataRegisters_Cnt_u08[8]	14
2cREG1_temp	target_i2cREG1_temp
ColSensorl2CAddress_Cnt_u08	84
c_SpurSensorI2CAddress_Cnt_u08	120
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
arget I2c GenStopCond I2cRegPtr Cnt T str.CLKH	1204
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
rarget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
rarget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
rarget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR	2309

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Name	Input Value	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	
arget I2c GenStopCond I2cRegPtr Cnt T str.SET	3	
rarget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	
rarget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	
rarget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	
	2309	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
target I2c SetRecv I2cRegPtr Cnt T str.OAR	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	556	
target_i2c_SetRecv_i2cRegPtr_Cnt_T_str.CLKL	2309	
arget_12c_SetRecv_12cRegPtr_Cnt_T_str.CLKH	1204	
	87	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.NTR	556	
	2309	
rarget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL		
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	
arget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR arget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR	67	
	55	

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Name	Input Value
	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target I2c SetStatus I2cRegPtr Cnt T str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
	3
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	66
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	3
	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target i2cREG1 temp.IMR	66
target_i2cREG1_temp.STR	556
	2309
target_i2cREG1_temp.CLKL	
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87



		(	- 100
Name	Input Value		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR	2309		
target i2cREG1_temp.EMDR	3		
target i2cREG1 temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET	3		
target i2cREG1 temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	~
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	<b>*</b>
DigColPoint_ColCustDatFound_Cnt_M_lgc	1 2580	1 2580	
DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08	120	120	
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_GETDATA	READ_SENSOR2_GETDATA	_
DigColPsInt_I2CHwCustData_Uls_M_u16	46	46	_
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	47	47	<b>✓</b>
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	~
DigColPsInt_RecvOverrunError_Cnt_M_Igc	1	1	~
DigColPsInt_RecvdDataType_Cnt_M_u08	5	5	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	
DigColPsInt_TransactionCnt_Cnt_M_u08	14	14	
I2c_SetRecv(Length_Cnt_T_u32) I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	_
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR	67	67	<b>*</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55 66	· ·
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR	66 2309	2309	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	_
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR	1	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CDR	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target 12c Send 12cDeaDtr Cnt T etr STD		556	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	000	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	556 2309	2309	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	2309 1204	2309 1204	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target I2c SetRecv I2cRegPtr Cnt T str.OAR	55	55	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	·
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	
target_12c_SetRecv_12cRegPtr_Cnt_1_str.CN1 target_12c_SetRecv_12cRegPtr_Cnt_T_str.DRR	67	67	
	55	55	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	66	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR			
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✓
target I2c SetRecv I2cRegPtr Cnt T str.PD	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<u> </u>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	87	87	•
target I2c SetStatus I2cRegPtr_Cnt_T_str.CNT	67	67	
		55	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	66	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	66		-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>v</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_i2c_SetStatus_i2cRegPtr_Cnt_T_str.PD	3	3	·
target_i2c_SetStatus_i2cRegPtr_Cnt_T_str.PSL	3	3	
	55	55	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR			
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	556	556	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>•</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	· ·

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>•</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✓

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Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	~
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	<b>✓</b>
I2c SetRecv	1	I2c SetRecv	1	<b>✓</b>

Test Step 2.17 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3
DigColPsInt_Buffer_Cnt_M_u08[0]	22
DigColPsInt_Buffer_Cnt_M_u08[1]	44
DigColPsInt_Buffer_Cnt_M_u08[2]	55
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	495
DigColPsInt_CurrentSlave_Cnt_M_u08	40
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_GETDATA
DigColPsInt_I2CHwCustData_Uls_M_u16	49
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	50
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0



Name	Input Value	
DigColPsInt_RecvdDataType_Cnt_M_u08	1	
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	
)igColPsInt_SpurSnsrData_Cnt_M_u16	897	
DigColPsInt_TransactionCnt_Cnt_M_u08	6	
Flags_Cnt_T_b16	32	
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str	
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str	
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str	
2c SetStatus(I2cRegPtr Cnt T str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str	
2c SetupMasterReceive(I2cRegPtr Cnt T str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str	
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str	
DataRegisters Cnt u08[0]	0	
uataRegisters_Cnt_u08[1]	32	
DataRegisters_Cnt_u08[2]	30	
DataRegisters_Cnt_u08[3]	36	
DataNegisters_Cnt_u08[4]	38	
	34	
DataRegisters_Cnt_u08[5]		
_DataRegisters_Cnt_u08[6]	10	
_DataRegisters_Cnt_u08[7]	12	
_DataRegisters_Cnt_u08[8]	14	
2cREG1_temp	target_i2cREG1_temp	
_ColSensorI2CAddress_Cnt_u08	89	
_SpurSensorl2CAddress_Cnt_u08	5	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	78	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	78	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	495	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	56	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	897	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	98	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	78	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	495	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	78	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	56	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	78	
arget I2c GenStopCond I2cRegPtr Cnt T str.DMAC	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	
arget I2c GenStopCond I2cRegPtr Cnt T str.DOUT	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	
liget_l2c_send_l2cRegPtr_Cnt_T_str.PID11	56	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	78	
	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	

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Name	Input Value
	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66
target I2c SetRecv I2cRegPtr Cnt T str.EMDR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78
	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
target I2c SetRecv I2cRegPtr Cnt T str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0
	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	0
target I2c SetStatus I2cRegPtr Cnt T str.OAR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	78
	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	495
	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	78
target I2c SetStatus I2cRegPtr Cnt T str.DMAC	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0
target I2c SetupMasterReceive I2cRegPtr Cnt T str.OAR	66
· ·	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DXR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	0

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Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	56 897		
target_12c_SetupMasterTransmit_12cRegPti_Cnt_T_str.CNT target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR	98		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	66		
target_i2cREG1_temp.OAR target_i2cREG1_temp.IMR	78		
target_i2cREG1_temp.STR	78		
target i2cREG1 temp.CLKL	495		
target i2cREG1 temp.CLKH	56		
target i2cREG1 temp.CNT	897		
target_i2cREG1_temp.DRR	98		
target_i2cREG1_temp.SAR	66		
target_i2cREG1_temp.DXR	78		
target_i2cREG1_temp.MDR	495		
target_i2cREG1_temp.IVR	66		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	78		
target_i2cREG1_temp.PID11	56		
target_i2cREG1_temp.PID12	78		
target_i2cREG1_temp.DMAC	0		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT	0		
target_i2cREG1_temp.SET	0		
target i2cREG1 temp.CLR	0		
target i2cREG1 temp.ODR	1		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3	3	- Result
DigColPsInt Buffer Cnt M u08[0]	0	0	- J
DigColPsInt_Buffer_Cnt_M_u08[1]	44	44	
DigColPsInt_Buffer_Cnt_M_u08[2]	55	55	-
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	-
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	-
DigColPsInt_ColSnsrData_Cnt_M_u16	5676	5676	-
DigColPsInt_CurrentSlave_Cnt_M_u08	5	5	<b>✓</b>
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_SETREG	READ_SENSOR2_SETREG	•
DigColPsInt_I2CHwCustData_UIs_M_u16	49	49	-
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	50	50	<b>✓</b>
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	•
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt RecvdDataType Cnt M u08	1	1	<b>✓</b>
		1.0	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	
	0 897 6	897 6	Š

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Name	Actual Value	Expected Value	Result
I2c_Send(Length_Cnt_T_u32)	1	1	<b>*</b>
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1 66	1 66	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR	78	78	
target I2c GenStopCond I2cRegPtr Cnt T str.STR	78	78	·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	495	495	_
target I2c GenStopCond I2cRegPtr Cnt T str.CLKH	56	56	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	98	98	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	66	66	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	78	78	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC	78	78	<b>~</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11	56	56	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	78	78	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	0	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target I2c GenStopCond I2cRegPtr Cnt T str.PD	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	<b>~</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	78	78	
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	495	495	<b>Y</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0 78	0 78	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	56	56	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11 target_l2c Send_l2cRegPtr_Cnt_T_str.PID12	78	78	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	
target I2c Send I2cRegPtr Cnt T str.FUN	0	0	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	78	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78	78	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	495	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	56	<b>*</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	897	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	98	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66 78	66 78	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	495	495	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	66	66	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	0	0	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.PSC	78	78	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	56	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78	78	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	~



Name	Actual Value	Expected Value	Resul
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	66	66	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR	78	78	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	78	78	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL	495	495	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	56	56	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	897	897	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	98	98	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	78 495	78 495	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	78	78	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	56	56	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	78	78	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR	0	0	·
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	
target_12c_SetStatus_12cRegPtr_Crit_1_str.SE1 target_12c_SetStatus_12cRegPtr_Crit_T_str.CLR	0	0	
target_i2c_SetStatus_i2cRegPtr_Cnt_T_str.ODR	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	66	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78	78	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78	78	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495	495	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56	56	•
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	897	897	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	98	98 66	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	78	78	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495	495	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66	66	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78	78	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56	56	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78	78	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	•
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	0	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR target_I2c SetupMasterReceive I2cRegPtr Cnt T str.DIN	0	0	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	0	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	0	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	78	78	·
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	78	78	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	56 897	56 897	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	98	98	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN		· · · · · · · · · · · · · · · · · · ·	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	•

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>

Τ			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c Send	1	I2c Send	1	-

Test Step 2.18 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	5
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	15
DigColPsInt_Buffer_Cnt_M_u08[2]	16
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	566
DigColPsInt_CurrentSlave_Cnt_M_u08	50
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_GETDATA
DigColPsInt_I2CHwCustData_Uls_M_u16	52
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	53
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt SpurSnsrData Cnt M u16	129
DigColPsInt_TransactionCnt_Cnt_M_u08	7
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c SetStatus(I2cRegPtr Cnt T str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
	14
T_DataRegisters_Cnt_u08[8]	
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	94
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44

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Name	
	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
arget I2c Send I2cRegPtr Cnt T str.STR	4444
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
arget_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	129
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
arget_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	554
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	44
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	4444
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
rarget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	4466
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554
arget I2c SetRecv I2cRegPtr Cnt T str.EMDR	1
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
rarget_12c_SetRecv_12cRegPtr_Cnt_T_str.PSL	3
arget_12c_SetStatus_12cRegPtr_Cnt_T_str.OAR	567
rarget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44
rarget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466
rarget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129
argor_120_00101atao_120110gFtt_011t_1_5tt.0111	6
arget 12c SatStatus 12cPacPtr Cnt T ctr DDP	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	
rarget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR rarget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	44 566
rarget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR rarget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44

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Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1 2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567 44
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	4444
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	554
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSC	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444 566
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	4466
target I2c SetupMasterTransmit I2cReqPtr Cnt T str.CNT	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	2 0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_1_str.ODR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6 567
	301
target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR	44 566

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Name	Input Value		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	44		
target_i2cREG1_temp.PID11	4466		
target_i2cREG1_temp.PID12	44		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	2		
target_i2cREG1_temp.DIN	0		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result

	1-		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	5	5	✓
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✓
DigColPsInt_Buffer_Cnt_M_u08[1]	15	15	✓
DigColPsInt_Buffer_Cnt_M_u08[2]	16	16	✓
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✓
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✓
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	<b>✓</b>
DigColPsInt_ColSnsrData_Cnt_M_u16	566	566	<b>✓</b>
DigColPsInt_CurrentSlave_Cnt_M_u08	50	50	<b>✓</b>
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE	READ_COMPLETE	<b>✓</b>
DigColPsInt_I2CHwCustData_Uls_M_u16	52	52	<b>✓</b>
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	53	53	<b>✓</b>
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	<b>✓</b>
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✓
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt_RecvdDataType_Cnt_M_u08	5	5	<b>✓</b>
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✓
DigColPsInt_SpurSnsrData_Cnt_M_u16	2575	2575	✓
DigColPsInt_TransactionCnt_Cnt_M_u08	8	8	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	567	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	44	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	4444	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566	566	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129	129	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	6	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	567	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	44	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	566	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	554	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	44	

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	/\tosuit
target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	1	1	
target_I2C_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	566	4444 566	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	1	1	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2C_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>*</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR	4444	4444	<b>*</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH	566 4466	566 4466	J
target_12c_SetStatus_12cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	554	554	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC	44	44	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target I2c SetStatus I2cRegPtr Cnt T str.PID12	44	44	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	1 2	1 2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566 4466	566 4466	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	129	129	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	~

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**Actual Value Expected Value**  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.PSC$ target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.PID11 target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.PID12  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.DMAC$ target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.FUN target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.DIR target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.DIN  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.DOUT$ target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.SET  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.CLR$ target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.ODR  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.PD$ target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.PSL target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IMR$  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.STR$  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKL$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKH  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CNT$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DRR  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SAR$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DXR  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.MDR$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IVR  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.EMDR$  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSC$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID11 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID12  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DMAC$  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.FUN$ target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIN n target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SET$  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLR$  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.ODR$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PD  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSL$ 

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Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 2.19 (Repeat Count = 1)	Innuit Value
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	7
DigColPsInt_Buffer_Cnt_M_u08[0]	28
DigColPsInt_Buffer_Cnt_M_u08[1]	56
DigColPsInt_Buffer_Cnt_M_u08[2]	100
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	7
DigColPsInt_CurrentSlave_Cnt_M_u08	60
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_GETDATA
DigColPsInt_I2CHwCustData_Uls_M_u16	55
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	56
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	88
DigColPsInt_TransactionCnt_Cnt_M_u08	8
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c SetRecv(I2cRegPtr Cnt T str)	target I2c SetRecv I2cRegPtr Cnt T str

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Input Value I2c\_SetStatus(I2cRegPtr\_Cnt\_T\_str)  $target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str$ I2c\_SetupMasterReceive(I2cRegPtr\_Cnt\_T\_str) target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str I2c\_SetupMasterTransmit(I2cRegPtr\_Cnt\_T\_str) target I2c SetupMasterTransmit I2cRegPtr Cnt T str T\_DataRegisters\_Cnt\_u08[0] T\_DataRegisters\_Cnt\_u08[1] 32 T\_DataRegisters\_Cnt\_u08[2] 30 T\_DataRegisters\_Cnt\_u08[3] 36 T\_DataRegisters\_Cnt\_u08[4] 38 T\_DataRegisters\_Cnt\_u08[5] 34 T\_DataRegisters\_Cnt\_u08[6] 10 T\_DataRegisters\_Cnt\_u08[7] 12 T\_DataRegisters\_Cnt\_u08[8] 14 target\_i2cREG1\_temp i2cREG1\_temp k ColSensorl2CAddress Cnt u08 99 k\_SpurSensorl2CAddress\_Cnt\_u08 15  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.OAR$ 65 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.IMR 89 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.STR 67 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKL 7 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKH 577 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CNT 88 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DRR 23  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.SAR$ 65 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DXR 89  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.MDR$ 7  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.IVR$ 44  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.EMDR$ 2 89 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PSC target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PID11 577  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PID12$ 89 target I2c GenStopCond I2cRegPtr Cnt T str.DMAC 2 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.FUN 0 target I2c GenStopCond I2cRegPtr Cnt T str.DIR 0  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DIN$ 1 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DOUT 2 target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.SET 2  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLR$ 0  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.ODR$ target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PD 2 target I2c GenStopCond I2cRegPtr Cnt T str.PSL 0 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.OAR 65 target I2c Send I2cRegPtr Cnt T str.IMR 89 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.STR 67 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKL  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKH$ 577 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CNT 88 23 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DRR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SAR 65  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DXR$ 89 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.MDR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IVR 44 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.EMDR 2 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSC 89 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID11 577 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PID12 89  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DMAC$ 2 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.FUN 0 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIR n target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIN 1  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DOUT$ 2 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SET 2 0 target I2c Send I2cRegPtr Cnt T str.CLR  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.ODR$ 1 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PD 2 target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSL 0 target I2c SetRecv I2cRegPtr Cnt T str.OAR 65 target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.IMR 89 target I2c SetRecv I2cRegPtr Cnt T str.STR 67 target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.CLKL 7 target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.CLKH 577 88  $target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.CNT$ target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DRR 23 65  $target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.SAR$ 

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Name	Input Value	
	·	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	89	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	
target I2c SetRecv I2cRegPtr Cnt T str.PSC	89	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	89	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	
	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577	
target I2c SetStatus I2cRegPtr Cnt T str.CNT	88	
	23	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR		
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	577	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	
target I2c SetStatus I2cRegPtr Cnt T str.CLR	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	
	2	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD		
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67	
target I2c SetupMasterReceive I2cReqPtr Cnt T str.CLKL	7	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKH	577	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	89	
	67	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	7	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	

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DigColPsInt\_InterruptNotification

DigColFSirit_Interruptivotinication		•	OIL CITORIO
Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11 target_I2c SetupMasterTransmit_I2cRegPtr_Cnt_T str.PID12	577 89		
target I2c SetupMasterTransmit I2cRegPtr_Cnt_1_str.PiD12	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target I2c SetupMasterTransmit I2cReqPtr Cnt T str.DIR	0		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
target_i2cREG1_temp.OAR	65		
target_i2cREG1_temp.IMR	89		
target_i2cREG1_temp.STR	67		
target_i2cREG1_temp.CLKL	7		
target_i2cREG1_temp.CLKH	577		
target_i2cREG1_temp.CNT	88		
target_i2cREG1_temp.DRR	23		
target_i2cREG1_temp.SAR	65		
target_i2cREG1_temp.DXR	89 7		
target_i2cREG1_temp.MDR	44		
target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR	2		
target_i2cREG1_temp.PSC	89		
target i2cREG1 temp.PID11	577		
target i2cREG1 temp.PID12	89		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	2		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	7	7	~
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	~
DigColPsInt_Buffer_Cnt_M_u08[1]	56	56	
DigColPsInt_Buffer_Cnt_M_u08[2]	100	100	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	<b>V</b>
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	0	· ·
DigColPsInt_ColCustDatFound_Cnt_M_lgc	7224	7224	
DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08	15	15	
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_SETREG	READ_SENSOR2_SETREG	_
DigColPsInt_I2CHwCustData_Uls_M_u16	55	55	
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	56	56	<b>✓</b>
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	<b>✓</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	<b>✓</b>
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	88	88	~
DigColPsInt_TransactionCnt_Cnt_M_u08	8	8	~
I2c_Send(Length_Cnt_T_u32)	1	1	_
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	1 65	1 65	· ·

89

67

577

88

23

89

67

577

88 23

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.IMR$ 

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.STR

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKL\\ target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKH\\$ 

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CNT$ 

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65	65 89	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR	89 7	7	
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.IVR	44	44	~
target I2c GenStopCond I2cRegPtr Cnt T str.EMDR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89	89	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR	0	0	<b>y</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT	2	2	
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	23 65	23 65	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	
target I2c Send I2cRegPtr Cnt T str.MDR	7	7	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0	0	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0 1	1	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65	65	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7 577	7 577	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	88	88	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.DRR	23	23	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	65	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	7	7	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44	44	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	89	89	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	2	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	0	0	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR	65	65	<b>*</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67 7	67 7	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH	577	577	
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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR	23	23	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7	7	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	65	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67	67	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23	23	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44	44	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89	89	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89	89	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIN	1	1	<b>~</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	2	2	~
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SET	2	2	
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLR	0	0	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	1	1	9
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	2	2	
			-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	<b>V</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	<b>V</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	88	88	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	23	23	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~
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T .		<b>✓</b>		
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c Send	1	I2c Send	1	<b>✓</b>

est Step 2.20 (Repeat Count = 1)	
ame	Input Value
igColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	9
igColPsInt_Buffer_Cnt_M_u08[0]	123
igColPsInt_Buffer_Cnt_M_u08[1]	145
igColPsInt_Buffer_Cnt_M_u08[2]	200
igColPsInt_BusBusySeqError_Cnt_M_lgc	1
igColPsInt_CmdFailOccurred_Cnt_M_lgc	1
igColPsInt_ColCustDatFound_Cnt_M_lgc	0
igColPsInt_ColSnsrData_Cnt_M_u16	554
igColPsInt_CurrentSlave_Cnt_M_u08	70
igColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_GETDATA
igColPsInt_I2CHwCustData_Uls_M_u16	58
igColPsInt_I2CHwIncompleteCustData_Uls_M_u16	59
igColPsInt_InitFailedOnce_Cnt_M_lgc	0
igColPsInt_NackOccured_Cnt_M_lgc	1
igColPsInt_PrevReqDataType_Cnt_M_u08	1
igColPsInt_RecvOverrunError_Cnt_M_lgc	1
igColPsInt RecvdDataType Cnt M u08	4
igColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
igColPsInt_SpurCustDatFound_Cnt_M_lgc	1
igColPsInt_SpurSnsrData_Cnt_M_u16	123
igColPsInt TransactionCnt Cnt M u08	0
ags_Cnt_T_b16	32
c_GenStopCond(I2cRegPtr_Cnt_T_str)	target I2c GenStopCond I2cRegPtr Cnt T str
c_Send(I2cRegPtr_Cnt_T_str)	target I2c Send I2cRegPtr Cnt T str
c SetRecv(I2cRegPtr_Cnt_T_str)	V V
_ , , , ,	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
tc_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
_DataRegisters_Cnt_u08[0]	0
_DataRegisters_Cnt_u08[1]	32
_DataRegisters_Cnt_u08[2]	30
_DataRegisters_Cnt_u08[3]	36
_DataRegisters_Cnt_u08[4]	38
_DataRegisters_Cnt_u08[5]	34
_DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
_DataRegisters_Cnt_u08[8]	14
cREG1_temp	target_i2cREG1_temp
_ColSensorl2CAddress_Cnt_u08	104
_SpurSensorI2CAddress_Cnt_u08	20
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	54
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC	66
rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11	344
rget I2c GenStopCond I2cRegPtr Cnt T str.PID12	66
rget_12c_GenStopCond_12cRegPtr_Cnt_T_str.DMAC	3
rget_12c_GenStopCond_12cRegPtr_Cnt_1_str.DMAC  rget_12c_GenStopCond_12cRegPtr_Cnt_T_str.FUN	1
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3
	2
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
rget_lzc_GenStopCond_lzcRegPtr_Cnt_1_str.DIN rget_lzc_GenStopCond_lzcRegPtr_Cnt_T_str.DOUT rget_lzc_GenStopCond_lzcRegPtr_Cnt_T_str.SET	3 3

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Name target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	Input Value 2 1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	
target_I2c_GenStopCond_I2cRegPtr_Cnt_I_str.PSL	
	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45
	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target I2c Send I2cRegPtr Cnt T str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target I2c Send I2cRegPtr Cnt T str.PSL	2
	54
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554
	344
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target I2c SetRecv I2cRegPtr Cnt T str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target I2c SetRecv I2cRegPtr Cnt T str.DIR	3
·	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	3
target I2c SetRecv I2cRegPtr Cnt T str.CLR	3
target I2c SetRecv I2cRegPtr Cnt T str.ODR	2
· · · · · · · · · · · · · · · ·	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	123
	45
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	
target_12c_SetStatus_12cRegPtr_Cnt_1_str.DMAC target_12c_SetStatus_12cRegPtr_Cnt_T_str.FUN	1
	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	

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Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	554 344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54
target I2c SetupMasterTransmit I2cReqPtr Cnt T str.DXR	66
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	66
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2
target_i2cREG1_temp.OAR	54
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	8
target_i2cREG1_temp.CLKL	554
target_i2cREG1_temp.CLKH	344
target_i2cREG1_temp.CNT	123
target_i2cREG1_temp.DRR	45
target_i2cREG1_temp.SAR	54
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	554
target_i2cREG1_temp.IVR	788
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	344
torget (2ePEC4 temp PID42	66
target_i2cREG1_temp.PID12	
target_izcREG1_temp.PHD12 target_izcREG1_temp.DMAC	3

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DigColPsInt\_InterruptNotification

Name	Input Value		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	3 2		
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	2		
Name	Actual Value	Expected Value	Result
DigColPsInt AttempOccurForCustDatRead Cnt M u08	9	9	Kesuk
DigColPsInt Buffer Cnt M u08[0]	123	123	•
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	-
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	<b>✓</b>
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	•
DigColPsInt_CmdFailOccurred_Cnt_M_Igc	1	1	<b>✓</b>
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt_ColSnsrData_Cnt_M_u16	554	554	<b>*</b>
DigColPsInt_CurrentSlave_Cnt_M_u08	70	70	•
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt I2CHwCustData Uls M u16	READ_COMPLETE 58	READ_COMPLETE 58	
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	59	59	
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	-
DigColPsInt_RecvdDataType_Cnt_M_u08	1	1	<b>✓</b>
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	31633	31633	<b>✓</b>
DigColPsInt_TransactionCnt_Cnt_M_u08	1	1	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR	54	54	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66 8	66 8	<b>✓</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	554	554	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344	344	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123	123	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45	45	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	54	54	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554	554	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788	788	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC	66	66	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344 66	344 66	• • • • • • • • • • • • • • • • • • •
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC	3	3	
target I2c GenStopCond I2cRegPtr Cnt T str.FUN	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	<u> </u>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	1	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54 66	54 66	Ž
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	8	8	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554	554	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	344	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	123	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	45	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	54	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	554	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	788	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344 66	344 66	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12 target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	-
target I2c Send I2cRegPtr Cnt T str DOLIT	3	3	

3

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 $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SET$ 

 $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DOUT$ 

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54	54	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8	8	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554	554	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344	344	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123	123	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	45	45	<b>~</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	54	54	· ·
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	66 554	66 554	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788	788	·
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344	344	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	2 3	
target I2c SetRecv I2cRegPtr Cnt T str.SET	3	3	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54	54	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8	8	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554	554	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH	344 123	344 123	-
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR	45	45	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54	54	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554	554	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	788	788	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344 66	344 66	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	· ·
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL	1 2	1 2	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	54	54	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8	8	·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554	554	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344	344	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123	123	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45	45	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54	54	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>~</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	554 788	554 788	~
target_lzc_SetupMasterReceive_lzcRegPtr_Cnt_1_str.IVR target_lzc_SetupMasterReceive_lzcRegPtr_Cnt_T_str.EMDR	3	3	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344	344	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54	54	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8	8	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554	554	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344	344	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123	123	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45	45	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54	54	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554	554	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788	788	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344	344	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	~

Τ				V
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Input Value	Test Step 2.21 (Repeat Count = 1)	✓
DigColPsInt_Buffer_Cnt_M_u08[1]   200   DigColPsInt_Buffer_Cnt_M_u08[2]   250   DigColPsInt_Buffer_Cnt_M_u08[2]   250   DigColPsInt_BusBusySeqError_Cnt_M_lgc   0   DigColPsInt_ColCustDafFound_Cnt_M_lgc   0   DigColPsInt_ColCustDafFound_Cnt_M_lgc   1   DigColPsInt_ColCustDafFound_Cnt_M_lgc   8   DigColPsInt_ColCustDafFound_Cnt_M_lgc   8   DigColPsInt_ColCustDafFound_Cnt_M_lgc   8   DigColPsInt_ColCustDafFound_Cnt_M_lgc   1   DigColPsInt_Dist_M_lgc   1   DigColPsInt_IntFailedOnce_Cnt_M_lgc   1   DigColPsInt_IntFailedOnce_Cnt_M_lgc   0   DigColPsInt_NewCoverrunError_Cnt_M_lgc   0   DigColPsInt_RevCoverrunError_Cnt_M_lgc   0   DigColPsInt_RevCoverrunError_Cnt_M_lgc   0   DigColPsInt_RevCoverrunError_Cnt_M_lgc   0   DigColPsInt_SkipRegisterWrite_Cnt_M_lgc   0   DigColPsInt_SkipRegisterWrite_Cnt_M_lgc   0   DigColPsInt_SkipRegisterWrite_Cnt_M_lgc   0   DigColPsInt_SkipRegisterWrite_Cnt_M_lgc   0   DigColPsInt_SkipRegisterWrite_Cnt_M_lgc   0   DigColPsInt_TsurasationCnt_Cnt_M_ugs   255   DigColPsInt_Tsurasa	Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[1]   200     DigColPsInt_BusbusySeqError_Cnt_M_u08[2]   250     DigColPsInt_BusbusySeqError_Cnt_M_u06   0     DigColPsInt_CmdFailOccurred_Cnt_M_u06   0     DigColPsInt_ColCustDatFound_Cnt_M_u16   2767     DigColPsInt_ColCustDat_Ont_M_u16   2767     DigColPsInt_CurrentSlave_Cnt_M_u08   80     DigColPsInt_CurrentSlave_Cnt_M_u08   80     DigColPsInt_CurrentSlave_Cnt_M_u08   80     DigColPsInt_CurrentSlave_Cnt_M_u08   80     DigColPsInt_LowertSlave_Cnt_M_u08   80     DigColPsInt_LowertSlave_Cnt_M_u08   80     DigColPsInt_I2CHWcustData_Uis_M_u16   61     DigColPsInt_I2CHWcustData_Uis_M_u16   62     DigColPsInt_I2CHWncompleteCustData_Uis_M_u16   62     DigColPsInt_I2CHWncompleteCustData_Uis_M_u16   62     DigColPsInt_I2CHWncompleteCustData_Uis_M_u16   62     DigColPsInt_I2CHWncompleteCustData_Uis_M_u16   62     DigColPsInt_PrevReqDataTyne_Cnt_M_u08   2     DigColPsInt_PrevReqDataTyne_Cnt_M_u08   2     DigColPsInt_PrevReqDataTyne_Cnt_M_u08   2     DigColPsInt_PrevReqDataTyne_Cnt_M_u08   5     DigColPsInt_RevOverrunError_Cnt_M_u08   5     DigColPsInt_RevOverrunError_Cnt_M_u08   5     DigColPsInt_SpurCustDatFound_Cnt_M_u08   2     DigColPsInt_SpurCustDatFound_Cnt_M_u08   2     DigColPsInt_TransactionCnt_Cnt_M_u08   2     DigColPsInt_Transa	DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[2]   250     DigColPsInt_BusBusySegError_Cnt_M_lgc	DigColPsInt_Buffer_Cnt_M_u08[0]	100
DigColPsInt_BusBusySeqError_Cnt_M_lgc         0           DigCoPlsInt_ColCustDatForton_Cnt_M_lgc         0           DigCoPlsInt_ColCustDatForton_Cnt_M_lgc         1           DigCoPlsInt_ColSnsrData_Cnt_M_u16         2767           DigColPsInt_CurrentSiave_Cnt_M_u08         80           DigColPsInt_LownestData_UIs_M_u16         61           DigColPsInt_IntRepNo_Cnt_M_enum         READ_SENSOR2_GETDATA           DigColPsInt_IntRepNo_Cnt_M_lgc         61           DigColPsInt_IntRepNo_Cnt_M_lgc         1           DigColPsInt_IntRepNo_Cnt_M_lgc         0           DigColPsInt_NackOccured_Cnt_M_lgc         0           DigColPsInt_NackOccured_Cnt_M_lgc         0           DigColPsInt_PrevReqDataType_Cnt_M_u08         2           DigColPsInt_RevOverunError_Cnt_M_lgc         0           DigColPsInt_SpuPcustDatFound_Cnt_M_lgc         0           DigColPsInt_SpuPcustDatFound_Cnt_M_lgc         0           DigColPsInt_SpuPcustDatFound_Cnt_M_lgc         0           DigColPsInt_TransactionCnt_Ont_M_lgc         32           DigColPsInt_TransactionCnt_Ont_M_u16         54           DigColPsInt_TransactionCnt_Ont_M_u08         255           Flags_Cnt_T_b16         32           12c_SentopCond(l2cregPtr_Cnt_T_str)         target_l2c_SentopCond_l2cregPtr_Cnt_T_str <td>DigColPsInt_Buffer_Cnt_M_u08[1]</td> <td>200</td>	DigColPsInt_Buffer_Cnt_M_u08[1]	200
DigColPsInt_ColCustDaFound_Cnt_M_lgc         1           DigColPsInt_ColCustDaFound_Cnt_M_lgc         1           DigColPsInt_CurrentSlave_Cnt_M_u08         80           DigColPsInt_CurrentSlave_Cnt_M_u08         80           DigColPsInt_CurrentSlave_Cnt_M_uenum         READ_SENSOR2_GETDATA           DigColPsInt_IZCHwCoustData_Uls_M_u16         61           DigColPsInt_IZCHwIncompleteGustData_Uls_M_u16         62           DigColPsInt_InitFailedOnce_Cnt_M_lgc         1           DigColPsInt_NecVocured_Cnt_M_lgc         0           DigColPsInt_NecVocured_Cnt_M_u08         2           DigColPsInt_RecvDataType_Cnt_M_u08         5           DigColPsInt_RecvDataType_Cnt_M_u08         5           DigColPsInt_SpurCustDaTeroud_Cnt_M_lgc         0           DigColPsInt_SpurCustDaTeroud_Cnt_M_lgc         0           DigColPsInt_SpurCustDaTeroud_Cnt_M_lgc         0           DigColPsInt_SpurCustDaTeroud_Cnt_M_lgc         0           DigColPsInt_SpurCustDaTeroud_Cnt_M_lgc         0           DigColPsInt_SpurCustDaTeroud_Cnt_M_lgc         0           DigColPsInt_SpurCust_Tant_SpurCust_Tsir)         target_I2c_GenStopCond_I2cRegPtr_Cnt_Tsir           I2c_GenStopCond(I2cRegPtr_Cnt_T_str)         target_I2c_Sent_Int_Tsir           I2c_SentQ(I2cRegPtr_Cnt_T_str)         target_I2c_Sent_Int_Int_Set <td>DigColPsInt_Buffer_Cnt_M_u08[2]</td> <td>250</td>	DigColPsInt_Buffer_Cnt_M_u08[2]	250
DigColPsInt_ColCustDatFound_Cnt_M_lgc	DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsint_CurrentSlave_Cnt_M_u08   80	DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_CurrentStepNo_Cnt_M_enum	DigColPsInt_ColSnsrData_Cnt_M_u16	2767
DigCoIPsInt_12CHwCustData_UIs_M_u16         61           DigCoIPsInt_IctFilledOnce_Cnt_M_lgc         1           DigCoIPsInt_InitFilledOnce_Cnt_M_lgc         0           DigCoIPsInt_PrevReqDataType_Cnt_M_u08         2           DigCoIPsInt_RecvOverrunError_Cnt_M_lgc         0           DigCoIPsInt_RecvOdataType_Cnt_M_u08         5           DigCoIPsInt_SkipRegisterWrite_Cnt_M_lgc         0           DigCoIPsInt_SpurCustDatFound_Cnt_M_lgc         0           DigCoIPsInt_SpurSpurStoatCound_Cnt_M_lgc         0           DigCoIPsInt_TransactionCnt_Cnt_M_u08         255           Flags_Cnt_T_b16         32           12c_GenStopCond(l2cRegPtr_Cnt_T_str)         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str           12c_SentRecv(l2cRegPtr_Cnt_T_str)         target_l2c_Send_l2cRegPtr_Cnt_T_str           12c_SetRecv(l2cRegPtr_Cnt_T_str)         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str           12c_SetStatus(l2cRegPtr_Cnt_T_str)         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str           12c_SetQupMasterReceive(l2cRegPtr_Cnt_T_str)         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str           12c_SetUpMasterReceive(l2cRegPtr_Cnt_T_str)         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str           12c_SetUpMasterReceive(l2cRegPtr_Cnt_T_str)         target_l2c_SetUpMasterReceive_l2cRegPtr_Cnt_T_str           12c_SetUpMasterReceive(l2cRegPtr_Cnt_T_str)         target_l2c_SetUpMasterRe	DigColPsInt_CurrentSlave_Cnt_M_u08	80
DigCoIPsInt_I2CHwincompleteCustData_Uls_M_u16         62           DigCoIPsInt_InitFailedOnce_Cnt_M_lgc         1           DigCoIPsInt_NackOccured_Cnt_M_lgc         0           DigCoIPsInt_PrevReqDataType_Cnt_M_u08         2           DigCoIPsInt_RecvOverrunError_Cnt_M_lgc         0           DigCoIPsInt_RecvdDataType_Cnt_M_u08         5           DigCoIPsInt_SkipRegisterWrite_Cnt_M_lgc         0           DigCoIPsInt_SpurCustDatFound_Cnt_M_lgc         0           DigCoIPsInt_SpurSnsrData_Cnt_M_u16         564           DigCoIPsInt_TransactionCnt_Cnt_M_u08         255           Ilags_Cnt_T_b16         32           12c_GenStopCond(I2cRegPtr_Cnt_T_str)         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str           12c_Send(I2cRegPtr_Cnt_T_str)         target_I2c_Send_I2cRegPtr_Cnt_T_str           12c_SetRecv(I2cRegPtr_Cnt_T_str)         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str           12c_SetStatus(I2cRegPtr_Cnt_T_str)         target_I2c_SetSetatus_I2cRegPtr_Cnt_T_str           12c_SetUpMasterReceive(I2cRegPtr_Cnt_T_str)         target_I2c_SetSetatus_I2cRegPtr_Cnt_T_str           12c_SetUpMasterReceive(I2cRegPtr_Cnt_T_str)         target_I2c_SetUpMasterTransmit(I2cRegPtr_Cnt_T_str           12c_SetUpMasterTransmit(I2cRegPtr_Cnt_T_str)         target_I2c_SetUpMasterTransmit(I2cRegPtr_Cnt_T_str           12c_SetUpMasterTransmit(I2cRegPtr_Cnt_T_str)         target_I2c	DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_GETDATA
DigColPsInt_InitFailedOnce_Cnt_M_lgc	DigColPsInt_I2CHwCustData_Uls_M_u16	61
DigColPsInt_NackOccured_Cnt_M_lgc         0           DigColPsInt_PrevReqDataType_Cnt_M_u08         2           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0           DigColPsInt_RecvObataType_Cnt_M_u08         5           DigColPsInt_SkipRegisterWrite_Cnt_M_lgc         0           DigColPsInt_SpurCustDatFound_Cnt_M_lgc         0           DigColPsInt_SpurSnzData_Cnt_M_u16         564           DigColPsInt_TransactionCnt_Cnt_M_u08         255           Flags_Cntb16         32           12c_GenStopCond(l2cRegPtr_Cnt_T_str)         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str           12c_Send(l2cRegPtr_Cnt_T_str)         target_l2c_Send_l2cRegPtr_Cnt_T_str           12c_SetRecv(l2cRegPtr_Cnt_T_str)         target_l2c_SelRecv_l2cRegPtr_Cnt_T_str           12c_SetStatus(l2cRegPtr_Cnt_T_str)         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str           12c_SetupMasterReceive(l2cRegPtr_Cnt_T_str)         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str           12c_SetupMasterTransmit(l2cRegPtr_Cnt_T_str)         target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str           12c_SetupMasterTransmit(l2cRegPtr_Cnt_T_str)         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str           1_DataRegisters_Cnt_u08[1]         32           1_DataRegisters_Cnt_u08[2]         30	DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	62
DigColPsInt_PrevReqDataType_Cnt_M_u08         2           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0           DigColPsInt_RecvdDataType_Cnt_M_u08         5           DigColPsInt_SkipRegisterWrite_Cnt_M_lgc         0           DigColPsInt_SpurCustDatFound_Cnt_M_lgc         0           DigColPsInt_SpurSnsrData_Cnt_M_u16         564           DigColPsInt_TransactionCnt_Cnt_M_u08         255           Flags_Cntb16         32           12c_GenStopCond(l2cRegPtr_Cnt_T_str)         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str           12c_Send(l2cRegPtr_Cnt_T_str)         target_l2c_Send_l2cRegPtr_Cnt_T_str           12c_SetRecv(l2cRegPtr_Cnt_T_str)         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str           12c_SetStatus(l2cRegPtr_Cnt_T_str)         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str           12c_SetUpMasterReceive(l2cRegPtr_Cnt_T_str)         target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str           12c_SetupMasterTransmit(l2cRegPtr_Cnt_T_str)         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str           12c_SetupMasterTransmit(l2cRegPtr_Cnt_T_str)         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str           12c_DataRegisters_Cnt_u08[0]         0           1_DataRegisters_Cnt_u08[1]         32           1_DataRegisters_Cnt_u08[2]         30	DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc         0           DigColPsInt_RecvdDataType_Cnt_M_u08         5           DigColPsInt_SkipRegisterWrite_Cnt_M_lgc         0           DigColPsInt_SpurCustDatFound_Cnt_M_lgc         0           DigColPsInt_SpurSnsrData_Cnt_M_u16         564           DigColPsInt_TransactionCnt_Cnt_M_u08         255           Flags_Cnt_T_b16         32           12c_GenStopCond(l2cRegPtr_Cnt_T_str)         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str           12c_Send(l2cRegPtr_Cnt_T_str)         target_l2c_Send_l2cRegPtr_Cnt_T_str           12c_SertRecv(l2cRegPtr_Cnt_T_str)         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str           12c_SetStatus_(l2cRegPtr_Cnt_T_str)         target_l2c_SetStatus_(l2cRegPtr_Cnt_T_str           12c_SetUpMasterReceive(l2cRegPtr_Cnt_T_str)         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str           12c_SetupMasterTransmit(l2cRegPtr_Cnt_T_str)         target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str           12c_SetupMasterTransmit(l2cRegPtr_Cnt_T_str)         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str           1_DataRegisters_Cnt_u08[0]         0           1_DataRegisters_Cnt_u08[1]         32           1_DataRegisters_Cnt_u08[2]         30	DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc 0 DigColPsInt_SpurCustDatFound_Cnt_M_lgc 0 DigColPsInt_SpurSnsrData_Cnt_M_u16 564 DigColPsInt_TransactionCnt_Cnt_M_u08 255 Flags_Cnt_T_b16 32 I2c_GenStopCond(I2cRegPtr_Cnt_T_str) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str I2c_Send(I2cRegPtr_Cnt_T_str) target_I2c_Send_I2cRegPtr_Cnt_T_str I2c_SetRecv(I2cRegPtr_Cnt_T_str) target_I2c_SetRecv_I2cRegPtr_Cnt_T_str I2c_SetStatus(I2cRegPtr_Cnt_T_str) target_I2c_SetStatus_I2cRegPtr_Cnt_T_str I2c_SetUpMasterReceive(I2cRegPtr_Cnt_T_str) target_I2c_SetStatus_I2cRegPtr_Cnt_T_str I2c_SetUpMasterTransmit(I2cRegPtr_Cnt_T_str) 12c_SetUpMasterTransmit(I2cRegPtr_Cnt_T_str) 12c_SetUpMasterTransmit(I2cRegPtr_Cnt_T_str) 12c_SetUpMasterTransmit(I2cRegPtr_Cnt_T_str) 12c_SetUpMasterTransmit(I2cRegPtr_Cnt_T_str) 12c_SetUpMasterTransmit(I2cRegPtr_Cnt_T_str) 12c_SetUpMasterTransmit_I2cRegPtr_Cnt_T_str	DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc         0           DigColPsInt_SpurCustDatFound_Cnt_M_lgc         0           DigColPsInt_SpurSnsrData_Cnt_M_u16         564           DigColPsInt_TransactionCnt_Cnt_M_u08         255           Flags_Cnt_T_b16         32           I2c_GenStopCond(I2cRegPtr_Cnt_T_str)         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str           I2c_Send(I2cRegPtr_Cnt_T_str)         target_I2c_Send_I2cRegPtr_Cnt_T_str           I2c_SetRecv(I2cRegPtr_Cnt_T_str)         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str           I2c_SetStatus(I2cRegPtr_Cnt_T_str)         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str           I2c_SetUpMasterReceive(I2cRegPtr_Cnt_T_str)         target_I2c_SetUpMasterReceive_I2cRegPtr_Cnt_T_str           I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str           I2c_SetupMasterScotu_u08[0]         0           T_DataRegisters_Cnt_u08[1]         32           T_DataRegisters_Cnt_u08[2]         30	DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_igc         0           DigColPsInt_SpurSnsrData_Cnt_M_u16         564           DigColPsInt_TransactionCnt_Cnt_M_u08         255           Flags_Cnt_T_b16         32           I2c_GenStopCond(I2cRegPtr_Cnt_T_str)         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str           I2c_Send(I2cRegPtr_Cnt_T_str)         target_I2c_Send_I2cRegPtr_Cnt_T_str           I2c_SetRecv(I2cRegPtr_Cnt_T_str)         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str           I2c_SetStatus(I2cRegPtr_Cnt_T_str)         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str           I2c_SetUpMasterReceive(I2cRegPtr_Cnt_T_str)         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str           I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str           I2c_SetupMasterScot_u08[0]         0           T_DataRegisters_Cnt_u08[1]         32           T_DataRegisters_Cnt_u08[2]         30	DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SpurSnsrData_Cnt_M_u16         564           DigColPsInt_TransactionCnt_Cnt_M_u08         255           Flags_Cnt_T_b16         32           I2c_GenStopCond(I2cRegPtr_Cnt_T_str)         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str           I2c_Send(I2cRegPtr_Cnt_T_str)         target_I2c_Send_I2cRegPtr_Cnt_T_str           I2c_SetRecv(I2cRegPtr_Cnt_T_str)         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str           I2c_SetStatus(I2cRegPtr_Cnt_T_str)         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str           I2c_SetUpMasterReceive(I2cRegPtr_Cnt_T_str)         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str           I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str           I2c_SetupMasterScnt_u08[0]         0           T_DataRegisters_Cnt_u08[1]         32           T_DataRegisters_Cnt_u08[2]         30	DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_TransactionCnt_Cnt_M_u08       255         Flags_Cnt_T_b16       32         I2c_GenStopCond(I2cRegPtr_Cnt_T_str)       target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str         I2c_Send(I2cRegPtr_Cnt_T_str)       target_I2c_Send_I2cRegPtr_Cnt_T_str         I2c_SetRecv(I2cRegPtr_Cnt_T_str)       target_I2c_SetRecv_I2cRegPtr_Cnt_T_str         I2c_SetStatus(I2cRegPtr_Cnt_T_str)       target_I2c_SetStatus_I2cRegPtr_Cnt_T_str         I2c_SetUpMasterReceive(I2cRegPtr_Cnt_T_str)       target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str         I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)       target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str         I2c_SetupMasterS_Cnt_u08[0]       0         T_DataRegisters_Cnt_u08[1]       32         T_DataRegisters_Cnt_u08[2]       30	DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
Flags_Cnt_T_b16         32           I2c_GenStopCond(I2cRegPtr_Cnt_T_str)         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str           I2c_Send(I2cRegPtr_Cnt_T_str)         target_I2c_Send_I2cRegPtr_Cnt_T_str           I2c_SetRecv(I2cRegPtr_Cnt_T_str)         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str           I2c_SetStatus(I2cRegPtr_Cnt_T_str)         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str           I2c_SetUpMasterReceive(I2cRegPtr_Cnt_T_str)         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str           I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str           T_DataRegisters_Cnt_u08[0]         0           T_DataRegisters_Cnt_u08[1]         32           T_DataRegisters_Cnt_u08[2]         30	DigColPsInt_SpurSnsrData_Cnt_M_u16	564
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)     target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str       I2c_Send(I2cRegPtr_Cnt_T_str)     target_I2c_Send_I2cRegPtr_Cnt_T_str       I2c_SetRecv(I2cRegPtr_Cnt_T_str)     target_I2c_SetRecv_I2cRegPtr_Cnt_T_str       I2c_SetStatus(I2cRegPtr_Cnt_T_str)     target_I2c_SetStatus_I2cRegPtr_Cnt_T_str       I2c_SetUpMasterReceive(I2cRegPtr_Cnt_T_str)     target_I2c_SetUpMasterReceive_I2cRegPtr_Cnt_T_str       I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)     target_I2c_SetUpMasterTransmit_I2cRegPtr_Cnt_T_str       I2c_SetupMasterScnt_u08[0]     0       T_DataRegisters_Cnt_u08[1]     32       T_DataRegisters_Cnt_u08[2]     30	DigColPsInt_TransactionCnt_Cnt_M_u08	255
I2c_Send(I2cRegPtr_Cnt_T_str)     target_I2c_Send_I2cRegPtr_Cnt_T_str       I2c_SetRecv(I2cRegPtr_Cnt_T_str)     target_I2c_SetRecv_I2cRegPtr_Cnt_T_str       I2c_SetStatus(I2cRegPtr_Cnt_T_str)     target_I2c_SetStatus_I2cRegPtr_Cnt_T_str       I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)     target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str       I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)     target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str       I2c_SetupMasterScnt_u08[0]     0       T_DataRegisters_Cnt_u08[1]     32       T_DataRegisters_Cnt_u08[2]     30	Flags_Cnt_T_b16	32
I2c_SetRecv(I2cRegPtr_Cnt_T_str)     target_I2c_SetRecv_I2cRegPtr_Cnt_T_str       I2c_SetStatus(I2cRegPtr_Cnt_T_str)     target_I2c_SetStatus_I2cRegPtr_Cnt_T_str       I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)     target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str       I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)     target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str       I2c_SetupMasterScnt_u08[0]     0       T_DataRegisters_Cnt_u08[1]     32       T_DataRegisters_Cnt_u08[2]     30	I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)     target_I2c_SetStatus_I2cRegPtr_Cnt_T_str       I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)     target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str       I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)     target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str       T_DataRegisters_Cnt_u08[0]     0       T_DataRegisters_Cnt_u08[1]     32       T_DataRegisters_Cnt_u08[2]     30	I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)     target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str       I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)     target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str       T_DataRegisters_Cnt_u08[0]     0       T_DataRegisters_Cnt_u08[1]     32       T_DataRegisters_Cnt_u08[2]     30	I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)     target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str       T_DataRegisters_Cnt_u08[0]     0       T_DataRegisters_Cnt_u08[1]     32       T_DataRegisters_Cnt_u08[2]     30	I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]       0         T_DataRegisters_Cnt_u08[1]       32         T_DataRegisters_Cnt_u08[2]       30	I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[1]       32         T_DataRegisters_Cnt_u08[2]       30	I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[2] 30	T_DataRegisters_Cnt_u08[0]	0
	T_DataRegisters_Cnt_u08[1]	32
T DataRenisters Cnt u08(3) 36	T_DataRegisters_Cnt_u08[2]	30
batanoglostio_oni_acotol	T_DataRegisters_Cnt_u08[3]	36

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Name	Input Value	
Γ_DataRegisters_Cnt_u08[4]	38	
Γ_DataRegisters_Cnt_u08[5]	34	
Γ_DataRegisters_Cnt_u08[6]	10	
	12	
t	14	
butantoglocio_oni_uoo(o) 2cREG1_temp	target_i2cREG1_temp	
C_ColSensorl2CAddress_Cnt_u08	109	
x_SpurSensorI2CAddress_Cnt_u08	25	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	7788	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100	
	2767	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR		
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	
	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT		
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET	0	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	
arget I2c Send I2cRegPtr Cnt T str.EMDR	0	
arget I2c Send I2cRegPtr Cnt T str.PSC	100	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	
	100	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
arget I2c Send I2cRegPtr Cnt T str.ODR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88	
	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556	
	100	

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Name	Input Value
1100	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	2
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767
	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	564
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SET	0
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	1
target I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	3
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	100
51	



Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR target_i2cREG1_temp.IMR	100		
target_i2cREG1_temp.STR	7788		
target_i2cREG1_temp.CLKL	2767		
target_i2cREG1_temp.CLKH	556		
target_i2cREG1_temp.CNT	564		
target_i2cREG1_temp.DRR	88		
target_i2cREG1_temp.SAR	3		
target_i2cREG1_temp.DXR	100 2767		
target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR	9		
target i2cREG1 temp.EMDR	0		
target i2cREG1 temp.PSC	100		
target_i2cREG1_temp.PID11	556		
target_i2cREG1_temp.PID12	100		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT	3 2		
target i2cREG1_temp.SET	0		
target i2cREG1 temp.CLR	1		
target_i2cREG1_temp.ODR	3		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	Actual Value	1	~
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0]	Actual Value 1 100	1 100	~
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	Actual Value  1 100 200	1 100 200	~
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0]	Actual Value 1 100	1 100	•
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	Actual Value  1 100 200 250	1 100 200 250	•
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc	Actual Value  1 100 200 250 0	1 100 200 250 0	•
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16	Actual Value  1 100 200 250 0	1 100 200 250 0	• • • • • • • • • • • • • • • • • • •
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08	Actual Value  1 100 200 250 0 0 1 2767 80	1 100 200 250 0 0 1 2767	
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE	1 100 200 250 0 0 1 2767 80 READ_COMPLETE	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_12CHwCustData_UIs_M_u16	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61	1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_12CHwCustData_UIs_M_u16  DigColPsInt_12CHwIncompleteCustData_UIs_M_u16	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62	1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_12CHwCustData_UIs_M_u16  DigColPsInt_12CHwIncompleteCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_IntFailedOnce_Cnt_M_lgc	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1	1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_12CHwCustData_UIs_M_u16  DigColPsInt_12CHwIncompleteCustData_UIs_M_u16	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62	1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_12CHwIncompleteCustData_Uls_M_u16  DigColPsInt_IntFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1	1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_12CHwIncompleteCustData_Uls_M_u16  DigColPsInt_IntFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0	1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_l2CHwCustData_Uls_M_u16  DigColPsInt_l12CHwCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvdDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 25800	1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 0 25800	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u16  DigColPsInt_L2CHwCustDatFound_LIS_M_u16  DigColPsInt_I2CHwCustData_UIS_M_u16  DigColPsInt_liTiFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 0 25800 0	1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 0 25800 0	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_latedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvdDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 0 25800 0 3	1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 0 25800 0 3	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_l12CHwCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvdDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 0 25800 0 3 100	1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 0 25800 0 3 100	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_u16  DigColPsInt_SpurSnsrData_Cnt_M_u18  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 2 0 25800 0 3 100 7788	1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 0 25800 0 3 100 7788	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_SpurCustDataFound_Cnt_M_lgc  DigColPsInt_SpurCustDataFound_Cnt_M_lgc  DigColPsInt_SpurCustDateTound_Cnt_M_lgc  DigColPsInt_SpurCustDateTound_Cnt_M_lgc  DigColPsInt_SpurCustDateTound_Cnt_M_u16  DigColPsInt_SpurSnsrData_Cnt_M_u18  DigColPsInt_SpurSnsrData_Cnt_M_u18  DigColPsInt_SpurSnsrData_Cnt_M_u18  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 25800 0 3 100 7788 2767	1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 0 25800 0 3 100 7788 2767	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_u16  DigColPsInt_SpurSnsrData_Cnt_M_u18  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 2 0 25800 0 3 100 7788	1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 0 25800 0 3 100 7788	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 2 0 25800 0 3 100 7788 2767 556	1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 0 25800 0 3 100 7788 2767 556	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	Actual Value  1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 0 25800 0 3 100 7788 2767 556 564 88 3	1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 0 25800 0 3 100 7788 2767 556 564 88 3	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 25800 0 3 100 7788 2767 556 564 88 3 100	1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 25800 0 25800 0 3 100 7788 2767 556 564 88 3 100	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvDataType_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_TransactionCnt_Cnt_M_u08 target_12c_GenStopCond_12cRegPtr_Cnt_T_str.OAR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.UKL target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKH target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKH target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.MDR	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 25800 0 0 3 100 7788 2767 556 564 88 3 100 2767	1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 25800 0 25800 0 3 100 7788 2767 556 564 88 3 100 2767	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.OAR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.STR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKH  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKH  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CNT  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 25800 0 0 3 100 7788 2767 556 564 88 3 100 2767 9	1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 25800 0 3 100 7788 2767 556 564 88 3 100 2767 9	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u16  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.OAR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.STR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CNT  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 25800 0 0 3 100 7788 2767 556 564 88 3 100 2767 9 0	1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 2 0 25800 0 3 100 7788 2767 556 564 88 3 100 2767 9	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_L2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 25800 0 3 100 7788 22767 556 564 88 3 100 2767 9 0 100	1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 0 25800 0 3 100 7788 2767 556 564 88 3 100 2767 9 0 100	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u16  DigColPsInt_L2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXPC  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DDR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DDR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PDD1	Actual Value  1 100 200 250 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 25800 0 0 3 100 7788 2767 556 564 88 3 100 2767 9 0	1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 2 2 0 25800 0 3 100 7788 2767 556 564 88 3 100 2767 9	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_L2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR	Actual Value  1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 25800 0 25800 0 3 100 7788 2767 556 564 88 3 100 2767 9 0 100 556	1 100 200 250 0 0 0 1 2767 80 READ_COMPLETE 61 62 1 0 0 25800 0 25800 0 3 100 7788 2767 556 564 88 3 100 2767 9 0 100 556	

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	3	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	E88	100	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	7788	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	556	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	564	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	88	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	100	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2 <b>E6</b> 8	2767	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	9	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	100	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	556	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3	3	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100	100	✓
target_I2c_SetReov_I2cRegPtr_Cnt_T_\$tr.STR	7788	7788	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556	556	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564	564	✓
target I2c SetRecv I2cRegPtr Cnt T str.DRR	88	88	

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100	100	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100	100	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788	7788	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556	556	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564	564	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88	88	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	100	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	2767	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.IVR	9	9	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	100	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556	556	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	100	·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	3	3	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	3	3	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	100	100	-
	7788	7788	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR			
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	2767 556	2767 556	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	564	564	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	88	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR			
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	100	100	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767	2767	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	100	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556	556	<b>Y</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	100	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>Y</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>Y</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	

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Actual Function	Count	Expected Function	Count	Result	
*none*	0	*** No Call Expected ***	0	-	ŗ

Test Step 2.22 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2
DigColPsInt_Buffer_Cnt_M_u08[0]	1



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Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[1]	5
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	56
DigColPsInt_CurrentSlave_Cnt_M_u08	90
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_GETDATA
DigColPsInt_I2CHwCustData_Uls_M_u16	64
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	65
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	7878
DigColPsInt_TransactionCnt_Cnt_M_u08	100
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	114
k_SpurSensorl2CAddress_Cnt_u08	30
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	678
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	45
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	6788
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	7878
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	678
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	45
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	778
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	45
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	6788
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	45
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	678
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	6788
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	7878
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	678
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	56
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Name	Input Value	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	778	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	45	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	6788	
arget I2c Send I2cRegPtr Cnt T str.PID12	45	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	
arget I2c Send I2cRegPtr Cnt T str.SET	1	
· ·	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	678	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	45	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	56	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	6788	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	7878	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	678	
arget I2c SetRecv I2cRegPtr Cnt T str.DXR	45	
	56	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	778	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	45	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	6788	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	45	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	
arget I2c SetRecv I2cRegPtr Cnt T str.PD	2	
arget I2c SetRecv I2cRegPtr Cnt T str.PSL	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	678	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	45	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	66	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	56	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	6788	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	7878	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	678	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	45	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	56	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	778	
rget I2c SetStatus I2cRegPtr Cnt T str.EMDR	1	
	45	
urget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC		
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	6788	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	45	
rget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	
irget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	
urget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	
irget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1	
riget_12c_Setofatus_12cRegPti_Cfit_1_str.F3E	678	
irget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	45	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	66	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	56	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	6788	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	7878	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12	

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Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	45		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.MDR	56		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	778		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	45		
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	6788		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	45		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	678		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	45		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	56		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	6788		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	7878		
	12		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	678 45		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR			
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	778		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	45		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	6788		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	45		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1		
target_i2cREG1_temp.OAR	678		
target_i2cREG1_temp.IMR	45		
target_i2cREG1_temp.STR	66		
target i2cREG1 temp.CLKL	56		
target_i2cREG1_temp.CLKH	6788		
target i2cREG1 temp.CNT	7878		
target_i2cREG1_temp.DRR	12		
target i2cREG1 temp.SAR	678		
target i2cREG1_temp.DXR	45		
target_i2cREG1_temp.MDR	56		
	778		
target_i2cREG1_temp.IVR			
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	45		
target_i2cREG1_temp.PID11	6788		
target_i2cREG1_temp.PID12	45		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	2		
target_i2cREG1_temp.PSL	1		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2	2	~
DigColPsInt_Buffer_Cnt_M_u08[0]	1	1	~
DigColPsInt_Buffer_Cnt_M_u08[1]	5	5	~
DigColPsInt_Buffer_Cnt_M_u08[2]	9	9	~
DisCollected Dura Dura Conference Out Malan	4	4	

DigColPsInt\_BusBusySeqError\_Cnt\_M\_lgc

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Name	Actual Value	Expected Value	Result
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	
DigColPsInt_ColSnsrData_Cnt_M_u16	56 90	56 90	•
DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt CurrentStepNo Cnt M enum	READ COMPLETE	READ COMPLETE	
DigColPsInt_I2CHwCustData_Uls_M_u16	64	64	
DigColPsInt I2CHwIncompleteCustData UIs M u16	65	65	
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	•
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	•
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	•
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	-
DigColPsInt SpurSnsrData Cnt M u16	261	261	•
DigColPsInt_TransactionCnt_Cnt_M_u08	101	101	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	678	678	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	45	45	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	56	56	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	7878	7878	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12	12	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	678	678	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	45	45	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	56	56	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	778	778	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	45	45	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	6788	6788	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	45	45	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	678	678	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	45	45	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	56	56	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	7878	7878	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	678	678	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	45	45	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	56	56	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	778	778	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	·
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	45	45	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	6788	6788	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	45	45	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>~</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	¥
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	<b>~</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	1	1	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	678	678	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	45	45	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	56	56	_
	6788	6788	Y
	7070	7070	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	7878	7878	•
	7878 12 678	7878 12 678	

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	56	56	<b>~</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	778	778	<b>Y</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	· ·
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	45 6788	45 6788	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	45	45	•
target I2c SetRecv I2cRegPtr Cnt T str.DMAC	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	<u> </u>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	678	678	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	45	45	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	56	56	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	<b>Y</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	7878	7878	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12	12	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR	678	678	<b>V</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	45	45	· ·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	56 778	56 778	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	1	1	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	45	45	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11	6788	6788	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	45	45	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.DMAC	1	1	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	<u> </u>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	678	678	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	45	45	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	56	56	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	7878	7878	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12	12	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	678	678	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	45	45	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	56	56	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	778	778	<b>Y</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	45	45	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	6788	6788	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	45	45	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR target_l2c SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	1	1	4
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DUT	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	<u> </u>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSL	1	1	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	678	678	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	45	45	_
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	56	56	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	7878	7878	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	<b>✓</b>
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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	678	678	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	45	45	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	778	778	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	45	45	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	6788	6788	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	45	45	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	~

Т				V
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 2.23 (Repeat Count = 1)	v v v v v v v v v v v v v v v v v v v
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3
DigColPsInt Buffer Cnt M u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt BusBusySeqError Cnt M Igc	1
DigColPsInt CmdFailOccurred Cnt M Igc	1
DigColPsInt ColCustDatFound Cnt M Igc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	566
DigColPsInt_CurrentSlave_Cnt_M_u08	30
DigColPsInt CurrentStepNo Cnt M enum	INIT SENSOR2 READEXTERR SETREG
DigColPsInt I2CHwCustData Uls M u16	67
DigColPsInt I2CHwIncompleteCustData UIs M u16	68
DigColPsInt InitFailedOnce Cnt M Igc	1
DigColPsInt NackOccured Cnt M Igc	1
DigColPsInt PrevReqDataType Cnt M u08	4
DigColPsInt RecvOverrunError Cnt M Igc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt SkipRegisterWrite Cnt M Igc	1
DigColPsInt SpurCustDatFound Cnt M lgc	1
DigColPsInt SpurSnsrData Cnt M u16	129
DigColPsInt TransactionCnt Cnt M u08	100
Flags_Cnt_T_b16	2
I2c GenStopCond(I2cRegPtr Cnt T str)	target I2c GenStopCond I2cRegPtr Cnt T str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c SetRecv(I2cRegPtr Cnt T str)	target I2c SetRecv I2cRegPtr Cnt T str
I2c SetStatus(I2cRegPtr Cnt T str)	target I2c SetStatus I2cRegPtr Cnt T str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c SetupMasterTransmit(I2cRegPtr Cnt T str)	target I2c SetupMasterTransmit I2cRegPtr Cnt T str
T DataRegisters Cnt u08[0]	0
T DataRegisters Cnt u08[1]	32
T DataRegisters Cnt u08[2]	30
T DataRegisters Cnt u08[3]	36
T DataRegisters Cnt u08[4]	38
T DataRegisters Cnt u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T DataRegisters Cnt u08[7]	12
T DataRegisters Cnt u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k ColSensorI2CAddress Cnt u08	0
k SpurSensorl2CAddress Cnt u08	120
target I2c GenStopCond I2cRegPtr Cnt T str.OAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444
target I2c GenStopCond I2cRegPtr Cnt T str.CLKL	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466

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Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR	6
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44
	4466
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target I2c GenStopCond I2cRegPtr Cnt T str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0
	1
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target I2c GenStopCond I2cRegPtr Cnt T str.PSL	3
	567
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
	6
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
	129
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444

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Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466
	129
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR	566
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target I2c SetStatus I2cRegPtr Cnt T str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
target I2c SetupMasterReceive I2cRegPtr Cnt T str.IMR	44
target I2c SetupMasterReceive I2cRegPtr Cnt T str.STR	4444
target 12c SetupMasterReceive 12cRegPtr Cnt T str.CLKL	566
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	4466
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CNT	129
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	0
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	3
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	4444
target I2c SetupMasterTransmit I2cRegPtr_Cnt_1_str.STR	566
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	4466
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3
target_izc_SetupinasterTransmit_izcRegPti_Cni_i_str.PSL target_izcREG1_temp.OAR	567
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DigColPsInt\_InterruptNotification

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Name	Input Value		
target_i2cREG1_temp.IMR	44		
target_i2cREG1_temp.STR	4444		
target_i2cREG1_temp.CLKL	566		
target_i2cREG1_temp.CLKH	4466		
target_i2cREG1_temp.CNT	129		
target_i2cREG1_temp.DRR	6		
target_i2cREG1_temp.SAR	567		
target_i2cREG1_temp.DXR	44		
target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR	566 554		
target_i2cREG1_temp.EMDR	1		
target i2cREG1 temp.PSC	44		
target_i2cREG1_temp.PID11	4466		
target_i2cREG1_temp.PID12	44		
target i2cREG1 temp.DMAC	1		
target i2cREG1 temp.FUN	1		
target_i2cREG1_temp.DIR	2		
target_i2cREG1_temp.DIN	0		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3	3	~
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	~
DigColPsInt_Buffer_Cnt_M_u08[1]	3	3	~
DigColPsInt_Buffer_Cnt_M_u08[2]	7	7	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	~
DigColPsInt_ColCustDatFound_Cnt_M_Igc	1	1	<b>V</b>
DigColPsInt_ColSnsrData_Cnt_M_u16	566	566	<b>*</b>
DigColPsInt_CurrentSlave_Cnt_M_u08	0	0	
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16	67	N INIT_SENSOR1_EXTREADADDRREG_SEN 67	
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	68	68	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	-
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	<b>~</b>
DigColPsInt RecvOverrunError Cnt M Igc	1	1	-
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	129	129	~
DigColPsInt_TransactionCnt_Cnt_M_u08	100	100	~
I2c_Send(Length_Cnt_T_u32)	3	3	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>~</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT	129	129	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6 567	6 567	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR	44	44	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	566	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	554	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	44	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	4466	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	44	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN	0	0	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	3	3	<b>~</b>
target I2c Send I2cRegPtr Cnt T str OAR	567	567	ı 🥒

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target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.OAR

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IMR

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	<u> </u>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44 566	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	554	- J
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554 1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	<u> </u>
target I2c Send I2cRegPtr Cnt T str.SET	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	_
target I2c Send I2cRegPtr Cnt T str.PD	3	3	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	_
target I2c SetRecv I2cRegPtr Cnt T str.STR	4444	4444	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>Y</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>Y</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>Y</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CNT	129	129	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DRR	6	6	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSC	44	44	<b>~</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	4466	4466	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID12	44	44	~
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIN	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	_
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	2	2	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	0	0	<b>~</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	3	3	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSL	3	3	<b>*</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	_
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	44	44	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	4444	4444	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	· ·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	
target I2c SetupMasterTransmit I2cReqPtr Cnt T str.CNT	129	129	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	6	6	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	567	567	-
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	44	44	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	566	566	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	
	44	44	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	4466	4466	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4400	44	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12		1	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	·	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	· 4
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	_
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	0	0	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>

T .				
Actual Function	Count	Expected Function	Count	Result
I2c_GenStopCond	1	I2c_GenStopCond	1	~
SetupWriteData	1	SetupWriteData	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c Send	1	I2c Send	1	

Test Step 2.24 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	4
DigColPsInt_Buffer_Cnt_M_u08[0]	100
DigColPsInt_Buffer_Cnt_M_u08[1]	200
DigColPsInt_Buffer_Cnt_M_u08[2]	250
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	7
DigColPsInt_CurrentSlave_Cnt_M_u08	35
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_DUMMY_READ

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DigColPsini_interruptiNotinication	
Name	Input Value
DigColPsInt_I2CHwCustData_Uls_M_u16	70
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	71
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	88
DigColPsInt_TransactionCnt_Cnt_M_u08	110
Flags_Cnt_T_b16	32
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
_DataRegisters_Cnt_u08[0]	0
DataRegisters_Cnt_u08[1]	32
_DataRegisters_Cnt_u08[2]	30
_DataRegisters_Cnt_u08[3]	36
_DataRegisters_Cnt_u08[4]	38
atanagatataataataataataata_	34
DataRegisters Cnt u08[6]	10
_DataRegisters_Cnt_u08[7]	12
_DataRegisters_Cnt_u08[8]	14
2cREG1_temp	target_i2cREG1_temp
_ColSensorI2CAddress_Cnt_u08	127
_SpurSensorI2CAddress_Cnt_u08	5
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89
	67
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	7
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	577
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	89
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR	2
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC	89
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2
urget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0
rget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67
rget_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	7
arget_12c_Send_12cRegPtr_Cnt_T_str.CLKH	577
arget_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	88
liget_l2c_send_l2cRegPtr_Cnt_T_str.DRR	23
	65
urget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	
irget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
irget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0

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Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67
target I2c SetRecv I2cRegPtr Cnt T str.CLKL	7
target I2c SetRecv I2cRegPtr Cnt T str.CLKH	577
target I2c SetRecv I2cRegPtr Cnt T str.CNT	88
· ·	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	1
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89
target I2c SetupMasterReceive I2cRegPtr Cnt T str.STR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	2
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DigColPsInt\_InterruptNotification

Name	Input Value	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	88	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	89	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	
	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	2 2	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	0	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	1	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	2	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	
target_i2cREG1_temp.OAR	65	
target_i2cREG1_temp.IMR	89	
target_i2cREG1_temp.STR	67	
target_i2cREG1_temp.CLKL	7	
target_i2cREG1_temp.CLKH	577	
target_i2cREG1_temp.CNT	88	
target i2cREG1 temp.DRR	23	
target i2cREG1 temp.SAR	65	
target i2cREG1 temp.DXR	89	
target i2cREG1 temp.MDR	7	
target_i2cREG1_temp.IVR	44	
target_i2cREG1_temp.EMDR	2	
target_i2cREG1_temp.PSC	89	
target i2cREG1 temp.PID11	577	
target_i2cREG1_temp.PID12	89	
target_i2cREG1_temp.DMAC	2	
target_i2cREG1_temp.FUN	0	
target_i2cREG1_temp.DIR	0	
target_i2cREG1_temp.DIN	1	
target_i2cREG1_temp.DOUT	2	
target_i2cREG1_temp.SET	2	
target_i2cREG1_temp.CLR	0	
target_i2cREG1_temp.ODR	1	
target_i2cREG1_temp.PD	2	
target_i2cREG1_temp.PSL	0	
Name	Actual Value Expected Value R	Resul
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	4 4	٠,
DigColPsInt_Buffer_Cnt_M_u08[0]	12 12	•
DigColPsInt_Buffer_Cnt_M_u08[1]	200 200	•
DigColPsInt_Buffer_Cnt_M_u08[2]	250 250	•
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0 0	•
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0 0	•
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0 0	•
DigColPsInt_ColSnsrData_Cnt_M_u16	7	•
DigColPsInt_CurrentSlave_Cnt_M_u08	127 127	٠,
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_SET INIT_SENSOR1_EXTREADCTRLREG_SET	•
DigColPsInt_I2CHwCustData_Uls_M_u16	70 70	•
DigColPsInt_I2CHwIncompleteCustData_Llls_M_u16	71 71	

71

0

71

0

 ${\tt DigColPsInt\_InitFailedOnce\_Cnt\_M\_Igc}$ 

DigColPsInt\_I2CHwIncompleteCustData\_Uls\_M\_u16

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Name	Actual Value	Expected Value	Result
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	<b>✓</b>
DigColPsInt_RecvdDataType_Cnt_M_u08	5	0	
DigColPoint_SpurCostDatFound_Cnt_M_lgc	88	88	~
DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08	110	110	
I2c Send(Length Cnt T u32)	1	1	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	,
target I2c GenStopCond I2cRegPtr Cnt T str.OAR	65	65	~
target I2c GenStopCond I2cRegPtr Cnt T str.IMR	89	89	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67	67	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23	23	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1 2	2	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	65	65	
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	89	89	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target I2c Send I2cRegPtr Cnt T str.MDR	7	7	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	0	0	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65	65	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577	577	-
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	88	88	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	23	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	65	<b>-</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	89	89	<b>V</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	44	44	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	2	2	-
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	89	89	-
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	577	577	_
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	89	89	-
			_

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Digoon din_monupavounoutor	1	1	
Name	Actual Value	Expected Value	Result
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target I2c SetRecv I2cRegPtr Cnt T str.DOUT	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65	65	<b>✓</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR	89 67	89 67	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577	577	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23	23	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7	7	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89	89	<b>✓</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11	577 89	577 89	-
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC	2	2	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65 89	89	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	67	67	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	7	7	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577	577	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23	23	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	<b>Y</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89	89 577	<b>V</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	577 89	89	-
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	2	2	
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>V</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	2	2	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	65	0 65	<b>V</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	~
$target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SAR$	65	65	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	2	<b>V</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	89	89	-
targot_rec_octuprinastor transmit_recitogr ti_ont_1_Sti.FOC	00	00	

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c_Send	1	I2c_Send	1	~

Test Step 2.25 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt AttempOccurForCustDatRead Cnt M u08	5
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt Buffer Cnt M u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt BusBusySeqError Cnt M Igc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt ColCustDatFound Cnt M Igc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	554
DigColPsInt CurrentSlave Cnt M u08	40
DigColPsInt CurrentStepNo Cnt M enum	INIT SENSOR2 READERROR READ
DigColPsInt_I2CHwCustData_Uls_M_u16	73
DigColPsInt I2CHwIncompleteCustData Uls M u16	74
DigColPsInt InitFailedOnce Cnt M Igc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt PrevReqDataType Cnt M u08	0
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt RecvdDataType Cnt M u08	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt SpurCustDatFound Cnt M Igc	1
DigColPsInt SpurSnsrData Cnt M u16	123
DigColPsInt_TransactionCnt_Cnt_M_u08	120
Flags Cnt T b16	2
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c Send(I2cRegPtr Cnt T str)	target I2c Send I2cRegPtr Cnt T str
I2c SetRecv(I2cRegPtr Cnt T str)	target I2c SetRecv I2cRegPtr Cnt T str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target I2c SetupMasterReceive I2cRegPtr Cnt T str
I2c SetupMasterTransmit(I2cRegPtr Cnt T str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T DataRegisters Cnt u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T DataRegisters Cnt u08[3]	36
T DataRegisters Cnt u08[4]	38
T DataRegisters Cnt u08[5]	34
T DataRegisters Cnt u08[6]	10
T DataRegisters Cnt u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1 temp	target i2cREG1 temp
k_ColSensorl2CAddress_Cnt_u08	111
k SpurSensorI2CAddress Cnt u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54
target I2c GenStopCond I2cRegPtr Cnt T str.IMR	66
target I2c GenStopCond I2cRegPtr Cnt T str.STR	8
target I2c GenStopCond I2cRegPtr Cnt T str.CLKL	554
target I2c GenStopCond I2cRegPtr Cnt T str.CLKH	344
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
augut_120_00.10.00001a_12010gt u_011t_1_0u.b/stt	

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Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
	3
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	123
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554
target I2c Send I2cRegPtr Cnt T str.IVR	788
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2
	54
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554
target I2c SetRecv I2cRegPtr Cnt T str.CLKH	344
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344
	66
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45
0.7 .7-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1	

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Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54
target I2c SetStatus I2cRegPtr Cnt T str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target I2c SetStatus I2cRegPtr Cnt T str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54
target I2c SetupMasterReceive I2cRegPtr Cnt T str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2
target_i2cREG1_temp.OAR	54
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	8
target_i2cREG1_temp.CLKL	554
target_i2cREG1_temp.CLKH	344



Name	Input Value		
target_i2cREG1_temp.CNT	123		
target_i2cREG1_temp.DRR	45		
target_i2cREG1_temp.SAR	54		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	788		
target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	344		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	3		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET target_i2cREG1_temp.CLR	3		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	2		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	5	5	~
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	~
DigColPsInt_Buffer_Cnt_M_u08[1]	3	3	~
DigColPsInt_Buffer_Cnt_M_u08[2]	7	7	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	•
DigColPsInt_ColCustDatFound_Cnt_M_Igc	1	1	<b>*</b>
DigColPoInt_ColSnsrData_Cnt_M_u16	111	554 111	
DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR1 EXTREADADDRREG SEN		~
DigColPsInt_I2CHwCustData_Uls_M_u16	73	73	
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	74	74	•
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	~
DigColPsInt NackOccured Cnt M Igc	1	1	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	~
DigColPsInt_RecvdDataType_Cnt_M_u08	1	1	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	123	123	~
DigColPsInt_TransactionCnt_Cnt_M_u08	120	120	~
I2c_Send(Length_Cnt_T_u32)	3	3	<b>V</b>
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54 66	54 66	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR	8	8	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554	554	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344	344	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123	123	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45	45	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	54	54	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554	554	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR	788	788	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344 66	344 66	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC	3	3	
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	54	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	- 0
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	8	8 554	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	344	344	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	123	~

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	45	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	54	54	✓
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	554	554	<b>~</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	788	788	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344	344	Ž
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3 1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	3	3	<u> </u>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	Ţ
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	<u> </u>
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54	54	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8	8	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554	554	
target I2c SetRecv I2cRegPtr Cnt T str.CLKH	344	344	<b>✓</b>
target I2c SetRecv I2cRegPtr Cnt T str.CNT	123	123	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45	45	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54	54	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554	554	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788	788	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344	344	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	2	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54	54	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8	8	<b>~</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL	554	554	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344	344	<b>V</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	123	123	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR	45	45	<u> </u>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54	54	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554	554	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	788	788	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66 344	66 344	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11		344 66	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC	66	3	Ž
target_I2c_SetStatus_I2cRegPtr_Cnt_I_str.DMAC target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	3 1	3 1	
	3	3	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DUT	3	3	<i>y</i>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	
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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344	344	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123	123	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45	45	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54	54	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554	554	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788	788	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344	344	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	54	54	✓
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	8	8	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554	554	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344	344	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123	123	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45	45	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54	54	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554	554	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788	788	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344	344	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	3	3	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	1	1	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	2	2	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c_GenStopCond	1	l2c_GenStopCond	1	~
SetupWriteData	1	SetupWriteData	1	<b>~</b>
I2c_SetupMasterTransmit	1	l2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	~

Test Step 2.26 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	0
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	2767
DigColPsInt_CurrentSlave_Cnt_M_u08	45
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	76
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	77
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0

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DigColPsini_Interruptivotilication		
Name	Input Value	
DigColPsInt_PrevReqDataType_Cnt_M_u08	2	
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	
DigColPsInt_RecvdDataType_Cnt_M_u08	2	
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	
DigColPsInt_SpurSnsrData_Cnt_M_u16	564	
DigColPsInt_TransactionCnt_Cnt_M_u08	130	
Flags_Cnt_T_b16	32	
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str	
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str	
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str	
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str	
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target I2c SetupMasterReceive I2cRegPtr Cnt T str	
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str	
_DataRegisters_Cnt_u08[0]	0	
aaanagaaaa_aaa_aaaga _DataRegisters_Cnt_u08[1]	32	
DataRegisters_Cnt_u08[2]	30	
DataRegisters_Cnt_u08[3]	36	
DataRegisters_Cnt_u08[4]	38	
	34	
DataRegisters_Cnt_u08[5]		
T_DataRegisters_Cnt_u08[6]	10	
DataRegisters_Cnt_u08[7]	12	
C_DataRegisters_Cnt_u08[8]	14	
2cREG1_temp	target_i2cREG1_temp	
ColSensorI2CAddress_Cnt_u08	7	
_SpurSensorI2CAddress_Cnt_u08	123	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR	7788	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	
arget I2c GenStopCond I2cRegPtr Cnt T str.PSC	100	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	
arget I2c GenStopCond I2cRegPtr Cnt T str.FUN	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	

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Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	3
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100
arget I2c SetStatus I2cRegPtr Cnt T str.MDR	2767
arget I2c SetStatus I2cRegPtr Cnt T str.IVR	9
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
arget I2c SetStatus I2cRegPtr Cnt T str.PSC	100
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
arget I2c SetStatus I2cRegPtr Cnt T str.FUN	0
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
arget I2c SetStatus I2cRegPtr Cnt T str.DIN	3
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
arget I2c SetStatus I2cRegPtr Cnt T str.SET	0
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
arget I2c SetStatus I2cRegPtr Cnt T str.ODR	3
arget I2c SetStatus I2cRegPtr Cnt T str.PD	0
arget I2c SetStatus I2cRegPtr Cnt T str.PSL	3
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3
arget I2c SetupMasterReceive I2cRegPtr Cnt T str.IMR	100
arget I2c SetupMasterReceive I2cRegPtr Cnt T str.STR	7788
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767
arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLKH	556
arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CNT	564
arget I2c SetupMasterReceive I2cRegPtr Cnt T str.DRR	88
arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	3
arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DXR	100
arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.MDR	2767
arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.IVR	9
riget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.EMDR	0
arget_12c_SetupMasterReceive_12cRegPtr_Cnt_1_str.EMDR arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PSC	100
	556
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	100
arget 12c SetupMasterDeceive 12cDecDtr Crt T at DID42	100
	2
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
arget_ 2c_SetupMasterReceive_ 2cRegPtr_Cnt_T_str.PID12 arget_ 2c_SetupMasterReceive_ 2cRegPtr_Cnt_T_str.DMAC arget_ 2c_SetupMasterReceive_ 2cRegPtr_Cnt_T_str.FUN arget_ 2c_SetupMasterReceive_ 2cRegPtr_Cnt_T_str.DIR arget_ 2c_SetupMasterReceive_ 2cRegPtr_Cnt_T_str.DIN	

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Name	Input Value		
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1		
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	7788		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	2767		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	556		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	88		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	100		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	2767		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	9		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	100		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	3		
target_i2cREG1_temp.IMR	100		
target_i2cREG1_temp.STR	7788		
target_i2cREG1_temp.CLKL	2767		
target_i2cREG1_temp.CLKH	556		
target_i2cREG1_temp.CNT	564		
target_i2cREG1_temp.DRR	88		
target_i2cREG1_temp.SAR	3		
target_i2cREG1_temp.DXR	100		
target_i2cREG1_temp.MDR	2767		
target_i2cREG1_temp.IVR	9		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	100		
target_i2cREG1_temp.PID11	556		
target_i2cREG1_temp.PID12	100		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	3		
target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT	2		
	0		
target_i2cREG1_temp.SET target_i2cREG1_temp.CLR	1		
target i2cREG1 temp.ODR	3		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	Result
DigColPsInt_Attempoccum orcustDativeau_Crit_wi_uoo	12	12	•
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	
DigColPsInt Buffer Cnt M u08[2]	200	200	•
DigColPsInt BusBusySegError Cnt M Igc	0	0	
DigColPsInt CmdFailOccurred Cnt M Igc	0	0	•
DigColPsInt_ColCustDatFound_Cnt_M_lgc		0	-
	1 ()		<b>✓</b>
DigColPsInt ColSnsrData Cnt M u16	2767	2767	
DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08	2767	2767	_
DigColPsInt_CurrentSlave_Cnt_M_u08	2767 7	7	•
DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum	2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET	7 INIT_SENSOR1_EXTREADCTRLREG_SET	
DigColPsInt_CurrentStave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16	2767 7	7	•
DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77	7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77	<b>V</b>
DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc	2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76	7 INIT_SENSOR1_EXTREADCTRLREG_SET 76	\ \ \
DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77	7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0	
DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc	2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0	7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0 0	\(\frac{1}{2}\)
DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc	2767 7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0 0 0	7 INIT_SENSOR1_EXTREADCTRLREG_SET 76 77 0 0 0	

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Name	Actual Value	Expected Value	Result
DigColPsInt_SpurSnsrData_Cnt_M_u16	564	564	
DigColPsInt_TransactionCnt_Cnt_M_u08	130	130	
I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	3	3	·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100	100	
target I2c GenStopCond I2cRegPtr Cnt T str.STR	7788	7788	·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
target I2c GenStopCond I2cRegPtr Cnt T str.CLKH	556	556	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564	564	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88	88	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100	100	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767	2767	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9	9	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	0	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100	100	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556	556	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100	100	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	· ·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	· ·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3 3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	100	100	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	7788	7788	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	556	
target_12c_Send_12cRegPtr_Cnt_T_str.CNT	564	564	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	88	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	100	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	2767	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.IVR	9	9	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	100	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	556	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3	3	<b>Y</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3	3	<b>Y</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100	100	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	7788	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	2767	2767	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556	556	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	564 88	564	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	3	88	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100	100	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767	2767	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9	9	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	100	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556	556	J
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100	100	•
target_12c_SetRecv_12cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	<b>✓</b>

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Name	Actual Value	Expected Value	Result
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	2	2	<b>Y</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	<b>~</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	1	1	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	3	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3	3	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.IMR	100	100	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.STR	7788	7788	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556	556	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564	564	<b>✓</b>
target I2c SetStatus I2cRegPtr Cnt T str.DRR	88	88	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100	100	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2767	2767	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9	9	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100	100	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556	556	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100	100	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	✓
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	0	0	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	✓
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100	100	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788	7788	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556	556	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564	564	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88	88	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	100	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	2767	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	9	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>-</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	100	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556	556	<b>Y</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	100	<b>Y</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>~</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	1	1	<b>V</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	3	3	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	0	0	· ·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	3	3	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	3	3	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	100	100	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	· ·
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	556	556	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	88	88	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100	100	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767	2767	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	0	0	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	100	100	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	556	556	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	100	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	<u> </u>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	
0	1.	<del>-</del>	

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PD  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSL$  2014-10-14, 23:42:41+0530

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DigColPsInt_InterruptNotification			azorcat
Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~

3

T				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c Send	1	I2c Send	1	<b>✓</b>

Test Step 2.27 (Repeat Count = 1)	🗸
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	11
DigColPsInt_Buffer_Cnt_M_u08[0]	100
DigColPsInt_Buffer_Cnt_M_u08[1]	200
DigColPsInt_Buffer_Cnt_M_u08[2]	250
DigColPsInt_BusBusySeqError_Cnt_M_Igc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	7846
DigColPsInt_CurrentSlave_Cnt_M_u08	10
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	79
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	80
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	98
DigColPsInt_TransactionCnt_Cnt_M_u08	12
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	11
k_SpurSensorl2CAddress_Cnt_u08	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	10

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Name target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11 target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12 target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	Input Value 8974 10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12 target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	10
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FUN	10
	1
	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target I2c GenStopCond I2cRegPtr Cnt T str.DIN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target I2c GenStopCond I2cRegPtr Cnt T str.CLR	2
target I2c GenStopCond I2cRegPtr Cnt T str.ODR	1
	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10
target I2c Send I2cRegPtr Cnt T str.MDR	7846
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10
	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	10
	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7846
	55

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Name	Input Value
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974
target I2c SetStatus I2cRegPtr Cnt T str.PID12	10
target I2c SetStatus I2cRegPtr Cnt T str.DMAC	1
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target I2c SetStatus I2cRegPtr Cnt T str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	8974
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID12	10
	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	10
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1
target_i2cREG1_temp.OAR	10
target_i2cREG1_temp.IMR	10
target_i2cREG1_temp.STR	1223
target_i2cREG1_temp.CLKL	7846
target i2cREG1 temp.CLKH	8974
target_i2cREG1_temp.CNT	98
target_i2cREG1_temp.DRR	12
target_i2cREG1_temp.SAR	10
target_i2cREG1_temp.DXR	10



DigCoiPsini_interruptivotilication		(MEC)	210
Name	Input Value		
target_i2cREG1_temp.MDR	7846		
target_i2cREG1_temp.IVR	55		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	10		
target_i2cREG1_temp.PID11	8974		
target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC	10		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	2		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	1		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	12	12	-
DigColPsInt_Buffer_Cnt_M_u08[0]	14	14	-
DigColPsInt_Buffer_Cnt_M_u08[1]	200	200	~
DigColPsInt_Buffer_Cnt_M_u08[2]	250	250	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	-
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	•
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	•
DigColPsInt_ColSnsrData_Cnt_M_u16	7846 11	7846 11	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt CurrentStepNo Cnt M enum		INIT SENSOR1 EXTREADDATREG SETR	
DigColPsInt_I2CHwCustData_Uls_M_u16	79	79	
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	80	80	-
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	-
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	-
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	-
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	-
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	-
DigColPsInt_SpurSnsrData_Cnt_M_u16	98	98	-
DigColPsInt_TransactionCnt_Cnt_M_u08	12	12	<b>✓</b>
I2c_Send(Length_Cnt_T_u32)	1	1	•
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10	10	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR	10	10	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR	1223	1223	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	7846	7846	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH	8974 98	8974 98	7
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR	12	12	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10	10	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10	10	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7846	7846	-
target I2c GenStopCond I2cRegPtr Cnt T str.IVR	55	55	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	10	10	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	8974	8974	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	10	10	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	-
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET	1	1	<b>V</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR	1	2	· ·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR		1	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	1	1	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10	10	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	10	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223	1223	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98	98	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10	10	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	10	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846	7846	<b>✓</b>

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Name	Actual Value	Expected Value 55	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10	10	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974	8974	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10	10	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10	10	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10	10	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223	1223	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98	98	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	12	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10	10	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10	10 7846	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	7846 55	55	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	1	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	10	10	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974	8974	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10	10	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10	10	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	1223	1223	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	98	98	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12	12	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	10	10	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	10	10	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7846	7846	<b>V</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	55	55 1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	10	10	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974	8974	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10	10	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10	10	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	10	10	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223	1223	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98	98	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12	12	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10	10	<b>✓</b>

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10	10	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846	7846	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55	55	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10	10	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	8974	8974	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	10	10	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10	10	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223	1223	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98	98	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10	10	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10	10	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55	55	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10	10	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10	10	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✓
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	<b>✓</b>

Т				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c_Send	1	l2c_Send	1	~

Test Step 2.28 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	5
DigColPsInt_Buffer_Cnt_M_u08[0]	1
DigColPsInt_Buffer_Cnt_M_u08[1]	5
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	847
DigColPsInt_CurrentSlave_Cnt_M_u08	20
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	82
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	83
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	4
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0

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Name	Input Value
DigColPsInt_SpurSnsrData_Cnt_M_u16	487
DigColPsInt_TransactionCnt_Cnt_M_u08	13
Flags_Cnt_T_b16	32
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
「_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
Γ_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
「_DataRegisters_Cnt_u08[8]	14
2cREG1_temp	target_i2cREG1_temp
C_ColSensorI2CAddress_Cnt_u08	15
x_SpurSensorI2CAddress_Cnt_u08	110
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	34
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	24
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	455
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	847
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	987
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	487
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	34
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	34
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	24
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	847
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	56
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	24
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11	987
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	24
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FUN	0
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR	3
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN	3
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT	2
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
a.got_120_00.1d_120.10g. ti_01.ti_1_0tt D	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2
	2 34

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Name	Input Value	
arget I2c SetRecv I2cRegPtr Cnt T str.STR	455	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	847	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	987	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	487	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	34	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	34	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	24	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	847	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	56	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	24	
arget I2c SetRecv I2cRegPtr Cnt T str.PID11	987	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	24	
	2	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	3	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	
irget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN		
irget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	2	
rget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	2	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	
irget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	34	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	24	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	455	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	847	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	987	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	487	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	34	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	34	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	24	
rget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR	847	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	56	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	24	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	987	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	24	
arget I2c SetStatus I2cRegPtr Cnt T str.DMAC	2	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	
arget I2c SetStatus I2cRegPtr Cnt T str.SET	2	
arget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	3	
riget_12c_SetStatus_12cRegPtr_Cnt_1_str.ODR	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	34	
rrget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	24	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	455	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	847	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	987	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	487	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	34	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	34	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	24	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	847	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	56	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	24	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	987	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	24	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	
rget I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	2	
	2	
arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	3	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR		
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	

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Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	2		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	2		
target i2cREG1 temp.OAR	34		
target i2cREG1 temp.IMR	24		
target i2cREG1 temp.STR	455		
target i2cREG1 temp.CLKL	847		
target i2cREG1 temp.CLKH	987		
target i2cREG1 temp.CNT	487		
target i2cREG1 temp.DRR	34		
target i2cREG1 temp.SAR	34		
target i2cREG1 temp.DXR	24		
target_i2cREG1_temp.MDR	847		
target_i2cREG1_temp.IVR	56		
target i2cREG1 temp.EMDR	2		
target i2cREG1 temp.PSC	24		
target i2cREG1 temp.PID11	987		
target i2cREG1 temp.PID12	24		
target i2cREG1 temp.DMAC	2		
target i2cREG1 temp.FUN	0		
target i2cREG1 temp.DIR	3		
target i2cREG1_temp.DIN	3		
target i2cREG1 temp.DOUT	2		
target i2cREG1_temp.boo1	2		
target i2cREG1_temp.CLR	3		
target i2cREG1_temp.ODR	3		
	2		
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL	2		
Name	Actual Value	Expected Value	Pocult

target_i2cREG1_temp.PSL	2		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	6	6	~
DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	•
DigColPsInt_Buffer_Cnt_M_u08[1]	5	5	~
DigColPsInt_Buffer_Cnt_M_u08[2]	9	9	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt_ColSnsrData_Cnt_M_u16	847	847	~
DigColPsInt_CurrentSlave_Cnt_M_u08	15	15	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_SET	INIT_SENSOR1_EXTREADCTRLREG_SET	~
DigColPsInt_I2CHwCustData_Uls_M_u16	82	82	~
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	83	83	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	487	487	~
DigColPsInt_TransactionCnt_Cnt_M_u08	13	13	~
I2c_Send(Length_Cnt_T_u32)	1	1	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	34	34	~

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	24	24	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR	455 847	455 847	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	987	987	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT	487	487	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	34	34	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	34	34	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	24	24	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	847	847	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	56	56	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	24	24	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	987	987	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	24	24	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	3	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34	34	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24	24	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	455	455	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	847 987	987	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	487	487	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34	34	
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	34	34	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24	24	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847	847	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56	56	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24	24	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987	987	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24	24	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	34	34	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	24	24	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	455	455	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	847	847	<b>V</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	987	987 487	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	487	34	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	34	34	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	34 24	24	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	847	847	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	56	56	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	24	24	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	987	987	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	24	24	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	~



Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	34	34	Ž
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR	24	24	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	455	455	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	847	847	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	987	987	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	487	487	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	34	34	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	34	34	<b>-</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR	24 847	24 847	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	56	56	J
target I2c SetStatus I2cRegPtr Cnt T str.EMDR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	24	24	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	987	987	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	24	24	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3 2	3 2	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	2	2	9
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SE1	3	3	~
target I2c SetStatus I2cRegPtr Cnt T str.ODR	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	34	34	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	24	24	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	455	455	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	847	847	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	987	987 487	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	487 34	34	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	34	34	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	24	24	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	847	847	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	56	56	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	24	24	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	987	987	-
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	24	24	<b>*</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.FUN	0	0	~
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	- 4
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	34	2 34	-
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	24	24	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455	455	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847	847	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987	987	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487	487	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34	34	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34	34	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24	24	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847	847 56	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	56 2	2	- J
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24	24	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987	987	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24	24	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	3	2 3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	, v	, <del>,</del>	

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DigColPsInt_In	terruptNotification
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Name	Actual Value	Expected Value	Result
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	3	3	<b>→</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	2	2	<b>✓</b>

Т				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	l2c_Send	1	~

Test Step 2.29 (Repeat Count = 1)	
	Innut Value
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	6
DigColPsInt_Buffer_Cnt_M_u08[0]	10 20
DigColPoint_Buffer_Cnt_M_u08[1]	30
DigColPoInt_Buffer_Cnt_M_u08[2]	1
DigColPoint_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColCustDatround_Cnt_M_gc  DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	30
DigColPsInt CurrentStepNo Cnt M enum	INIT_SENSOR2_EXTREADCTRLREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	85
DigColPsInt I2CHwIncompleteCustData Uls M u16	86
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt SkipRegisterWrite Cnt M Igc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt TransactionCnt Cnt M u08	14
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	19
k_SpurSensorI2CAddress_Cnt_u08	120
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55 66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	2309
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR	5
target 12c GenStopCond 12cRegPtr_Cnt_T_str.tvR	3
target 12c GenStopCond 12cRegPtr Cnt T str.PSC	66
target 12c GenStopCond 12cRegPtr_Cnt_T_str.PSC	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.FUN	1
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DIR	1
g-1	

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Input Value 2 3 3	Name target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT
3	
	arget 12c GenStonCond 12cRegPtr Cnt T str DOUT
3	a.gotzo_conctopcondzor.cg.
	arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET
1	arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR
2	arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR
3	arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD
3	arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL
55	arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR
66	arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR
556	arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR
2309	arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL
1204	arget I2c Send I2cRegPtr Cnt T str.CLKH
87	arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT
67	
	arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR
55	arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR
66	arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR
2309	arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR
5	arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR
3	arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR
66	arget_l2c_Send_l2cRegPtr_Cnt_T_str.PSC
1204	arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11
66	arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12
3	arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC
1	arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN
1	arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR
2	arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN
3	arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT
3	arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET
1	arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR
2	arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR
3	arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD
3	arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL
55	arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR
66	arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR
556	rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR
2309	arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL
1204	rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH
87	arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT
67	
	rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR
55	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR
66	rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR
2309	arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR
5	arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR
3	arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR
66	arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC
1204	arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11
66	arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12
3	arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC
1	arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN
1	arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR
2	arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN
3	arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT
3	arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET
1	arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR
2	arget I2c SetRecv I2cRegPtr Cnt T str.ODR
3	arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD
3	arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL
55	arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR
66	arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR
556	arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR
2309	arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL
1204	arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH
87	arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT
67	arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR
55	arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR
66	
2309	
66	arget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PlD12 arget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC
66	target_Izc_setstatus_IzcRegPtr_Cntstr.sAR  target_Izc_setStatus_IzcRegPtr_Cnt_T_str.DXR  target_Izc_setStatus_IzcRegPtr_Cnt_T_str.MDR  target_Izc_setStatus_IzcRegPtr_Cnt_T_str.IVR  target_Izc_setStatus_IzcRegPtr_Cnt_T_str.EMDR  target_Izc_setStatus_IzcRegPtr_Cnt_T_str.PSC  target_Izc_setStatus_IzcRegPtr_Cnt_T_str.PID11  target_Izc_setStatus_IzcRegPtr_Cnt_T_str.PID12

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Name	Input Value
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
	2309
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
	66
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	67
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target i2cREG1 temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target i2cREG1 temp.CNT	87
target i2cREG1 temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target i2cREG1 temp.EMDR	3
target i2cREG1 temp.PSC	66
	100
target i2cREG1 temp.PID11	1204



Name	Input Value		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result

target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	7	7	~
DigColPsInt Buffer Cnt M u08[0]	12	12	<b>~</b>
DigColPsInt Buffer Cnt M u08[1]	20	20	_
DigColPsInt Buffer Cnt M u08[2]	30	30	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	
DigColPsInt CmdFailOccurred Cnt M Igc	1	1	-
DigColPsInt ColCustDatFound Cnt M Igc	0	0	
DigColPsInt ColSnsrData Cnt M u16	2309	2309	-
DigColPsInt CurrentSlave Cnt M u08		19	
·	19		<b>V</b>
DigColPsInt_CurrentStepNo_Cnt_M_enum		INIT_SENSOR1_EXTREADCTRLREG_SET	
DigColPsInt_I2CHwCustData_UIs_M_u16	85	85	~
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	86	86	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	~
DigColPsInt_RecvdDataType_Cnt_M_u08	5	5	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	~
DigColPsInt_TransactionCnt_Cnt_M_u08	14	14	~
I2c_Send(Length_Cnt_T_u32)	1	1	<b>✓</b>
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
target I2c GenStopCond I2cRegPtr Cnt T str.OAR	55	55	~
target I2c GenStopCond I2cRegPtr Cnt T str.IMR	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	_
target I2c GenStopCond I2cRegPtr Cnt T str.CLKH	1204	1204	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>~</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR	55	55	
target I2c GenStopCond I2cRegPtr Cnt T str.DXR	66	66	~
· · - · · ·	2309	2309	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR			-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	J
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	~
target I2c Send I2cRegPtr Cnt T str.CLKL	2309	2309	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>~</b>
target I2c Send I2cRegPtr Cnt T str.DRR	67	67	_
target I2c Send I2cRegPtr Cnt T str.SAR	55	55	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR			
	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	66	66	
torget 12a Sond 12aBoaBtr Cnt T etr IVD	2309	2309	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	2309 5	2309 5	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2309 5 3	2309 5 3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	2309 5 3 66	2309 5 3 66	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2309 5 3	2309 5 3	~

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN target_l2c Send_l2cRegPtr_Cnt_T str.DOUT	3	2 3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>Y</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	87 67	87 67	<i>y</i>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	55	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>*</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	<i>y</i>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	3	3	Ž
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66 2309	66 2309	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	5	5	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	<b>~</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	1	1	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	2	2	-
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL	3	3 3	
target_I2c_SetStatus_I2cRegPtI_Cnt_T_str.PSL target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>

T				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c Send	1	I2c Send	1	_

Test Step 2.30 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	7
DigColPsInt_Buffer_Cnt_M_u08[0]	22
DigColPsInt_Buffer_Cnt_M_u08[1]	44
DigColPsInt_Buffer_Cnt_M_u08[2]	55
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	495
DigColPsInt_CurrentSlave_Cnt_M_u08	40
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	88
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	89
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	897
DigColPsInt_TransactionCnt_Cnt_M_u08	6
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str



DigColPSInt_Interruptivotinication		MACILIA
Name	Input Value	
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str	
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str	
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str	
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str	
Γ_DataRegisters_Cnt_u08[0]	0	
_DataRegisters_Cnt_u08[1]	32	
_DataRegisters_Cnt_u08[2]	30	
_DataRegisters_Cnt_u08[3]	36	
	38	
	34	
	10	
	12	
	14	
2cREG1_temp	target_i2cREG1_temp	
_ColSensorl2CAddress_Cnt_u08	23	
SpurSensorI2CAddress Cnt u08	5	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	78	
	78	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR		
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	495	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	56	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	897	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	98	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	78	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	495	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	78	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	56	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	78	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	
arget I2c Send I2cRegPtr Cnt T str.OAR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	
	56	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.UMR	78	
arget_l2c_SetRecv_l2cRegPti_Cnt_T_str.lmiR arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	78	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	
arget_12c_SetRecv_12cRegPtr_Cnt_T_str.CLKL  arget_12c_SetRecv_12cRegPtr_Cnt_T_str.CLKH  arget_12c_SetRecv_12cRegPtr_Cnt_T_str.CNT	56 897	

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Name	Input Value
	66
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target I2c SetRecv I2cRegPtr Cnt T str.DIR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
	0
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	56
target I2c SetStatus I2cRegPtr Cnt T str.CNT	897
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	66
	0
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
	0
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
	0
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	495
	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495
target I2c SetupMasterReceive I2cRegPtr Cnt T str.IVR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	0
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78
	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56

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DigColPsInt\_InterruptNotification

Name target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	Input Value 897		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	98		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0 78		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	56		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
target_i2cREG1_temp.OAR	66		
target_i2cREG1_temp.IMR	78		
target_i2cREG1_temp.STR	78		
target_i2cREG1_temp.CLKL	495		
target_i2cREG1_temp.CLKH	56		
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	98 98		
target_i2cREG1_temp.SAR	66		
target_i2cREG1_temp.DXR	78		
target i2cREG1 temp.MDR	495		
target_i2cREG1_temp.IVR	66		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	78		
target_i2cREG1_temp.PID11	56		
target_i2cREG1_temp.PID12	78		
target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target i2cREG1 temp.DIN	1		
target_i2cREG1_temp.DOUT	0		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	0	l=	<u> </u>
Name  DisColleget Attemp@courForCustDatDood Ont M u00	Actual Value 8	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	· ·
DigColPsInt_Buffer_Cnt_M_u08[1]	44	44	
DigColPsInt Buffer Cnt M u08[2]	55	55	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	495	495	<b>V</b>
DigColPsInt_CurrentSlave_Cnt_M_u08	23	23	<b>V</b>
DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16	INIT_SENSOR1_EXTREADCTRLREG_SET	INIT_SENSOR1_EXTREADCTRLREG_SET 88	~
DigColPsInt_I2CHwCustData_Ois_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	89	89	-
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1	1	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	•
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_RecvdDataType_Cnt_M_u08	1	1	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	897	897	<b>V</b>
DigColPsInt_TransactionCnt_Cnt_M_u08	6	6	_
I2c_Send(Length_Cnt_T_u32) I2c SetupMasterTransmit(DataLength Cnt T u16)	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	66	66	- V
target I2c GenStopCond I2cRegPtr Cnt T str.IMR	78	78	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	78	78	<b>~</b>
target 12c GenStonCond 12cRegPtr Cnt T str CLKI	495	495	-

495

56

897

495

56

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKL

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKH$ 

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	98 66	98 66	<b>-</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR	78	78	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	495	495	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0	0	<b>✓</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FUN target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR	0	0	, v
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	0	0	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78 78	78 78	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	56	56	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	78 56	78 56	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	0	1	- V
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	78	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	98	<b>*</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66 78	66 78	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495	495	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66	66	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	78	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1 0	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	0	0	- v
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	0	0	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	·
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	•
	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL			
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	66	66	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66 78	78	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	66		· ·

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<u> </u>	I		
Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	56	56	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	897	897	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR	98	98	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR	66	66	<b>V</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	78	78	<b>V</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR	495	495	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	66 0	66 0	<b>Y</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR			
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC	78 56	78 56	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11	78	78	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12	0	0	-
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC	0	0	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN		0	-4
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR	0		
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN		1	-4
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	0	0	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	0	0	-4
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78	78	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78	78	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>~</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~
	'		-



T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c Send	1	I2c Send	1	_

est Step 2.31 (Repeat Count = 1)	Innut Value
ame	Input Value
igColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8
igColPsInt_Buffer_Cnt_M_u08[0]	10
igColPsInt_Buffer_Cnt_M_u08[1]	15
igColPsInt_Buffer_Cnt_M_u08[2]	16
igColPsInt_BusBusySeqError_Cnt_M_lgc	1
igColPsInt_CmdFailOccurred_Cnt_M_lgc	1
igColPsInt_ColCustDatFound_Cnt_M_lgc	1
igColPsInt_ColSnsrData_Cnt_M_u16	566
igColPsInt_CurrentSlave_Cnt_M_u08	50
igColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADDATREG_READ
igColPsInt_I2CHwCustData_Uls_M_u16	91
igColPsInt_I2CHwIncompleteCustData_Uls_M_u16	0
igColPsInt_InitFailedOnce_Cnt_M_Igc	0
igColPsInt_NackOccured_Cnt_M_lgc	1
igColPsInt_PrevReqDataType_Cnt_M_u08	5
igColPsInt_RecvOverrunError_Cnt_M_lgc	1
igColPsInt_RecvdDataType_Cnt_M_u08	2
igColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
igColPsInt_SpurCustDatFound_Cnt_M_lgc	1
igColPsInt_SpurSnsrData_Cnt_M_u16	129
igColPsInt TransactionCnt Cnt M u08	7
lags_Cnt_T_b16	32
c GenStopCond(I2cRegPtr Cnt T str)	target I2c GenStopCond I2cRegPtr Cnt T str
cc_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
c SetRecv(I2cRegPtr Cnt T str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
c SetStatus(I2cRegPtr Cnt T str)	target I2c SetStatus I2cRegPtr Cnt T str
c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
	0
_DataRegisters_Cnt_u08[0]	32
_DataRegisters_Cnt_u08[1]	30
_DataRegisters_Cnt_u08[2]	36
_DataRegisters_Cnt_u08[3]	
_DataRegisters_Cnt_u08[4]	38
_DataRegisters_Cnt_u08[5]	34
_DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
_DataRegisters_Cnt_u08[8]	14
cREG1_temp	target_i2cREG1_temp
_ColSensorl2CAddress_Cnt_u08	27
_SpurSensorI2CAddress_Cnt_u08	10
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567
rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR	44
irget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566
irget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
rget I2c GenStopCond I2cRegPtr Cnt T str.PSC	44
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44
riget I2c GenStopCond I2cRegPtr Cnt T str.DMAC	1
irget_12c_GenStopCond_12cRegPtr_Cnt_T_str.FUN	1
	2
urget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
irget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
irget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT	
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1

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DigColPSint_Interruptivotilication		
Name	Input Value	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.STR	4444	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR arget_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	44	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	
arget I2c Send I2cRegPtr Cnt T str.DMAC	1	
arget I2c Send I2cRegPtr Cnt T str.FUN	1	
arget I2c Send I2cRegPtr Cnt T str.DIR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	129	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1 44	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC arget l2c SetRecv l2cRegPtr Cnt T str.PID11	4466	
arget I2c SetRecv I2cRegPtr Cnt T str.PID12	44	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PIDI2	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	

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	(
Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	1
target I2c SetupMasterReceive I2cRegPtr Cnt T str.FUN	1
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	2
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	44
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	44
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target i2cREG1 temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44
target i2cREG1 temp.MDR	566
target i2cREG1 temp.IVR	554
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	44
target_i2cREG1_temp.PID11	4466
	44
target_i2cREG1_temp.PID12	
	1
target_i2cREG1_temp.DMAC	1
	1 1 2

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Name	Innut Value		
	Input Value		
target_i2cREG1_temp.DIN	0		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8	8	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✓
DigColPsInt_Buffer_Cnt_M_u08[1]	15	15	✓
DigColPsInt_Buffer_Cnt_M_u08[2]	16	16	✓
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✓
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✓
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✓
DigColPsInt_ColSnsrData_Cnt_M_u16	566	566	✓
DigColPsInt_CurrentSlave_Cnt_M_u08	50	50	<b>✓</b>
DigColPsInt_CurrentStepNo_Cnt_M_enuo			

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	· ·
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3	3	· ·
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	·
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	129	129	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	6	6	<b>v</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	567	567 44	· ·
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	566	566	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	· ·
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	4466 129	4466 129	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	✓
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	3 567	3 567	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	· ·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	44	1 44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	44 4466	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PD

 $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSL$ 

DigColPsInt\_InterruptNotification

2014-10-14, 23:42:41+0530



**Actual Value Expected Value** target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.DOUT  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.SET$ target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.CLR 2 2  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.ODR$ 0 0 target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.PD 3 3 target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.PSL 3 3 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.OAR 567 567  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IMR$ 44 44 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.STR 4444 4444  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKL$ 566 566 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKH 4466 4466  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CNT$ 129 129  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DRR$ 6 567  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SAR$ 567  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DXR$ 44 44 566 566 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.MDR  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IVR$ 554 554  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.EMDR$ 1 1  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSC$ 44 44  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID11$ 4466 4466  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID12$ 44 44 **Y Y** target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DMAC 1  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.FUN$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIR 2 2 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIN 0 0  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DOUT$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SET 1  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLR$ 2 2 target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR 0 0

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

3

3

3

3

Name	Test Step 2.32 (Repeat Count = 1)	<b>✓</b>
DigCoIPsInt_Buffer_Cnt_M_u08[0]   28   DigCoIPsint_Buffer_Cnt_M_u08[1]   56   DigCoIPsint_Buffer_Cnt_M_u08[2]   100   DigCoIPsint_Buffer_Cnt_M_u08[2]   100   DigCoIPsint_BusBusySeqError_Cnt_M_lgc   0   DigCoIPsint_ColicustalGound_Cnt_M_lgc   0   DigCoIPsint_ColicustalGound_Cnt_M_lgc   1   DigCoIPsint_ColicustalGound_Cnt_M_lgc   1   DigCoIPsint_ColicustalGound_Cnt_M_lgc   1   DigCoIPsint_ColicustalGound_Cnt_M_lgc   1   DigCoIPsint_ColicustalGound_Cnt_M_lgc   0   DigCoIPsint_ColicustalGound_Cnt_M_lgc   0   DigCoIPsint_ColicustalGound_Cnt_M_lgc   0   DigCoIPsint_ColicustalGound_Cnt_M_lgc   0   DigCoIPsint_InitialGoting_ColicustalGound_Cnt_M_lgc   0   DigCoIPsint_DigCoIPsint_DigCoIPsint_DigCoIPsint_DigCoIPsint_DigCoIPsint_DigCoIPsint_DigCoIPsint_DigCoIPsint_DigCoIPsint_DigCoIPsint_DigCoIPsint_DigCoIPsint_DigCoIPsint_DigCoIPsint_DigCoIPsint_DigCoIPsint_DigCoIPsint_DigCoIPsint_DigCoIPsint_PirexPeapOstatType_Cnt_M_u08   3   DigCoIPsint_RecvOverrunError_Cnt_M_lgc   0   DigCoIPsint_RecvOverrunError_Cnt_M_lgc   0   DigCoIPsint_SpurCustDigCoIPc_Cnt_M_lgc   0   DigCoIPsint_TransactionCnt_Cnt_M_u08   8   Bigg_Coil_Tit_SpurCustDigCoIPc_Cnt_M_lgc   0   DigCoIPsint_TransactionCnt_Cnt_M_u08   8   Bigg_Coil_Tit_SpurCustDigCoIPc_Cnt_T_str)   target_I2c_SenSport_Cnt_T_str   target_I2c_SenSport_Cnt_T_str   I2c_SenSport_Cnt_T_str)   target_I2c_SenSport_Cnt_T_str   I2c_SenSport_Cnt_T_str   target_I2c_Sent_DigCoIPc_Lot_T_str   I2c_Sent_DigCoIPc_Cnt_T_str   target_I2c_Sent_DigCoIPc_Lot_T_str   I2c_Sent_DigCoIPc_Cnt_T_str   target_I2c_Sent_DigCoIPc_Lot_T_str   I2c_Sent_DigCoIPc_Cnt_T_str   target_I2c_Sent_DigCoIPc_Lot_T_str   I2c_Sent_DigCoIPc_Cnt_T_str   target_I2c_Sent_DigCoIPc_Lot_T_str   I2c_Sent_DigCoIPc_Lot_T_str   targ		Input Value
DigColPsInt_Buffer_Cnt_M_u08[1]   56     DigColPsint_Buffer_Cnt_M_u08[2]   100     DigColPsint_BusBusysepErr_Cnt_M_u08   0     DigColPsint_ColCustDalFound_Cnt_M_lgc   0     DigColPsint_ColCustDalFound_Cnt_M_u1gc   1     DigColPsint_ColCustDalFound_Cnt_M_u1gc   1     DigColPsint_ColFostPolat_Cnt_M_u1gc   0     DigColPsint_CurrentSlave_Cnt_M_u08   60     DigColPsint_CurrentSlave_Cnt_M_u08   60     DigColPsint_CurrentSlave_Cnt_M_u08   60     DigColPsint_IcCurrentSlave_Cnt_M_u08   60     DigColPsint_IcChWcustData_Uis_M_u16   94     DigColPsint_IcChWcustData_Uis_M_u16   94     DigColPsint_IcChWcustData_Uis_M_u16   255     DigColPsint_IcChWcustData_Uis_M_u16   255     DigColPsint_IcChWcustData_Uis_M_u16   255     DigColPsint_IcChWcustData_Uis_M_u18   0     DigColPsint_IcChWcustData_Uis_M_u18   0     DigColPsint_NackOccured_Cnt_M_lgc   0     DigColPsint_NackOccured_Cnt_M_lgc   0     DigColPsint_NewQeartunError_Cnt_M_u08   3     DigColPsint_NewQeartunError_Cnt_M_u08   3     DigColPsint_RevOverrunError_Cnt_M_u08   3     DigColPsint_RevOverrunError_Cnt_M_u08   3     DigColPsint_SpurCustDalFound_Cnt_M_lgc   0     DigColPsint_SpurCustDalFound_Cnt_M_lgc   0     DigColPsint_SpurCustDalFound_Cnt_M_lgc   0     DigColPsint_SpurCustDalFound_Cnt_M_lgc   0     DigColPsint_TransactionCnt_Cnt_M_u08   8     Flags_Cnt_T_b16   32     L2_GenStopCond(!2cRepPtr_Cnt_T_str)   target_!2c_GenStopCond_!2cRepPtr_Cnt_T_str     L2c_Sent(!2cRepPtr_Cnt_T_str)   target_!2c_SentStopCond_!2cRepPtr_Cnt_T_str     L2c_Sent(!2cRepPtr_Cnt_T_str)   target_!2c_SentStopCond_!2cRepPtr_Cnt_T_str     L2c_SentStatus(!2cRepPtr_Cnt_T_str)   target_!2c_SentStatus !2cRepPtr_Cnt_T_str     L2c_SetUpMasterTransmit_!2cRepPtr_Cnt_T_str   target_!2c_SetUpMasterTransmit_!2cRepPtr_Cnt_T_str     L2c_SetUpMasterTransmit_!2cRepPtr_Cnt_T_str   target_!2c_SetUpMasterTransmit_!2cRepPtr_Cnt_T_str     L2c_SetUpMasterTransmit_!2cRepPtr_Cnt_T_str   target_!2c_SetUpMasterTransmit_!2cRepPtr_Cnt_T_str     L2c_SetUpMasterTransmit_!2cRepPtr_Cnt_T_str   target_!2c_SetUpMasterTransmit_!2cR	DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	9
DigColPsint Buffer Cnt_N_u08[2]   100     DigColPsint_BusBusySegError_Cnt_M_lgc	DigColPsInt_Buffer_Cnt_M_u08[0]	28
DigColPsInt_BusBusySeqError_Cnt_M_lgc         0           DigCoPsInt_ColCustDatFortond_Cnt_M_lgc         0           DigCoPsInt_ColCustDatFortond_Cnt_M_lgc         1           DigCoPsInt_ColFsnrData_Cnt_M_u16         7           DigColPsInt_CurrentSiave_Cnt_M_u08         60           DigColPsInt_CurrentSiave_Cnt_M_u08         60           DigColPsInt_IZCHWcustData_UIs_M_u16         94           DigColPsInt_IZCHWcustData_UIs_M_u16         94           DigColPsInt_IZCHWcustData_UIs_M_u16         255           DigColPsInt_InitFailedOnce_Cnt_M_lgc         1           DigColPsInt_InitFailedOnce_Cnt_M_lgc         0           DigColPsInt_PrevReqDataType_Cnt_M_u08         3           DigColPsInt_RevOverunError_Cnt_M_lgc         0           DigColPsInt_RevOverunError_Cnt_M_lgc         0           DigColPsInt_SpurCoutDatFound_Cnt_M_lgc         0           DigColPsInt_SpurCoutDatFound_Cnt_M_lgc         0           DigColPsInt_SpurCoutDatFound_Cnt_M_lgc         0           DigColPsInt_TransactionCnt_M_u16         88           DigColPsInt_TransactionCnt_Ont_M_u16         88           DigColPsInt_TransactionCnt_Ont_M_u16         88           DigColPsInt_TransactionCnt_Ont_M_u16         32           12c_SentopCond(l2cRegPtr_Cnt_T_str)         target_l2c_SentScot_L0ct_Cnt_T_	DigColPsInt_Buffer_Cnt_M_u08[1]	56
DigColPsInt_CodCustDatFound_Cnt_M_lgc         1           DigColPsInt_ColCustDatFound_Cnt_M_lgc         1           DigColPsInt_ColInstData_Cnt_M_u16         7           DigColPsInt_CurrentSlave_Cnt_M_u08         60           DigColPsInt_CurrentSlave_Cnt_M_u08         60           DigColPsInt_IzCHwCustData_Uls_M_u16         94           DigColPsInt_IzCHwIncompleteCustData_Uls_M_u16         255           DigColPsInt_InitFailedOnce_Cnt_M_lgc         1           DigColPsInt_NewCocured_Cnt_M_lgc         0           DigColPsInt_NewCocured_Cnt_M_lgc         0           DigColPsInt_RecvOverrunError_Cnt_M_u08         3           DigColPsInt_RecvDataType_Cnt_M_u08         3           DigColPsInt_RecvDataType_Cnt_M_u08         3           DigColPsInt_SpurCustDatGroud_Cnt_M_lgc         0           DigColPsInt_SpurCustDatGroud_Cnt_M_lgc         0           DigColPsInt_SpurCustDatGroud_Cnt_M_u16         88           DigColPsInt_TransactionCnt_Cnt_M_u08         8           Flags_Cnt_T_b16         32           12c_GenStopCond(l2cRegPtr_Cnt_T_str)         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str           12c_Send(l2cRegPtr_Cnt_T_str)         target_l2c_Send_l2cRegPtr_Cnt_T_str           12c_SetupMasterTransmit(l2cRegPtr_Cnt_T_str)         target_l2c_SetNewAsterTransmit_l2cRegPtr_Cnt_T_str	DigColPsInt_Buffer_Cnt_M_u08[2]	100
DigColPsInt_ColCustDatFound_Cnt_M_Igc	DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_CurrentSlave_Cnt_M_u08	DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_CurrentStepNo_Cnt_M_enum	DigColPsInt_ColSnsrData_Cnt_M_u16	7
DigColPsInt_2CHwCustData_Uls_M_u16         94           DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16         255           DigColPsInt_InitFailedOnce_Cnt_M_lgc         1           DigColPsInt_NackOccured_Cnt_M_lgc         0           DigColPsInt_PrevReqDataType_Cnt_M_u08         3           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0           DigColPsInt_RecvDataType_Cnt_M_u08         3           DigColPsInt_RecvDataType_Cnt_M_u08         3           DigColPsInt_SpurCustDatFound_Cnt_M_lgc         0           DigColPsInt_SpurCustDatFound_Cnt_M_lgc         0           DigColPsInt_SpurSnsrData_Cnt_M_u16         88           DigColPsInt_TransactionCnt_Cnt_M_u08         8           Flags_Cnt_T_b16         32           12c_GenStopCond(l2cRegPtr_Cnt_T_str)         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str           12c_Send(l2cRegPtr_Cnt_T_str)         target_l2c_Send_l2cRegPtr_Cnt_T_str           12c_Sent(l2cRegPtr_Cnt_T_str)         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str           12c_SetStatus(l2cRegPtr_Cnt_T_str)         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str           12c_SetUpMasterReceive(l2cRegPtr_Cnt_T_str)         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str           12c_SetUpMasterTransmit(l2cRegPtr_Cnt_T_str)         target_l2c_SetUpMasterTransmit_l2cRegPtr_Cnt_T_str           12c_SetUpMasterTransmit(l2cRegPtr_Cnt_T_str) <td>DigColPsInt_CurrentSlave_Cnt_M_u08</td> <td>60</td>	DigColPsInt_CurrentSlave_Cnt_M_u08	60
DigCoIPsInt_I2CHwIncompleteCustData_UIs_M_u16         255           DigCoIPsInt_InitFalledOnce_Cnt_M_lgc         1           DigCoIPsInt_NackOccured_Cnt_M_lgc         0           DigCoIPsInt_PrevReqDataType_Cnt_M_u08         3           DigCoIPsInt_RecvOverrunError_Cnt_M_lgc         0           DigCoIPsInt_RecvDataType_Cnt_M_u08         3           DigCoIPsInt_SkipRegisterWrite_Cnt_M_lgc         0           DigCoIPsInt_SpurCustDatFound_Cnt_M_lgc         0           DigCoIPsInt_SpurSnsrData_Cnt_M_u16         88           DigCoIPsInt_TransactionCnt_Cnt_M_u08         8           Flags_Cnt_T_b16         32           12c_GenStopCond(I2cRegPtr_Cnt_T_str)         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str           12c_Send(I2cRegPtr_Cnt_T_str)         target_I2c_Send_I2cRegPtr_Cnt_T_str           12c_SetRecv(I2cRegPtr_Cnt_T_str)         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str           12c_SetStatus(I2cRegPtr_Cnt_T_str)         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str           12c_SetUpMasterReceive(I2cRegPtr_Cnt_T_str)         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str           12c_SetUpMasterReceive_I2cRegPtr_Cnt_T_str         target_I2c_SetUpMasterTransmit(I2cRegPtr_Cnt_T_str           12c_SetUpMasterTransmit(I2cRegPtr_Cnt_T_str)         target_I2c_SetUpMasterTransmit(I2cRegPtr_Cnt_T_str           12c_SetUpMasterReceive_I2cRegPtr_Cnt_T_str         target_I2c_SetUpMa	DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADDATREG_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	DigColPsInt_I2CHwCustData_Uls_M_u16	94
DigColPsInt_NackOccured_Cnt_M_lgc         0           DigColPsInt_PrevReqDataType_Cnt_M_u08         3           DigColPsInt_RecvOverrunError_Cnt_M_lgc         0           DigColPsInt_RecvDataType_Cnt_M_u08         3           DigColPsInt_SkipRegisterWrite_Cnt_M_lgc         0           DigColPsInt_SpurCustDatFound_Cnt_M_lgc         0           DigColPsInt_SpurSnsData_Cnt_M_u16         88           DigColPsInt_TransactionCnt_Cnt_M_u08         8           Flags_Cntb16         32           12c_GenStopCond(l2cRegPtr_Cnt_T_str)         target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str           12c_Send(l2cRegPtr_Cnt_T_str)         target_l2c_Send_l2cRegPtr_Cnt_T_str           12c_SetRecv(l2cRegPtr_Cnt_T_str)         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str           12c_SetStatus(l2cRegPtr_Cnt_T_str)         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str           12c_SetUpMasterReceive(l2cRegPtr_Cnt_T_str)         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str           12c_SetUpMasterTransmit(l2cRegPtr_Cnt_T_str)         target_l2c_SetUpMasterReceive_l2cRegPtr_Cnt_T_str           12c_SetUpMasterTransmit(l2cRegPtr_Cnt_T_str)         target_l2c_SetUpMasterTransmit_l2cRegPtr_Cnt_T_str           1_DataRegisters_Cnt_u08[1]         32           1_DataRegisters_Cnt_u08[2]         30	DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	255
DigColPsInt_PrevReqDataType_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvdDataType_Cnt_M_u08 3 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc 0 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16 88 DigColPsInt_TransactionCnt_Cnt_M_u08 8 Flags_Cnt_T_b16 32 I2c_GenStopCond(I2cRegPtr_Cnt_T_str) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str I2c_Send(I2cRegPtr_Cnt_T_str) target_I2c_Send_I2cRegPtr_Cnt_T_str I2c_SetRecv(I2cRegPtr_Cnt_T_str) target_I2c_SetRecv_I2cRegPtr_Cnt_T_str I2c_SetRecv_I2cRegPtr_Cnt_T_str I2c_SetRecv_I2cRegPtr_Cnt_T_str I2c_SetStatus(I2cRegPtr_Cnt_T_str) target_I2c_SetStatus(I2cRegPtr_Cnt_T_str I2c_SetUpMasterReceive(I2cRegPtr_Cnt_T_str) target_I2c_SetUpMasterReceive_I2cRegPtr_Cnt_T_str I2c_SetUpMasterTransmit(I2cRegPtr_Cnt_T_str) I2c_SetUpMasterTransmit(I2cRegPtr_Cnt_T_str) T_DataRegisters_Cnt_u08[0] 0 T_DataRegisters_Cnt_u08[2] 30	DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc         0           DigColPsInt_RecvdDataType_Cnt_M_u08         3           DigColPsInt_SkipRegisterWrite_Cnt_M_lgc         0           DigColPsInt_SpurCustDatFound_Cnt_M_lgc         0           DigColPsInt_SpurSnsrData_Cnt_M_u16         88           DigColPsInt_TransactionCnt_Cnt_M_u08         8           Flags_Cnt_T_b16         32           !2c_GenStopCond(!2cRegPtr_Cnt_T_str)         target_!2c_GenStopCond_!2cRegPtr_Cnt_T_str           !2c_Send(!2cRegPtr_Cnt_T_str)         target_!2c_Send_!2cRegPtr_Cnt_T_str           !2c_Send(!2cRegPtr_Cnt_T_str)         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str           !2c_SetRecv(!2cRegPtr_Cnt_T_str)         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str           !2c_SetStatus(!2cRegPtr_Cnt_T_str)         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str           !2c_SetUpMasterReceive(!2cRegPtr_Cnt_T_str)         target_!2c_SetUpMasterReceive_!2cRegPtr_Cnt_T_str           !2c_SetUpMasterTransmit(!2cRegPtr_Cnt_T_str)         target_!2c_SetUpMasterTransmit_!2cRegPtr_Cnt_T_str           !2c_SetUpMasterSecrie_u08[0]         0           T_DataRegisters_Cnt_u08[1]         32           T_DataRegisters_Cnt_u08[2]         30	DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08         3           DigColPsInt_SkipRegisterWrite_Cnt_M_lgc         0           DigColPsInt_SpurCustDatFound_Cnt_M_u16         0           DigColPsInt_SpurSnsrData_Cnt_M_u16         88           DigColPsInt_TransactionCnt_Cnt_M_u08         8           Flags_Cnt_T_b16         32           I2c_GenStopCond(I2cRegPtr_Cnt_T_str)         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str           I2c_Send(I2cRegPtr_Cnt_T_str)         target_I2c_Send_I2cRegPtr_Cnt_T_str           I2c_SetRecv(I2cRegPtr_Cnt_T_str)         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str           I2c_SetStatus(I2cRegPtr_Cnt_T_str)         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str           I2c_SetUpMasterReceive(I2cRegPtr_Cnt_T_str)         target_I2c_Setstatus_I2cRegPtr_Cnt_T_str           I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str           I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str           I_DataRegisters_Cnt_u08[0]         0           T_DataRegisters_Cnt_u08[1]         32           T_DataRegisters_Cnt_u08[2]         30	DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc         0           DigColPsInt_SpurCustDatFound_Cnt_M_lgc         0           DigColPsInt_SpurSnsrData_Cnt_M_u16         88           DigColPsInt_TransactionCnt_Cnt_M_u08         8           Flags_Cnt_T_b16         32           I2c_GenStopCond(I2cRegPtr_Cnt_T_str)         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str           I2c_Send(I2cRegPtr_Cnt_T_str)         target_I2c_Send_I2cRegPtr_Cnt_T_str           I2c_SetRecv(I2cRegPtr_Cnt_T_str)         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str           I2c_SetStatus(I2cRegPtr_Cnt_T_str)         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str           I2c_SetUpMasterReceive(I2cRegPtr_Cnt_T_str)         target_I2c_SetUpMasterReceive_I2cRegPtr_Cnt_T_str           I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str           I2c_SetupMasterScot_u08[0]         0           T_DataRegisters_Cnt_u08[1]         32           T_DataRegisters_Cnt_u08[2]         30	DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_igc         0           DigColPsInt_SpurSnsrData_Cnt_M_u16         88           DigColPsInt_TransactionCnt_Cnt_M_u08         8           Flags_Cnt_T_b16         32           I2c_GenStopCond(I2cRegPtr_Cnt_T_str)         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str           I2c_Send(I2cRegPtr_Cnt_T_str)         target_I2c_Send_I2cRegPtr_Cnt_T_str           I2c_SetRecv(I2cRegPtr_Cnt_T_str)         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str           I2c_SetStatus(I2cRegPtr_Cnt_T_str)         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str           I2c_SetUpMasterReceive(I2cRegPtr_Cnt_T_str)         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str           I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str           I2c_SetupMasterScnt_u08[0]         0           T_DataRegisters_Cnt_u08[1]         32           T_DataRegisters_Cnt_u08[2]         30	DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SpurSnsrData_Cnt_M_u16         88           DigColPsInt_TransactionCnt_Cnt_M_u08         8           Flags_Cnt_T_b16         32           I2c_GenStopCond(I2cRegPtr_Cnt_T_str)         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str           I2c_Send(I2cRegPtr_Cnt_T_str)         target_I2c_Send_I2cRegPtr_Cnt_T_str           I2c_SetRecv(I2cRegPtr_Cnt_T_str)         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str           I2c_SetStatus(I2cRegPtr_Cnt_T_str)         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str           I2c_SetUpMasterReceive(I2cRegPtr_Cnt_T_str)         target_I2c_SetUpMasterReceive_I2cRegPtr_Cnt_T_str           I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str           T_DataRegisters_Cnt_u08[0]         0           T_DataRegisters_Cnt_u08[1]         32           T_DataRegisters_Cnt_u08[2]         30	DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_TransactionCnt_Cnt_Mu08         8           Flags_Cnt_T_b16         32           I2c_GenStopCond(I2cRegPtr_Cnt_T_str)         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str           I2c_Send(I2cRegPtr_Cnt_T_str)         target_I2c_Send_I2cRegPtr_Cnt_T_str           I2c_SetRecv(I2cRegPtr_Cnt_T_str)         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str           I2c_SetStatus(I2cRegPtr_Cnt_T_str)         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str           I2c_SetUpMasterReceive(I2cRegPtr_Cnt_T_str)         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str           I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str           T_DataRegisters_Cnt_u08[0]         0           T_DataRegisters_Cnt_u08[1]         32           T_DataRegisters_Cnt_u08[2]         30	DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
Flags_Cnt_T_b16         32           I2c_GenStopCond(I2cRegPtr_Cnt_T_str)         target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str           I2c_Send(I2cRegPtr_Cnt_T_str)         target_I2c_Send_I2cRegPtr_Cnt_T_str           I2c_SetRecv(I2cRegPtr_Cnt_T_str)         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str           I2c_SetStatus(I2cRegPtr_Cnt_T_str)         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str           I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str           I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str           T_DataRegisters_Cnt_u08[0]         0           T_DataRegisters_Cnt_u08[1]         32           T_DataRegisters_Cnt_u08[2]         30	DigColPsInt_SpurSnsrData_Cnt_M_u16	88
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)     target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str       I2c_Send(I2cRegPtr_Cnt_T_str)     target_I2c_Send_I2cRegPtr_Cnt_T_str       I2c_SetRecv(I2cRegPtr_Cnt_T_str)     target_I2c_SetRecv_I2cRegPtr_Cnt_T_str       I2c_SetStatus(I2cRegPtr_Cnt_T_str)     target_I2c_SetStatus_I2cRegPtr_Cnt_T_str       I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)     target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str       I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)     target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str       I2c_SetupMasterScnt_u08[0]     0       T_DataRegisters_Cnt_u08[1]     32       T_DataRegisters_Cnt_u08[2]     30	DigColPsInt_TransactionCnt_Cnt_M_u08	8
I2c_Send(I2cRegPtr_Cnt_T_str)     target_I2c_Send_I2cRegPtr_Cnt_T_str       I2c_SetRecv(I2cRegPtr_Cnt_T_str)     target_I2c_SetRecv_I2cRegPtr_Cnt_T_str       I2c_SetStatus(I2cRegPtr_Cnt_T_str)     target_I2c_SetStatus_I2cRegPtr_Cnt_T_str       I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)     target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str       I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)     target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str       I2c_SetupMasterScnt_u08[0]     0       T_DataRegisters_Cnt_u08[1]     32       T_DataRegisters_Cnt_u08[2]     30	Flags_Cnt_T_b16	32
I2c_SetRecv(I2cRegPtr_Cnt_T_str)     target_I2c_SetRecv_I2cRegPtr_Cnt_T_str       I2c_SetStatus(I2cRegPtr_Cnt_T_str)     target_I2c_SetStatus_I2cRegPtr_Cnt_T_str       I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)     target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str       I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)     target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str       T_DataRegisters_Cnt_u08[0]     0       T_DataRegisters_Cnt_u08[1]     32       T_DataRegisters_Cnt_u08[2]     30	I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)     target_I2c_SetStatus_I2cRegPtr_Cnt_T_str       I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)     target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str       I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)     target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str       T_DataRegisters_Cnt_u08[0]     0       T_DataRegisters_Cnt_u08[1]     32       T_DataRegisters_Cnt_u08[2]     30	I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)     target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str       I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)     target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str       T_DataRegisters_Cnt_u08[0]     0       T_DataRegisters_Cnt_u08[1]     32       T_DataRegisters_Cnt_u08[2]     30	I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)     target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str       T_DataRegisters_Cnt_u08[0]     0       T_DataRegisters_Cnt_u08[1]     32       T_DataRegisters_Cnt_u08[2]     30	I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]       0         T_DataRegisters_Cnt_u08[1]       32         T_DataRegisters_Cnt_u08[2]       30	I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[1]       32         T_DataRegisters_Cnt_u08[2]       30	I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[2] 30	T_DataRegisters_Cnt_u08[0]	0
	T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[3] 36	T_DataRegisters_Cnt_u08[2]	30
	T_DataRegisters_Cnt_u08[3]	36

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Name	Input Value	
T_DataRegisters_Cnt_u08[4]	38	
T DataRegisters Cnt u08[5]	34	
T_DataRegisters_Cnt_u08[6]	10	
T_DataRegisters_Cnt_u08[7]	12	
T DataRegisters Cnt u08[8]	14	
2cREG1_temp	target_i2cREG1_temp	
COISensorI2CAddress_Cnt_u08	31	
CSpurSensorl2CAddress_Cnt_u08	15	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	577	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	89	
	7	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR		
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR	44	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	
arget I2c GenStopCond I2cRegPtr Cnt T str.DOUT	2	
	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET		
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	
target I2c Send I2cRegPtr Cnt T str.CNT	88	
	23	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	89	
arget I2c Send I2cRegPtr Cnt T str.DMAC	2	
arget I2c Send I2cRegPtr Cnt T str.FUN	0	
· · · · ·	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65	
arget I2c SetRecv I2cRegPtr Cnt T str.IMR	89	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44	
	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89	

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Name         Input Value           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC         2           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN         0           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR         0           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN         1           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT         2           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET         2           target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR         0	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC       2         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN       0         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR       0         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN       1         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT       2         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET       2         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR       0	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN       0         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR       0         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN       1         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT       2         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET       2         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR       0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR       0         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN       1         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT       2         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET       2         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR       0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN       1         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT       2         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET       2         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR       0	
target l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT 2 target l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET 2 target l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR 0	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET 2 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR 0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR 0	
0 0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR 1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD 2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL 0	
. 3.2 2.11 1.2 1.3 12.1 2.21	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR 89	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR 67	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL 7	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH 577	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT 88	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR 23	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR 65	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR 89	
target I2c SetStatus I2cReqPtr Cnt T str.MDR 7	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR 44	
0 0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR 2	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC 89	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11 577	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12 89	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC 2	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN 0	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR 0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN 1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT 2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET 2	
0 0	
312 12111111112 1 1 1 1 1 2 2 1 1 1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD 2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL 0	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR 65	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR 89	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR 67	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL 7	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH 577	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT 88	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR 23	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR 65	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR 89	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR 7	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR 44	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR 2	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC 89	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11 577	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID12 89	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC 2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN 0	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIR 0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT 2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET 2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR 0	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR 1	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD 2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL 0	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR 65	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR 89	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR 67	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH 577	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT 88	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR 23	
angot_izo_compinación transmit_izonogi u_cini_ r_cin.Dritt	
target_I2c_SetupMasterTransmit_I2cRegPti_Cnt_T_str.SAR	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR 65	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR 65 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR 89 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR 7	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR  65 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR 89 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR 7 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR 44	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR 65 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR 89 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR 7	

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Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
target_i2cREG1_temp.OAR	65		
target i2cREG1 temp.IMR	89		
	67		
target_i2cREG1_temp.STR	7		
target_i2cREG1_temp.CLKL			
target_i2cREG1_temp.CLKH	577		
target_i2cREG1_temp.CNT	88		
target_i2cREG1_temp.DRR	23		
target_i2cREG1_temp.SAR	65		
target_i2cREG1_temp.DXR	89		
target_i2cREG1_temp.MDR	7		
target_i2cREG1_temp.IVR	44		
target_i2cREG1_temp.EMDR	2		
target_i2cREG1_temp.PSC	89		
target_i2cREG1_temp.PID11	577		
target_i2cREG1_temp.PID12	89		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target i2cREG1 temp.DIN	1		
target i2cREG1 temp.DOUT	2		
target i2cREG1 temp.SET	2		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
	2		
target_i2cREG1_temp.PD			
target_i2cREG1_temp.PSL	0	Formanda d Valura	D#
target_i2cREG1_temp.PSL  Name	0 Actual Value	Expected Value	Result
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	0 Actual Value	9	~
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]	0 Actual Value 9 28	9 28	~
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]	0 Actual Value 9 28 56	9 28 56	~
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]	0 Actual Value 9 28 56 100	9 28 56 100	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc	0 Actual Value 9 28 56 100 0	9 28 56 100 0	•
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0 Actual Value 9 28 56 100 0	9 28 56 100 0	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc	0 Actual Value 9 28 56 100 0 1	9 28 56 100 0 0	• • • • • • • • • • • • • • • • • • •
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0 Actual Value 9 28 56 100 0	9 28 56 100 0	•
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08	0 Actual Value 9 28 56 100 0 1	9 28 56 100 0 0	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc	0 Actual Value 9 28 56 100 0 1 7	9 28 56 100 0 0 1	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08	0 Actual Value 9 28 56 100 0 1 7 60	9 28 56 100 0 0 1 7	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum	0 Actual Value 9 28 56 100 0 1 7 60 INIT_COMPLETE	9 28 56 100 0 0 1 7 60 INIT_COMPLETE	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_l2CHwCustData_UIs_M_u16	0 Actual Value 9 28 56 100 0 1 7 60 INIT_COMPLETE 255	9 28 56 100 0 0 1 7 60 INIT_COMPLETE 255	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_l2CHwCustData_UIs_M_u16  DigColPsInt_l2CHwIncompleteCustData_UIs_M_u16	0 Actual Value 9 28 56 100 0 1 7 60 INIT_COMPLETE 255 255	9 28 56 100 0 0 1 7 60 INIT_COMPLETE 255 255	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_l2CHwCustData_UIs_M_u16  DigColPsInt_l2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_l2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_l2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_litFailedOnce_Cnt_M_lgc	0 Actual Value 9 28 56 100 0 1 7 60 INIT_COMPLETE 255 255	9 28 56 100 0 0 1 7 60 INIT_COMPLETE 255 255	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_igc  DigColPsInt_CmdFailOccurred_Cnt_M_igc  DigColPsInt_ColCustDatFound_Cnt_M_igc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_i2CHwCustData_Uis_M_u16  DigColPsInt_i2CHwIncompleteCustData_Uis_M_u16  DigColPsInt_i2CHwIncompleteCustData_Uis_M_u16  DigColPsInt_intFailedOnce_Cnt_M_igc  DigColPsInt_NackOccured_Cnt_M_igc	0 Actual Value 9 28 56 100 0 1 7 60 INIT_COMPLETE 255 255 1	9 28 56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_igc  DigColPsInt_CmdFailOccurred_Cnt_M_igc  DigColPsInt_ColCustDatFound_Cnt_M_igc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_i2CHwCustData_Uis_M_u16  DigColPsInt_i2CHwCustData_Uis_M_u16  DigColPsInt_i2CHwIncompleteCustData_Uis_M_u16  DigColPsInt_initFailedOnce_Cnt_M_igc  DigColPsInt_NackOccured_Cnt_M_igc  DigColPsInt_RecvOverrunError_Cnt_M_igc  DigColPsInt_RecvdDataType_Cnt_M_u08	0 Actual Value 9 28 56 100 0 1 7 60 INIT_COMPLETE 255 255 1 0 0	9 28 56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_igc  DigColPsInt_CmdFailOccurred_Cnt_M_igc  DigColPsInt_ColCustDatFound_Cnt_M_igc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_i2CHwCustData_Uis_M_u16  DigColPsInt_i2CHwCustData_Uis_M_u16  DigColPsInt_initFailedOnce_Cnt_M_igc  DigColPsInt_NackOccured_Cnt_M_igc  DigColPsInt_RecvOverrunError_Cnt_M_igc  DigColPsInt_RecvdDataType_Cnt_M_u08  DigColPsInt_RecvdDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_igc	0 Actual Value 9 28 56 100 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 3	9 28 56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 3	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvdDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustData_Cnt_M_u16	0 Actual Value 9 28 56 100 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 3 0 88	9 28 56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 3 0 88	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_L2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_I1ElledOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_u08  DigColPsInt_RecvData_Type_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustData_Cnt_M_u16  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08	0 Actual Value 9 28 56 100 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 3 0 88	9 28 56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 3 0 88	
target_i2cREG1_temp.PSL.  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I12CHwCustData_UIs_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvdDataType_Cnt_M_u08  DigColPsInt_RecvdDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	0 Actual Value 9 28 56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 0 3 0 88 8	9 28 56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 3 0 88 8	
target_i2cREG1_temp.PSL.  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I12CHwCustData_UIs_M_u16  DigColPsInt_I12CHwCustData_UIs_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvdDataType_Cnt_M_u08  DigColPsInt_RecvdDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	0 Actual Value 9 28 56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 3 0 88 8 8 65	9 28 56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 3 0 88 8 8 65	
target_i2cREG1_temp.PSL.  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvdDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	0 Actual Value 9 28 56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 3 0 88 8 8 65 89 67	9 28 56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 0 88 8 8 65 89 67	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_I3EdOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Ont_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	0 Actual Value 9 28 56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 0 3 0 88 8 8 65 89 67 7	9 28 56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 3 0 88 8 8 65 89 67 7	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_u18  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_litFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOvertunError_Cnt_M_u08  DigColPsInt_SpurCustDataFound_Cnt_M_lgc  DigColPsInt_SpurCustDataFound_Cnt_M_lgc  DigColPsInt_SpurCustDateTound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u08  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	0 Actual Value 9 28 56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 0 88 8 8 65 89 67 7 577	9 28 56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 3 0 88 8 8 65 89 67 7 577	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_u18  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_litFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_u08  DigColPsInt_RecvOverrunError_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	0 Actual Value 9 28 56 100 0 0 11 7 60 INIT_COMPLETE 255 255 1 0 0 0 3 0 88 88 8 65 89 67 7 577 88	9 28 56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 88 8 8 65 89 67 7 577 88	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u18  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	0 Actual Value 9 28 56 100 0 0 11 7 60 INIT_COMPLETE 255 255 1 0 0 0 3 0 88 88 8 65 89 67 7 577 88 23	9 28 56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 88 8 8 65 89 67 7 577 88 23	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	0 Actual Value 9 28 56 100 0 0 11 7 60 INIT_COMPLETE 255 255 1 0 0 0 3 0 88 8 65 89 67 7 577 88 23 65	9 28 56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 3 0 88 8 8 65 89 67 7 577 88 23 65	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvObataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.OAR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.STR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CNT  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR	0 Actual Value 9 28 56 100 0 0 11 7 60 INIT_COMPLETE 255 255 1 0 0 0 3 0 88 8 65 89 67 7 577 88 23 65 89	9 28 56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 3 0 88 8 8 65 89 67 7 577 88 23 65 89	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I1cHailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.OAR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.STR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CNT  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR	0 Actual Value 9 28 56 100 0 0 11 7 60 INIT_COMPLETE 255 255 1 0 0 0 3 0 88 8 65 89 67 7 577 88 23 65 89 7	9 28 56 100 0 0 17 7 60 INIT_COMPLETE 255 255 1 0 0 0 3 0 88 8 65 89 67 7 577 88 23 65 89 7	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_igc  DigColPsInt_ColCustDatFound_Cnt_M_igc  DigColPsInt_ColCustDatFound_Cnt_M_igc  DigColPsInt_ColCustDatFound_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I3cHoncompleteCustData_UIs_M_u16  DigColPsInt_NackOccured_Cnt_M_igc  DigColPsInt_RecvOverrunError_Cnt_M_igc  DigColPsInt_RecvOverrunError_Cnt_M_igc  DigColPsInt_SpurCustDatFound_Cnt_M_igc  DigColPsInt_SpurCustDatFound_Cnt_M_igc  DigColPsInt_TransactionCnt_Cnt_M_u08  target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.OAR  target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.STR  target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.STR  target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.CLKL  target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.CLKL  target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DRR	0 Actual Value 9 28 56 100 0 0 11 7 60 INIT_COMPLETE 255 255 1 0 0 0 3 0 88 8 8 65 89 67 7 577 88 23 65 89 7 44	9 28 56 100 0 0 17 7 60 INIT_COMPLETE 255 255 1 0 0 0 3 0 88 8 65 89 67 7 577 88 23 65 89 7 44	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_igc  DigColPsInt_ColCustDatFound_Cnt_M_igc  DigColPsInt_ColCustDatFound_Cnt_M_igc  DigColPsInt_ColCustDatFound_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I3cHoncompleteCustData_UIs_M_u16  DigColPsInt_NackOccured_Cnt_M_igc  DigColPsInt_NackOccured_Cnt_M_igc  DigColPsInt_RecvOverrunError_Cnt_M_igc  DigColPsInt_RecvOverrunError_Cnt_M_igc  DigColPsInt_SpurCustDatFound_Cnt_M_igc  DigColPsInt_SpurCustDatFound_Cnt_M_igc  DigColPsInt_TransactionCnt_Cnt_M_u08  target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.OAR  target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.IMR  target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.STR  target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.CkL  target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.CkL  target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DRR  target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DRR  target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DRR  target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DRR  target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DRR  target_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DXR	0 Actual Value 9 28 56 100 0 0 11 7 60 INIT_COMPLETE 255 255 1 0 0 0 88 8 65 89 67 7 577 88 23 65 89 7 44	9 28 56 100 0 0 17 7 60 INIT_COMPLETE 255 255 1 0 0 0 3 0 88 8 65 89 67 7 577 88 23 65 89 7 44	
target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_u16  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_I1ETailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_u08  DigColPsInt_RecvOverrunError_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR	0 Actual Value 9 28 56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 3 0 88 8 8 65 89 67 7 577 88 23 65 89 7 44 2	9 28 56 100 0 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 0 3 0 88 8 65 89 67 7 7 577 88 23 65 89 7 44 2	
target_i2cREG1_temp.PSL.  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_u16  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.NR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR	0 Actual Value 9 28 56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 0 3 0 88 8 8 65 89 67 7 577 88 23 65 89 7 44 2 89 577	9 28 56 100 0 0 0 17 7 60 INIT_COMPLETE 255 255 1 0 0 3 0 88 8 65 89 67 7 577 88 23 65 89 7 44 2 89 577	
target_i2cREG1_temp.PSL.  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_u16  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_I2cHwCustData_UIs_M_u16  DigColPsInt_I1itFailedOnce_Cnt_M_lgc  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_u08  DigColPsInt_RecvOverrunError_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	0 Actual Value 9 28 56 100 0 0 17 7 60 INIT_COMPLETE 255 255 1 0 0 0 3 0 88 8 65 89 67 7 577 88 23 65 89 7 44 2 89 577 89	9 28 56 100 0 0 0 11 7 60 INIT_COMPLETE 255 255 1 0 0 3 0 88 8 65 89 67 7 577 88 23 65 89 7 44 2 89 577 89	
target_i2cREG1_temp.PSL.  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_u16  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.NR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR	0 Actual Value 9 28 56 100 0 0 1 7 60 INIT_COMPLETE 255 255 1 0 0 0 3 0 88 8 8 65 89 67 7 577 88 23 65 89 7 44 2 89 577	9 28 56 100 0 0 0 17 7 60 INIT_COMPLETE 255 255 1 0 0 3 0 88 8 65 89 67 7 577 88 23 65 89 7 44 2 89 577	

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	65	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	89	89	<b>V</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7	7 577	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577 88	88	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	23	23	~
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.SAR	65	65	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DXR	89	89	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7	7	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.IVR	44	44	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	_
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSC	89	89	•
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	577	577	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	<b>V</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	<b>V</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	577	577	-4
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	88	88	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	23 65	23 65	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	00	00	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	7	7	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	

T			<b>✓</b>		
Actual Function	Count	Expected Function	Count	Resu	lt
*none*	0	*** No Call Expected ***	0		_

est Step 2.33 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	10
DigColPsInt_Buffer_Cnt_M_u08[0]	123

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DigColPSIIIL_InterruptiNotification	(WAC)
Name	Input Value
igColPsInt_Buffer_Cnt_M_u08[1]	145
igColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
igColPsInt_CmdFailOccurred_Cnt_M_lgc	1
igColPsInt_ColCustDatFound_Cnt_M_lgc	0
igColPsInt_ColSnsrData_Cnt_M_u16	554
igColPsInt_CurrentSlave_Cnt_M_u08	70
igColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADDATREG_READ
igColPsInt_I2CHwCustData_Uls_M_u16	97
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	147
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0
higColPsInt_NackOccured_Cnt_M_lgc	1
ligColPsInt_PrevReqDataType_Cnt_M_u08	1
igColPsInt_RecvOverrunError_Cnt_M_lgc	1
igColPsInt_RecvdDataType_Cnt_M_u08	4
igColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
igColPsInt_SpurCustDatFound_Cnt_M_lgc	1
igColPsInt_SpurSnsrData_Cnt_M_u16	123
igColPsInt_TransactionCnt_Cnt_M_u08	0
ags_Cnt_T_b16	32
Cc_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
_DataRegisters_Cnt_u08[0]	0
DataRegisters Cnt u08[1]	32
_DataRegisters_Cnt_u08[2]	30
_DataRegisters_Cnt_u08[3]	36
_DataRegisters_Cnt_u08[4]	38
_DataRegisters_Cnt_u08[5]	34
_DataRegisters_Cnt_u08[6]	10
DataRegisters_Cnt_u08[7]	12
DataRegisters_Cnt_u08[8]	14
2cREG1_temp	target_i2cREG1_temp
_ColSensorI2CAddress_Cnt_u08	35
_SpurSensorI2CAddress_Cnt_u08	20
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54
	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123
irget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	54
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
rrget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
rrget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
rrget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1.
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2
rget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54
rget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
urget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8
rget_I2c_send_I2cRegPtr_Cnt_T_str.CLKL	554
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344
arget_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	123
ngot_izo_ochiq_izortogi il_Olit_i_sii.Olit i	45
rget 12c Send 12cRegPtr Cnt T str DRR	170
arget_l2c_Send_l2cRegPtr_Cnt_T_str.DRR arget_l2c_Send_l2cRegPtr_Cnt_T_str.SAR arget_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	54 66

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Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788
target I2c Send I2cRegPtr Cnt T str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target I2c SetStatus I2cRegPtr Cnt T str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3
	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	3 3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54

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DigColPsInt\_InterruptNotification

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Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.MDR	554		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66		
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	344		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	344		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	123		
	45		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54 66		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR			
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	554		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2		
target_i2cREG1_temp.OAR	54		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	8		
target i2cREG1 temp.CLKL	554		
target_i2cREG1_temp.CLKH	344		
target i2cREG1 temp.CNT	123		
target i2cREG1 temp.DRR	45		
target i2cREG1 temp.SAR	54		
target i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	554		
	788		
target_i2cREG1_temp.IVR			
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	344		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	3		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	3		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	2		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	10	10	~
DigColPsInt_Buffer_Cnt_M_u08[0]	123	123	<b>V</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	_
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	<b>~</b>
D: 0 ID 1 1 D D 0 5 0 1 M 1	4	4	

DigColPsInt\_BusBusySeqError\_Cnt\_M\_lgc

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Name	Actual Value	Expected Value	Resu
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	
DigColPsInt_ColSnsrData_Cnt_M_u16	554	554	
DigColPsInt_CurrentSlave_Cnt_M_u08	70	70	•
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE	INIT_COMPLETE	
DigColPsInt_I2CHwCustData_Uls_M_u16	147	147	
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	0	0	
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	
DigColPsInt_RecvOverrunError_Cnt_M_lgc	4	4	
DigColPsInt_RecvdDataType_Cnt_M_u08	1	1	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	123	123	
DigColPsInt_SpurSnsrData_Cnt_M_u16	0	0	
DigColPsInt_TransactionCnt_Cnt_M_u08 arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54	54	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR	8	8	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554	554	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH	344	344	
rarget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT	123	123	
rarget_12c_GenStopCond_12cRegPtr_Cnt_1_str.CN1	45	45	
target_l2c_GenStopCond_l2cRegPtr_Cnt_1_str.DRR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR	54	54	
target_12c_GenStopCond_12cRegPtr_Cnt_1_str.SAR target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR	66	66	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DAR	554	554	
target I2c GenStopCond I2cRegPtr Cnt T str.IVR	788	788	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FWR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_l2c_GenStopCond_l2cRegPtr_Cnt_1_str.ENIDK	66	66	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11	344	344	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12	66	66	
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.Pib12	3	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	
rarget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR	3	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	
rarget_12c_GenStopCond_12cRegPtr_Cnt_T_str.D0UT	3	3	
arget_12c_GenStopCond_12cRegPtr_Cnt_T_str.SET	3	3	
rarget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR	3	3	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR	2	2	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD	1	1	
rarget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	2	2	
arget I2c Send I2cRegPtr Cnt T str.OAR	54	54	
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	66	66	
target I2c Send I2cRegPtr Cnt T str.STR	8	8	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554	554	
target I2c Send I2cRegPtr Cnt T str.CLKH	344	344	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	123	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	45	
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	54	54	
target_12c_Send_12cRegPtr_Cnt_T_str.DXR	66	66	
target I2c Send I2cRegPtr Cnt T str.MDR	554	554	
target_12c_Send_12cRegPtr_Cnt_T_str.IVR	788	788	
target I2c Send I2cRegPtr Cnt T str.EMDR	3	3	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	344	344	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	66	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.D0UT	3	3	
target_12c_Send_12cRegPtr_Cnt_T_str.SET	3	3	
arget_12c_Send_12cRegPtr_Cnt_1_str.SE1 arget_12c_Send_12cRegPtr_Cnt_T_str.CLR	3	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54	54	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_1_str.lmR arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8	8	
	554	554	
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	344	344	
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	123	123	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	45	45	
	4:1	40	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54	54	

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554	554	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788	788	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	3 66	3 66	
target I2c SetRecv I2cRegPtr Cnt T str.PID11	344	344	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>V</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	3	3	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	3 2	3 2	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54	54	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8	8	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554	554	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH	344	344	<b>V</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	123	123	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45 54	45 54	<i>y</i>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	
target I2c SetStatus I2cRegPtr Cnt T str.MDR	554	554	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	788	788	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344	344	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>v</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	1	1	<i>y</i>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3 2	3 2	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	3	3	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54	54	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	8 554	8 554	
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLKH	344	344	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CNT	123	123	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45	45	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54	54	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554	554	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788	788	•
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11 target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	344 66	344 66	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	2	2	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	· ·
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	2	2 54	· · · · · · · · · · · · · · · · · · ·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	54 66	54 66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8	8	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	554	554	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344	344	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123	123	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45	45	<b>✓</b>

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54	54	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554	554	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788	788	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344	344	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	~

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Sept   December   De		
The property of the property o	Name	Input Value
Bayer, P.P.   Gendeligotinal (Scrippin) Colif   Text POR	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
Barger   12. Genfellspründ   Scheight Coll   1 m/SSA	target I2c GenStopCond I2cRegPtr Cnt T str.DRR	67
Long   12, Confession   Engine   Conf   En MOR		55
Barget 120, Constitutional Distriction Conf.   1 m MINR		
bags 12, Genésophore (2016pp) Cot   T. B. F. M. S.		
Image_IR_C_ROWSEQUENT_DRIVER_COT_LET_ENDOT   104   Image_IR_C_ROWSEQUENT_DRIVER_COT_LET_ENDOT    104   Image_IR_C_ROWSEQUENT_DRIVER_COT_LET_ENDOT    104   Image_IR_C_ROWSEQUENT_DRIVER_COT_LET_ENDOT    105   Image_IR_C_ROWSEQUENT_COT_LET_ENDOT    105		
Hanger, Die, Gereichberger, Der Ferner, Der Price 1  Hanger, Die, Gereichberger, Der Ferner, Der Price 1  Hanger, Die, Gereichberger, Der Ferner, Der Price 1  Hanger, Die, Gereichberger, Der Ferner, Der Ferner, Der Price 1  Hanger, Die, Gereichberger, Der Ferner, Der Ferner, Der Price 1  Hanger, Die, Gereichberg, Der Ferner, Der Ferner, Der Price 1  Hanger, Die, Gereichberg, Der Ferner, Der Ferner, Der Price 1  Hanger, Die, Gereichberg, Der Ferner, Der Ferner, Der Price 1  Hanger, Die, Gereichberg, Der Ferner, Der Ferner, Der Price 1  Hanger, Die, Gereichberg, Der Ferner, Der Ferner, Der Price 1  Hanger, Die, Gereichberg, Der Ferner, Der Ferner, Der Price 1  Hanger, Die, Gereichberg, Der Ferner, Der Ferner, Der Price 1  Hanger, Die, Gereichberg, Der Ferner, Der Ferner, Der Price 1  Hanger, Die, Gereichberg, Der Ferner, Der Ferner, Der Price 1  Hanger, Die, Gereichberg, Der Ferner, Der Ferner, Der Price 1  Hanger, Die, Gereichberg, Der Ferner, Der Ferne		
Image:   Dec.   Ger-Shepford   Zelegaph Cont.   1 st   1 price	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
taggs   Dec   Contribution of   25 contribution   25 contribution	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
Bargal Pick, Ser-Septonul (248)-pipe Cont.   1 ser DNA	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
Bargal Pick, Ser-Septonul (248)-pipe Cont.   1 ser DNA	target I2c GenStopCond I2cRegPtr Cnt T str.PID12	66
Langer, D.C. emblogorous (Designing-Cut_starDNR)  Langer, D.C. emblogorous (Designing-Cut_starDN		3
Langer   12. GenStoot Cont   2016/Plp   Cont   1. str 2018		
Langer I.D. GewiSchool I. Zelegin C. I. Far DNI  langer I.D. GewiSchool I. Zelegin C. I. Far DNI  langer I.D. GewiSchool I. Zelegin C. I. Far DNI  langer I.D. GewiSchool I. Zelegin C. I. Far DNI  langer I.D. GewiSchool I. Zelegin C. I. Far DNI  langer I.D. GewiSchool I. Zelegin C. I. Far DNI  langer I.D. GewiSchool I. Zelegin C. I. Far DNI  langer I.D. GewiSchool I. Zelegin C. I. Far DNI  langer I.D. GewiSchool I. Zelegin C. I. Far DNI  langer I.D. GewiSchool I. Zelegin C. I. Far DNI  langer I.D. GewiSchool I. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  langer I.D. Send J. Zelegin C. I. Far DNI  la		
Larget ID. Centhologomou, Exclusive Cut T, set STT 3  Larget ID. Centhologomou, Exclusive Cut T, set STT 3  Larget ID. Centhologomou, Exclusive Cut T, set STT 3  Larget ID. Centhologomou, Exclusive Cut T, set STR 3  Larget ID. Centhologomou, Exclusive Cut T, set STR 3  Larget ID. Centhologomou, Exclusive Cut T, set STR 3  Larget ID. Centhologomou, Exclusive Cut T, set STR 3  Larget ID. Centhologomou, Exclusive Cut T, set STR 3  Larget ID. Centhologomou, Exclusive Cut T, set STR 3  Larget ID. Centhologomou, Exclusive Cut T, set STR 3  Larget ID. Centhologomou, Exclusive Cut T, set STR 3  Larget ID. Centhologomou, Centhologomou, Cut T, set STR 3  Larget ID. Centhologomou, Centhologomou, Cut T, set STR 3  Larget ID. Centhologomou, Centhologomou, Cut T, set STR 3  Larget ID. Centhologomou, Cut T, set STR 3		
target I.P.C. constantOrom_Delegin_Cont_Tart SET  target I.P.C. constantOrom_Delegin_Cont_Tart CAR  target I.P.C. send_Delegin_Cont_Tart CAR  target I.P.C. se		
Image Lies, Centrologonian, Deckapin Cont.   1 str. DRIS		
Larger I.D.C. densityDochus (Darkepin Cont. T. art.DDR 1 targer I.D.C. densityDochus (Darkepin Cont. T. art.DDR 1 targer I.D.C. densityDochus (Darkepin Cont. T. art.DDR 1 targer I.D.C. send (Darkepin Cont. T. art.DDR 1 tar	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET	
Image   12.6. Send   2.6 Region   Cot   1 str PD	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
Integral   Dec. Commission Control   Commission Commission Control   Commission Commission Control   Commission	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
Integral Loss -   Proceedings -   Process -   Process -	target I2c GenStopCond I2cRegPtr Cnt T str.PD	3
Sept   1.2. Send		3
timput (L.S. Sand (L.Skapin*)* Cot. T. art INES ITS         558           timput (L.S. Sand (L.Skapin*)* Cot. T. art CLUL         2000           timput (L.S. Sand (L.Skapin*)* Cot. T. art CLUL         2000           timput (L.S. Sand (L.Skapin*)* Cot. T. art CLUT         87           timput (L.S. Sand (L.Skapin*)* Cot. T. art CLUT         87           timput (L.S. Sand (L.Skapin*)* Cot. T. art CLUT         87           timput (L.S. Sand (L.Skapin*)* Cot. T. art CLUT         87           timput (L.S. Sand (L.Skapin*)* Cot. T. art CLUT         88           timput (L.S. Sand (L.Skapin*)* Cot. T. art CLUT         86           timput (L.S. Sand (L.Skapin*)* Cot. T. art CLUT         85           timput (L.S. Sand (L.Skapin*)* Cot. T. art CLUT         86           timput (L.S. Sand (L.Skapin*)* Cot. T. art DIM         5           timput (L.S. Sand (L.Skapin*)* Cot. T. art DIM         6           timput (L.S. Sand (L.Skapin*)* Cot. T. art DIM         1           timput (L.S. Sand (L.Skapin*)* Cot. T. art DIM         1           timput (L.S. Sand (L.Skapin*)* Cot. T. art DIM         1           timput (L.S. Sand (L.Skapin*)* Cot. T. art DIM         1           timput (L.S. Sand (L.Skapin*)* Cot. T. art DIM         2           timput (L.S. Sand (L.Skapin*)* Cot. T. art DIM         2           timput (L.S. Sand (L.Skapin*)* Cot. T. art DIM		
Integral Los, Send Lickepth Cot   T. at STR   556		
Large LE Send LeReight Cont_Tat CLINL  1200  Hange LES Send LeReight Cont_Tat CLIN  1370  Hange LES Send LeReight Cont_Tat CDR  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370  1370		
Image Lize Send LizeRegiff Cost T air CLUCH   Image Lize Send LizeRegiff Cost T air DNR   97		
target, R.S., Send, Lickephr, Cott., T., str. DNR target, R.S., Sendre, Lickephr, Cott.,	target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	
Integral Loo. Send   DeRepPir Cont   T. INS DRR   57	target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
Image L.P. Send LORR-PyP. CNT_SENDER   Send LORR-PyP. CN	target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_De_Send_LicRespPL_CH_T_str_DNR         55           target_De_Send_LicRespPL_CH_T_str_DNR         66           target_De_Send_LicRespPL_CH_T_str_NMR         2309           target_De_Send_LicRespPL_CH_T_str_NMR         5           target_De_Send_LicRespPL_CH_T_str_NMR         3           target_De_Send_LicRespPL_CH_T_str_NMR         3           target_De_Send_LicRespPL_CH_T_str_NDD         1204           target_De_Send_LicRespPL_CH_T_str_NDD         1204           target_De_Send_LicRespPL_CH_T_str_NDD         3           target_De_Send_LicRespPL_CH_T_str_NDD         1           target_De_Send_LicRespPL_CH_T_str_NDD         1           target_De_Send_LicRespPL_CH_T_str_NDD         1           target_De_Send_LicRespPL_CH_T_str_NDD         1           target_De_Send_LicRespPL_CH_T_str_NDD         1           target_De_Send_LicRespPL_CH_T_str_NDD         3           target_De_Send_LicRespPL_CH_T_str_NDD         3           target_De_Send_LicRespPL_CH_T_str_NDD         3           target_De_Send_LicRespPL_CH_T_str_NDD         3           target_De_Send_LicRespPL_CH_T_str_NDD         3           target_De_Send_LicRespPL_CH_T_str_NDD         3           target_De_Send_LicRespPL_CH_T_str_NDB         3           target_De_Send_LicRespPL_CH_T_str_NDB         3 <td></td> <td>67</td>		67
Barget Lab Send   Jacksephr Cot T_str NDR		
target 122. Send 12cRegPT_Cnt_T str MDR		
staget_12b_ Send_12cRegPt_Cnt_T_str.PRD         5           target_12b_ Send_12cRegPt_Cnt_T_str.PSC         66           target_12b_ Send_12cRegPt_Cnt_T_str.PSC         66           target_12b_ Send_12cRegPt_Cnt_T_str.PSC         66           target_12b_ Send_12cRegPt_Cnt_T_str.PDI11         1204           target_12b_ Send_12cRegPt_Cnt_T_str.DNAC         3           target_12b_ Send_12cRegPt_Cnt_T_str.DNAC         3           target_12b_ Send_12cRegPt_Cnt_T_str.DN         1           target_12b_ Send_12cRegPt_Cnt_T_str.DN         1           target_12b_ Send_12cRegPt_Cnt_T_str.DNT         2           target_12b_ Send_12cRegPt_Cnt_T_str.DNT         3           target_12b_ Send_12cRegPt_Cnt_T_str.DNT         3           target_12b_ Send_12cRegPt_Cnt_T_str.DNT         1           target_12b_ Send_12cRegPt_Cnt_T_str.DNT         3           target_12b_ Send_12cRegPt_Cnt_T_str.DNT         1           target_12b_ Send_12cRegPt_Cnt_T_str.DNT         3           target_12b_ Send_12cRegPt_Cnt_T_str.DNT         3           target_12b_ Send_12cRegPt_Cnt_T_str.DNT         3           target_12b_ Send_12cRegPt_Cnt_T_str.DNT         4           target_12b_ Send_12cRegPt_Cnt_T_str.DNT         5           target_12b_ Send_12cRegPt_Cnt_T_str.DNT         5           target_12b_ Send_12c		
target_12e_Send_12cRegPT_Cnt_T_str_ENC         86           target_12e_Send_12cRegPT_Cnt_T_str_PDC         86           target_12e_Send_12cRegPT_Cnt_T_str_PD11         1204           target_12e_Send_12cRegPT_Cnt_T_str_PD12         66           target_12e_Send_12cRegPT_Cnt_T_str_PD12         66           target_12e_Send_12cRegPT_Cnt_T_str_DtmAC         3           target_12e_Send_12cRegPT_Cnt_T_str_DtmAC         1           target_12e_Send_12cRegPT_Cnt_T_str_DtmAC         1           target_12e_Send_12cRegPT_Cnt_T_str_DtmAC         3           target_12e_Send_12cRegPT_Cnt_T_str_DtmAC         3           target_12e_Send_12cRegPT_Cnt_T_str_DtmAC         3           target_12e_Send_12cRegPT_Cnt_T_str_DtmAC         3           target_12e_Send_12cRegPT_Cnt_T_str_DtmAC         1           target_12e_Send_12cRegPT_Cnt_T_str_DtmAC         2           target_12e_Send_12cRegPT_Cnt_T_str_DtmAC         2           target_12e_Send_12cRegPT_Cnt_T_str_DtmAC         3           target_12e_Send_12cRegPT_Cnt_T_str_DtmAC         55           target_12e_Send_12cRegPT_Cnt_T_str_DtmAC         55           target_12e_Send_12cRegPT_Cnt_T_str_DtmAC         2009           target_12e_Send_12cRegPT_Cnt_T_str_DtmAC         2009           target_12e_Send_12cRegPT_Cnt_T_str_DtmAC         3 <td< td=""><td></td><td></td></td<>		
target 12c. Send 12cRepPtr Cnt_Tst PID11         1224           target 12c. Send 12cRepPtr Cnt_Tst PID11         1224           target 12c. Send 12cRepPtr Cnt_Tst PID12         68           target 12c. Send 12cRepPtr Cnt_Tst PID12         68           target 12c. Send 12cRepPtr Cnt_Tst PID18         1           target 12c. Send 12cRepPtr Cnt_Tst PID18         1           target 12c. Send 12cRepPtr Cnt_Tst DIN         2           target 12c. Send 12cRepPtr Cnt_Tst DIN         2           target 12c. Send 12cRepPtr Cnt_Tst DIN         3           target 12c. Send 12cRepPtr Cnt_Tst DIN         3           target 12c. Send 12cRepPtr Cnt_Tst DIN         2           target 12c. Send 12cRepPtr Cnt_Tst DIN         3           target 12c. Send 12cRepPtr Cnt_Tst DIN         3           target 12c. Send 12cRepPtr Cnt_Tst DIN         3           target 12c. Send 2cRepPtr Cnt_Tst DIN         3           target 12c. Send 2cRepPtr Cnt_Tst DIN         5           target 12c. Send 2cRepPtr Cnt_Tst DIN         6           target 12c. Send 2crepPtr Cnt_Tst DI		
target 12c. Send (2cRepPtr_Cnt_T str PID11 arget 12c. Send (2cRepPtr_Cnt_T str PID12 bright 12c. Send (2cRepPtr_Cnt_T str DIMAC arget 12c. Send (2cRepPtr_Cnt_T str DIMAC arget 12c. Send (2cRepPtr_Cnt_T str DIMAC bright 12c. Send (2cRepPtr_C	target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
Images   Jac   Send   Jacksepht Cnt_I str PIDI2   65	target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_12c_Send_12cRegPtr_Cnt_1_str.DNAC  target_12c_Send_12cRegPtr_Cnt_1_str.DN  target_12c_Send_12cRegPtr_Cnt_1_str.DN  target_12c_Send_12cRegPtr_Cnt_1_str.DN  target_12c_Send_12cRegPtr_Cnt_1_str.DN  target_12c_Send_12cRegPtr_Cnt_1_str.DN  target_12c_Send_12cRegPtr_Cnt_1_str.DLT  target_12c_Send_12cRegPtr_Cnt_1_str.DLT  target_12c_Send_12cRegPtr_Cnt_1_str.DLR  target_12c_Sendev_12cRegPtr_Cnt_1_str.DLR  target_12c_Sendev_12cR	target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target J2c, Send J2cRepPtr_Cnt_Tstr.DNAC  target J2c, Send J2cRepPtr_Cnt_Tstr.DN  target J2c, Send J2cRepPtr_Cnt_Tstr.DCT	target I2c Send I2cRegPtr Cnt T str.PID12	66
target   Ze, Send   ZeRegPtr Cnt_T str.FUN   1   target   Ze, Send   ZeRegPtr Cnt_T str.DIR   1   target   Ze, Send   ZeRegPtr Cnt_T str.DIR   2   target   Ze, Send   ZeRegPtr Cnt_T str.DUT   3   target   Ze, Send   ZeRegPtr Cnt_T str.DUT   3   target   Ze, Send   ZeRegPtr Cnt_T str.DUT   3   target   Ze, Send   ZeRegPtr Cnt_T str.DUR   2   target   Ze, Send   ZeRegPtr Cnt_T str.DUR   3   target   Ze, Send   ZeRegPtr Cnt_T str.DUR   3   target   Ze, Send   ZeRegPtr Cnt_T str.DUR   5   target   Ze, Send   ZeRegPtr Cnt_T str.DUR   6   target   Ze, Send   ZeRegPtr Cnt_T str.DUR   6   target   Ze, Send   ZeRegPtr Cnt_T str.DUR   7   target   Ze, Send   ZeRegPtr Cnt_T str.DUR   6   target   Ze, Send   ZeRegPtr Cnt_T str.DUN   1   target   Ze, Send   ZeRegPtr Cnt_T str.DUN   2   target   Ze, Send   ZeRegPtr Cnt_T str.DUN   3   target   Ze, Send   ZeRegPtr Cnt_T		
target_12c_Send_12cRegPtr_Cnt_T_str.DIR		
target_12c_Send_12cRegPtr_Cnt_T_str.DUT  arget_12c_Send_12cRegPtr_Cnt_T_str.DUT  arget_12c_Send_12cRegPtr_Cnt_T_str.SET  arget_12c_Send_12cRegPtr_Cnt_T_str.CLR  arget_12c_Send_12cRegPtr_Cnt_T_str.CLR  arget_12c_Send_12cRegPtr_Cnt_T_str.DUR  arget_12c_Send_12cRegPtr_Cnt_T_str.DUR  arget_12c_Send_12cRegPtr_Cnt_T_str.DUR  arget_12c_Send_12cRegPtr_Cnt_T_str.DUR  arget_12c_Send_12cRegPtr_Cnt_T_str.DUR  arget_12c_Send_12cRegPtr_Cnt_T_str.DUR  arget_12c_SenRecv_12cRegPtr_Cnt_T_str.DUR  arget_12c_SenR		
target_12c_Send_12cRegPtr_Cnt_Tstr.DUT  arget_12c_Send_12cRegPtr_Cnt_Tstr.SET  arget_12c_Send_12cRegPtr_Cnt_Tstr.CDR  target_12c_Send_12cRegPtr_Cnt_Tstr.DOR  2 target_12c_Send_12cRegPtr_Cnt_Tstr.DOR  arget_12c_Send_12cRegPtr_Cnt_Tstr.DD  arget_12c_Send_12cRegPtr_Cnt_Tstr.DD  arget_12c_Send_12cRegPtr_Cnt_Tstr.DD  arget_12c_Send_12cRegPtr_Cnt_Tstr.DD  arget_12c_SetRecv_12cRegPtr_Cnt_Tstr.DAR  55  target_12c_SetRecv_12cRegPtr_Cnt_Tstr.DAR  66  target_12c_SetRecv_12cRegPtr_Cnt_Tstr.CLK  arget_12c_SetRecv_12cRegPtr_Cnt_Tstr.CLK  arget_12c_SetRecv_12cRegPtr_Cnt_Tstr.CLK  target_12c_SetRecv_12cRegPtr_Cnt_Tstr.CLK  target_12c_SetRecv_12cRegPtr_Cnt_Tstr.CLK  target_12c_SetRecv_12cRegPtr_Cnt_Tstr.DAR  67  target_12c_SetRecv_12cRegPtr_Cnt_Tstr.DAR  67  target_12c_SetRecv_12cRegPtr_Cnt_Tstr.DAR  arget_12c_SetRecv_12cRegPtr_Cnt_Tstr.DAR  55  target_12c_SetRecv_12cRegPtr_Cnt_Tstr.DAR  56  target_12c_SetRecv_12cRegPtr_Cnt_Tstr.DAR  57  target_12c_SetRecv_12cRegPtr_Cnt_Tstr.DAR  58  target_12c_SetRecv_12cRegPtr_Cnt_Tstr.DAR  59  target_12c_SetRecv_12cRegPtr_Cnt_Tstr.DAR  50  target_12c_SetRecv_12cRegPtr_Cnt_Tstr.DAR  50  target_12c_SetRecv_12cRegPtr_Cnt_Tstr.DAR  51  target_12c_SetRecv_12cRegPtr_Cnt_Tstr.DAR  52  target_12c_SetRecv_12cRegPtr_Cnt_Tstr.DAR  51  target_12c_SetRecv_12cRegPtr_Cnt_Tstr.DAR  52  target_12c_SetRecv_12cRegPtr_Cnt_Tstr.DAR  53  target_12c_SetRecv_12cRegPtr_Cnt_Tstr.DAR  54  target_12c_SetRecv_12cRegPtr_Cnt_Tstr.DAR  55  target_12c_SetRecv_12cRegPtr_Cnt_Tstr.DAR  56  target_12c_SetRecv_12cRegPtr_Cnt_Tstr.DAR  57  target_12c_SetRecv_12cRegPtr_Cnt_Tstr.DAR  58  target_12c_SetRecv_12cRegPtr_Cnt_Tstr.DAR  59  target_12c_SetRecv_12cRegPtr_Cnt_Tstr.DAR  50  target_12c_SetRecv_12cRegPtr_Cnt_Tstr.DAR  51  target_12c_SetRecv_12cRegPtr_Cnt_Tstr.DAR  52  target_12c_SetRecv_12cRegPtr_Cnt_Tstr.DAR  53  target_12c_SetRecv_12cRegPtr_Cnt_Tstr.DAR  54  target_12c_SetRecv_12cRegPtr_Cnt_Tstr.DAR  55  target_12c_SetRecv_12cRegPtr_Cnt_Tstr.DAR  56  57  target_12c_SetRecv_12cRegPtr_Cnt_Tstr.DAR  57  target_12c_SetRecv_12cRegP		
target_12c_Send_12cRegPtr_Cnt_Tstr.CtR		
target_12c_Send_12cRegPtr_Cnt_T_str.ORR 2 target_12c_Send_12cRegPtr_Cnt_T_str.ORR 2 target_12c_Send_12cRegPtr_Cnt_T_str.PD 3 target_12c_Send_12cRegPtr_Cnt_T_str.PD 3 target_12c_Send_12cRegPtr_Cnt_T_str.PSL 3 target_12c_SentRecv_12cRegPtr_Cnt_T_str.ORR 55 target_12c_SentRecv_12cRegPtr_Cnt_T_str.DRR 66 target_12c_SentRecv_12cRegPtr_Cnt_T_str.STR 556 target_12c_SentRecv_12cRegPtr_Cnt_T_str.CtkL 2309 target_12c_SentRecv_12cRegPtr_Cnt_T_str.CtkL 2309 target_12c_SentRecv_12cRegPtr_Cnt_T_str.CtkL 2309 target_12c_SentRecv_12cRegPtr_Cnt_T_str.CtkL 2309 target_12c_SentRecv_12cRegPtr_Cnt_T_str.DRR 67 target_12c_SentRecv_12cRegPtr_Cnt_T_str.DRR 67 target_12c_SentRecv_12cRegPtr_Cnt_T_str.DRR 67 target_12c_SentRecv_12cRegPtr_Cnt_T_str.DRR 66 target_12c_SentRecv_12cRegPtr_Cnt_T_str.DRR 2309 target_12c_SentRecv_12cRegPtr_Cnt_T_str.DRR 2309 target_12c_SentRecv_12cRegPtr_Cnt_T_str.DRR 2309 target_12c_SentRecv_12cRegPtr_Cnt_T_str.DRR 3 target_12c_SentRecv_12cRegPtr_Cnt_T_str.DRR 1 target_12c_SentRecv_12cRegPtr_Cnt_T_str.DRR 2 target_12c_SentRecv_12cRegPtr_Cnt_T_str.DRR 3 target_12c_SentRecv_12cRegPtr_Cnt_T_str.DRR 3 target_12c_SentRecv_12cRegPtr_Cnt_T_str.DRR 5 target_12c_SentRecv_12cRegPtr_Cnt_T_str.DRR 5 target_12c_SentRecv_12cRegPtr_Cnt_T_str.DRR 5 target_12c_SentRecv_12cRegPtr_Cnt_T_str.DRR 5 target_12c_		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DDR         2           target_I2c_Send_I2cRegPtr_Cnt_T_str.PD         3           target_I2c_Send_I2cRegPtr_Cnt_T_str.DAR         5           target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR         55           target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR         66           target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR         66           target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL         2309           target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL         1204           target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT         87           target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR         67           target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR         67           target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR         66           target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR         66           target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR         55           target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR         66           target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR         5           target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR         5           target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR         5           target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DDR         3           target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DINA         3           target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DUN	target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_!2c_Send_!2cRegPtr_Cnt_T_str.PD         3           target_!2c_Send_!2cRegPtr_Cnt_T_str.PSL         3           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR         55           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR         66           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.Str.R         556           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKL         2309           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKL         1204           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CNT         87           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR         67           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR         67           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR         66           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.MDR         2309           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.MDR         3           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.MDR         30           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PDT         1           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PDT         1           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DMAC         3           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DM         1           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DM         1           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DM         2           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DOM	target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_!2c_Senfecv_!2cRegPtr_Cnt_T_str.DAR         55           target_!2c_Senfecv_!2cRegPtr_Cnt_T_str.DAR         55           target_!2c_Senfecv_!2cRegPtr_Cnt_T_str.BMR         66           target_!2c_Senfecv_!2cRegPtr_Cnt_T_str.BTR         556           target_!2c_Senfecv_!2cRegPtr_Cnt_T_str.CLKL         2309           target_!2c_Senfecv_!2cRegPtr_Cnt_T_str.CLKH         1204           target_!2c_Senfecv_!2cRegPtr_Cnt_T_str.DAR         67           target_!2c_Senfecv_!2cRegPtr_Cnt_T_str.DAR         67           target_!2c_Senfecv_!2cRegPtr_Cnt_T_str.DAR         55           target_!2c_Senfecv_!2cRegPtr_Cnt_T_str.DAR         66           target_!2c_Senfecv_!2cRegPtr_Cnt_T_str.DAR         66           target_!2c_Senfecv_!2cRegPtr_Cnt_T_str.DAR         5           target_!2c_Senfecv_!2cRegPtr_Cnt_T_str.DAR         5           target_!2c_Senfecv_!2cRegPtr_Cnt_T_str.DAR         66           target_!2c_Senfecv_!2cRegPtr_Cnt_T_str.DAR         3           target_!2c_Senfecv_!2cRegPtr_Cnt_T_str.DAR         3           target_!2c_Senfecv_!2cRegPtr_Cnt_T_str.DAR         3           target_!2c_Senfecv_!2cRegPtr_Cnt_T_str.DIA         1           target_!2c_Senfecv_!2cRegPtr_Cnt_T_str.DIA         1           target_!2c_Senfecv_!2cRegPtr_Cnt_T_str.DUT         3           target_!2c_Senfecv_!2cRegPtr_Cnt_T_str.DUT </td <td>target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR</td> <td>2</td>	target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL         3           target_I2c_SenRecv_I2cRegPtr_Cnt_T_str.DAR         55           target_I2c_SenRecv_I2cRegPtr_Cnt_T_str.MR         66           target_I2c_SenRecv_I2cRegPtr_Cnt_T_str.STR         556           target_I2c_SenRecv_I2cRegPtr_Cnt_T_str.CLKL         2309           target_I2c_SenRecv_I2cRegPtr_Cnt_T_str.CLKH         1204           target_I2c_SenRecv_I2cRegPtr_Cnt_T_str.CNT         87           target_I2c_SenRecv_I2cRegPtr_Cnt_T_str.DAR         67           target_I2c_SenRecv_I2cRegPtr_Cnt_T_str.SAR         55           target_I2c_SenRecv_I2cRegPtr_Cnt_T_str.DAR         66           target_I2c_SenRecv_I2cRegPtr_Cnt_T_str.NDR         2309           target_I2c_SenRecv_I2cRegPtr_Cnt_T_str.NDR         5           target_I2c_SenRecv_I2cRegPtr_Cnt_T_str.ENDR         3           target_I2c_SenRecv_I2cRegPtr_Cnt_T_str.ENDR         3           target_I2c_SenRecv_I2cRegPtr_Cnt_T_str.PDD         66           target_I2c_SenRecv_I2cRegPtr_Cnt_T_str.PDD         3           target_I2c_SenRecv_I2cRegPtr_Cnt_T_str.DIN         1           target_I2c_SenRecv_I2cRegPtr_Cnt_T_str.DIN         2           target_I2c_SenRecv_I2cRegPtr_Cnt_T_str.DOUT         3           target_I2c_SenRecv_I2cRegPtr_Cnt_T_str.DOUT         3           target_I2c_SenRecv_I2cRegPtr_Cnt_T_str.DOUT	target I2c Send I2cRegPtr Cnt T str.PD	3
target_I2c_SelReov_I2cRegPtr_Cnt_T_str.DAR         55           target_I2c_SelReov_I2cRegPtr_Cnt_T_str.IMR         66           target_I2c_SelReov_I2cRegPtr_Cnt_T_str.STR         556           target_I2c_SelReov_I2cRegPtr_Cnt_T_str.CLKL         2309           target_I2c_SelReov_I2cRegPtr_Cnt_T_str.CNT         87           target_I2c_SelReov_I2cRegPtr_Cnt_T_str.DRR         67           target_I2c_SelReov_I2cRegPtr_Cnt_T_str.DRR         67           target_I2c_SelReov_I2cRegPtr_Cnt_T_str.DXR         66           target_I2c_SelReov_I2cRegPtr_Cnt_T_str.DXR         66           target_I2c_SelReov_I2cRegPtr_Cnt_T_str.DXR         5           target_I2c_SelReov_I2cRegPtr_Cnt_T_str.DNR         3           target_I2c_SelReov_I2cRegPtr_Cnt_T_str.ENDR         3           target_I2c_SelReov_I2cRegPtr_Cnt_T_str.PSC         66           target_I2c_SelReov_I2cRegPtr_Cnt_T_str.DD11         1204           target_I2c_SelReov_I2cRegPtr_Cnt_T_str.DMAC         3           target_I2c_SelReov_I2cRegPtr_Cnt_T_str.DMAC         3           target_I2c_SelReov_I2cRegPtr_Cnt_T_str.DIN         1           target_I2c_SelReov_I2cRegPtr_Cnt_T_str.DIN         2           target_I2c_SelReov_I2cRegPtr_Cnt_T_str.DOUT         3           target_I2c_SelReov_I2cRegPtr_Cnt_T_str.ON         2           target_I2c_SelReov_I2cRegPtr_Cnt_T_str.ON<		3
target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.STR         66           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.STR         556           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKL         2309           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKH         1204           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CNT         87           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR         67           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR         65           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR         66           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR         66           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.MDR         2309           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.BMDR         3           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.BDDR         3           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PDC         66           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DD11         1204           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DNAC         3           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DNAC         3           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DIR         1           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DIN         1           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DUT         3           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DUT         3           target_!2c_SetRecv_!2cRegPtr_Cnt_T_		
target   2c_ SetRecv_   12cRegPtr_Cnt_T_str.CtKl.       2309         target   2c_ SetRecv_   12cRegPtr_Cnt_T_str.CtKl.       2309         target   2c_ SetRecv_   12cRegPtr_Cnt_T_str.CtKH       1204         target   2c_ SetRecv_   12cRegPtr_Cnt_T_str.DRR       67         target   2c_ SetRecv_   12cRegPtr_Cnt_T_str.DRR       67         target   2c_ SetRecv_   12cRegPtr_Cnt_T_str.DXR       66         target   2c_ SetRecv_   12cRegPtr_Cnt_T_str.DXR       66         target   2c_ SetRecv_   12cRegPtr_Cnt_T_str.MRR       2309         target   2c_ SetRecv_   12cRegPtr_Cnt_T_str.DRR       3         target   2c_ SetRecv_   12cRegPtr_Cnt_T_str.PIDT       3         target   2c_ SetRecv_   12cRegPtr_Cnt_T_str.PID11       1204         target   2c_ SetRecv_   12cRegPtr_Cnt_T_str.PID12       66         target   2c_ SetRecv_   12cRegPtr_Cnt_T_str.DIAC       3         target   2c_ SetRecv_   12cRegPtr_Cnt_T_str.DIA       1         target   2c_ SetRecv_   12cRegPtr_Cnt_T_str.DIA       1         target   2c_ SetRecv_   12cRegPtr_Cnt_T_str.DIA       2         target   2c_ SetRecv_   12cRegPtr_Cnt_T_str.DIA       3         targ		
target 12c_SetRecv 12cRegPtr_CntT_str.CLKL       2309         target 12c_SetRecv 12cRegPtr_CntT_str.CLKH       1204         target 12c_SetRecv 12cRegPtr_CntT_str.CNT       87         target 12c_SetRecv 12cRegPtr_CntT_str.DRR       67         target 12c_SetRecv 12cRegPtr_CntT_str.DRR       67         target 12c_SetRecv 12cRegPtr_CntT_str.DRR       55         target 12c_SetRecv 12cRegPtr_CntT_str.DRR       66         target 12c_SetRecv 12cRegPtr_CntT_str.WDR       2309         target 12c_SetRecv 12cRegPtr_CntT_str.WDR       5         target 12c_SetRecv 12cRegPtr_CntT_str.PBDR       3         target 12c_SetRecv 12cRegPtr_CntT_str.PDDT       1204         target 12c_SetRecv 12cRegPtr_CntT_str.PDD11       1204         target 12c_SetRecv 12cRegPtr_CntT_str.DMAC       3         target 12c_SetRecv 12cRegPtr_CntT_str.DM       1         target 12c_SetRecv 12cRegPtr_CntT_str.DM       1         target 12c_SetRecv 12cRegPtr_CntT_str.DIN       2         target 12c_SetRecv 12cRegPtr_CntT_str.DIN       2         target 12c_SetRecv 12cRegPtr_CntT_str.DIN       3         target 12c_SetRecv 12cRegPtr_CntT_str.DIT       3         target 12c_SetRecv 12cRegPtr_CntT_str.DIT       3         target 12c_SetRecv 12cRegPtr_CntT_str.DIT       3         target 12c_SetRecv 12cRegPtr_CntT_str	· · · · · - ·	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.CLKH 1204 target_12c_SetRecv_12cRegPtr_Cnt_T_str.CNT 87 target_12c_SetRecv_12cRegPtr_Cnt_T_str.DRR 67 target_12c_SetRecv_12cRegPtr_Cnt_T_str.DRR 55 target_12c_SetRecv_12cRegPtr_Cnt_T_str.DXR 66 target_12c_SetRecv_12cRegPtr_Cnt_T_str.DXR 66 target_12c_SetRecv_12cRegPtr_Cnt_T_str.DXR 66 target_12c_SetRecv_12cRegPtr_Cnt_T_str.DXR 55 target_12c_SetRecv_12cRegPtr_Cnt_T_str.DNR 2309 target_12c_SetRecv_12cRegPtr_Cnt_T_str.EMDR 3 target_12c_SetRecv_12cRegPtr_Cnt_T_str.PSC 66 target_12c_SetRecv_12cRegPtr_Cnt_T_str.PSC 66 target_12c_SetRecv_12cRegPtr_Cnt_T_str.PID11 1204 target_12c_SetRecv_12cRegPtr_Cnt_T_str.DMAC 3 target_12c_SetRecv_12cRegPtr_Cnt_T_str.DMAC 3 target_12c_SetRecv_12cRegPtr_Cnt_T_str.DMAC 3 target_12c_SetRecv_12cRegPtr_Cnt_T_str.DMAC 3 target_12c_SetRecv_12cRegPtr_Cnt_T_str.DIR 1 target_12c_SetRecv_12cRegPtr_Cnt_T_str.DIR 1 target_12c_SetRecv_12cRegPtr_Cnt_T_str.DIR 1 target_12c_SetRecv_12cRegPtr_Cnt_T_str.DIR 2 target_12c_SetRecv_12cRegPtr_Cnt_T_str.DUT 3 target_12c_SetRecv_12cRegPtr_Cnt_T_str.D		
target_12c_SetRecv_12cRegPtr_Cnt_T_str.CNT       87         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DRR       67         target_12c_SetRecv_12cRegPtr_Cnt_T_str.SAR       55         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DXR       66         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DNR       2309         target_12c_SetRecv_12cRegPtr_Cnt_T_str.VR       5         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DNR       3         target_12c_SetRecv_12cRegPtr_Cnt_T_str.PBC       66         target_12c_SetRecv_12cRegPtr_Cnt_T_str.PID11       1204         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DID12       66         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DMAC       3         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DIN       1         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DIN       1         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DIN       2         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DOUT       3         target_12c_SetRecv_12cRegPtr_Cnt_T_str.SET       3         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DR       2         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DR       2         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DR       3         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DR       3         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DAR       5         target_12c_SetSetatus_12cReg	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_ 2c_SetRecv_ 2cRegPtr_Cnt_T_str.DRR	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_ 2c_SetRecv_ 2cRegPtr_Cnt_T_str.DRR	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_12c_SetRecv_12cRegPtr_Cnt_T_str.SAR       55         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DXR       66         target_12c_SetRecv_12cRegPtr_Cnt_T_str.MDR       2309         target_12c_SetRecv_12cRegPtr_Cnt_T_str.WNB       5         target_12c_SetRecv_12cRegPtr_Cnt_T_str.EMDR       3         target_12c_SetRecv_12cRegPtr_Cnt_T_str.PID11       1204         target_12c_SetRecv_12cRegPtr_Cnt_T_str.PID12       66         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DMAC       3         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DMAC       3         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DIR       1         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DIR       1         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DUT       3         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DUT       3         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DUT       3         target_12c_SetRecv_12cRegPtr_Cnt_T_str.SET       3         target_12c_SetRecv_12cRegPtr_Cnt_T_str.ODR       2         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DOR       2         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DAR       3         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DAR       3         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DAR       5         target_12c_SetStatus_12cRegPtr_Cnt_T_str.DAR       5		67
target_12c_SetRecv_12cRegPtr_Cnt_T_str.DXR		55
target_12c_SetRecv_12cRegPtr_Cnt_T_str.MDR       2309         target_12c_SetRecv_12cRegPtr_Cnt_T_str.IVR       5         target_12c_SetRecv_12cRegPtr_Cnt_T_str.EMDR       3         target_12c_SetRecv_12cRegPtr_Cnt_T_str.PSC       66         target_12c_SetRecv_12cRegPtr_Cnt_T_str.PID11       1204         target_12c_SetRecv_12cRegPtr_Cnt_T_str.PID12       66         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DMAC       3         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DMAC       3         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DIR       1         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DIN       2         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DOUT       3         target_12c_SetRecv_12cRegPtr_Cnt_T_str.SET       3         target_12c_SetRecv_12cRegPtr_Cnt_T_str.CLR       1         target_12c_SetRecv_12cRegPtr_Cnt_T_str.ODR       2         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DD       3         target_12c_SetRecv_12cRegPtr_Cnt_T_str.PSL       3         target_12c_SetRecv_12cRegPtr_Cnt_T_str.OAR       55         target_12c_SetStatus_12cRegPtr_Cnt_T_str.IMR       66		
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR  3 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC  66 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11 1204 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12 66 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DID12 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC 3 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN 1 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN 1 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR 1 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN 2 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT 3 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT 3 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DET 3 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR 2 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DDR 2 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DDR 3 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DDR 4 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DDR 5 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DDR 5 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DDR 5 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DAR 5 target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DAR 5 target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DAR 66		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11       1204         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN       1         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR       1         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR       1         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOR       2         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DD       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR       55         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DAR       56		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11       1204         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN       1         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR       1         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN       2         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OLR       1         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR       2         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DD       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR       55         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR       66		
target_i2c_SetRecv_i2cRegPtr_Cnt_T_str.PiD11       1204         target_i2c_SetRecv_i2cRegPtr_Cnt_T_str.PiD12       66         target_i2c_SetRecv_i2cRegPtr_Cntstr.DMAC       3         target_i2c_SetRecv_i2cRegPtr_Cnt_T_str.FUN       1         target_i2c_SetRecv_i2cRegPtr_Cnt_T_str.DIR       1         target_i2c_SetRecv_i2cRegPtr_Cnt_T_str.DIN       2         target_i2c_SetRecv_i2cRegPtr_Cnt_T_str.DOUT       3         target_i2c_SetRecv_i2cRegPtr_Cnt_T_str.SET       3         target_i2c_SetRecv_i2cRegPtr_Cnt_T_str.CLR       1         target_i2c_SetRecv_i2cRegPtr_Cnt_T_str.ODR       2         target_i2c_SetRecv_i2cRegPtr_Cnt_T_str.DD       3         target_i2c_SetRecv_i2cRegPtr_Cnt_T_str.PSL       3         target_i2c_SetStatus_i2cRegPtr_Cnt_T_str.OAR       55         target_i2c_SetStatus_i2cRegPtr_Cnt_T_str.IMR       66	·	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN       1         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR       1         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN       2         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR       1         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR       2         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DD       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR       55         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR       66	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN       1         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR       1         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN       2         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR       1         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR       2         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DD       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR       55         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR       66	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN       1         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR       1         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN       2         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR       1         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR       2         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DD       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR       55         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR       66	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.FUN       1         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DIR       1         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DIN       2         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DOUT       3         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.SET       3         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLR       1         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.ODR       2         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DD       3         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PSL       3         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.OAR       55         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.IMR       66		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR       1         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DUN       2         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR       1         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR       2         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DD       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR       55         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR       66		
target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DIN       2         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DOUT       3         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.SET       3         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLR       1         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.ODR       2         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DD       3         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.PSL       3         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.OAR       55         target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.IMR       66		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR       1         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR       2         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR       55         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR       66		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR       1         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR       2         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR       55         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR       66		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR       1         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR       2         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR       55         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR       66		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR       2         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL       3         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR       55         target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR       66	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD 3 target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL 3 target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR 55 target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR 66	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD       3         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL       3         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR       55         target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR       66	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL 3 target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR 55 target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR 66		
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR 55 target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR 66		
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR 66		
target_izc_setstatus_izcRegPtr_Cnt_1_str.STR 556		
	target_izc_SetStatus_i2cRegPtr_Cnt_i_str.STR	556

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Name		
taggs (I.P., Serfolders, Designing Cort.) ≥ oct. CIX.  taggs (I.P	Name	Input Value
Bayes LD   Sedisistan Discipling OF   1 sed CLIN		•
Barger LD, Senderson Edelegin CH 1 and		
Barger 126   Sedicional Calcaging Cont   1 st DRR   10	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
Section   Description   Desc	target I2c SetStatus I2cRegPtr Cnt T str.CNT	87
Sept   12.5		67
Bingle Dec.   Sections, Discopy   Cont.   Sections		
bigger (De, SestSteiner, DeRicksphr), Cirt (T.) art MURC         5           bigger (De, SestSteiner, DeRicksphr), Cirt (T.) art MURC         3           bigger (De, SestSteiner, DeRicksphr), Cirt (T.) art MURC         6           bigger (De, SestSteiner, DeRicksphr), Cirt (T.) art MURC         6           bigger (De, SestSteiner, DeRicksphr), Cirt (T.) art MURC         3           bigger (De, SestSteiner, DeRicksphr), Cirt (T.) art MURC         3           bigger (De, SestSteiner, DeRicksphr), Cirt (T.) art MURC         3           bigger (De, SestSteiner, DeRicksphr), Cirt (T.) art MURC         3           bigger (De, SestSteiner, DeRicksphr), Cirt (T.) art MURC         3           bigger (De, SestSteiner, DeRicksphr), Cirt (T.) art MURC         3           bigger (De, SestSteiner, DeRicksphr), Cirt (T.) art MURC         3           bigger (De, SestSteiner, DeRicksphr), Cirt (T.) art MURC         3           bigger (De, SestSteiner, DeRicksphr), Cirt (T.) art MURC         3           bigger (De, SestSteiner, DeRicksphr), Cirt (T.) art MURC         3           bigger (De, SestSteiner, DeRicksphr), Cirt (T.) art MURC         3           bigger (De, SestSteiner, DeRicksphr), Cirt (T.) art MURC         3           bigger (De, SestSteiner, DeRicksphr), Cirt (T.) art MURC         3           bigger (De, SestSteiner, DeRicksphr), Cirt (T.) art MURC         3           bigger	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
Bigging   12.5   Selfishian   2.246/pg/F (CRT_ 1 M FMOR   3   1	target I2c SetStatus I2cRegPtr Cnt T str.DXR	66
Bigging   12.5   Selfishian   2.246/pg/F (CRT_ 1 M FMOR   3   1	· ·	2200
Signate   Dec. SerSchaus   2016  Per   Dr.   Ser DUDR		
Signature   Deck   Series   Series   Deck   Series   Se	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	5
Begin   Dispet   Di	target I2c SetStatus I2cRegPtr Cnt T str.EMDR	3
Target LP, SalSahan LPR-Reptin CM, Tas PHO11  Target LP, SalSahan LPR-Reptin CM, Tas PHO12  Target LP, SalSahan LPR-Reptin CM, Tas PHO13  Target LP, SalSahan LPR-Reptin CM, Tas PHO14  Target LP, Salsahan LP		
Sept   1.00   Self-Statu   2/Respire   Cut   Tat / Discourage   Cut		
Image   12.5 SetShaha   22ReptPC PC   T of DIAPAC	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11	1204
target ID., Selfstate, J. Pickippi C. m.T. Jar D. MAC  target ID. Selfstate, J. Pickippi C. m.T. Jar D. M.  target ID. Selfstate, J. Defengin C. m.T. Jar D. M.  target ID. Selfstate, J. Defengin C. m.T. Jar D. M.  target ID. Selfstate, J. Defengin C. m.T. Jar D. M.  target ID. Selfstate, J. Defengin C. m.T. Jar D. M.  target ID. Selfstate, J. Defengin C. m.T. Jar D. M.  target ID. Selfstate, J. Defengin C. m.T. Jar D. M.  target ID. Selfstate, J. Defengin C. m.T. Jar D. M.  target ID. Selfstate, J. Defengin C. m.T. Jar D. M.  target ID. Selfstate, J. Defengin C. m.T. Jar D. M.  target ID. Selfstate, J. Defengin C. m.T. Jar D. M.  target ID. Selfstate, J. Defengin C. m.T. Jar D. M.  target ID. Selfstate, J. Defengin C. m.T. Jar D. M.  target ID. Selfstate, J. Defengin C. m.T. Jar D. M.  target ID. Selfstate Interference J. Defengin C. m.T. Jar D. M.  target ID. Selfstate Interference J. Defengin C. m.T. Jar D. M.  target ID. Selfstate Interference J. Defengin C. m.T. Jar D. M.  target ID. Selfstate Interference J. Defengin C. m.T. Jar D. M.  target ID. Selfstate Interference J. Defengin C. m.T. Jar D. M.  target ID. Selfstate Interference J. Defengin C. m.T. Jar D. M.  target ID. Selfstate Interference J. Defengin C. m.T. Jar D. M.  target ID. Selfstate Interference J. Defengin C. m.T. Jar D. M.  target ID. Selfstate Interference J. Defengin C. m.T. Jar D. M.  target ID. Selfstate Interference J. Defengin C. m.T. Jar D. M.  target ID. Selfstate Interference J. Defengin C. m.T. Jar D. M.  target ID. Selfstate Interference J. Defengin C. m.T. Jar D. M.  target ID. Selfstate Interference J. Defengin C. m.T. Jar D. M.  target ID. Selfstate Interference J. Defengin C. m.T. Jar D. M.  target ID. Selfstate Interference J. Defengin C. m.T. Jar D. M.  target ID. Selfstate Interference J. Defengin C. m.T. Jar D. M.  target ID. Selfstate Interference J. Defengin C. m.T. Jar D. M.  target ID. Selfstate Interference J. Defengin C. m.T. Jar D. M.  target ID. Selfstate Interference J. Defengin C. m.T. Jar D. M.  target ID. Sel	target I2c SetStatus I2cRegPtr Cnt T str.PID12	66
Sept   Dec   Sept   S		2
signet 12.9 Selfsteins (24RepPir CNT ± M DIR  1 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  3 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  3 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  3 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ± M DOVT  4 triggs 12.9 Selfsteins (24RepPir CNT ±		
Seption   December	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
	target I2c SetStatus I2cRegPtr Cnt T str.DIR	1
target, I.S. Selfstates, Dichespit, Cont., T. at DOUT  1 staget, I.S. Selfstates, Dichespit, Cont., T. at DCLR  1 target, I.S. Selfstates, Dichespit, Cont., T. at DCLR  1 target, I.S. Selfstates, Dichespit, Cont., T. at DCLR  1 target, I.S. Selfstates, Dichespit, Cont., T. at DCLR  1 target, I.S. Selfstates, Dichespit, Cont., T. at DCLR  1 target, I.S. Selfstates, Dichespit, Cont., T. at DCLR  1 target, I.S. Selfstates, Dichespit, Cont., T. at DCLR  1 target, I.S. Selfstates, Dichespit, Cont., T. at DCLR  1 target, I.S. Selfstates Receives, Dichespit, Cont., T. at DCLR  1 target, I.S. Selfstates Receives, Dichespit, Cont., T. at DCLR  1 target, I.S. Selfstates Receives, Dichespit, Cont., T. at DCLR  1 target, I.S. Selfstates Receives, Dichespit, Cont., T. at DCLR  1 target, I.S. Selfstates Receives, Dichespit, Cont., T. at DCLR  1 target, I.S. Selfstates Receives, Dichespit, Cont., T. at DCLR  1 target, I.S. Selfstates Receives, Dichespit, Cont., T. at DCLR  1 target, I.S. Selfstates Receives, Dichespit, Cont., T. at DCLR  1 target, I.S. Selfstates Receives, Dichespit, Cont., T. at DCLR  1 target, I.S. Selfstates Receives, Dichespit, Cont., T. at DCLR  1 target, I.S. Selfstates Receives, Dichespit, Cont., T. at DCLR  1 target, I.S. Selfstates Receives, Dichespit, Cont., T. at DCLR  1 target, I.S. Selfstates Receives, Dichespit, Cont., T. at DCLR  1 target, I.S. Selfstates Receives, Dichespit, Cont., T. at DCLR  1 target, I.S. Selfstates Receives, Dichespit, Cont., T. at DCLR  1 target, I.S. Selfstates Receives, Dichespit, Cont., T. at DCLR  1 target, I.S. Selfstates Receives, Dichespit, Cont., T. at DCLR  1 target, I.S. Selfstates Receives, Dichespit, Cont., T. at DCLR  1 target, I.S. Selfstates Receives, Dichespit, Cont., T. at DCLR  1 target, I.S. Selfstates Receives, Dichespit, Cont., T. at DCLR  1 target, I.S. Selfstates Receives, Dichespit, Cont., T. at DCLR  1 target, I.S. Selfstates Receives, Dichespit, Cont., T. at DCLR  1 target, I.S. Selfstates Receives, Dichespit, Cont., T. at DCLR  1 target, I.S. S		
Image: 1.02. Selfstate:	· ·	
Langer   L.S. SetSabas   Exchanger   Con T   Str. COR	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
Langer   L.S. SetSabas   Exchanger   Con T   Str. COR	target I2c SetStatus I2cRegPtr Cnt T str.SET	3
Image   12.5 SetSubus   Defengin   Cont   Turk DOR		
Longel, E.S., Selfablas, (Directoph', CMT_LISTPD)         3           Longel, E.S., Selfablaste/Receive, (2016ppřf., CMT_LIST NR)         5           Longel, E.S., Selfablaste/Receive, (2016ppřf., CMT_LIST NR)         66           Longel, E.S., Selfablaste/Receive, (2016ppřf., CMT_LIST NR)         66           Longel, E.S., Selfablaste/Receive, (2016ppřf., CMT_LIST NR)         55           Longel, E.S., Selfablaste/Receive, (2016ppřf., CMT_LIST NR)         56           Longel, E.S., Selfablaste/Receive, (2016ppřf., CMT_LIST NR)         120           Longel, E.S., Selfablaste/Receive, (2016ppřf., CMT_LIST NR)         67           Longel, E.S., Selfablaste/Receive, (2016ppřf., CMT_LIST NR)         67           Longel, E.S., Selfablaste/Receive, (2016ppřf., CMT_LIST NR)         57           Longel, E.S., Selfablaste/Receive, (2016ppřf., CMT_LIST NR)         58           Longel, E.S., Selfablaste/Receive, (2016ppřf., CMT_LIST NR)         5           Longel, E.S., Selfablaste/Receive, (2016ppřf., CMT_LIST PD101         124           Longel, E.S., Selfablaste/Receive, (2016ppřf., CMT_LIST PD102         6           Longel, E.S., Selfablaste/Receive, (2016ppřf., CMT_LIST DD102         6           Longel, E.S., Selfablaste/Receive, (2016ppřf., CMT_LIST DD102         6           Longel, E.S., Selfablaste/Receive, (2016ppřf., CMT_LIST DD102         6           Longel, E.S., Selfablaste/Receive, (2016ppřf., CMT_LIST		
September   Comment   Co	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
September   Comment   Co	target I2c SetStatus I2cRegPtr Cnt T str.PD	3
tingel, Zo, SchlighblasterRockey, 12/RopPtr. Cell. T.; sh. DAR         55           tingel, Zo, SchlighblasterRockey, 12/RopPtr. Cell. T.; sh. DAR         56           tingel, Zo, SchlighblasterRockey, 12/RopPtr. Cell. T.; sh. DAR         55           tingel, Zo, SchlighblasterRockey, 12/RopPtr. Cell. T.; sh. CLRL         1204           tingel, Zo, SchlighblasterRockey, 12/RopPtr. Cell. T.; sh. CLRL         1204           tingel, Zo, SchlighblasterRockey, 12/RopPtr. Cell. T.; sh. CLRL         127           tingel, Zo, SchlighblasterRockey, 12/RopPtr. Cell. T.; sh. DAR         67           tingel, Zo, SchlighblasterRockey, 12/RopPtr. Cell. T.; sh. DAR         65           tingel, Zo, SchlighblasterRockey, 12/RopPtr. Cell. T.; sh. DAR         20           tingel, Zo, SchlighblasterRockey, 12/RopPtr. Cell. T.; sh. DAR         3           tingel, Zo, SchlighblasterRockey, 12/RopPtr. Cell. T.; sh. DAR         3           tingel, Zo, SchlighblasterRockey, 12/RopPtr. Cell. T.; sh. PDD1         1204           tingel, Zo, SchlighblasterRockey, 12/RopPtr. Cell. T.; sh. PDD1         1204           tingel, Zo, SchlighblasterRockey, 12/RopPtr. Cell. T.; sh. PDD1         1204           tingel, Zo, SchlighblasterRockey, 12/RopPtr. Cell. T.; sh. DAR         3           tingel, Zo, SchlighblasterRockey, 12/RopPtr. Cell. T.; sh. DAR         3           tingel, Zo, SchlighblasterRockey, 12/RopPtr. Cell. T.; sh. DAR         3		
target J.D. SchuphasterReceive Jockeght Cnit J. str SIR         558           target J.D. SchuphasterReceive Jockeght Cnit J. str SIR         559           target J.D. SchuphasterReceive Jockeght Cnit J. str CLIK         209           target J.D. SchuphasterReceive Jockeght Cnit J. str CLIK         1204           target J.D. SchuphasterReceive Jockeght Cnit J. str CNT         87           target J.D. SchuphasterReceive Jockeght Cnit J. str CNR         67           target J.D. SchuphasterReceive Jockeght Cnit J. str CNR         68           target J.D. SchuphasterReceive Jockeght Cnit J. str CNR         68           target J.D. SchuphasterReceive Jockeght Cnit J. str CNR         68           target J.D. SchuphasterReceive Jockeght Cnit J. str CNR         30           target J.D. SchuphasterReceive Jockeght Cnit J. str CNR         3           target J.D. SchuphasterReceive Jockeght Cnit J. str CNR         3           target J.D. SchuphasterReceive Jockeght Cnit J. str CNR         3           target J.D. SchuphasterReceive Jockeght Cnit J. str CNR         6           target J.D. SchuphasterReceive Jockeght Cnit J. str CNR         3           target J.D. SchuphasterReceive Jockeght Cnit J. str CNR         1           target J.D. SchuphasterReceive Jockeght Cnit J. str CNR         1           target J.D. SchuphasterReceive Jockeght Cnit J. str CNR         1           target J	· ·	
target_D2, Sehuphatserffeedere, J2cRepht_Cott_1 at CIX.         2009           target_D2, Sehuphatserffeedere, J2cRepht_Cott_1 at CIX.         2009           target_D2, Sehuphatserffeedere, J2cRepht_Cott_1 at CIX.         2004           target_D2, Sehuphatserfeedere, J2cRepht_Cott_1 at CIX.         67           target_D2, Sehuphatserfeedere, J2cRepht_Cott_1 at CIX.         67           target_D2, Sehuphatserfeedere, J2cRepht_Cott_1 at XDR         65           target_D2, Sehuphatserfeedere, J2cRepht_Cott_1 at XDR         66           target_D2, Sehuphatserfeedere, J2cRepht_Cott_1 at XDR         66           target_D2, Sehuphatserfeedere, J2cRepht_Cott_1 at XDR         7           target_D2, Sehuphatserfeedere, J2cRepht_Cott_1 at XDR         7           target_D2, Sehuphatserfeedere, J2cRepht_Cott_1 at XDR         8           target_D2, Sehuphatserfeedere, J2cRepht_Cott_1 at XDR         10           target_D2, Sehuphatserfeedere, J2cRepht_Cott_1 at XDR         10           target_D2, Sehuphatserfeedere, J2cRepht_Cott_1 at XDR         1           target_D2, Sehuphatserfeedere, J2cRep	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_D2, Setuphatest/Receive_D2Reptr_COLT_str_STR         558           target_D2, Setuphatest/Receive_D2Reptr_COLT_str_CULH         2209           target_D2, Setuphatest/Receive_D2Reptr_COLT_str_CULH         1204           target_D2, Setuphatest/Receive_D2Reptr_COLT_str_CULH         1204           target_D2, Setuphatest/Receive_D2Reptr_COLT_str_DTDRR         67           target_D2, Setuphatest/Receive_D2Reptr_COLT_str_DTDRR         67           target_D2, Setuphatest/Receive_D2Reptr_COLT_str_DTDRR         65           target_D2, Setuphatest/Receive_D2Reptr_COLT_str_DTDRR         26           target_D2, Setuphatest/Receive_D2Reptr_COLT_str_DTDRR         209           target_D2, Setuphatest/Receive_D2Reptr_COLT_str_DTDRR         3           target_D2, Setuphatest/Receive_D2Reptr_COLT_str_DTDRR         3           target_D2, Setuphatest/Receive_D2Reptr_COLT_str_DTDRR         3           target_D2, Setuphatest/Receive_D2Reptr_COLT_str_DTDR         1204           target_D2, Setuphatest/Receive_D2Reptr_COLT_str_DTDR         1           target_D2, Setuphatest/Receive_D2Reptr_COLT_str_DTDR         1           target_D2, Setuphatest/Receive_D2Reptr_COLT_str_DTDR         1           target_D2, Setuphatest/Receive_D2Reptr_COLT_str_DTDR         2           target_D2, Setuphatest/Receive_D2Reptr_COLT_str_DT_SCDR         2           target_D2, Setuphatest/Receive_D2Reptr_COLT_str_D	target I2c SetupMasterReceive I2cRegPtr Cnt T str IMR	66
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target_12c_SebupMasterReceive_12cRegiptr_CNLT_str.CNH singet_12c_SebupMasterReceive_12cRegiptr_CNLT_str.DNR singet_12c_SebupMasterReceive_12cRegiptr_CNLT_st		
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target_12b_SetupMasterReceive_12cRepPtr_Cntstr.DXR         65           target_12b_SetupMasterReceive_12cRepPtr_Cntstr.DXR         66           target_12b_SetupMasterReceive_12cRepPtr_Cntstr.DXR         5           target_12b_SetupMasterReceive_12cRepPtr_Cntstr.DMR         3           target_12b_SetupMasterReceive_12cRepPtr_Cntstr.DMR         3           target_12b_SetupMasterReceive_12cRepPtr_Cntstr.DMR         3           target_12b_SetupMasterReceive_12cRepPtr_Cntstr.DMR         12           target_12b_SetupMasterReceive_12cRepPtr_Cntstr.DMR         3           target_12b_SetupMasterReceive_12cRepPtr_Cntstr.DMR         3           target_12b_SetupMasterReceive_12cRepPtr_Cntstr.DMR         1           target_12b_SetupMasterReceive_12cRepPtr_Cntstr.DMR         1           target_12b_SetupMasterReceive_12cRepPtr_Cntstr.DMR         1           target_12b_SetupMasterReceive_12cRepPtr_Cntstr.DMR         2           target_12b_SetupMasterReceive_12cRepPtr_Cntstr.DMR         3           target_12b_SetupMasterReceive_12cRepPtr_Cntstr.DMR         3           target_12b_SetupMasterReceive_12cRepPtr_Cntstr.DMR         3           target_12b_SetupMasterTarannt_str.DCRepPtr_Cntstr.DMR         3           target_12b_SetupMasterTarannt_str.DCRepPtr_Cntstr.DMR         6           target_12b_SetupMasterTarannt_str.DCRepPtr_Cntstr.DMR         <	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_I_str.CNI	87
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target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.NDR         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PDDR         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PDDT         1204           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PDDT         66           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PDDT         66           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDMC         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDM         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDM         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDM         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDM         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDM         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDM         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDM         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDM         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDM         3           target_12c_SetupMasterTransmt_12cRegPtr_Cnt_T_str.DDM         3           target_12c_SetupMasterTransmt_12cRegPtr_Cnt_T_str.DMR         5           target_12c_SetupMasterTransmt_12cRegPtr_Cnt_T_str.DMR         6           target_12c_SetupMasterTransmt_12cRegPtr_Cnt_T_str.D	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
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Sarget   122   SetupMasterReceive   128-RepPir Cnt   1 str ENDR   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294   1294		5
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_PIC1         1204           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_PID11         1204           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DID12         66           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DID13         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DID1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DID1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DID1         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DID1         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DID1         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DID1         4           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DID1         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DID1         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DID1         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str_DID1         3           target_12c_SetupMasterTarasmit_12cRegPtr_Cnt_T_str_DID1         4           target_12c_SetupMasterTarasmit_12cRegPtr_Cnt_T_str_DID1         6           target_12c_SetupMasterTarasmit_12cRegPtr_Cnt_T_str_DID1         8           target_12c_SetupMasterTarasmit_12cRegPtr_Cnt_T_str_DID1         8           target_12c_SetupMasterTarasmi		
target   2c. SetupMasterReceive   2cRegPtr. Cnt.   str. PD11   1204	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target   12c. SetupMasterReceive   12cRegPtr_Cnt_T_str.PD12   66	target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSC	66
target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.PID12         66           target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DNAC         3           target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DN         1           target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DIN         1           target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DIN         2           target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DOUT         3           target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DOR         1           target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DOR         2           target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DOR         2           target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DOR         2           target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DOR         2           target_J2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DOR         3           target_J2c_SetupMasterTransmit_J2cRegPtr_Cnt_T_str.DAR         55           target_J2c_SetupMasterTransmit_J2cRegPtr_Cnt_T_str.DAR         56           target_J2c_SetupMasterTransmit_J2cRegPtr_Cnt_T_str.CLKH         1204           target_J2c_SetupMasterTransmit_J2cRegPtr_Cnt_T_str.DAR         67           target_J2c_SetupMasterTransmit_J2cRegPtr_Cnt_T_str.DAR         66           target_J2c_SetupMasterTransmit_J2cRegPtr_Cnt_T_str.DAR         66           target_J2c_SetupMasterTransmit_J2cRegPtr_C		
larget   2c. SetupMasterReceive   2cRegPtr_Cnt_T.str.DNAC   1   1   1   1   1   1   1   1   1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT         3           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT         3           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN         3           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN         3           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         55           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         66           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ClkL         2309           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ClkL         2309           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         67           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         67           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         66           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         66           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         67           target_I2c_SetupMasterTransmit_I2cR	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT         3           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT         3           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT         3           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOR         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOR         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOR         3           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         3           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         55           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         66           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL         2309           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL         2309           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         67           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         67           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         66           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         66           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         67           target_I2c_SetupMasterTransmit_I2	target I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	3
target_    2c_SetupMasterReceive_    2cRegPtr_Cnt_T_str_DIR		
target_12c_SetupMasterReceive_12cRegPtr_Cnt_Tstr.DIN         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_Tstr.DOUT         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_Tstr.SET         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_Tstr.DDR         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_Tstr.DDR         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_Tstr.DDR         3           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_Tstr.DAR         55           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_Tstr.DAR         55           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_Tstr.DAR         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_Tstr.CKL         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_Tstr.CKT         120           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_Tstr.CKT         120           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_Tstr.CKT         87           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_Tstr.DAR         67           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_Tstr.DAR         68           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_Tstr.DAR         55           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_Tstr.DAR         5           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_Tstr.DAR         5           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_Tstr.DA		
target_ 2c_SetupMasterReceive_ 2cRegPtr_Cnt_T_str.DOUT	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_ 2c_SetupMasterReceive_ 2cRegPtr_Cnt_T_str.DOUT	target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIN	2
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.SET 1 arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDR 1 arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDR 2 target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DD 3 arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DD 3 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR 5 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR 5 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR 6 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR 6 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLK 1 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLK 1 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLK 1 arget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR 6 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR 7 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR 7 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR 7 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR 7 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR 7 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR 8 target_1		
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.OLR 1 target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DD 2 target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DD 3 target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DD 3 target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DA 5 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DA 5 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DA 6 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DA 6 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLK 1 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLK 1 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DA 7 target_12c_SetupMasterTransmit_1	target_izc_SetupiviasterReceive_izcRegPti_Gnt_i_str.b001	
target_12c_SetupMasterReceive_12cRegPtr_CntT_str.ODR         2           target_12c_SetupMasterReceive_12cRegPtr_CntT_str.PD         3           target_12c_SetupMasterTransmit_12cRegPtr_CntT_str.DAR         55           target_12c_SetupMasterTransmit_12cRegPtr_CntT_str.OAR         55           target_12c_SetupMasterTransmit_12cRegPtr_CntT_str.MR         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CtkL         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CtkL         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CtkL         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CtkL         87           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.Ctt_R         67           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         65           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         3           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         3           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDT         1204           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDT         1204           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDT         1           target_12c_SetupMas	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_Tstr.DDR         2           target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_Tstr.PD         3           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_Tstr.DR         3           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_Tstr.OAR         55           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_Tstr.MR         66           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_Tstr.STR         556           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_Tstr.CtkL         2309           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_Tstr.CtkH         1204           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_Tstr.CtkH         1204           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_Tstr.DRR         67           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_Tstr.DRR         67           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_Tstr.DRR         55           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_Tstr.MDR         2309           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_Tstr.DRR         3           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_Tstr.DRR         66           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_Tstr.DDT         1204           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_Tstr.DDT         1204           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_Tstr.DDT         3           target_!2c_SetupMasterTransmit_!2cReg	target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	1
target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PD         3           target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PSL         3           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.OAR         55           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR         66           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL         2309           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKH         1204           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CKNT         87           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT         87           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR         67           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR         55           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR         66           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR         2309           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR         3           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR         3           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DID11         1204           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DID2         66           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DID4         3           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DID         1           target_!2c_SetupMas		
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 55 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 55 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 66 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR 556 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL 2309 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL 2309 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL 1204 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT 87 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 67 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 55 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 66 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 1209 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 2309 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 3 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 1 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 1 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 1 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 1 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 1 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 1 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 2 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 1 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 2 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 2 target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR 2 target_!2c_SetupMasterTr		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.NR	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.NR	target_I2c_SetupMasterReceive I2cRegPtr Cnt T str.PSL	3
target_12c_SetupMasterTransmit_12cRegPtr_CnLT_str.IMR		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL 2309 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL 2309 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH 1204 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT 87 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR 67 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR 67 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR 66 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR 2309 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.NDR 2309 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.NDR 3 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.NDR 3 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSC 66 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID11 1204 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DID12 66 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DID12 66 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DID12 66 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DID13 1204 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DID14 1204 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DID15 1204 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DID15 1204 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DID16 1204 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DID16 1204 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DID16 1204 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DID16 1204 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DID16 1204 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DID17 3 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DUT 3 target_12c_SetupMasterTr	· ·	
target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.CLKL	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.CLKL	target_I2c_SetupMasterTransmit I2cRegPtr Cnt T str.STR	556
target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.CLKH target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.DTR target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.DRR darget_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.DRR darget_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.DRR def target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.DRR def target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.DRR def target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.MDR def target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.MDR def target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.EMDR def target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.PSC def target_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.PID11 darget_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.DID12 darget_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.DID12 darget_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.DID13 darget_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.DID14 darget_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.DID15 darget_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.DID16 darget_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.DID17 darget_ 2c_SetupMasterTransmit_ 2cRegPtr_Cn		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.SAR target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR 66 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR 2309 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PRDR 3 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR 3 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PDT 1204 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID11 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DID12 66 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DINAC 3 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN 1 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIR 1 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN 2 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DUT 3 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DUR 2 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DUR 2 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DUR 2 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DUR 2 target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DUR 3		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR 55  target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR 66  target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR 66  target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MDR 2309  target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.NDR 5  target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR 3  target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR 3  target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PDC 66  target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID11 1204  target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID12 66  target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DMAC 3  target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIR 1  target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIR 1  target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIR 2  target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DOUT 3  target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DOUT 3  target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DOUT 3  target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DOUT 3  target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DOUR 2  target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDR 2  target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDR 2  target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDR 3  target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDR 3  target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDR 3  target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDR 3  target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDR 3	target_izc_SetupMasterTransmit_izcRegPtr_Cnt_T_str.CLKH	1204
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR 55 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR 66 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR 66 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR 2309 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR 5 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR 3 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR 3 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 1204 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 66 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 66 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 3 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR 1 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR 1 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR 2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT 3 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUR 2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUR 2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUR 2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUR 3	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_ str.CNT	87
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR  atarget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DCLR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  target_l2c_SetupMaste		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR 2309  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.NVR 5  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR 3  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC 66  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PDD1 1204  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 1204  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 66  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 3  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 3  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR 1  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR 1  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN 2  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT 3  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT 3  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR 1  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR 2  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR 2  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR 2  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR 2  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR 3  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD 3  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD 3  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD 3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PNR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PUN  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  2  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  2  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  3  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  3  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  3  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  3  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  3	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PNR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PUN  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  2  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  2  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  3  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  3  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  3  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  3  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  3	target_I2c_SetupMasterTransmit I2cRegPtr Cnt T str.DXR	66
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DW  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DET  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DER  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DER  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD  3  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD  3  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD  3  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD  3  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD  3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DET  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DS  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DS  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DS  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DS  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DS  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DS  target_l2c_SetupMasterTransmit_l2cRegPtr_Cn		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DW target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD 3 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DSL 3	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD target_l2c_SetupMasterTransmit	target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 1204  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 66  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 3  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN 1  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR 1  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN 2  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT 3  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET 3  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR 1  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR 2  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR 2  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD 3  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD 3  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL 3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 66  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC 3  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN 1  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR 1  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN 2  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT 3  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET 3  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR 1  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR 2  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR 2  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD 3  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL 3	· ·	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DSL  3	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DSL	target_I2c_SetupMasterTransmit I2cRegPtr Cnt T str.PID12	66
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN 1 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR 1 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN 2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT 3 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET 3 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR 1 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR 2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR 3 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL 3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN  2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT  3 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET  4 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR  4 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  4 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DDR  5 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD  6 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  7 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  8		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  3	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN 2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT 3 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET 3 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR 1 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR 2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD 3 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL 3	target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	1
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  3  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD  3  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL  3	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD  3  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL  3	target I2c SetupMasterTransmit I2cReqPtr Cnt T str.SET	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR 2 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD 3 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL 3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD 3 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL 3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL 3	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL 3	target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	3
target_i2cREG1_temp.OAR 55	target_i2cREG1_temp.OAR	55



DigColPsInt\_InterruptNotification

Name	Input Value		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	556		
target_i2cREG1_temp.CLKL	2309		
target_i2cREG1_temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66 2309		
target_i2cREG1_temp.MDR	5		
target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target i2cREG1 temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target i2cREG1 temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target i2cREG1 temp.DIN	2		
target i2cREG1 temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target i2cREG1 temp.CLR	1		
target i2cREG1 temp.ODR	2		
target_i2cREG1_temp.PD	3		
target i2cREG1 temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt AttempOccurForCustDatRead Cnt M u08	4	4	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	
	1	1	
DigColPoint_ColCustDatFound_Cnt_M_lgc	2309	2309	
DigColPoint_ColSnsrData_Cnt_M_u16		47	
DigColPsInt_CurrentSlave_Cnt_M_u08	47		
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTF		LREG_SET
DigColPoint_I2CHwCustData_Uls_M_u16	106 180	106 180	
DigColPoint_I2CHwincompleteCustData_Uls_M_u16	0	0	
DigColPoint_InitFailedOnce_Cnt_M_lgc	1	1	
DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	
	5	5	
DigColPoint_RecvdDataType_Cnt_M_u08	0	0	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	
	14	14	
DigColPsInt_TransactionCnt_Cnt_M_u08			
I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	
· · · · · · ·			
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR	55 66	55 66	
	556	556	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target I2c GenStopCond I2cRegPtr Cnt T str.CLKH	1204	1204	
	87	87	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	67	67	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR	55	55	
	66	66	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR	5	5	
	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	66	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC			
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204 66	1204 66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12			
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN			
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	3	3	•
target I2c Send I2cRegPtr Cnt T str.OAR	55	55	· · · · · · · · · · · · · · · · · · ·

55

66

55

66

 $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.OAR$ 

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IMR

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	Ž
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	67 55	67 55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	2309	2309	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>~</b>
target I2c Send I2cRegPtr Cnt T str.PSC	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	<i>-</i>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67 55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55 66	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	5	5	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	·
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67 55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55 66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	2309	2309	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FMDR	3	3	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	_

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Name	Actual Value	Expected Value	Resul
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKH	1204	1204	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CNT	87	87	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DRR	67	67	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DXR	66	66	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.MDR	2309	2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.EMDR	3	3	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSC	66	66	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	1204	1204	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID12	66	66	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	3	3	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.FUN	1	1	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIR	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	
rarget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	
target I2c SetupMasterReceive I2cReqPtr Cnt T str.ODR	2	2	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	3	3	
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	
	2309	2309	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	1204	1204	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	87	87	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	67	67	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	•

T .				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c_Send	1	I2c_Send	1	<b>✓</b>

Test Step 2.35 (Repeat Count = 1)		✓
Name	Input Value	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2	
DigColPsInt_Buffer_Cnt_M_u08[0]	22	
DigColPsInt_Buffer_Cnt_M_u08[1]	44	
DigColPsInt_Buffer_Cnt_M_u08[2]	55	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	
DigColPsInt_ColSnsrData_Cnt_M_u16	495	
DigColPsInt_CurrentSlave_Cnt_M_u08	40	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_READ	
DigColPsInt_I2CHwCustData_Uls_M_u16	109	

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Name	Input Value
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	191
DigColPsInt InitFailedOnce Cnt M Igc	1
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt PrevReqDataType Cnt M u08	0
	0
DigColPsInt_RecvOverrunError_Cnt_M_lgc	
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	897
DigColPsInt_TransactionCnt_Cnt_M_u08	6
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	
T_DataRegisters_Cnt_u08[1]	32
	30
T_DataRegisters_Cnt_u08[2]	36
T_DataRegisters_Cnt_u08[3]	
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	51
k_SpurSensorl2CAddress_Cnt_u08	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	78
	495
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	56
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT	897
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR	98
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	78
target I2c GenStopCond I2cRegPtr Cnt T str.DMAC	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	66
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	

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Name	Input Value
	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78
	495
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78
target I2c SetRecv I2cRegPtr Cnt T str.PID11	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78
target I2c SetRecv I2cRegPtr Cnt T str.DMAC	0
	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
	1
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	56
	897
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	0
target 12c SetStatus 12cRegPtr_Cnt_T_str.bOUT	0
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target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
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Name	Input Value		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIR	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	0		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	1		
target I2c SetupMasterReceive I2cRegPtr_Cnt_T_str.ODK	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0		
	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	0		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	0		
target_i2cREG1_temp.OAR	66		
target_i2cREG1_temp.IMR	78		
target_i2cREG1_temp.STR	78		
target i2cREG1 temp.CLKL	495		
target_i2cREG1_temp.CLKH	56		
target_i2cREG1_temp.CNT	897		
target i2cREG1 temp.DRR	98		
	66		
target_i2cREG1_temp.SAR	66		
target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR	78		
target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR	78 495		
target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR	78 495 66		
target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR	78 495 66 0		
target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC	78 495 66 0 78		
target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11	78 495 66 0 78 56		
target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12	78 495 66 0 78 56 78		
target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC	78 495 66 0 78 56 78		
target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN	78 495 66 0 78 56 78 0		
target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR	78 495 66 0 78 56 78 0 0		
target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIR target_i2cREG1_temp.DIR	78 495 66 0 78 56 78 0 0		
target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR	78 495 66 0 78 56 78 0 0 0		
target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIR target_i2cREG1_temp.DIR	78 495 66 0 78 56 78 0 0 0 1		
target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT	78 495 66 0 78 56 78 0 0 0		
target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DMAC target_i2cREG1_temp.DIR target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET	78 495 66 0 78 56 78 0 0 0 1		
target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DIN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DUT target_i2cREG1_temp.DUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR	78 495 66 0 78 56 78 0 0 0 1 0 0 0		
target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DIN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR	78 495 66 0 78 56 78 0 0 1 0 0 1		
target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DIN target_i2cREG1_temp.DIN target_i2cREG1_temp.DIN target_i2cREG1_temp.DUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR	78 495 66 0 78 56 78 0 0 0 1 0 0 1 0 0 1	Expected Value	Result
target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.HVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DIN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.PDL	78 495 66 0 78 56 78 0 0 0 1 0 0 1 0 0 0 0 1	Expected Value 3	Result
target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.PID12 target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.DOUT target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.PDL target_i2cREG1_temp.PD target_i2cREG1_temp.PSL Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	78 495 66 0 78 56 78 0 0 0 1 0 0 1 0 0 Actual Value	•	Result
target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.HVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DIMAC target_i2cREG1_temp.DIN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.DCUT target_i2cREG1_temp.DCLR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0]	78 495 66 0 78 56 78 0 0 0 1 0 0 Actual Value 3	3 12	~
target_i2cREG1_temp.SAR  target_i2cREG1_temp.DXR  target_i2cREG1_temp.MDR  target_i2cREG1_temp.HVR  target_i2cREG1_temp.EMDR  target_i2cREG1_temp.PSC  target_i2cREG1_temp.PID11  target_i2cREG1_temp.PID12  target_i2cREG1_temp.DMAC  target_i2cREG1_temp.DIN  target_i2cREG1_temp.DIR  target_i2cREG1_temp.DIR  target_i2cREG1_temp.DIN  target_i2cREG1_temp.DUT  target_i2cREG1_temp.DOUT  target_i2cREG1_temp.CLR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.PD  target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]	78 495 66 0 78 56 78 0 0 0 1 0 0 Actual Value 3 12	3 12 44	~
target_i2cREG1_temp.DXR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.HVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DMAC target_i2cREG1_temp.DIN target_i2cREG1_temp.DIN target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.DOUT target_i2cREG1_temp.DCLR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	78 495 66 0 78 56 78 0 0 0 1 0 0 Actual Value 3	3 12	~ ~
target_i2cREG1_temp.DXR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.HVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DMAC target_i2cREG1_temp.DIR target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DUT target_i2cREG1_temp.DOUT target_i2cREG1_temp.DCLR target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc	78 495 66 0 78 56 78 0 0 0 1 0 0 1 0 0 Actual Value 3 12 44 55	3 12 44 55 0	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.DXR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.HVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DMAC target_i2cREG1_temp.DIR target_i2cREG1_temp.DIR target_i2cREG1_temp.DIR target_i2cREG1_temp.DOUT target_i2cREG1_temp.DOUT target_i2cREG1_temp.CLR target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR target_i2cREG1_temp.DD target_i2cREG1_temp.DD target_i2cREG1_temp.DD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CndFailOccurred_Cnt_M_lgc	78 495 66 0 78 56 78 0 0 0 1 0 0 1 0 0 Actual Value 3 12 44 55 0 0	3 12 44 55 0	~ ~
target_i2cREG1_temp.DXR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.HVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DIN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.DOUT target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc	78 495 66 0 78 56 78 0 0 0 1 0 0 1 0 0 Actual Value 3 12 44 55 0 0 0	3 12 44 55 0 0	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
target_i2cREG1_temp.DXR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.HVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DMAC target_i2cREG1_temp.DIR target_i2cREG1_temp.DIR target_i2cREG1_temp.DIR target_i2cREG1_temp.DIR target_i2cREG1_temp.DUT target_i2cREG1_temp.DDUT target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16	78 495 66 0 78 56 78 0 0 0 1 0 0 1 0 0 Actual Value 3 12 44 55 0 0 0 0 495	3 12 44 55 0 0 0 495	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.DXR  target_i2cREG1_temp.DXR  target_i2cREG1_temp.MDR  target_i2cREG1_temp.HVR  target_i2cREG1_temp.EMDR  target_i2cREG1_temp.PSC  target_i2cREG1_temp.PID11  target_i2cREG1_temp.PID12  target_i2cREG1_temp.DMAC  target_i2cREG1_temp.DIN  target_i2cREG1_temp.DIR  target_i2cREG1_temp.DIR  target_i2cREG1_temp.DIN  target_i2cREG1_temp.DOUT  target_i2cREG1_temp.DDR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.PD  target_i2cREG1_temp.PD  target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CndFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08	78 495 66 0 78 56 78 0 0 0 1 0 0 1 0 0 Actual Value 3 12 44 55 0 0 0 0 495 51	3 12 44 55 0 0 0 495 51	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.DXR  target_i2cREG1_temp.DXR  target_i2cREG1_temp.MDR  target_i2cREG1_temp.BMDR  target_i2cREG1_temp.EMDR  target_i2cREG1_temp.PSC  target_i2cREG1_temp.PID11  target_i2cREG1_temp.PID12  target_i2cREG1_temp.DMAC  target_i2cREG1_temp.DIN  target_i2cREG1_temp.DIR  target_i2cREG1_temp.DIR  target_i2cREG1_temp.DIN  target_i2cREG1_temp.DOUT  target_i2cREG1_temp.DDR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.PD  target_i2cREG1_temp.PD  target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_enum	78 495 66 0 78 56 78 0 0 0 0 1 0 0 1 0 0 <b>Actual Value</b> 3 12 44 55 0 0 0 0 495 51 INIT_SENSOR1_EXTREADCTRLREG_SET	3 12 44 55 0 0 0 495 51 INIT_SENSOR1_EXTREADCTRLREG_SET	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.DXR  target_i2cREG1_temp.DXR  target_i2cREG1_temp.MDR  target_i2cREG1_temp.HVR  target_i2cREG1_temp.EMDR  target_i2cREG1_temp.PSC  target_i2cREG1_temp.PID11  target_i2cREG1_temp.PID12  target_i2cREG1_temp.DMAC  target_i2cREG1_temp.DIN  target_i2cREG1_temp.DIN  target_i2cREG1_temp.DIN  target_i2cREG1_temp.DIN  target_i2cREG1_temp.DOUT  target_i2cREG1_temp.DDR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.PDL  target_i2cREG1_temp.PDL  target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CndFailOccurred_Cnt_M_lgc  DigColPsInt_CndFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08	78 495 66 0 78 56 78 0 0 0 0 1 0 0 1 0 0 <b>Actual Value</b> 3 12 44 55 0 0 0 0 495 51 INIT_SENSOR1_EXTREADCTRLREG_SET	3 12 44 55 0 0 0 495 51 INIT_SENSOR1_EXTREADCTRLREG_SET 109	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.DXR  target_i2cREG1_temp.DXR  target_i2cREG1_temp.MDR  target_i2cREG1_temp.IVR  target_i2cREG1_temp.EMDR  target_i2cREG1_temp.PSC  target_i2cREG1_temp.PID11  target_i2cREG1_temp.PID12  target_i2cREG1_temp.DMAC  target_i2cREG1_temp.DIN  target_i2cREG1_temp.DIN  target_i2cREG1_temp.DIN  target_i2cREG1_temp.DIN  target_i2cREG1_temp.DOUT  target_i2cREG1_temp.DOUT  target_i2cREG1_temp.CLR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.PDL  target_i2cREG1_temp.PDL  target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwCustData_UIs_M_u16	78 495 66 0 78 56 78 0 0 0 0 1 0 0 1 0 0 Actual Value 3 12 44 55 0 0 0 0 495 51 INIT_SENSOR1_EXTREADCTRLREG_SET 109 191	3 12 44 55 0 0 0 495 51 INIT_SENSOR1_EXTREADCTRLREG_SET 109 191	· · · · · · · · · · · · · · · · · · ·
target_i2cREG1_temp.DXR  target_i2cREG1_temp.DXR  target_i2cREG1_temp.MDR  target_i2cREG1_temp.HVR  target_i2cREG1_temp.EMDR  target_i2cREG1_temp.PSC  target_i2cREG1_temp.PID11  target_i2cREG1_temp.PID12  target_i2cREG1_temp.DMAC  target_i2cREG1_temp.DIN  target_i2cREG1_temp.DIN  target_i2cREG1_temp.DIN  target_i2cREG1_temp.DIN  target_i2cREG1_temp.DOUT  target_i2cREG1_temp.DDR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.DDR  target_i2cREG1_temp.PDL  target_i2cREG1_temp.PDL  target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_CndFailOccurred_Cnt_M_lgc  DigColPsInt_CndFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08	78 495 66 0 78 56 78 0 0 0 0 1 0 0 1 0 0 <b>Actual Value</b> 3 12 44 55 0 0 0 0 495 51 INIT_SENSOR1_EXTREADCTRLREG_SET	3 12 44 55 0 0 0 495 51 INIT_SENSOR1_EXTREADCTRLREG_SET 109	· · · · · · · · · · · · · · · · · · ·

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Name	Actual Value	Expected Value	Result
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_RecvdDataType_Cnt_M_u08	1	1	<b>✓</b>
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	<b>Y</b>
DigColPsInt_SpurSnsrData_Cnt_M_u16	897	897	<b>~</b>
DigColPsInt_TransactionCnt_Cnt_M_u08	6	6	•
I2c_Send(Length_Cnt_T_u32)	1	1	
l2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR	1 66	1 66	
target I2c GenStopCond I2cRegPtr Cnt T str.IMR	78	78	
target I2c GenStopCond I2cRegPtr Cnt T str.STR	78	78	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	495	495	
target I2c GenStopCond I2cRegPtr Cnt T str.CLKH	56	56	<b>→</b>
target I2c GenStopCond I2cRegPtr Cnt T str.CNT	897	897	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	98	98	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	66	66	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	78	78	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	495	495	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	78	78	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	56	56	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>Y</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>~</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD	0	0	<b>Y</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	0	· ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	78 78	78 78	
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	495	495	
target_12c_Send_12cRegPtr_Cnt_T_str.CLKH	56	56	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	<u> </u>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	
target I2c Send I2cRegPtr Cnt T str.MDR	495	495	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>Y</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>Y</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	66	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	78	<b>~</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	78	78	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495 56	495 56	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	897	897	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	98	98	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66	66	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	78	78	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495	495	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	66	66	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	0	0	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.PSC	78	78	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	56	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78	78	<u> </u>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	0	

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Name	Actual Value	Expected Value	Result
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	0	0	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	0	0	
target I2c SetRecv I2cRegPtr Cnt T str.SET	0	0	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	_
target I2c SetRecv I2cRegPtr Cnt T str.ODR	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	0	0	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	78	78	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	495	495	✓
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	897	897	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	98	98	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	66 78	66 78	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	495	495	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	66	66	
target I2c SetStatus I2cRegPtr Cnt T str.EMDR	0	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	78	78	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	56	56	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	0	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR	0	0	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	0	0	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	1	1	<b>~</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD	0	0	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	· ·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66 78	66 78	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	78	78	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495	495	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKH	56	56	·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897	897	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98	98	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78	78	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495	495	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78	78	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	56	56	<b>~</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	78	78	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	<b>V</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN target_l2c SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	0	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_I_str.DIR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	0	0	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SET	0	0	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	0	0	_
target I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	1	1	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	66	66 0	
target_I2c_SetupMasterTransmit_I2cRegPti_Cnt_T_str.PsC	78	78	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	
	100	100	

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	~

Τ				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	~

Test Step 2.36 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	0
DigColPsInt_Buffer_Cnt_M_u08[0]	0
DigColPsInt_Buffer_Cnt_M_u08[1]	0
DigColPsInt_Buffer_Cnt_M_u08[2]	0
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	0
DigColPsInt_CurrentSlave_Cnt_M_u08	0
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_NOT_INITIALIZED
DigColPsInt_I2CHwCustData_Uls_M_u16	0
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	0
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt SpurCustDatFound Cnt M lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	0
DigColPsInt TransactionCnt Cnt M u08	0
Flags_Cnt_T_b16	1
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target I2c GenStopCond I2cRegPtr Cnt T str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c SetRecv(I2cRegPtr Cnt T str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_12c_SetStatus_12cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
	32
T_DataRegisters_Cnt_u08[1]	30
T_DataRegisters_Cnt_u08[2]	36
T_DataRegisters_Cnt_u08[3]	
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	0
k_SpurSensorI2CAddress_Cnt_u08	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	0

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Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	0
target I2c GenStopCond I2cRegPtr Cnt T str.EMDR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	0
	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
target I2c GenStopCond I2cRegPtr Cnt T str.DIN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0
	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	0
target I2c Send I2cRegPtr Cnt T str.EMDR	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	0
	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	0
target I2c SetRecv I2cRegPtr Cnt T str.IVR	0
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target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	0
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	0
	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	
	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	0

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Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
	0
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0
	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	0
target I2c SetupMasterReceive I2cRegPtr Cnt T str.STR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	0
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	0
target I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	0
	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	0
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
	0
target_i2cREG1_temp.OAR	
target_i2cREG1_temp.IMR	0
target_i2cREG1_temp.STR	0
target_i2cREG1_temp.CLKL	0
target_i2cREG1_temp.CLKH	0
target_i2cREG1_temp.CNT	0

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		( = = 10	<i></i>
Name	Input Value		
target_i2cREG1_temp.DRR	0		
target_i2cREG1_temp.SAR	0		
target_i2cREG1_temp.DXR	0		
target_i2cREG1_temp.MDR	0		
target_i2cREG1_temp.IVR	0		
target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC	0		
target_i2cREG1_temp.PID11	0		
target i2cREG1 temp.PID12	0		
target_i2cREG1_temp.DMAC	0		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	0		
target_i2cREG1_temp.DOUT	0		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	0	0	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	0	0	
DigColPsInt_Buffer_Cnt_M_u08[1]	0	0	
DigColPsInt_Buffer_Cnt_M_u08[2]	0	0	-
DigColPsInt_BusBusySeqError_Cnt_M_Igc	1	1	-
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	-
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	-
DigColPsInt_ColSnsrData_Cnt_M_u16	0	0	•
DigColPsInt_CurrentSlave_Cnt_M_u08	0	0	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE	INIT_COMPLETE	-
DigColPsInt_I2CHwCustData_UIs_M_u16	0	0	•
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	0	0	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc	0	0	
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	-
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	-
DigColPsInt_SpurSnsrData_Cnt_M_u16	0	0	-
DigColPsInt_TransactionCnt_Cnt_M_u08	0	0	-
I2c_SetStatus(Status_Cnt_T_u16)	7	7	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	0	0	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR	0	0	· ·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	0	0 0	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT	0	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	0	0	j
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	0	0	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	0	0	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	0	0	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	0	0	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	0	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	0	0	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	0	0	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0	0	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FUN target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR	0	0	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	0	j
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	0	0	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	0	0	<b>•</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	0	0	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	0	0	· ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	0	0	Ž
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	0	0	-



Name	Actual Value	Expected Value	
Name target I2c Send I2cRegPtr Cnt T str.DXR	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	0	0	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	0	0	<b>*</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11 target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	0	0	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	0	0	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	0	0	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	0	0	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	0	0	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	0	0	<b>Y</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	0	0	Ž
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	0	0	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	0	0	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	0	0	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	0	0	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	0	0	<b>V</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	0	0	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	0	0	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	0	0	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	0	0	<b>*</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	0	0	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	0	0	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	0	0	Ž
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH	0	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	0	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	0	0	<b>*</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC	0	0	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	0	0	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN	0	0	<b>Y</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	0	0	· ·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	~
	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL			_
	0	0	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	0	0	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	0	0	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	0	0	· · ·

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	0	0	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	0	0	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	0	0	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	0	0	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	0	0	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	0	0	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	•

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c_SetStatus	1	l2c_SetStatus	1	~

Test Step 2.37 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	11
DigColPsInt_Buffer_Cnt_M_u08[0]	255
DigColPsInt_Buffer_Cnt_M_u08[1]	255
DigColPsInt_Buffer_Cnt_M_u08[2]	255
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	65535
DigColPsInt_CurrentSlave_Cnt_M_u08	127
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE
DigColPsInt_I2CHwCustData_Uls_M_u16	511
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	255
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1

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Name	Input Value	
DigColPsInt_SpurSnsrData_Cnt_M_u16	65535	
DigColPsInt_TransactionCnt_Cnt_M_u08	255	
Flags_Cnt_T_b16	64	
I2c GenStopCond(I2cRegPtr Cnt T str)	target I2c GenStopCond I2cRegPtr Cnt T str	
I2c Send(I2cRegPtr Cnt T str)	target I2c Send I2cRegPtr Cnt T str	
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str	
I2c SetStatus(I2cRegPtr Cnt T str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str	
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str	
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target I2c SetupMasterTransmit I2cRegPtr Cnt T str	
T_DataRegisters_Cnt_u08[0]	0	
T_DataRegisters_Cnt_u08[1]	32	
T DataRegisters Cnt u08[2]	30	
T_DataRegisters_Cnt_u08[3]	36	
T_DataRegisters_Cnt_u08[4]	38	
T_DataRegisters_Cnt_u08[5]	34	
T_DataRegisters_Cnt_u08[6]	10	
T_DataRegisters_Cnt_u08[7]	12	
T_DataRegisters_Cnt_u08[8]	14	
i2cREG1_temp	target_i2cREG1_temp	
k_ColSensorl2CAddress_Cnt_u08	127	
k_SpurSensorl2CAddress_Cnt_u08	127	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	1023	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	255	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	32767	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	65535	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	65535	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	65535	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	255	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	1023	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	255	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	65535	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	4095	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	255	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	65535	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	255	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	
	3	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD	3	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	255	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	32767	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	65535	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	65535	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	255	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	1023	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	255	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	65535	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	4095	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	255	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	65535	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	255	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	
	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN		
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	1023	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	255	

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Name	Input Value	
arget I2c SetRecv I2cRegPtr Cnt T str.STR	32767	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	65535	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	65535	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	65535	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	255	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	1023	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	255	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	65535	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	4095	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	255	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	65535	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	255	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	1023	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	255	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	32767	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	65535	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	65535	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	65535	
	255	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	1023	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR		
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	255	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	65535	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	4095	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	255	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	65535	
arget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12	255	
arget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	1023	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	255	
arget I2c SetupMasterReceive I2cRegPtr Cnt T str.STR	32767	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	65535	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	65535	
arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CNT	65535	
	255	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	1023	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR		
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	255	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	65535	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	4095	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	255	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	65535	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	255	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	
arget I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	3	
arget I2c SetupMasterReceive I2cRegPtr Cnt T str.SET	3	
arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.Str	3	
"got_120_Octupiniastori\cocive_1201\egr ti_Orit_1_\$ti.OLR	3	
arget 12c SetupMasterPaceive 12cPecPtr Cnt T at CDD		
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3 3	

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Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	1023		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	255		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	32767		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	65535		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	65535		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	65535		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	255		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	1023		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	255		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	65535		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	4095		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	255		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	65535		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	255		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	1		
	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.Din target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DOUT	3		
	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3		
	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL target_i2cREG1_temp.OAR	1023		
	255		
target_i2cREG1_temp.IMR	32767		
target_i2cREG1_temp.STR	65535		
target_i2cREG1_temp.CLKL	65535		
target_i2cREG1_temp.CLKH	65535		
target_i2cREG1_temp.CNT	'''''		
target_i2cREG1_temp.DRR	255		
target_i2cREG1_temp.SAR	1023		
target_i2cREG1_temp.DXR	255		
target_i2cREG1_temp.MDR	65535		
target_i2cREG1_temp.IVR	4095		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	255		
target_i2cREG1_temp.PID11	65535		
target_i2cREG1_temp.PID12	255		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	3		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	3		
target_i2cREG1_temp.ODR	3		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result

target_12cREG1_temp.PSL	ა		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	11	11	✓
DigColPsInt_Buffer_Cnt_M_u08[0]	255	255	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	255	255	✓
DigColPsInt_Buffer_Cnt_M_u08[2]	255	255	<b>✓</b>
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✓
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✓
DigColPsInt_ColSnsrData_Cnt_M_u16	65535	65535	✓
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	✓
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE	READ_COMPLETE	✓
DigColPsInt_I2CHwCustData_Uls_M_u16	511	511	<b>✓</b>
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	255	255	<b>✓</b>
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt_RecvdDataType_Cnt_M_u08	5	5	<b>✓</b>
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt_SpurSnsrData_Cnt_M_u16	65535	65535	<b>✓</b>
DigColPsInt_TransactionCnt_Cnt_M_u08	255	255	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	1023	1023	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	255	255	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	32767	32767	<b>✓</b>

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	65535	65535	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	255	255	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	1023	1023	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	255	255	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	65535	65535	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	4095	4095	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	255	255	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	65535	65535	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	255	255	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD	3	3	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023	1023	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	255	255	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	32767	32767	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	65535	65535	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	255	255	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	1023	1023	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	255	255	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	65535	65535	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	4095	4095	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	255	255	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	65535	65535	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	255	255	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>→</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	<b>→</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	1023	1023	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	255	255	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	32767	32767	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	65535	65535	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	65535	65535	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	255	255	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	1023	1023	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	255	255	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	65535	65535	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	4095	4095	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	255	255	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	65535	65535	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	255	255	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	

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Name	Actual Value	Expected Value	Result
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR	255	255	- Nooule
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	32767	32767	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	65535	65535	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	255	255	j
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	1023	1023	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	255	255	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR	65535	65535	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	4095	4095	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	255	255	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	65535	65535	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	255	255	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>→</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	-
target I2c SetStatus I2cRegPtr Cnt T str.DOUT	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	
	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR			
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	<b>*</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	1023	1023	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	255	255	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	32767	32767	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	-
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKH	65535	65535	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	65535	65535	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	255	255	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	1023	1023	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	255	255	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	65535	65535	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	4095	4095	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	255	255	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	65535	65535	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	255	255	<b>→</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIN	3	3	-
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	3	3	
	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET			
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	1023	1023	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	255	255	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	32767	32767	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	65535	65535	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	65535	65535	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	255	255	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	1023	1023	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	255	255	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	65535	65535	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	4095	4095	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	255	255	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	65535	65535	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	255	255	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	
	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>*</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	
		•	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	_
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	3 3 3	3 3 3	

DigColPsInt\_InterruptNotification

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~

Т				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

DigColPsInt\_InterruptNotification

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Test Case 3: Path Test

DigColPsInt\_InterruptNotification



#### Description

Test Vector Description:

TS3.1(DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum < INIT\_SENSOR2\_READERROR\_SETREG) = TRUE TS3.2"(DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum < INIT\_SENSOR2\_READERROR\_SETREG) = FALSE (DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum < INIT\_COMPLETE) = TRUE"
TS3.3"(DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum < INIT\_SENSOR2\_READERROR\_SETREG) = FALSE (DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum < INIT\_COMPLETE) = FALSE" TS3.4Case: I2C\_AL\_INT;(DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum < INIT\_COMPLETE) = TRUE TS3.5Case: I2C\_AL\_INT;(DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum < INIT\_COMPLETE) = FALSE TS3.6"Case: INIT\_SENSOR1\_CHECKSTAT\_READ; TS3.5Case: IZC\_AL\_IN1;(DIgCoIPsInt\_CurrentStepNo\_Cnt\_M\_ent TS3.6"Case: INIT\_SENSOR1\_CHECKSTAT\_READ;
((DigCoIPsInt\_Buffer\_Cnt\_M\_u08[0] & 0x40U) != 0U) = TRUE &&
(DigCoIPsInt\_InitFailedOnce\_Cnt\_M\_lgc == FALSE) = TRUE"
TS3.7"Case: INIT\_SENSOR1\_CHECKSTAT\_READ;
((DigCoIPsInt\_Buffer\_Cnt\_M\_u08[0] & 0x40U) != 0U) = TRUE &&
(DigCoIPsInt\_InitFailedOnce\_Cnt\_M\_lgc == FALSE) = FALSE"
TS3.8"Case: INIT\_SENSOR1\_CHECKSTAT\_READ;
((DigCoIPsInt\_Buffer\_Cnt\_M\_u08[0] & 0x40U) != 0U) = FALSE &&
(DigCoIPsInt\_InitFailedOnce\_Cnt\_M\_lgc == FALSE) = TRUE"
TS3.9" Case: INIT\_SENSOR2\_CHECKSTAT\_READ
((DigCoIPsInt\_Buffer\_Cnt\_M\_u08[0] & 0x40U) != 0U) = TRUE&&
(DigCoIPsInt\_InitFailedOnce\_Cnt\_M\_lgc == FALSE) = TRUE"
TS3.10" Case: INIT\_SENSOR2\_CHECKSTAT\_READ
((DigCoIPsInt\_Buffer\_Cnt\_M\_u08[0] & 0x40U) != 0U) = TRUE&&
(DigCoIPsInt\_InitFailedOnce\_Cnt\_M\_lgc == FALSE) = FALSE"
TS3.11" Case: INIT\_SENSOR2\_CHECKSTAT\_READ
((DigCoIPsInt\_Buffer\_Cnt\_M\_u08[0] & 0x40U) != 0U) = TRUE&&
(DigCoIPsInt\_InitFailedOnce\_Cnt\_M\_lgc == FALSE) = FALSE"
TS3.11" Case: INIT\_SENSOR2\_CHECKSTAT\_READ
((DigCoIPsInt\_Buffer\_Cnt\_M\_u08[0] & 0x40U) != 0U) = FALSE&&
(DigCoIPsInt\_InitFailedOnce\_Cnt\_M\_lgc == FALSE) = TRUE"
TS3.12"Case: READ\_SENSOR1\_GETDATA;
(DigCoIPsInt\_SkipRegisterWrite\_Cnt\_M\_lgc == TRUE) = TRUE"
TS3.13"Case: READ\_SENSOR1\_GETDATA; TS3.13"Case: READ\_SENSOR1\_GETDATA; TS3.13"Case: READ\_SENSOR1\_GETDATA;
(DigCoIPSInt\_SkipRegisterWrite\_Cnt\_M\_lgc == TRUE) = FALSE"
TS3.14"case l2C\_SCD\_INT;
case INIT\_SENSOR2\_READERROR\_READ:"
TS3.15"case l2C\_SCD\_INT;
case INIT\_SENSOR1\_READERROR\_READ: "
TS3.16"case l2C\_SCD\_INT;
case INIT\_SENSOR1\_READEXTERR\_READ:"
TS3.17"case l2C\_SCD\_INT;
case INIT\_SENSOR2\_READEXTERR\_READ: "
TS3.18"case l2C\_SCD\_INT; TS3.18"case I2C\_SCD\_INT; case READ\_SENSOR2\_GETDATA:" TS3.19"case I2C\_ARDY\_INT; case INIT\_SENSOR1\_READERROR\_SETREG:"
TS3.20"case I2C\_ARDY\_INT;
case INIT\_SENSOR1\_READEXTERR\_SETREG:" TS3.21"case I2C\_ARDY\_INT; case INIT\_SENSOR1\_CHECKSTAT\_SETREG:"TS3.22"case I2C\_ARDY\_INT; case INIT\_SENSOR2\_READERROR\_SETREG:" TS3.23"case I2C\_ARDY\_INT; case INIT\_SENSOR2\_READEXTERR\_SETREG: TS3.24"case I2C\_ARDY\_INT; case INIT\_SENSOR2\_CHECKSTAT\_SETREG:" TS3.25"case I2C\_ARDY\_INT; case READ\_SENSOR1\_SETREG: case READ\_SENSOR1\_SETREG:
TS3.26'case 12C\_ARDY\_INT;
case READ\_SENSOR2\_SETREG:"
TS3.27"case 12C\_ARDY\_INT;
case INIT\_SENSOR1\_SENDCMD:"
TS3.28'case 12C\_ARDY\_INT;
case INIT\_SENSOR2\_SENDCMD:"
TS3.29case INIT\_SENSOR1\_EXTREADCTRLREG\_SENDCMD:
TS3.29case INIT\_SENSOR1\_EXTREADCTRLREG\_SENDCMD: TS3.30case INIT\_SENSOR1\_DUMMY\_SEND: TS3.31case INIT\_SENSOR2\_EXTREADCTRLREG\_SENDCMD: TS3.32case INIT\_SENSOR2\_DUMMY\_SEND: TS3.33"switch (DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum) default: TS3.34"case I2C\_NACK\_INT: (DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum < INIT\_SENSOR2\_READERROR\_SETREG)=False (DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum < INIT\_COMPLETE)=True" TS3.35"case I2C\_NACK\_INT: (DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum < INIT\_SENSOR2\_READERROR\_SETREG)=False
(DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum < INIT\_COMPLETE)=False"
TS3.36case INIT\_SENSOR1\_READERROR\_READ:
TS3.37case INIT\_SENSOR2\_READEXTERR\_READ:
TS3.38case INIT\_SENSOR1\_EXTREADDATREG\_READ:
TS3.39case INIT\_SENSOR2\_EXTREADCTRLREG\_READ:
TS3.39case INIT\_SENSOR2\_EXTREADCTRLREG\_READ: TS3.39"case INIT\_SENSOR2\_EXTREADCTRLREG\_READ:
( DigColPsInt\_AttempOccurForCustDatRead\_Cnt\_M\_u08 > D\_MAXATTEMPTSFORCUSTDATREAD\_CNT\_U08 )=True"
TS3.40"case INIT\_SENSOR1\_EXTREADCTRLREG\_READ:
if( (DigColPsInt\_Buffer\_Cnt\_M\_u08[1] & 0x01U) == 0x01U )=true"
TS3.41"case INIT\_SENSOR2\_CHECKSTAT\_READ:
((DigColPsInt\_Buffer\_Cnt\_M\_u08[0] & 0x40U) != 0U )=False"
TS3.42"case INIT\_SENSOR1\_CHECKSTAT\_READ:
((DigColPsInt\_Buffer\_Cnt\_M\_u08[0] & 0x40U) != 0U )=True"
TS3.43"case INIT\_SENSOR2\_CHECKSTAT\_READ:
(((DigColPsInt\_Buffer\_Cnt\_M\_u08[0] & 0x40U) != 0U) >= True"
TS3.43"case INIT\_SENSOR2\_CHECKSTAT\_READ:
(((DigColPsInt\_Buffer\_Cnt\_M\_u08[0] & 0x40U) != 0U) && ((DigColPsInt\_InitFailedOnce\_Cnt\_M\_lgc == FALSE))=true"
TS3.44case INIT\_SENSOR1\_READERROR\_READ:
TS3.45"switch (((iZcIntFlags)Flags\_Cnt\_T\_b16))
default:" default: TS3.46case INIT SENSOR1 DUMMY READ: TS3.47case INIT\_SENSOR2\_READERROR\_READ:
TS3.48case INIT\_SENSOR2\_DUMMY\_READ:
TS3.49case READ\_SENSOR2\_GETDATA: TS3.50"switch (DigColPsInt\_CurrentStepNo\_Cnt\_M\_enum) default:

TS3.51case INIT SENSOR2 EXTREADDATREG READ:



Test Step 3.1 (Repeat Count = 1)	variable and the second se
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	1
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	9
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
	2309 1204

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Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR	556
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
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DigColPsInt\_InterruptNotification

- ,		
Name	Input Value	
	·	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	
	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	
	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.FUN	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	3	
	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	2309	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	66	
	1204	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	
	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	
target_i2cREG1_temp.OAR	55	
target_i2cREG1_temp.IMR	66	
target_i2cREG1_temp.STR	556	
target i2cREG1 temp.CLKL	2309	
targot_zorteor_tomp.oerte		
toward in-DEOA toward OLIVII		
target_i2cREG1_temp.CLKH	1204	
target_i2cREG1_temp.CLKH target_i2cREG1_temp.CNT		
target_i2cREG1_temp.CNT	1204	
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	1204 87 67	
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR target_i2cREG1_temp.SAR	1204 87 67 55	
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	1204 87 67	
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR target_i2cREG1_temp.SAR	1204 87 67 55	
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR	1204 87 67 55 66 2309	
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR	1204 87 67 55 66 2309 5	
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR	1204 87 67 55 66 2309 5	
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR	1204 87 67 55 66 2309 5	
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR	1204 87 67 55 66 2309 5	
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR target_i2cREG1_temp.DXR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11	1204 87 67 55 66 2309 5 3 66 1204	
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR target_i2cREG1_temp.DXR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12	1204 87 67 55 66 2309 5 3 66 1204 66	
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR target_i2cREG1_temp.DXR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC	1204 87 67 55 66 2309 5 3 66 1204 66 3	
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR target_i2cREG1_temp.DXR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12	1204 87 67 55 66 2309 5 3 66 1204 66	
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR target_i2cREG1_temp.DXR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC	1204 87 67 55 66 2309 5 3 66 1204 66 3	
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR target_i2cREG1_temp.DXR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.HVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR	1204 87 67 55 66 2309 5 3 66 1204 66 3 1	
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR target_i2cREG1_temp.DXR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.HVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DMAC target_i2cREG1_temp.DIR target_i2cREG1_temp.DIR target_i2cREG1_temp.DIR target_i2cREG1_temp.DIR	1204 87 67 55 66 2309 5 3 66 1204 66 3 1	
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR target_i2cREG1_temp.DXR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.EMDR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DMAC target_i2cREG1_temp.DIR target_i2cREG1_temp.DIR target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT	1204 87 67 55 66 2309 5 3 66 1204 66 3 1 1	
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR target_i2cREG1_temp.DXR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.EMDR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIR target_i2cREG1_temp.DIR	1204 87 67 55 66 2309 5 3 66 1204 66 3 1	
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR target_i2cREG1_temp.DXR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.EMDR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DMAC target_i2cREG1_temp.DIR target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET	1204 87 67 55 66 2309 5 3 66 1204 66 3 1 1	
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR target_i2cREG1_temp.DXR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.EMDR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DMAC target_i2cREG1_temp.DIR target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DUT target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR	1204 87 67 55 66 2309 5 3 66 1204 66 3 1 1 2 3 3	
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR target_i2cREG1_temp.DXR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.HVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DMAC target_i2cREG1_temp.DIN target_i2cREG1_temp.DIN target_i2cREG1_temp.DIN target_i2cREG1_temp.DUT target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.CDR	1204 87 67 55 66 2309 5 3 66 1204 66 3 1 1 2 3 3	
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR target_i2cREG1_temp.DXR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.HVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DIR target_i2cREG1_temp.DIR target_i2cREG1_temp.DIR target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR	1204 87 67 55 66 2309 5 3 66 1204 66 3 1 1 2 3 3	
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR target_i2cREG1_temp.DXR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.HVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DMAC target_i2cREG1_temp.DIR target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR	1204 87 67 55 66 2309 5 3 66 1204 66 3 1 1 2 3 3	
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR target_i2cREG1_temp.DXR target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR target_i2cREG1_temp.HVR target_i2cREG1_temp.EMDR target_i2cREG1_temp.PSC target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DIR target_i2cREG1_temp.DIR target_i2cREG1_temp.DIR target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR	1204 87 67 55 66 2309 5 3 66 1204 66 3 1 1 2 3 3 1 1 2 3	sult

 $DigColPsInt\_AttempOccurForCustDatRead\_Cnt\_M\_u08$ 

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Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	•
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	•
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	•
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	•
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	•
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	•
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE	INIT_COMPLETE	
DigColPsInt_I2CHwCustData_UIs_M_u16	1	1	
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	
DigColPsInt_RecvdDataType_Cnt_M_u08	0		
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0 87	0 87	
DigColPsInt_SpurSnsrData_Cnt_M_u16		· ·	
DigColPsInt_TransactionCnt_Cnt_M_u08	10 7	10 7	
I2c_SetStatus(Status_Cnt_T_u16)			
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	
2	1	1 **	

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~

T			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
I2c_SetStatus	1	I2c_SetStatus	1	~

Test Step 3.2 (Repeat Count = 1)	
Name	Input Value
DigColPsInt AttempOccurForCustDatRead Cnt M u08	4
DigColPsInt_Buffer_Cnt_M_u08[0]	28
DigColPsInt_Buffer_Cnt_M_u08[1]	56
DigColPsInt_Buffer_Cnt_M_u08[2]	100
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	7
DigColPsInt_CurrentSlave_Cnt_M_u08	120
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_NOT_INITIALIZED
DigColPsInt_I2CHwCustData_Uls_M_u16	10
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	11
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	4
DigColPsInt_RecvOverrunError_Cnt_M_Igc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	88
DigColPsInt_TransactionCnt_Cnt_M_u08	40
Flags_Cnt_T_b16	2
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	24
k_SpurSensorI2CAddress_Cnt_u08	40

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Name	Input Value
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR	65
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65
	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2
target I2c GenStopCond I2cRegPtr Cnt T str.PSC	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
target I2c GenStopCond I2cRegPtr Cnt T str.SET	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89
target I2c Send I2cRegPtr Cnt T str.STR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
	7
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89
	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target I2c Send I2cRegPtr Cnt T str.CLR	0
	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89
target I2c SetRecv I2cRegPtr Cnt T str.STR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7
	577
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44
	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1

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Name	Input Value
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65
target I2c SetStatus I2cRegPtr Cnt T str.DXR	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target I2c SetStatus I2cRegPtr Cnt T str.SET	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577
	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	88
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	23
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2



arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DD arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL arget_I2cREG1_temp.OAR arget_I2cREG1_temp.DAR arget_I2cREG1_temp.CLKL arget_I2cREG1_temp.CLKH arget_I2cREG1_temp.CLKH arget_I2cREG1_temp.CNT arget_I2cREG1_temp.DNR arget_I2cREG1_temp.DNR arget_I2cREG1_temp.DXR arget_I2cREG1_temp.DXR arget_I2cREG1_temp.MDR arget_I2cREG1_temp.MDR arget_I2cREG1_temp.MDR arget_I2cREG1_temp.MDR arget_I2cREG1_temp.LMDR	Input Value  0  1  2  0  65  89  67  7  577  88  23  65  89		
arget_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.ODR arget_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.PD arget_ 2c_SetupMasterTransmit_ 2cRegPtr_Cnt_T_str.PSL arget_ 2cReG1_temp.OAR arget_ 2cReG1_temp.IMR arget_ 2cReG1_temp.STR arget_ 2cReG1_temp.CLKL arget_ 2cReG1_temp.CLKH arget_ 2cReG1_temp.CNT arget_ 2cReG1_temp.DRR arget_ 2cReG1_temp.DRR arget_ 2cReG1_temp.DXR arget_ 2cReG1_temp.DXR arget_ 2cReG1_temp.DXR arget_ 2cReG1_temp.DXR arget_ 2cReG1_temp.MDR arget_ 2cReG1_temp.MDR arget_ 2cReG1_temp.MDR arget_ 2cReG1_temp.MDR arget_ 2cReG1_temp.MDR	1 2 0 65 89 67 7 577 88 23 65		
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL arget_I2cREG1_temp.OAR arget_I2cREG1_temp.IMR arget_I2cREG1_temp.STR arget_I2cREG1_temp.CLKL arget_I2cREG1_temp.CLKH arget_I2cREG1_temp.CNT arget_I2cREG1_temp.DRR arget_I2cREG1_temp.DRR arget_I2cREG1_temp.DXR arget_I2cREG1_temp.DXR arget_I2cREG1_temp.DXR arget_I2cREG1_temp.DXR arget_I2cREG1_temp.MDR arget_I2cREG1_temp.MDR arget_I2cREG1_temp.MDR arget_I2cREG1_temp.IVR	2 0 65 89 67 7 577 88 23 65		
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL arget_i2cREG1_temp.OAR arget_i2cREG1_temp.IMR arget_i2cREG1_temp.STR arget_i2cREG1_temp.CLKL arget_i2cREG1_temp.CLKH arget_i2cREG1_temp.CNT arget_i2cREG1_temp.DRR arget_i2cREG1_temp.DRR arget_i2cREG1_temp.DXR arget_i2cREG1_temp.DXR arget_i2cREG1_temp.DXR arget_i2cREG1_temp.MDR arget_i2cREG1_temp.MDR arget_i2cREG1_temp.MDR	0 65 89 67 7 577 88 23 65		
arget_i2cREG1_temp.OAR arget_i2cREG1_temp.IMR arget_i2cREG1_temp.STR arget_i2cREG1_temp.CLKL arget_i2cREG1_temp.CLKH arget_i2cREG1_temp.CNT arget_i2cREG1_temp.DRR arget_i2cREG1_temp.DRR arget_i2cREG1_temp.DXR arget_i2cREG1_temp.DXR arget_i2cREG1_temp.DXR arget_i2cREG1_temp.MDR arget_i2cREG1_temp.MDR arget_i2cREG1_temp.MDR	65 89 67 7 577 88 23 65		
arget_i2cREG1_temp.IMR arget_i2cREG1_temp.STR arget_i2cREG1_temp.CLKL arget_i2cREG1_temp.CLKH arget_i2cREG1_temp.CNT arget_i2cREG1_temp.DRR arget_i2cREG1_temp.DRR arget_i2cREG1_temp.DXR arget_i2cREG1_temp.DXR arget_i2cREG1_temp.DXR arget_i2cREG1_temp.MDR arget_i2cREG1_temp.MDR arget_i2cREG1_temp.MDR	89 67 7 577 88 23 65		
arget_i2cREG1_temp.STR arget_i2cREG1_temp.CLKL arget_i2cREG1_temp.CLKH arget_i2cREG1_temp.CNT arget_i2cREG1_temp.DRR arget_i2cREG1_temp.SAR arget_i2cREG1_temp.DXR arget_i2cREG1_temp.DXR arget_i2cREG1_temp.DXR arget_i2cREG1_temp.MDR arget_i2cREG1_temp.MDR	67 7 577 88 23 65		
arget_i2cREG1_temp.CLKL arget_i2cREG1_temp.CLKH arget_i2cREG1_temp.CNT arget_i2cREG1_temp.DRR arget_i2cREG1_temp.SAR arget_i2cREG1_temp.DXR arget_i2cREG1_temp.DXR arget_i2cREG1_temp.MDR arget_i2cREG1_temp.MDR arget_i2cREG1_temp.MDR	7 577 88 23 65		
arget_i2cREG1_temp.CLKH arget_i2cREG1_temp.CNT arget_i2cREG1_temp.DRR arget_i2cREG1_temp.SAR arget_i2cREG1_temp.DXR arget_i2cREG1_temp.DXR arget_i2cREG1_temp.MDR arget_i2cREG1_temp.MDR	577 88 23 65		
arget_i2cREG1_temp.CNT arget_i2cREG1_temp.DRR arget_i2cREG1_temp.SAR arget_i2cREG1_temp.DXR arget_i2cREG1_temp.MDR arget_i2cREG1_temp.MDR arget_i2cREG1_temp.IVR	88 23 65		
arget_i2cREG1_temp.DRR arget_i2cREG1_temp.SAR arget_i2cREG1_temp.DXR arget_i2cREG1_temp.MDR arget_i2cREG1_temp.IVR	23 65		
arget_i2cREG1_temp.SAR arget_i2cREG1_temp.DXR arget_i2cREG1_temp.MDR arget_i2cREG1_temp.IVR	65		
arget_i2cREG1_temp.DXR arget_i2cREG1_temp.MDR arget_i2cREG1_temp.IVR	80		
arget_i2cREG1_temp.IVR	109		
	7		
arget i2cREG1 temp EMDR	44		
arget_izerteor_temp.embrt	2		
arget_i2cREG1_temp.PSC	89		
arget_i2cREG1_temp.PID11	577		
arget_i2cREG1_temp.PID12	89		
arget_i2cREG1_temp.DMAC	2		
arget_i2cREG1_temp.FUN	0		
arget_i2cREG1_temp.DIR	0		
arget_i2cREG1_temp.DIN	1		
arget_i2cREG1_temp.DOUT	2		
arget_i2cREG1_temp.SET	2		
arget_i2cREG1_temp.CLR	0		
arget_i2cREG1_temp.ODR	1 2		
arget_i2cREG1_temp.PD arget_i2cREG1_temp.PSL	0		
		Francis d Value	Danuli
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	
DigColPsInt_Buffer_Cnt_M_u08[1]	56	56	
DigColPsInt_Buffer_Cnt_M_u08[2]	100	100	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	-
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	-
DigColPsInt ColSnsrData Cnt M u16	7	7	•
DigColPsInt_CurrentSlave_Cnt_M_u08	40	40	-
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_SETREG	INIT_SENSOR2_READERROR_SETREG	•
DigColPsInt_I2CHwCustData_Uls_M_u16	10	10	-
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	11	11	-
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	•
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	-
DigColPsInt_RecvOverrunError_Cnt_M_Igc	1	1	~
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	•
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	88	88	•
DigColPsInt_TransactionCnt_Cnt_M_u08	40	40	~
2c_Send(Length_Cnt_T_u32)	1	1	•
2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	•
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65	65	•
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89 67	89 67	<b>*</b>
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	7	7	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH	577	577	-
arget I2c GenStopCond I2cRegPtr Cnt T str.CNT	88	88	j
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23	23	-
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65	65	-
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	89	89	-
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7	7	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44	44	•
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	2	-
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89	89	•
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577	577	~
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89	89	•
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	•
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	0	~
arget_ize_Genotopoond_izertegFit_Ont_i_str.birt		1	
arget_i2c_GenStopCond_i2cRegPtr_Cnt_T_str.DIN	1		
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	-
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN			

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD	0	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	89	89	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	2 89	2 89	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	577	577	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	
target I2c Send I2cRegPtr Cnt T str.DMAC	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	65	65	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	89	89 67	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	67 7	7	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	577	577	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	88	88	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	23	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	65	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89	89	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7	7	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44	44	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89	89	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577	577	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89	89	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	2	2	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65	65	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89	89	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67	67	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7	7	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577	577	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	88	88	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23	23	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65	65	·
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	89	89	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44	44	
target_l2c_SetStatus_l2cRegPti_Cnt_T_str.IVR	2	2	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC	89	89	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11	577	577	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89	89	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	



Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	65	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577	577	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23	23	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65	65	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89	89	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44	44	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89	89	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	89	89	-
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	7	7	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	-
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	577	577	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	0	0	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	-
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	_
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	2	2	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	0	0	~
0	11	1.	

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c_GenStopCond	1	I2c_GenStopCond	1	~
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c Send	1	I2c Send	1	_

Test Step 3.3 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	5
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0



DigColPsInt_InterruptNotification			
Name	Input Value		
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1		
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0		
DigColPsInt_ColSnsrData_Cnt_M_u16	554		
DigColPsInt_CurrentSlave_Cnt_M_u08	5		
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE		
DigColPsInt_I2CHwCustData_Uls_M_u16	13		
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	14		
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0		
DigColPsInt_NackOccured_Cnt_M_lgc	0		
DigColPsInt_PrevReqDataType_Cnt_M_u08	5		
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0		
DigColPsInt_RecvdDataType_Cnt_M_u08	4		
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0		
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0		
DigColPsInt_SpurSnsrData_Cnt_M_u16	123		
DigColPsInt_TransactionCnt_Cnt_M_u08	50		
Flags_Cnt_T_b16			
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str target_I2c_Send_I2cRegPtr_Cnt_T_str		
I2c_Send(I2cRegPtr_Cnt_T_str)	target I2c SetRecv I2cRegPtr Cnt T str		
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_I_str		
I2c_SetStatus(I2cRegPtr_Cnt_T_str) I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	_ · ·		
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str) I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str		
T_DataRegisters_Cnt_u08[0]	target_izc_SetupMaster Hansfillt_izcRegPti_Citt_i_str		
T_DataRegisters_Cnt_u08[1]	32		
T_DataRegisters_Cnt_u08[2]	30		
T_DataRegisters_Cnt_u08[3]	36		
T_DataRegisters_Cnt_u08[4]	38		
T_DataRegisters_Cnt_u08[5]	34		
T_DataRegisters_Cnt_u08[6]	10		
T_DataRegisters_Cnt_u08[7]	12		
T_DataRegisters_Cnt_u08[8]	14		
i2cREG1 temp	target_i2cREG1_temp		
k ColSensorl2CAddress Cnt u08	29		
k_SpurSensorI2CAddress_Cnt_u08	50		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	54		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2		
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54		
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66		
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45		
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66		
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554		
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788		
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66		

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Name	Input Value	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	
	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR		
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554	
	344	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	
	54	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR		
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	123	
target I2c SetStatus I2cRegPtr Cnt T str.DRR	45	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	788	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	
target I2c SetStatus I2cRegPtr Cnt T str.DMAC	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	
	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD		
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788	
0 = - 1		

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Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSC	66		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66		
	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC			
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2		
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	344		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123		
	45		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3		
	2		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2		
target_i2cREG1_temp.OAR	54		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	8		
target_i2cREG1_temp.CLKL	554		
target_i2cREG1_temp.CLKH	344		
target_i2cREG1_temp.CNT	123		
target_i2cREG1_temp.DRR	45		
target_i2cREG1_temp.SAR	54		
target i2cREG1 temp.DXR	66		
target_i2cREG1_temp.MDR	554		
target i2cREG1 temp.IVR	788		
target i2cREG1 temp.EMDR	3		
target_i2cREG1_temp.PSC			
	66		
target_i2cREG1_temp.PID11	66 344		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12	66 344 66		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC	66 344 66 3		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN	66 344 66 3		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR	66 344 66 3 1		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN	66 344 66 3 1 3		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR	66 344 66 3 1		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN	66 344 66 3 1 3		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT	66 344 66 3 1 3 2		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET	66 344 66 3 1 3 2 3 3		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR	66 344 66 3 1 3 2 3 3 3		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR	66 344 66 3 1 3 2 3 3 3		
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.DDR target_i2cREG1_temp.PDL	66 344 66 3 1 3 2 3 3 3 3 2 1 1	Expected Value	Pasult
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.DDR target_i2cREG1_temp.DDR target_i2cREG1_temp.PD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL Name	66 344 66 3 1 3 2 3 3 3 4 4 Actual Value	Expected Value	Result
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL.  Name  DigCoIPsInt_AttempOccurForCustDatRead_Cnt_M_u08	66 344 66 3 1 3 2 3 3 3 2 1 2 Actual Value 5	5	Result
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL.  Name  DigCoIPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigCoIPsInt_Buffer_Cnt_M_u08[0]	66 344 66 3 1 3 2 3 3 3 4 2 1 2 Actual Value 5	5 123	<b>*</b>
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12 target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigCoIPsInt_AttempOccurForCustDatRead_Cnt_M_u08	66 344 66 3 1 3 2 3 3 3 2 1 2 Actual Value 5	5	Result

1

0

554

1

0

554

DigColPsInt\_BusBusySeqError\_Cnt\_M\_lgc DigColPsInt\_CmdFailOccurred\_Cnt\_M\_lgc

DigColPsInt\_ColCustDatFound\_Cnt\_M\_lgc

DigColPsInt\_ColSnsrData\_Cnt\_M\_u16

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Name	Actual Value	Expected Value	Result
DigColPsInt_CurrentSlave_Cnt_M_u08	5	5	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE	READ_COMPLETE	•
DigColPsInt_I2CHwCustData_Uls_M_u16	13	13	•
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	14	14	•
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	•
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	•
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	•
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	
DigColPsInt_SpurSnsrData_Cnt_M_u16	123	123	
DigColPsInt_TransactionCnt_Cnt_M_u08	50 7	50	
I2c_SetStatus(Status_Cnt_T_u16)	54	7 54	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR			
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR	66	66	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR	8	8	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	554	554	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH	344	344	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123	123	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45	45	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	54	54	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR	66	66	Ž
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554	554	- J
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788	788	Ž
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR		3	- J
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66 344	66 344	Ž
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12	66	66	- J
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	Ž
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	2	Ž
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT		3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	Ž
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	Ž
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>→</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	54	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8	8	· ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554	554	· ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	344	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	123	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	45	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	54	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	<u> </u>
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	554	<b>•</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	788	<u> </u>
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344	344	• • • • • • • • • • • • • • • • • • •
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	·
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	<u> </u>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	·
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	2	2	<u> </u>
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	1	1	_
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	2	2	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	54	54	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	66	66	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	8	8	· ·
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554	554	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344	344	<u> </u>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	123	123	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45	45	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54	54	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	<u> </u>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	554	554	<u> </u>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788	788	· · · · · · · · · · · · · · · · · · ·

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Name	Actual Value	Expected Value	Result
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	66	66	· ·
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	344	344	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_i2c_SetRecv_i2cRegPtr_Cnt_T_str.DOUT	3	3	
target_i2c_SetRecv_i2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54	54	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8	8	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554	554	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344	344	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	123	123	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45	45	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54	54	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554	554	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	788	788	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344	344	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	3	3	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN	2	2	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	3	3	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	
target I2c SetStatus I2cRegPtr Cnt T str.PD	1	1	
target I2c SetStatus I2cRegPtr Cnt T str.PSL	2	2	•
target I2c SetupMasterReceive I2cRegPtr Cnt T str.OAR	54	54	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8	8	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554	554	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344	344	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123	123	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45	45	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54	54	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554	554	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788	788	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC	66	66	·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344	344	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	· ·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3 3	3	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_1_str.CLR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	2	2	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	1	1	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	2	2	
target_i2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54	54	
target_i2c_SetupMasterTransmit_i2cRegPtr_Cnt_T_str.UMR	66	66	
target_i2c_SetupMasterTransmit_i2cRegPtr_Cnt_T_str.NrR	8	8	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	554	554	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344	344	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123	123	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45	45	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54	54	
		66	

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554	554	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788	788	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344	344	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c_SetStatus	1	l2c_SetStatus	1	~

Test Step 3.4 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8
DigColPsInt_Buffer_Cnt_M_u08[0]	28
DigColPsInt_Buffer_Cnt_M_u08[1]	56
DigColPsInt_Buffer_Cnt_M_u08[2]	100
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	20
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_READ
DigColPsInt I2CHwCustData Uls M u16	22
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	23
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt PrevReqDataType Cnt M u08	2
DigColPsInt_RecvOverrunError_Cnt_M_Igc	1
DigColPsInt RecvdDataType Cnt M u08	2
DigColPsInt SkipRegisterWrite Cnt M Igc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt SpurSnsrData Cnt M u16	87
DigColPsInt TransactionCnt Cnt M u08	80
Flags Cnt T b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit( 2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T DataRegisters Cnt u08[0]	0
T DataRegisters Cnt u08[1]	32
T_DataRegisters Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
	12
T_DataRegisters_Cnt_u08[7]	14
T_DataRegisters_Cnt_u08[8]	
i2cREG1_temp	target_i2cREG1_temp 44
k_ColSensorl2CAddress_Cnt_u08	
k_SpurSensorI2CAddress_Cnt_u08	127
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR	556
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67

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Name	Input Value
target I2c GenStopCond I2cRegPtr Cnt T str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	55
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	66
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target I2c Send I2cRegPtr Cnt T str.PSL	3
target I2c SetRecv I2cRegPtr Cnt T str.OAR	55
target I2c SetRecv I2cRegPtr Cnt T str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	3
target I2c SetRecv I2cRegPtr Cnt T str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH	1204

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Name	Input Value
	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target I2c SetStatus I2cRegPtr Cnt T str.PID12	66
target I2c SetStatus I2cRegPtr Cnt T str.DMAC	3
	1
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target I2c SetupMasterReceive I2cRegPtr Cnt T str.OAR	55
	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
	3
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	3
	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556



Name	Input Value		
target_i2cREG1_temp.CLKL	2309		
target_i2cREG1_temp.CLKH	1204 87		
target_i2cREG1_temp.CNT target_i2cREG1_temp.DRR	67		
target i2cREG1 temp.SAR	55		
target i2cREG1 temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66 3		
target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN	1		
target i2cREG1 temp.DIR	1		
target i2cREG1 temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8 12	8 12	<i>y</i>
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	56	56	,
DigColPsInt_Buffer_Cnt_M_u08[2]	100	100	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	-
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	~
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	~
DigColPsInt_CurrentStepNo_Cnt_M_enum		INIT_SENSOR2_EXTREADCTRLREG_SET	~
DigColPsInt_I2CHwCustData_Uls_M_u16	22	22	<b>V</b>
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	23	23	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc	1	1	<b>*</b>
DigColPsInt_NackOccured_Crit_M_gc  DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	,
DigColPsInt_RecvdDataType_Cnt_M_u08	2	2	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	~
DigColPsInt_TransactionCnt_Cnt_M_u08	80	80	~
I2c_Send(Length_Cnt_T_u32)	1	1	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66 556	66 556	<b>~</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	2309	2309	,
target I2c GenStopCond I2cRegPtr Cnt T str.CLKH	1204	1204	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR	5	5	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66 1204	66 1204	<b>*</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	V
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55 66	55 66	- V
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	556	556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	·
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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target I2c SetRecv I2cRegPtr Cnt T str.STR	556	556	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID12	66	66	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	3	3	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.FUN	1	1	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIR	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	66	66	<b>v</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	556	556	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	2309	2309	<b>v</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	1204	1204	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	87	87	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	67	67	_
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	55	55	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	66	66	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	2309	2309	_
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	5	5	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	3	3	-
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	1	1	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	1	1	-
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	2	2	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	3	3	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	
	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	-
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD			
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c_Send	1	I2c_Send	1	<b>✓</b>

Test Step 3.5 (Repeat Count = 1)		
Name	Input Value	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	10	
DigColPsInt_Buffer_Cnt_M_u08[0]	0	
DigColPsInt_Buffer_Cnt_M_u08[1]	0	
DigColPsInt_Buffer_Cnt_M_u08[2]	0	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	
DigColPsInt_ColSnsrData_Cnt_M_u16	566	
DigColPsInt_CurrentSlave_Cnt_M_u08	30	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ	
DigColPsInt_I2CHwCustData_Uls_M_u16	28	
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	29	
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1	

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DigColPsint_interruptivotilication	
lame	Input Value
ligColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	4
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
igColPsInt_RecvdDataType_Cnt_M_u08	4
igColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
igColPsInt_SpurCustDatFound_Cnt_M_lgc	1
igColPsInt_SpurSnsrData_Cnt_M_u16	129
igColPsInt_TransactionCnt_Cnt_M_u08	100
lags_Cnt_T_b16	32
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
cc_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
_DataRegisters_Cnt_u08[0]	0
_DataRegisters_Cnt_u08[1]	32
_DataRegisters_Cnt_u08[2]	30
_DataRegisters_Cnt_u08[3]	36
_DataRegisters_Cnt_u08[4]	38
_DataRegisters_Cnt_u08[5]	34
_DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
_DataRegisters_Cnt_u08[8]	14
cREG1_temp	target_i2cREG1_temp
_ColSensorl2CAddress_Cnt_u08	54
_SpurSensorl2CAddress_Cnt_u08	120
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466
rrget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554
	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0
urget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	3
rget_12c_Send_12cRegPtr_Cnt_T_str.OAR	567
	44
rget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
rget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
rget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
rget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
rget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
rget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
rget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
rget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
rget_12c_Send_12cRegPtr_Cnt_T_str.PID12	44
	1
rget I2c Send I2cDegDtr Cat T atr DMAC	
irget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
rget_l2c_Send_l2cRegPtr_Cnt_T_str.FUN rget_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	2
rget_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC  rget_l2c_Send_l2cRegPtr_Cnt_T_str.FUN  rget_l2c_Send_l2cRegPtr_Cnt_T_str.DIR  rget_l2c_Send_l2cRegPtr_Cnt_T_str.DIN  rget_l2c_Send_l2cRegPtr_Cnt_T_str.DUT	

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Name	Input Value
	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
target I2c SetRecv I2cRegPtr Cnt T str.CNT	129
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target I2c SetRecv I2cRegPtr Cnt T str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566
	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0
target I2c SetStatus I2cRegPtr Cnt T str.DOUT	1
target I2c SetStatus I2cRegPtr Cnt T str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target I2c SetupMasterReceive I2cRegPtr Cnt T str.OAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44
target I2c SetupMasterReceive I2cRegPtr Cnt T str.STR	4444
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
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Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	567 44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566 554		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	2		
target_12c_SetupiwasterTransmit_12cRegPtr_Cnt_T_str.ODR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	567		
target_i2cREG1_temp.IMR	44		
target_i2cREG1_temp.STR	4444		
target_i2cREG1_temp.CLKL	566		
target_i2cREG1_temp.CLKH	4466		
target_i2cREG1_temp.CNT	129 6		
target_i2cREG1_temp.DRR target_i2cREG1_temp.SAR	567		
target_i2cREG1_temp.DXR	44		
target_i2cREG1_temp.MDR	566		
target_i2cREG1_temp.IVR	554		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	44		
target_i2cREG1_temp.PID11	4466		
target_i2cREG1_temp.PID12	44		
target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN	1		
target i2cREG1_temp.DIR	2		
target i2cREG1 temp.DIN	0		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3	Form and ad Vol	
Name  DigCalPalat AttampOcaurEarCustDatBoad Cat M u09	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0]	36	10 36	
DigColPsInt Buffer Cnt M u08[1]	0	0	
DigColPsInt_Buffer_Cnt_M_u08[2]	0	0	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	•
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	•
DigColPsInt_ColSnsrData_Cnt_M_u16	566	566	•
DigColPsInt_CurrentSlave_Cnt_M_u08	120	120	•
DigColPoint_I2CHwCustDate_Lile_M_u16	INIT_SENSOR2_READERROR_SETREG	INIT_SENSOR2_READERROR_SETREG	•
DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	28	28 29	
DigColPsint_lzCHwincompleteCustData_Uis_M_u16  DigColPsint_InitFailedOnce_Cnt_M_lgc	0	0	
DigColPsInt NackOccured Cnt M Igc	1	1	
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	•
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	•

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Nama	A stud Value	Fire stad Value	Desuit
Name DigColPsInt_SpurCustDatFound_Cnt_M_lgc	Actual Value	Expected Value	Result
DigColPsInt_SpurSnsrData_Cnt_M_u16	129	129	-
DigColPsInt_TransactionCnt_Cnt_M_u08	100	100	-
I2c_Send(Length_Cnt_T_u32)	1	1	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	567	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	4444	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	44	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11	4466	4466	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	-
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FUN target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR	2	2	
	0	0	-
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT	1	1	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET	1	1	~
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLR	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	¥
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	44	44	-4
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2C_Send_I2cRegPtr_Cnt_T_str.SET	1	1	
target_I2C_Send_I2cRegPtr_Cnt_T_str.SLT  target_I2C_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target I2c SetRecv I2cRegPtr Cnt T str.STR	4444	4444	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	

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target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	0 1 1 2 0 3 3 567	0 1 1 2 0	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR	1 2 0 3 3 3	1 2 0	· ·
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR	2 0 3 3	2 0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	0 3 3	0	• • • • • • • • • • • • • • • • • • •
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR	3		<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR		3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	567	3	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR		567	~
	44	44	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	4444	4444	~
	566	566	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	· ·
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR	129	129 6	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	<i>y</i>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✓
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	· ·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444 566	4444 566	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	4466	4466	•
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CNT	129	129	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	4466	4466	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>✓</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	44	44	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	4444 566	566	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	4466	4466	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	129	129	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	<b>V</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	44	44	· ·

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	•

Т				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>~</b>
I2c_Send	1	l2c_Send	1	~

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	6
DigColPsInt_Buffer_Cnt_M_u08[0]	123
	145
DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	200
	0
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	2767
DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt CurrentSlave Cnt M u08	45
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ
DigColPsInt_I2CHwCustData_UIs_M_u16	37
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	38
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
ligColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_Igc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	564
DigColPsInt_TransactionCnt_Cnt_M_u08	130
Flags_Cnt_T_b16	32
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
_DataRegisters_Cnt_u08[0]	0
CDataRegisters_Cnt_u08[1]	32
Γ_DataRegisters_Cnt_u08[2]	30
_DataRegisters_Cnt_u08[3]	36
Γ_DataRegisters_Cnt_u08[4]	38
_DataRegisters_Cnt_u08[5]	34
_DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
_DataRegisters_Cnt_u08[8]	14
2cREG1_temp	target_i2cREG1_temp
_ColSensorl2CAddress_Cnt_u08	69
SpurSensorl2CAddress_Cnt_u08	123
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	7788
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0

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Name	Input Value	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100	
target I2c GenStopCond I2cRegPtr Cnt T str.PID11	556	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1.	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	
target I2c GenStopCond I2cRegPtr Cnt T str.ODR	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	
target I2c Send I2cRegPtr Cnt T str.CNT	564	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	
target I2c Send I2cRegPtr Cnt T str.SAR	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	
target_12c_Send_12cRegPtr_Cnt_T_str.IVR	9	
target I2c Send I2cRegPtr Cnt T str.EMDR	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	
	100	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	7788	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	2767	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	88	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR	3	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	100	
	2767	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	<u> </u> 2101	

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Name	Input Value
	9
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target I2c SetStatus I2cRegPtr Cnt T str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0
target I2c SetStatus I2cRegPtr Cnt T str.PSL	3
	3
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKH	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	7788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556
	564
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	556
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	3
target_i2cREG1_temp.IMR	100
target i2cREG1 temp.STR	7788
·	
target_i2cREG1_temp.CLKL	2767
target_i2cREG1_temp.CLKH	556
target_i2cREG1_temp.CNT	564
target_i2cREG1_temp.DRR	88
target_i2cREG1_temp.SAR	3



Name	Input Value		
target_i2cREG1_temp.DXR	100		
target_i2cREG1_temp.MDR	2767		
target_i2cREG1_temp.IVR	9		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	100		
target_i2cREG1_temp.PID11	556		
target_i2cREG1_temp.PID12	100		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	3		
target_i2cREG1_temp.DUT	2		
target_i2cREG1_temp.SET	0		
target i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	3		
target i2cREG1 temp.PD	0		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	6	6	result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	-
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	-
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	-
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	-
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	
DigColPsInt_ColSnsrData_Cnt_M_u16	2767	2767	-
DigColPsInt_CurrentSlave_Cnt_M_u08	45	45	
DigColPsInt CurrentStepNo Cnt M enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	•
DigColPsInt_I2CHwCustData_Uls_M_u16	37	37	-
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	38	38	-
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	-
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	•
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	-
DigColPsInt_RecvdDataType_Cnt_M_u08	2	2	•
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	-
DigColPsInt_SpurSnsrData_Cnt_M_u16	564	564	<b>✓</b>
DigColPsInt_TransactionCnt_Cnt_M_u08	130	130	-
I2c_Send(Length_Cnt_T_u32)	1	1	•
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	3	3	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100	100	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	<b> </b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556	556	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564	564	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88	88	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100	100	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767	2767	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9	9	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100	100	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11	556	556	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12	100	100	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FUN	0	0	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR	1	1	-
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN	3	3	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT	2	2	<b>•</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	100	100	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	7788	7788	Ĭ
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	2767	2767	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	556	556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	564	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	88	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	100	
0	1 **	1 **	

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Name	Actual Value	Expected Value	Resul
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	2767	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	9	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	100	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	556	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	,
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100	100	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556	556	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564	564	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88	88	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100	100	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767	2767	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9	9	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	100	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556	556	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100	100	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100	100	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556	556	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564	564	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88	88	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100	100	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2767	2767	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9	9	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100	100	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556	556	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100	100	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100	100	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556	556	
	564	564	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	004		

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3	3	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	100	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	2767	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	9	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	100	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556	556	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	100	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	100	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	556	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	88	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100	100	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767	2767	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	100	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556	556	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	100	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3	3	<b>✓</b>

T				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c_Send	1	I2c_Send	1	~

Test Step 3.7 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8
DigColPsInt_Buffer_Cnt_M_u08[0]	100
DigColPsInt_Buffer_Cnt_M_u08[1]	200
DigColPsInt_Buffer_Cnt_M_u08[2]	250
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	7846
DigColPsInt_CurrentSlave_Cnt_M_u08	10
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	40
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	41
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0

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Digoon onic_interruptivetilieation		
Name	Input Value	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	
DigColPsInt_SpurSnsrData_Cnt_M_u16	98	
DigColPsInt_TransactionCnt_Cnt_M_u08	12	
Flags_Cnt_T_b16	32	
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str	
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str	
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str	
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str	
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str	
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str	
Γ_DataRegisters_Cnt_u08[0]	0	
Γ_DataRegisters_Cnt_u08[1]	32	
「_DataRegisters_Cnt_u08[2]	30	
Γ_DataRegisters_Cnt_u08[3]	36	
	38	
	34	
_DataRegisters_Cnt_u08[6]	10	
_DataRegisters_Cnt_u08[7]	12	
_DataRegisters_Cnt_u08[8]	14	
2cREG1_temp	target_i2cREG1_temp	
_ColSensorl2CAddress_Cnt_u08	74	
_SpurSensorI2CAddress_Cnt_u08	100	
arget I2c GenStopCond I2cRegPtr Cnt T str.OAR	10	
arget I2c GenStopCond I2cRegPtr Cnt T str.IMR	10	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223	
arget   12c GenStopCond   12cRegPtr	7846	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT	98	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7846	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	55	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	10	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	8974	
	10	
rarget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12		
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	
arget I2c GenStopCond I2cRegPtr Cnt T str.PD	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974	
arget I2c Send I2cRegPtr Cnt T str.CNT	98	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	
	10	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10	
argot_120_00tt100v_120t10gFtt_Offt_1_5tt.OAR	IV	

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Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846
	8974
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10
target I2c SetStatus I2cRegPtr Cnt T str.STR	1223
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846
	8974
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	98
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target I2c SetStatus I2cRegPtr Cnt T str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10
target I2c SetupMasterReceive I2cRegPtr Cnt T str.IMR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10
target I2c SetupMasterReceive I2cRegPtr Cnt T str.MDR	7846
target I2c SetupMasterReceive I2cRegPtr Cnt T str.IVR	55
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
	1
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1

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Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1		
target_i2cREG1_temp.OAR	10		
target_i2cREG1_temp.IMR	10		
target_i2cREG1_temp.STR	1223		
target_i2cREG1_temp.CLKL	7846		
target_i2cREG1_temp.CLKH	8974		
target_i2cREG1_temp.CNT	98		
target_i2cREG1_temp.DRR	12		
target_i2cREG1_temp.SAR	10		
target_i2cREG1_temp.DXR	10		
target_i2cREG1_temp.MDR	7846		
target_i2cREG1_temp.IVR	55		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	10		
target_i2cREG1_temp.PID11	8974		
target_i2cREG1_temp.PID12	10		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	2		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	1		
Name	Actual Value	Expected Value	Result

target_I2CREG1_temp.PSL	1		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8	8	~
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	~
DigColPsInt_Buffer_Cnt_M_u08[1]	3	3	~
DigColPsInt_Buffer_Cnt_M_u08[2]	7	7	<b>✓</b>
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	•
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	7846	7846	•
DigColPsInt_CurrentSlave_Cnt_M_u08	74	74	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR1 EXTREADADDRREG SEN	INIT SENSOR1 EXTREADADDRREG SEN	~
DigColPsInt_I2CHwCustData_UIs_M_u16	40	40	~
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	41	41	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	~
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	<b>✓</b>
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	98	98	•
DigColPsInt_TransactionCnt_Cnt_M_u08	12	12	~
I2c_Send(Length_Cnt_T_u32)	3	3	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	~

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10	10	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10	10	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223	1223	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846 8974	7846 8974	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98	98	
target I2c GenStopCond I2cRegPtr_Cnt_T_str.CNT	12	12	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR	10	10	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10	10	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7846	7846	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	55	55	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	10	10	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	8974	8974	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	10	10	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	· ·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD	1	1	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10	10	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	10	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223	1223	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98	98	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10	10	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	10	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846	7846	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55	55	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10	10	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11 target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	8974 10	8974 10	
target_12c_Send_12cRegPtr_Cnt_T_str.DMAC	1	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1	1	
target I2c Send I2cRegPtr Cnt T str.DIR	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target I2c Send I2cRegPtr Cnt T str.DOUT	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10	10	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10	10	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223	1223	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	8974	8974	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	98 12	98	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	10	10	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10	10	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	7846	7846	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10	10	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974	8974	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10	10	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	•
	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN			
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
	1 1 2	1 1 2	

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10	10	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	1223	1223	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	8974 98	8974 98	· ·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	12	12	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR	10	10	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	10	10	
target I2c SetStatus I2cRegPtr Cnt T str.MDR	7846	7846	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	55	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	10	10	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974	8974	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10	10	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1	1	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10	10	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	10	10	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223	1223	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98	98	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12	12	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10	10	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10	10	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846	7846	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55	55	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10	10	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	10	10	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1	1	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10	10	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10	10	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223	1223	<b>v</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98	98	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10	10	<b>v</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10	10	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846	7846	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10	10	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974	8974	<b>*</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>~</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	2	2	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	1	1	<b>~</b>
	1	1	<b>✓</b>

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DigColPsInt_	_InterruptNotification
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Name	Actual Value	Expected Value	Result
Name	Actual value	Expected value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	<b>✓</b>

Τ				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteData	1	SetupWriteData	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c_Send	1	I2c_Send	1	~

Test Step 3.8 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	10
DigColPsInt_Buffer_Cnt_M_u08[0]	1
DigColPsInt_Buffer_Cnt_M_u08[1]	5
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	847
DigColPsInt_CurrentSlave_Cnt_M_u08	20
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_GETDATA
DigColPsInt_I2CHwCustData_Uls_M_u16	43
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	44
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	4
DigColPsInt_RecvOverrunError_Cnt_M_Igc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	487
DigColPsInt_TransactionCnt_Cnt_M_u08	13
Flags_Cnt_T_b16	32
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
Γ_DataRegisters_Cnt_u08[1]	32
Γ_DataRegisters_Cnt_u08[2]	30
Γ_DataRegisters_Cnt_u08[3]	36
Γ_DataRegisters_Cnt_u08[4]	38
Γ_DataRegisters_Cnt_u08[5]	34
Γ_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
Γ_DataRegisters_Cnt_u08[8]	14
2cREG1_temp	target_i2cREG1_temp
COISensorl2CAddress_Cnt_u08	79
_SpurSensorl2CAddress_Cnt_u08	110
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	34
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	24
arget I2c GenStopCond I2cRegPtr Cnt T str.STR	455
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	847
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	987
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	487
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	34
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	34
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	24
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	847
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	56
arget I2c GenStopCond I2cRegPtr Cnt T str.EMDR	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	987
rarget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	24
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC	2
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FUN	0

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lame  strget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR strget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN strget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT	Input Value 3 3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT		
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	
	3	
	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24	
arget I2c Send I2cRegPtr Cnt T str.STR	455	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847	
arget_l2c_send_l2cRegPtr_Cnt_T_str.CLKH	987	
	487	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	
	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	34	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	24	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	455	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	847	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	987	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	487	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	34	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	34	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	24	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	847	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	56	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	
arget I2c SetRecv I2cRegPtr Cnt T str.PSC	24	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	987	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	24	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	34	
arget_12c_SetStatus_12cRegPtr_Cnt_T_str.UMR	24	
arget_l2c_setStatus_l2cRegPtr_Cnt_T_str.fivik	455	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	847	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	987	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	487	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	34	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	34	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	24	
	847	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR		
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	56	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR		
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR		

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Name	Input Value
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3
target I2c SetStatus I2cRegPtr Cnt T str.DIN	3
target I2c SetStatus I2cRegPtr Cnt T str.DOUT	2
	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	847
	987
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSC	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SET	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	487
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	987
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	2
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	2
target_i2cREG1_temp.OAR	34
target_i2cREG1_temp.IMR	24
target_i2cREG1_temp.STR	455
target_i2cREG1_temp.CLKL	847
target_i2cREG1_temp.CLKH	987
target_i2cREG1_temp.CNT	487
target_i2cREG1_temp.DRR	34
target_i2cREG1_temp.SAR	34
target_i2cREG1_temp.DXR	24
	847
target_i2cREG1_temp.MDR	
target_i2cREG1_temp.IVR	56
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	24

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Name	Input Value		
target_i2cREG1_temp.PID11	987		
target_i2cREG1_temp.PID12	24		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	3		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.CLR	3		
target_i2cREG1_temp.ODR	3		
target_i2cREG1_temp.PD	2		
target_i2cREG1_temp.PSL	2		
Name	Actual Value	Expected Value	Result

target_i2cREG1_temp.ODR	3			
target_i2cREG1_temp.PD	2			
target_i2cREG1_temp.PSL	2			
Name	Actual Value	Expected Value	Result	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	10	10	~	
DigColPsInt_Buffer_Cnt_M_u08[0]	38	38	•	
DigColPsInt_Buffer_Cnt_M_u08[1]	5	5	-	
DigColPsInt_Buffer_Cnt_M_u08[2]	9	9	•	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	<b>✓</b>	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	~	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	~	
DigColPsInt_ColSnsrData_Cnt_M_u16	261	261	~	
DigColPsInt_CurrentSlave_Cnt_M_u08	110	110	~	
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_SETREG	READ_SENSOR2_SETREG	~	
DigColPsInt_I2CHwCustData_Uls_M_u16	43	43	~	
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	44	44	~	
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1	1	~	
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~	
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~	
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	~	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	~	
DigColPsInt_SpurSnsrData_Cnt_M_u16	487	487	<b>✓</b>	
DigColPsInt_TransactionCnt_Cnt_M_u08	13	13	~	
I2c_Send(Length_Cnt_T_u32)	1	1	~	
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	34	34	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	24	24	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	455	455	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	847	847	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	987	987	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	487	487	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	34	34	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	34	34	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	24	24	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	847	847	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	56	56	•	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	2	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	24	24	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	987	987	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	24	24	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	3	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	3	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	2	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	~	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR	3	3	~	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD	2	2	~	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	2	~	
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	34	34	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24	24	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455	455	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847	847	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987	987	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487	487	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34	34	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34	34	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24	24	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847	847	~	
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	56	56	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	~	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24	24	<b>✓</b>	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987	987	<b>→</b>	

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Manage	Actual Value	Francisco Value	Daguit
Name	Actual Value	Expected Value 24	Result
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12 target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	2	2	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>*</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	24	34 24	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	455	455	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	847	847	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	987	987	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	487	487	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	34	34	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	34	34	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	24	24	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	847	847	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	56	56	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	24	24	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	987	987	<b>V</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	24	24	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	0	_
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	34	34	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	24	24	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	455	455	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	847	847	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH	987	987	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	34	487 34	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	34	34	-
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	24	24	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	847	847	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	56	56	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	24	24	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	987	987	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	24	24	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN	3	3	<b>V</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	3	2 3	-
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	3	3	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	34	34	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	24	24	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	455	455	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	847	847	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	987	987	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	487	487	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	34	34	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	34	34	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	24	24	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	847	847	<b>*</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	2	56 2	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR			

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	24	24	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	987	987	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	24	24	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34	34	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24	24	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455	455	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847	847	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987	987	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487	487	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34	34	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34	34	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24	24	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847	847	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56	56	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24	24	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987	987	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24	24	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	<b>✓</b>

Τ				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c_Send	1	I2c_Send	1	~

Test Step 3.9 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	30
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_GETDATA
DigColPsInt_I2CHwCustData_Uls_M_u16	46
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	47
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	14
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str

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Name	Input Value
I2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T DataRegisters Cnt u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T DataRegisters Cnt u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target i2cREG1 temp
k ColSensorl2CAddress Cnt u08	84
k_SpurSensorI2CAddress_Cnt_u08	120
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target I2c GenStopCond I2cRegPtr Cnt T str.STR	556
target I2c GenStopCond I2cRegPtr Cnt T str.CLKL	2309
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH	1204
target I2c GenStopCond I2cRegPtr Cnt T str.CNT	87
target_lzc_GenStopCond_lzcRegPtr_Cnt_l_str.Cn1 target_lzc GenStopCond_lzcRegPtr_Cnt_T_str.DRR	67
	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_I_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
	5
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_i2c_Send_i2cRegPtr_Cnt_T_str.PD	3
target_i2c_Send_i2cRegPtr_Cnt_T_str.PSL	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	55
.a.gs25_000.004_1201.0gi ti_Oiit_1_30.07ii\	66
target 12c SetRecy 12cRegPtr Cnt T etr IMP	00
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
	556 2309 1204

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Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target I2c SetRecv I2cRegPtr Cnt T str.SAR	55
· · - · · · · - · · · · · · · · · · · ·	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	66
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target I2c SetStatus I2cRegPtr Cnt T str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target I2c SetStatus I2cRegPtr Cnt T str.CNT	87
target I2c SetStatus I2cRegPtr Cnt T str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR	2309
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target I2c SetupMasterReceive I2cRegPtr Cnt T str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CNT	87
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DRR	67
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	55
	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	556
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	2309
targot_120_Octupinastor transmit_1201/69Fit_Offt_1_Str.OEML	2000

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DigColPsInt_InterruptNotification		Kaz	Ollat
Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	66		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	2309		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	3		
	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	55		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	556		
target_i2cREG1_temp.CLKL	2309		
target_i2cREG1_temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target i2cREG1 temp.EMDR	3		
target i2cREG1 temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target i2cREG1 temp.FUN	1		
target i2cREG1 temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target i2cREG1 temp.SET	3		
target i2cREG1 temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target i2cREG1 temp.PD	3		
target_i2cREG1_temp.PSL	3		
		From a stand Malana	D16
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	•
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	<b>✓</b>
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	2580	2580	~
DigColPsInt_CurrentSlave_Cnt_M_u08	120	120	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_GETDATA	READ_SENSOR2_GETDATA	<b>✓</b>
DigColPsInt_I2CHwCustData_Uls_M_u16	46	46	<b>✓</b>
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	47	47	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	~
DigColPsInt_RecvdDataType_Cnt_M_u08	5	5	~

87

14

2

2

55

66

556

2309

1204

87

14

2

2

55

66

556

2309

1204

I2c\_SetupMasterReceive(DataLength\_Cnt\_T\_u16)

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.OAR

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.IMR$ 

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.STR

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKL$ 

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKH$ 

DigColPsInt\_SpurCustDatFound\_Cnt\_M\_Igc DigColPsInt\_SpurSnsrData\_Cnt\_M\_u16

DigColPsInt\_TransactionCnt\_Cnt\_M\_u08

I2c\_SetRecv(Length\_Cnt\_T\_u32)

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5 3	3	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC	66	66	
target I2c GenStopCond I2cRegPtr Cnt T str.PID11	1204	1204	
target I2c GenStopCond I2cRegPtr Cnt T str.PID12	66	66	
target I2c GenStopCond I2cRegPtr Cnt T str.DMAC	3	3	
target I2c GenStopCond I2cRegPtr Cnt T str.FUN	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	55	55	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	3	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target I2c Send I2cRegPtr Cnt T str.DIR	1	1	•
target I2c Send I2cRegPtr Cnt T str.DIN	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	87	87	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66 1204	66 1204	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	66	66	
target_I2C_SetRecv_I2cRegPtr_Cnt_I_str.PID12 target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2C_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	•

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	I		
Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.CLR	1	1	~
	2	2	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	3	3	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD			
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	~
	3	3	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC			
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	¥
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	~
	66	66	-
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR			-
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	_
0	1	1	



T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	~
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	<b>✓</b>
I2c SetRecv	1	I2c SetRecv	1	<b>✓</b>

Test Step 3.10 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	566
DigColPsInt CurrentSlave Cnt M u08	30
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR2 READEXTERR SETREG
DigColPsInt I2CHwCustData Uls M u16	67
DigColPsInt I2CHwIncompleteCustData Uls M u16	68
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
	4
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	·
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	129
DigColPsInt_TransactionCnt_Cnt_M_u08	100
Flags_Cnt_T_b16	2
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
Γ_DataRegisters_Cnt_u08[0]	0
Γ_DataRegisters_Cnt_u08[1]	32
Γ_DataRegisters_Cnt_u08[2]	30
Γ_DataRegisters_Cnt_u08[3]	36
Γ_DataRegisters_Cnt_u08[4]	38
「_DataRegisters_Cnt_u08[5]	34
「_DataRegisters_Cnt_u08[6]	10
「_DataRegisters_Cnt_u08[7]	12
DataRegisters Cnt u08[8]	14
2cREG1 temp	target i2cREG1 temp
 ColSensorl2CAddress_Cnt_u08	0
 _SpurSensorI2CAddress_Cnt_u08	120
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567
arget I2c GenStopCond I2cRegPtr Cnt T str.IMR	44
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444
arget I2c GenStopCond I2cRegPtr Cnt T str.CLKL	566
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466
arget I2c GenStopCond I2cRegPtr Cnt T str.CNT	129
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6
arget_l2c_GenStopCond_l2cRegPti_Cnt_T_str.DRR arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR	567
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44
arget_l2c_GenStopCond_l2cRegPti_Cnt_T_str.MDR	566
	554
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC	44
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2

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Name	Input Value	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
	567	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR		
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	44	
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	4444	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	129	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	
target I2c Send I2cRegPtr Cnt T str.DOUT	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	
target I2c Send I2cRegPtr Cnt T str.ODR	0	
target I2c Send I2cRegPtr Cnt T str.PD	3	
	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL		
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	567	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	
target I2c SetRecv I2cRegPtr Cnt T str.DMAC	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
target I2c SetRecv I2cRegPtr Cnt T str.DIR	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	
target I2c SetRecv I2cRegPtr Cnt T str.PD	3	
	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL		
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR	567	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR	44	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	
	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	ı'	

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Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
target I2c SetupMasterReceive I2cRegPtr Cnt T str.IMR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIN	0
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	1
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	2
	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target i2cREG1 temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.MDR	566
target i2cREG1 temp.IVR	554
	1
target_i2cREG1_temp.EMDR	
target_i2cREG1_temp.PSC	44
target_i2cREG1_temp.PID11	4466
target_i2cREG1_temp.PID12	44
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target i2cREG1 temp.DIR	2
gozor.zo	1-



3			
Name	Input Value		
target_i2cREG1_temp.DIN	0		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	0		
target i2cREG1 temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3	3	- COUNT
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	•
DigColPsInt_Buffer_Cnt_M_u08[1]	3	3	_
DigColPsInt_Buffer_Cnt_M_u08[2]	7	7	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	-
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	-
DigColPsInt_ColSnsrData_Cnt_M_u16	566	566	~
DigColPsInt_CurrentSlave_Cnt_M_u08	0	0	-
DigColPsInt_CurrentStepNo_Cnt_M_enum		INIT SENSOR1 EXTREADADDRREG SEN	~
DigColPsInt_I2CHwCustData_Uls_M_u16	67	67	-
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	68	68	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	J
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	-
	1	1	J
DigColPoint_RecvOverrunError_Cnt_M_lgc	4	4	~
DigColPoint_RecvdDataType_Cnt_M_u08			Ž
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	
DigColPsInt_SpurSnsrData_Cnt_M_u16	129	129	<b>V</b>
DigColPsInt_TransactionCnt_Cnt_M_u08	100	100	~
I2c_Send(Length_Cnt_T_u32)	3	3	
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	~

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	1	<b>✓</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	0	0	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	3	3	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3	3	-
target I2c SetRecv I2cRegPtr Cnt T str.OAR	567	567	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	V
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0	1	
	1	1	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	0	0	-
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	<i>y</i>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	1	1	-
target_l2c_SetStatus_l2cRegPtr_Cnt_1_str.SE1 target_l2c_SetStatus_l2cRegPtr_Cnt_T str.CLR	2	2	- v
target_lzc_SetStatus_lzcRegPtr_Cnt_1_str.CLR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	0	0	
target I2c SetStatus I2cRegPtr Cnt T str.PD	3	3	4
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL	3	3	9
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	567	567	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	•
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	566	566	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	~
torget 12e CetupMeeterPeeding 12ePeePtr Cnt T etr DVP	44	44	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	566	566	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR			
	554	554	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR		554 1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554		*
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	554 1 44 4466	1 44 4466	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	554 1 44 4466 44	1 44 4466 44	· · · · · · · · · · · · · · · · · · ·
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	554 1 44 4466	1 44 4466	· · · · · · · · · · · · · · · · · · ·

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	<u> </u>

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c_GenStopCond	1	I2c_GenStopCond	1	~
SetupWriteData	1	SetupWriteData	1	<b>✓</b>
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c Send	1	I2c Send	1	<b>✓</b>

Test Step 3.11 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	0
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	2767
DigColPsInt_CurrentSlave_Cnt_M_u08	45
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	76
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	77
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	564
DigColPsInt_TransactionCnt_Cnt_M_u08	130
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str

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Name	Input Value	
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str	
	0	
T_DataRegisters_Cnt_u08[0]	32	
T_DataRegisters_Cnt_u08[1]		
T_DataRegisters_Cnt_u08[2]	30	
T_DataRegisters_Cnt_u08[3]	36	
T_DataRegisters_Cnt_u08[4]	38	
T_DataRegisters_Cnt_u08[5]	34	
T_DataRegisters_Cnt_u08[6]	10	
T_DataRegisters_Cnt_u08[7]	12	
T_DataRegisters_Cnt_u08[8]	14	
i2cREG1_temp	target i2cREG1 temp	
k ColSensorl2CAddress Cnt u08	7	
k_SpurSensorI2CAddress_Cnt_u08	123	
	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	7788	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88	
target I2c GenStopCond I2cRegPtr Cnt T str.SAR	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100	
target I2c GenStopCond I2cRegPtr Cnt T str.MDR	2767	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR	9	
	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	
target I2c Send I2cRegPtr Cnt T str.MDR	2767	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	2	
target_i2c_Send_i2cRegPtr_Cnt_T_str.SET	0	
	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR		
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	556	
	564	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767	

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Name	Input Value
	9
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	0
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788
target I2c SetStatus I2cRegPtr Cnt T str.CLKL	2767
target I2c SetStatus I2cRegPtr Cnt T str.CLKH	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564
target I2c SetStatus I2cRegPtr Cnt T str.DRR	88
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100
target I2c SetStatus I2cRegPtr Cnt T str.MDR	2767
	9
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
	· ·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100
target I2c SetupMasterReceive I2cRegPtr Cnt T str.STR	7788
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	2767
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKH	556
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CNT	564
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DRR	88
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100
target I2c SetupMasterReceive I2cRegPtr Cnt T str.MDR	2767
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_1_str.MDR target_l2c SetupMasterReceive_l2cRegPtr_Cnt_T str.IVR	9
0 = = 1 = 0 = ==	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	2767
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	556
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	564
	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	J. Company of the com

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Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	2		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.SET	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	3		
target_i2cREG1_temp.IMR	100		
target_i2cREG1_temp.STR	7788		
target_i2cREG1_temp.CLKL	2767		
target_i2cREG1_temp.CLKH	556		
target_i2cREG1_temp.CNT	564		
target_i2cREG1_temp.DRR	88		
target_i2cREG1_temp.SAR	3		
target_i2cREG1_temp.DXR	100		
target_i2cREG1_temp.MDR	2767		
target_i2cREG1_temp.IVR	9		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	100		
target_i2cREG1_temp.PID11	556		
target_i2cREG1_temp.PID12	100		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	1 3		
target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.BET	0		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	3		
target i2cREG1 temp.PD	0		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt AttempOccurForCustDatRead Cnt M u08	1	1	-
DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	-
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	-
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	-
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	-
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	-
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	-
DigColPsInt_ColSnsrData_Cnt_M_u16	2767	2767	•
DigColPsInt_CurrentSlave_Cnt_M_u08	7	7	-
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR1 EXTREADCTRLREG SET	INIT SENSOR1 EXTREADCTRLREG SET	•
DigColPsInt_I2CHwCustData_Uls_M_u16	76	76	~
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	77	77	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	<b>✓</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_RecvdDataType_Cnt_M_u08	2	2	•
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	564	564	<b>V</b>
DigColPsInt_TransactionCnt_Cnt_M_u08	130	130	· ·
I2c_Send(Length_Cnt_T_u32)	1	1	· ·
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1 3	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	100	3	Ž
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	7788	7788	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	7788 2767	2767	Ž
target_I2c_GenStopCond_I2cRegPtr_Cnt_I_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556	556	
target_I2c_GenStopCond_I2cRegPti_Cnt_T_str.CNT	564	564	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88	88	-
a.got_i_onotopoona_i_onogra_ont_i_st.Ditt			
target I2c GenStopCond I2cRegPtr Cnt T str.SAR			-
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR	3	3	•

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767	2767	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9	9	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>→</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100	100	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556	556	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12	100	100	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FUN	0	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3 2	3 2	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET	0	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	
target I2c GenStopCond I2cRegPtr Cnt T str.PSL	3	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	100	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	7788	
target_12c_Send_12cRegPtr_Cnt_T_str.CLKL	2767	2767	
target I2c Send I2cRegPtr Cnt T str.CLKH	556	556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	564	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	88	88	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	100	
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	2767	2767	
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	9	9	
target_l2c_Send_l2cRegPtr_Cnt_T_str.FMDR	0	0	
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDK	100	100	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	
target I2c Send I2cRegPtr Cnt T str.FUN	0	0	
target_12c_Send_12cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	
target_12c_Send_12cRegPtr_Cnt_T_str.CLR	1	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.OAR	3	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	100	100	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	7788	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556	556	•
target I2c SetRecv I2cRegPtr Cnt T str.CNT	564	564	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88	88	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	3	3	
target I2c SetRecv I2cRegPtr Cnt T str.DXR	100	100	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	2767	2767	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9	9	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	100	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556	556	
target I2c SetRecv I2cRegPtr Cnt T str.PID12	100	100	
target I2c SetRecv I2cRegPtr Cnt T str.DMAC	2	2	-
target I2c SetRecv I2cRegPtr Cnt T str.FUN	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	-
target I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100	100	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788	7788	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556	556	-
target I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564	564	•

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3	3	ixesuit
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100	100	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2767	2767	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9	9	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100	100	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556	556	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100	100	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100	100	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	7788	7788	•
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	2767	2767	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	556	556	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564	564	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88	88	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	100	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	2767	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	9	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	100	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556	556	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	100	•
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	0	0	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	1	1	•
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	0	-
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	0	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR target_l2c SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	0	0	
	3	3	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.UAR  target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	100	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.NrR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	556	556	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	88	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100	100	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	2767	2767	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	-
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	100	-
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	556	556	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	100	100	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3	3	~



T			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c Send	1	I2c Send	1	<b>✓</b>

Test Step 3.12 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	11
DigColPsInt_Buffer_Cnt_M_u08[0]	100
DigColPsInt_Buffer_Cnt_M_u08[1]	200
DigColPsInt_Buffer_Cnt_M_u08[2]	250
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	7846
DigColPsInt_CurrentSlave_Cnt_M_u08	10
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	79
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	80
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPoint_SpurCustDatFound_Cnt_M_lgc	
DigColPsInt_SpurSnsrData_Cnt_M_u16	98
DigColPsInt_TransactionCnt_Cnt_M_u08 Flags Cnt T b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target I2c Send I2cRegPtr Cnt T str
I2c SetRecv(I2cRegPtr Cnt T str)	target I2c SetRecv I2cRegPtr Cnt T str
I2c SetStatus(I2cRegPtr Cnt T str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T DataRegisters Cnt u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	11
k_SpurSensorI2CAddress_Cnt_u08	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR	7846 55
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR	1
target I2c GenStopCond_I2cRegPtr_Cnt_1_str.EMDR	10
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11	8974
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12	10
target I2c GenStopCond I2cRegPtr Cnt T str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2
0	

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Name	Input Value	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	10	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974	
arget I2c Send I2cRegPtr Cnt T str.CNT	98	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	
arget I2c Send I2cRegPtr Cnt T str.SAR	10	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846	
	55	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	10	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	8974	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	55	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	
arget I2c SetRecv I2cRegPtr Cnt T str.PSC	10	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974	
arget I2c SetRecv I2cRegPtr Cnt T str.PID12	10	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	
arget I2c SetRecv I2cRegPtr Cnt T str.FUN	1	
arget I2c SetRecv I2cRegPtr Cnt T str.DIR	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	10	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	1223	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	8974	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	98	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	10	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	10	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7846	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	55	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	10	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10	
	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN		
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	

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Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	8974
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
	1
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1
	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98
	12
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	55
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	1
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	10
	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	1
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	1
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1
target_i2cREG1_temp.OAR	10
target_i2cREG1_temp.IMR	10
target_i2cREG1_temp.STR	1223
target_i2cREG1_temp.CLKL	7846
target_i2cREG1_temp.CLKH	8974
target_i2cREG1_temp.CNT	98
target_i2cREG1_temp.DRR	12
target_i2cREG1_temp.SAR	10
target_i2cREG1_temp.DXR	10
target_i2cREG1_temp.MDR	7846
target_i2cREG1_temp.IVR	55
target_i2cREG1_temp.EMDR	1
target i2cREG1 temp.PSC	10
	8974
target_i2cREG1_temp.PID11	
target_i2cREG1_temp.PID12	10
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
	·

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Name	Input Value		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	1		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	12	12	- TOO LITE
DigColPsInt_Buffer_Cnt_M_u08[0]	14	14	•
DigColPsInt_Buffer_Cnt_M_u08[1]	200	200	
DigColPsInt_Buffer_Cnt_M_u08[2]	250	250	~
DigColPsInt BusBusySeqError Cnt M Igc	1	1	
	1	1	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc			
DigColPsInt_ColCustDatFound_Cnt_M_Igc	1	1	
DigColPsInt_ColSnsrData_Cnt_M_u16	7846	7846	~
DigColPsInt_CurrentSlave_Cnt_M_u08	11	11	~
DigColPsInt_CurrentStepNo_Cnt_M_enum		INIT SENSOR1 EXTREADDATREG SETR	~
DigColPsInt_I2CHwCustData_Uls_M_u16	79	79	~
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	80	80	<b>✓</b>
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	~
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	~
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	98	98	~
DigColPsInt_TransactionCnt_Cnt_M_u08	12	12	~
I2c_Send(Length_Cnt_T_u32)	1	1	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223	1223	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98	98	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12	12	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7846	7846	~
target I2c GenStopCond I2cRegPtr Cnt T str.IVR	55	55	~
target I2c GenStopCond I2cRegPtr Cnt T str.EMDR	1	1	_
target I2c GenStopCond I2cRegPtr Cnt T str.PSC	10	10	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	8974	8974	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	-
target 12c GenStopCond 12cRegPtr Cnt T str.ODR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	1	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1	1	~
	10	10	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	10	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223	1223	
	7846	7846	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL			
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98	98	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10	10	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	10	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846	7846	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55	55	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974	8974	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~



Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1 2	2	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	1	1	
target_12c_Send_12cRegPtr_Cnt_T_str.PD	1	1	~
target I2c Send I2cRegPtr Cnt T str.PSL	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10	10	<b>✓</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	10	10	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223	1223	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	7846	7846	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	98	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10	10	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10	10	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846	7846	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55	55	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10	10	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974	8974	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10	10	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	-4
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10	10	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	1223	1223	<b>*</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846 8974	7846 8974	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	98	98	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12	12	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	10	10	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	10	10	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7846	7846	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	55	55	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC	10	10	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974	8974	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC	10	10	-
target_12c_SetStatus_12cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target I2c SetStatus I2cRegPtr Cnt T str.DIN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	1	1	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	1223	1223	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98	98	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12	12	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10	10	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	10	10	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	7846	7846	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	55	55	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10	10	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	8974 10	8974 10	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.Pib12	1	1	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1	1	~
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Name	Actual Value	Expected Value	Result
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223	1223	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98	98	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10	10	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846	7846	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974	8974	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	~

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Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c_Send	1	I2c_Send	1	-

Test Step 3.13 (Repeat Count = 1)	<u>√</u>
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str

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Name	Input Value	
T_DataRegisters_Cnt_u08[0]	0	
T_DataRegisters_Cnt_u08[1]	32	
T_DataRegisters_Cnt_u08[2]	30	
T_DataRegisters_Cnt_u08[3]	36	
T_DataRegisters_Cnt_u08[4]	38	
T_DataRegisters_Cnt_u08[5]	34	
T_DataRegisters_Cnt_u08[6]	10	
T_DataRegisters_Cnt_u08[7]	12	
T_DataRegisters_Cnt_u08[8]	14	
i2cREG1_temp	target_i2cREG1_temp	
k_ColSensorl2CAddress_Cnt_u08	9	
k_SpurSensorI2CAddress_Cnt_u08	10	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	
	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
target_i2c_Send_i2cRegPtr_Cnt_T_str.DIN	2	
target_i2c_send_i2cRegPti_Cnt_1_str.Din target_i2c_send_i2cRegPtr_Cnt_T_str.DOUT	3	
	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR		
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	
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Name	Input Value
	·
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target I2c SetRecv I2cRegPtr Cnt T str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target I2c SetRecv I2cRegPtr Cnt T str.DIR	1
· · ·	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target I2c SetRecv I2cRegPtr Cnt T str.PD	3
· · ·	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
	1204
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target I2c SetStatus I2cRegPtr Cnt T str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
	2
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target I2c SetupMasterReceive I2cRegPtr Cnt T str.STR	556
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target I2c SetupMasterReceive I2cRegPtr Cnt T str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	3
target I2c SetupMasterReceive I2cReqPtr Cnt T str.FUN	1
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	66
5	

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Name	Input Value		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	2309		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	55		
target i2cREG1 temp.IMR	66		
target i2cREG1 temp.STR	556		
target_i2cREG1_temp.CLKL	2309		
target_i2cREG1_temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2 3		
target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target i2cREG1 temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt AttempOccurForCustDatRead Cnt M u08	1	1	
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	~
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	•
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	~
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ	INIT_SENSOR1_READERROR_READ	~
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	~
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	2	2	<b>V</b>
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	•
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	<b>Y</b>
DigColPsInt_RecvOverrunError_Cnt_M_Igc	0	0	<b>V</b>
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	<b>*</b>
DigColPsInt_SpurCustDatFound_Cnt_M_lgc			
DigColPsInt_SpurSnsrData_Cnt_M_u16	87 10	87 10	
DigColPsInt_TransactionCnt_Cnt_M_u08 target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2C_GenStopCond_I2cRegPtr_Cnt_I_str.UAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.NRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FUN	1	1	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD	3	3	
target I2c GenStopCond I2cRegPtr Cnt T str.PSL	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target I2c Send I2cRegPtr Cnt T str.CNT	87	87	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target I2c Send I2cRegPtr Cnt T str.DXR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target I2c Send I2cRegPtr Cnt T str.IVR	5	5	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	-

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL	3	3	•
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	55	55	<b>Y</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	556	556	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	-
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	67	67	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	66	66	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	66	66	-
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	1204	1204	
	66	66	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	87	87	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	~
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	<b>✓</b>
I2c SetRecv	1	I2c SetRecv	1	<b>✓</b>



Test Step 3.14 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0 1
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	87
DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt TransactionCnt Cnt M u08	10
DigColPsint_TransactionCnt_Cnt_M_u08 Flags_Cnt_T_b16	4
Flags_Cnt_1_b16   I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str
I2C_GensiopCond(I2CRegPti_Cni_1_str) I2C_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Genstopcond_l2cRegPtr_Cnt_T_str
I2C_Seria(I2CRegPtr_Crit_1_str)  I2C SetRecv(I2cRegPtr_Crit_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target i2cREG1 temp
k_ColSensorl2CAddress_Cnt_u08	9
k SpurSensorI2CAddress Cnt u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204

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		.0
Name	Input Value	
	87	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT		
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	556	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	
target I2c SetRecv I2cRegPtr Cnt T str.DRR	67	
target I2c SetRecv I2cRegPtr Cnt T str.SAR	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	
target I2c SetRecv I2cRegPtr Cnt T str.PSL	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	
	87	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT		
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	
	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	

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Name	Input Value
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66

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Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	~
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	~
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	~
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	~
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	<b>~</b>
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_READ	INIT_SENSOR1_READEXTERR_READ	~
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	~
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	<b>~</b>
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	<b>V</b>
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	<b>V</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	<b>V</b>
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	~
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR	556	556	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR	67	67	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	67	67	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	1	1	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	2	2	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>*</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>*</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55 66	55 66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	2309	2309	J
target _l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR target l2c SetRecv l2cRegPtr Cnt T str.IVR	5	5	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	J
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	,
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	_
target I2c SetRecv I2cRegPtr Cnt T str.FUN	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>V</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	87	87	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55 66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	3	5 3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	66	3 66	-
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSC target_l2c SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	1204	1204	-
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_I_str.PID11 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	66	1204 66	-
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	3	3	_
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1	1	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	2	2	J
target_lzc_SetupMasterReceive_lzcRegPtr_Cnt_I_str.DliN target_l2c_SetupMasterReceive_lzcRegPtr_Cnt_T_str.DOUT	3	3	-
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_I_str.DOUT target_l2c SetupMasterReceive_l2cRegPtr_Cnt_T str.SET	3	3	-
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	1	1	_
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	2	2	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DDR	3	3	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	_
goroctuprinactor francinit_izortogr ti_ont_i_ott.OAIt	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	l nn		



Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~

T .			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	~
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	•
I2c_SetRecv	1	I2c_SetRecv	1	<b>~</b>

Test Step 3.15 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt Buffer Cnt M u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt Buffer Cnt M u08[2]	30
DigColPsInt BusBusySeqError Cnt M Igc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp

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Name	Input Value
k ColSensorl2CAddress Cnt u08	9
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target I2c Send I2cRegPtr Cnt T str.DIR	1
	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target I2c Send I2cRegPtr Cnt T str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
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Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	3
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSL	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
targot_120_octupmiaator rransmit_1201/egr ti_Ont_1_50.OLNL	2000
t	1004
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	1204 87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	87 67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	87 67 55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	87 67 55 66
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	87 67 55 66 2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	87 67 55 66
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	87 67 55 66 2309
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	87 67 55 66 2309 5
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	87 67 55 66 2309 5 3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	87 67 55 66 2309 5 3 66
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	87 67 55 66 2309 5 3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	87 67 55 66 2309 5 3 66
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	87 67 55 66 2309 5 3 66 1204 66
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	87 67 55 66 2309 5 3 66 1204 66 3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	87 67 55 66 2309 5 3 66 1204 66

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Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	55		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	556		
target_i2cREG1_temp.CLKL	2309		
target_i2cREG1_temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Namo	Actual Value	Expected Value	Pocul

target i3aPEC1 temp PSI	3		
target_i2cREG1_temp.PSL		Function Value	Desult
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	10	10	
DigColPsInt_Buffer_Cnt_M_u08[0]	20	20	
DigColPsInt_Buffer_Cnt_M_u08[1]			
DigColPsInt_Buffer_Cnt_M_u08[2]	0	0	
DigColPsInt_BusBusySeqError_Cnt_M_lgc			
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	~
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	-
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ	INIT_SENSOR1_CHECKSTAT_READ	~
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	~
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	2	2	<b>Y</b>
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	<b>~</b>
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	~
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	~

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	· ·
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	3 55	3 55	
target I2c Send I2cRegPtr Cnt T str.IMR	66	66	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	55	55	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	· ·
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	2309	2309	Ž
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>•</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	Ž
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	2	2	
target I2c Send I2cRegPtr Cnt T str.PD	3	3	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	87	87	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	67	67	<b>V</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	55 66	55 66	· · · · · · · · · · · · · · · · · · ·
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	1	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	2	2	· ·
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	3 3	3	<i>y</i>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>V</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR	55	55	· ·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66 2309	66 2309	<i>y</i>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✓

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~

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Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	~
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	<b>✓</b>
I2c SotDocy	1	I2c SotPocy	1	

Test Step 3.16 (Repeat Count = 1)		<b>✓</b>
Name	Input Value	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	
DigColPsInt_Buffer_Cnt_M_u08[0]	10	
DigColPsInt_Buffer_Cnt_M_u08[1]	20	
DigColPsInt_Buffer_Cnt_M_u08[2]	30	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	

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DigColPsini_interruptivotilication	TOLO (M
Name	Input Value
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt RecvOverrunError Cnt M Igc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt SkipRegisterWrite Cnt M Igc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
lags_Cnt_T_b16	4
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target I2c Send I2cRegPtr Cnt T str
	• •
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
tc_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
_DataRegisters_Cnt_u08[0]	0
_DataRegisters_Cnt_u08[1]	32
_DataRegisters_Cnt_u08[2]	30
_DataRegisters_Cnt_u08[3]	36
_DataRegisters_Cnt_u08[4]	38
_DataRegisters_Cnt_u08[5]	34
_DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
_DataRegisters_Cnt_u08[8]	14
2cREG1_temp	target_i2cREG1_temp
ColSensorl2CAddress_Cnt_u08	9
SpurSensorI2CAddress Cnt u08	10
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	2309
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
	2
urget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
irget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
rget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
rget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
rget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
irget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
rget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
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irget 12c Send 12cRegPtr Cnt T str CNT	87
	87 67
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	67 55
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	67 55 66
rrget_l2c_Send_l2cRegPtr_Cnt_T_str.DRR rrget_l2c_Send_l2cRegPtr_Cnt_T_str.SAR rrget_l2c_Send_l2cRegPtr_Cnt_T_str.DXR rrget_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	67 55 66 2309
orget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR orget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR orget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR orget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	67 55 66 2309 5
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	67 55 66 2309
arget_l2c_Send_l2cRegPtr_Cnt_T_str.CNT arget_l2c_Send_l2cRegPtr_Cnt_T_str.DRR arget_l2c_Send_l2cRegPtr_Cnt_T_str.SAR arget_l2c_Send_l2cRegPtr_Cnt_T_str.DXR arget_l2c_Send_l2cRegPtr_Cnt_T_str.MDR arget_l2c_Send_l2cRegPtr_Cnt_T_str.IVR arget_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR arget_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR arget_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR arget_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	67 55 66 2309 5

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Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target I2c Send I2cRegPtr Cnt T str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target I2c Send I2cRegPtr Cnt T str.DIN	2
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target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	3
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target I2c SetRecv I2cRegPtr Cnt T str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target I2c SetRecv I2cRegPtr Cnt T str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target I2c SetRecv I2cRegPtr Cnt T str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target I2c SetStatus I2cRegPtr Cnt T str.PID12	66
target I2c SetStatus I2cRegPtr Cnt T str.DMAC	3
target I2c SetStatus I2cRegPtr Cnt T str.FUN	1
	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
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DigColPsInt\_InterruptNotification

Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55 66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3 3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL target_i2cREG1_temp.OAR	55		
target_i2cREG1_temp.IMR	66		
target i2cREG1 temp.STR	556		
target i2cREG1 temp.CLKL	2309		
target i2cREG1 temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DUT	3		
target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET	3		
target i2cREG1_temp.SE1 target i2cREG1 temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt AttempOccurForCustDatRead Cnt M u08	1	1	Kesult
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	_
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	<b>✓</b>
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	<b>✓</b>

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DigColPsInt\_CmdFailOccurred\_Cnt\_M\_lgc DigColPsInt\_ColCustDatFound\_Cnt\_M\_lgc

DigColPsInt\_ColSnsrData\_Cnt\_M\_u16

 $DigColPsInt\_CurrentSlave\_Cnt\_M\_u08$ 

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Name	Actual Value	Expected Value	Resul
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_READ	INIT_SENSOR2_READERROR_READ	•
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	•
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	•
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	•
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	•
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	-
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	-
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	•
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	٠,
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR	55	55	
target I2c GenStopCond I2cRegPtr Cnt T str.DXR	66	66	
· · - ·	2309	2309	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR			
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target I2c Send I2cRegPtr Cnt T str.CLKH	1204	1204	
target_i2c_Send_i2cRegPtr_Cnt_T_str.CNT	87	87	
target I2c Send I2cRegPtr Cnt T str.DRR	67	67	
	55	55	
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	66	66	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR			
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	j
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	•
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	
target_12c_Send_12cRegPtr_Cnt_T_str.PSL	3	3	j
target_l2c_SerRecv_l2cRegPtr_Cnt_T_str.OAR	55	55	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	66	66	
	556	556	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR			
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	•
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	-
<del></del>	66	66	-

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	3 3	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	
target I2c SetStatus I2cRegPtr Cnt T str.CLKL	2309	2309	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	66	66	-
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	<u> </u>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	_
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKH	1204	1204	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>→</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	2	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	55	55	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.NrR	556	556	
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL	2309	2309	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	1204	1204	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	-
	2309	2309	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309		

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3	3	~

Τ				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	~
I2c_SetupMasterReceive	1	l2c_SetupMasterReceive	1	~
I2c_SetRecv	1	I2c_SetRecv	1	~

Test Step 3.17 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt Buffer Cnt M u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt BusBusySeqError Cnt M Igc	0
DigColPsInt CmdFailOccurred Cnt M Igc	1
DigColPsInt ColCustDatFound Cnt M Igc	1
DigColPsInt ColSnsrData Cnt M u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt CurrentStepNo Cnt M enum	INIT SENSOR2 READEXTERR SETREG
DigColPsInt I2CHwCustData Uls M u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt InitFailedOnce Cnt M Igc	0
DigColPsInt NackOccured Cnt M Igc	0
DigColPsInt_NackOccured_Cnt_M_igc  DigColPsInt PrevReqDataType Cnt M u08	1
DigColPsInt_PrevReqDataType_Cnt_M_u006  DigColPsInt RecvOverrunError Cnt M Igc	0
	0
DigColPsInt_RecvdDataType_Cnt_M_u08 DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	9
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67

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Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2 3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204

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Name	Input Value
	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target I2c SetStatus I2cRegPtr Cnt T str.PID12	66
target I2c SetStatus I2cRegPtr Cnt T str.DMAC	3
	1
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target I2c SetupMasterReceive I2cRegPtr Cnt T str.OAR	55
	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DRR	67
<u> </u>	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
	3
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	3
	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556

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Name	Input Value		
target_i2cREG1_temp.CLKL	2309		
target_i2cREG1_temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✓
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	<b>✓</b>
DigColPsInt_BusBusySeqError_Cnt_M_Igc	0	0	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✓
DigColPsInt_ColCustDatFound_Cnt_M_Igc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	<b>✓</b>
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READEXTERR_READ	INIT_SENSOR2_READEXTERR_READ	✓
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	~
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	2	2	✓
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✓
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target I2c Send I2cRegPtr Cnt T str.EMDR	3	3	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	~
target I2c Send I2cRegPtr Cnt T str.PSL	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target I2c SetRecv I2cRegPtr Cnt T str.IMR	66	66	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	-
target_12c_SetRecv_12cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	
	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	2309	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	5	5	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	66	66	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC		1204	J
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204 66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	3	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	2	2	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	3	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET			J
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	1	1	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	2	2	Ž
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR	66	66	<b>~</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>~</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	87	87	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	· ·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	556	556	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	3	3	_
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3	3	_

T			V	
Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	~
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	<b>✓</b>
I2c_SetRecv	1	I2c_SetRecv	1	<b>✓</b>

Test Step 3.18 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1

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Name	Input Value
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	9
k_SpurSensorl2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target I2c GenStopCond I2cRegPtr Cnt T str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target I2c GenStopCond I2cRegPtr Cnt T str.PSL	3
target I2c Send I2cRegPtr Cnt T str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
gotbo_oond_nbortogr d_Ont_1_btt.Obit	

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Name	Input Value	
	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	
	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	
target I2c SetRecv I2cRegPtr Cnt T str.MDR	2309	
· ·	5	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	
	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	
	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12		
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	
target I2c SetStatus I2cRegPtr Cnt T str.DIN	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	
target I2c SetStatus I2cRegPtr Cnt T str.SET	3	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.OAR	55	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	3	

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Name target 12c SetupMacterPeccine 12cPeqPtr Cnt T etr CLP	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	1204 87		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	67		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC	66   1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	55		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	556		
target_i2cREG1_temp.CLKL	2309		
target_i2cREG1_temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55 66		
target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target i2cREG1 temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1 10	1 10	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt Buffer Cnt M u08[1]	20	20	
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	-
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	~
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_READ	INIT_SENSOR2_CHECKSTAT_READ	~
DigColPoint_I2CHwinoomplotoCustPoto_UI0 M_u16	1 2	2	<b>✓</b>
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	
DigColPsInt_InteralledOrtce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc	0	0	-
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	-
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	•
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	•
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	~

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Name	Actual Value	Expected Value	Result
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66		

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Name	Actual Value	Expected Value	Resul
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3 3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	
target I2c SetStatus I2cRegPtr Cnt T str.IMR	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3 3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET			
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	2	1 2	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR target_l2c SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	3	3	
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PSL	3	3	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	55	55	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	556	556	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	87	87	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	67	67	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	

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DigCoIPsInt_InterruptNotification
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Name	Actual Value	Expected Value	Result
Hame	Actual Value	Expected value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3	3	<b>✓</b>

T				V
Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	~
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	-
I2c_SetRecv	1	I2c_SetRecv	1	~

Fest Step 3.19 (Repeat Count = 1)	Input Value
	·
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_Igc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_Igc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
「_DataRegisters_Cnt_u08[0]	0
Γ_DataRegisters_Cnt_u08[1]	32
「_DataRegisters_Cnt_u08[2]	30
「_DataRegisters_Cnt_u08[3]	36
Γ_DataRegisters_Cnt_u08[4]	38
Γ_DataRegisters_Cnt_u08[5]	34
「_DataRegisters_Cnt_u08[6]	10
Γ_DataRegisters_Cnt_u08[7]	12
「_DataRegisters_Cnt_u08[8]	14
2cREG1_temp	target_i2cREG1_temp
c_ColSensorl2CAddress_Cnt_u08	9
s_SpurSensorl2CAddress_Cnt_u08	10
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
arget I2c GenStopCond I2cRegPtr Cnt T str.DMAC	3

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Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
	3
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target I2c Send I2cRegPtr Cnt T str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
	5
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target I2c Send I2cRegPtr Cnt T str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target I2c SetRecv I2cRegPtr Cnt T str.SAR	55
target I2c SetRecv I2cRegPtr Cnt T str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2C_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_12c_SetStatus_12cRegPtr_Cnt_T_str.DXR	66
	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204

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Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	3
target I2c SetupMasterReceive I2cRegPtr Cnt T str.FUN	1
	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	2
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target i2cREG1 temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3



Name	Input Value		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result

target_izcREGT_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	~
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	~
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	•
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt ColSnsrData Cnt M u16	2309	2309	•
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR1 EXTREADCTRLREG REA	INIT SENSOR1 EXTREADCTRLREG REA	<b>~</b>
DigColPsInt I2CHwCustData UIs M u16	1	1	~
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	2	2	<b>~</b>
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	<b>~</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	_
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	_
DigColPsInt SpurSnsrData Cnt M u16	87	87	~
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	
target I2c GenStopCond I2cRegPtr Cnt T str.DRR	67	67	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVIR	5	5	-
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FMDR	3	3	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC	66	66	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12	66	66	-
	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN		1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN			
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET		3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	_

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Name	Actual Value	Expected Value	Result
target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	2	2	•
target_12c_Send_12cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	1204 87	1204 87	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	67	67	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	3	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	1	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66 2309	66 2309	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	
	1.0	3	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.QAR		55	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55 66	55 66	
	55		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	55 66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	55 66 556	66 556	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	55 66 556 2309	66 556 2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	55 66 556 2309 1204	66 556 2309 1204	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	55 66 556 2309 1204 87 67	66 556 2309 1204 87 67	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	55 66 556 2309 1204 87 67 55	66 556 2309 1204 87 67 55	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	55 66 556 2309 1204 87 67 55 66 2309	66 556 2309 1204 87 67 55 66 2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55 66 556 2309 1204 87 67 55 66 2309	66 556 2309 1204 87 67 55 66 2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	55 66 556 2309 1204 87 67 55 66 2309	66 556 2309 1204 87 67 55 66 2309	

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	

Т				V
Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	~
I2c_SetupMasterReceive	1	l2c_SetupMasterReceive	1	~
I2c_SetRecv	1	l2c_SetRecv	1	~

Test Step 3.20 (Repeat Count = 1) ✓			
Name	Input Value		
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1		
DigColPsInt_Buffer_Cnt_M_u08[0]	10		
DigColPsInt_Buffer_Cnt_M_u08[1]	20		
DigColPsInt_Buffer_Cnt_M_u08[2]	30		
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0		
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1		
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1		
DigColPsInt_ColSnsrData_Cnt_M_u16	2309		
DigColPsInt_CurrentSlave_Cnt_M_u08	123		
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_SETREG		
DigColPsInt_I2CHwCustData_Uls_M_u16	1		
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2		
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0		
DigColPsInt_NackOccured_Cnt_M_lgc	0		
DigColPsInt_PrevReqDataType_Cnt_M_u08	1		
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0		
DigColPsInt_RecvdDataType_Cnt_M_u08	0		
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0		
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0		
DigColPsInt_SpurSnsrData_Cnt_M_u16	87		
DigColPsInt_TransactionCnt_Cnt_M_u08	10		
Flags_Cnt_T_b16	4		
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str		
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str		

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Name	Input Value
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7] T DataRegisters Cnt u08[8]	12
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	9
k SpurSensorI2CAddress Cnt u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR	3
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC	66
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	3 55
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	1204
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12 target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	66
target_l2c_Send_l2cRegPtr_Cnt_1_str.DIMAC target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_12c_Send_12cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	2309
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	1204 87
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	67
targot_120_00t100v_12010gt tt_Offt_1_5tt.DMN	VI .

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Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target I2c SetRecv I2cRegPtr Cnt T str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target I2c SetupMasterReceive I2cRegPtr Cnt T str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target I2c SetupMasterReceive I2cRegPtr Cnt T str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	1204
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Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	2309		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT target_l2c SetupMasterTransmit_l2cRegPtr_Cnt_T str.SET	3		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	55		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	556		
target_i2cREG1_temp.CLKL	2309		
target_i2cREG1_temp.CLKH target_i2cREG1_temp.CNT	1204 87		
target_i2cREG1_temp.DRR	67		
target i2cREG1 temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC target_i2cREG1_temp.FUN	1		
target i2cREG1 temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3	l=	l
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0]	1 10	1 10	~
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	J
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	~
DigColPsInt BusBusySeqError Cnt M Igc	0	0	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	~
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	~
DigColPsInt_CurrentStepNo_Cnt_M_enum		INIT_SENSOR2_EXTREADCTRLREG_REA	
DigColPsInt_I2CHwCustData_UIs_M_u16	1 2	2	<b>*</b>
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	7
	0	0	~
DigColPsint NackOccured Cnt M ldc			J
DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt RecvOverrunError Cnt M lgc	0	0	_
	0	0	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc			
DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	
DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvdDataType_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08	0 0 87 10	0 0 87 10	
DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvdDataType_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR	0 0 87 10 55	0 0 87 10 55	· ·
DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvdDataType_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08	0 0 87 10	0 0 87 10	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \

2309

1204

87

67

55

2309

1204

87

67

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKL

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKH target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CNT

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DRR$ 

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.SAR$ 

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	J
target_I2c_GenStopCoMd_VI2cR@gPtr_Cnt_T_str.PSC	66	66	

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	Result
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR	55	55	<b>*</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	66	66	
target I2c SetStatus I2cRegPtr Cnt T str.MDR	2309	2309	-
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	5	5	
	3	3	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR			
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC	66 1204	66 1204	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11			
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12	66	66	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC	3	3	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>v</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	
	3	3	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	3	3	-
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR			
	55	55	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>V</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	87	87	<b>v</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~
0 1 2 2 2 2 2 3 5 5 5 5 5 5 5 5 5 5 5 5 5 5	1.5	·	



T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	~
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	<b>✓</b>
I2c SetRecv	1	I2c SetRecv	1	-

Test Step 3.21 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR1 EXTREADDATREG SETREG
digColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt I2CHwIncompleteCustData Uls M u16	2
ligColPsInt_InitFailedOnce_Cnt_M_lgc	0
bigColPsInt_NackOccured_Cnt_M_lgc	0
igColPsInt_PrevReqDataType_Cnt_M_u08	1
igColPsInt_RecvOverrunError_Cnt_M_lgc	0
igColPsInt_RecvdDataType_Cnt_M_u08	0
ligColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
igColPsInt_SkipIxegisterWrite_Crit_w_gc	0
igColPsInt_SpurSnsrData_Cnt_M_u16	87
ligColPsInt_TransactionCnt_Cnt_M_u08	10
lags_Cnt_T_b16	4
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target I2c GenStopCond I2cRegPtr Cnt T str
2c Send(I2cRegPtr Cnt T str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_12c_SetStatus_12cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
_DataRegisters_Cnt_u08[0]	32
_DataRegisters_Cnt_u08[1]	
_DataRegisters_Cnt_u08[2]	30 36
_DataRegisters_Cnt_u08[3]	
_DataRegisters_Cnt_u08[4]	38
_DataRegisters_Cnt_u08[5]	34
_DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
_DataRegisters_Cnt_u08[8]	14
tcREG1_temp	target_i2cREG1_temp
_ColSensorI2CAddress_Cnt_u08	9
_SpurSensorI2CAddress_Cnt_u08	10
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1

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Name	Input Value	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	
target I2c GenStopCond I2cRegPtr Cnt T str.PD	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	
	556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309 1204	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
target I2c Send I2cRegPtr Cnt T str.PSL	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
	556	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR		
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	2309	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	1204	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	87	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	
target I2c SetRecv I2cRegPtr Cnt T str.PD	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	
target I2c SetStatus I2cRegPtr Cnt T str.IMR	66	
	556	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR		
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	
	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN		
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	

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DigColPSITIL_Interruptivotification		
Name	Input Value	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	
arget I2c SetupMasterReceive I2cRegPtr Cnt T str.SAR	55	
rarget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	
rarget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	
rarget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.FUN	1	
arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_1_str.Pun arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	
arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	3	
arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	55	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	
arget I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	3	
arget I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	1	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	
rarget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	
arget I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	3	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	
arget I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	2	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2C_SetupMasterTransmit_I2CRegPtr_Cnt_1_str.PD arget_I2C_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	
arget_i2cREG1_temp.OAR	55	
arget_i2cREG1_temp.IMR	66	
arget_i2cREG1_temp.STR	556	
arget_i2cREG1_temp.CLKL	2309	
arget_i2cREG1_temp.CLKH	1204	
arget_i2cREG1_temp.CNT	87	
arget_i2cREG1_temp.DRR	67	
arget_i2cREG1_temp.SAR	55	
arget_i2cREG1_temp.DXR	66	
arget_i2cREG1_temp.MDR	2309	
arget_i2cREG1_temp.IVR	5	
arget_i2cREG1_temp.EMDR	3	
arget_i2cREG1_temp.PSC	66	
target_i2cREG1_temp.PID11	1204	
target_i2cREG1_temp.PID12	66	
arget_i2cREG1_temp.DMAC	3	
target_i2cREG1_temp.FUN	1	

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Name	3			
Septiment   September   Sept	Name	Input Value		
	target_i2cREG1_temp.DIN	2		
	target_i2cREG1_temp.DOUT	3		
	target_i2cREG1_temp.SET	3		
Sample   Delicion   Image   Part   Sample   Sample   Sample   Sample   Delicion   Image   Delicion   Image   Sample	target_i2cREG1_temp.CLR	1		
Samp   Activation   Activatio				
	0 =			
DipoCarlier, ManipoCourforOuts/Deliver Cort, M. 1089   1				
Digical Paul Burller Cort M, 1980  10   10   10   10   10   10   10   1			·	Result
Digitable   Lander   Cort   Lander   December   Lander   Cort   Lander   December   Decem				~
DipoCheFile_MarkerSeySerm_Cin_M_sign   0   0   0   0   0   0   0   0   0				
DOCOMENT, ENERGY SOUTH COLVENT SOUTH SOU				
DipoCaPartic Confessionary Cont. M. Isla   DipoCaPartic Record Cont. M. Isla   DipoCaPartic Report Cont. T. Isla   DipoCaPar				
DipoCharlar Confusionarious (D. M. Mys. 100   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   2099   209				
DipOpPerIni Contentions Cost M, 106   100   101   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   102   10				
Dispositional   Cumentiative   Cut   M   J08   Dispositional   Cumentiative   Cut   J08   Dispositional   Cut   Dispositional   Cu				
DigicaPartin   Christopseys Out M, enum   INT SENSOR1 EXTREADDATEGE REAL				
DigGOPBHI ICCHANGEMENT LIN MUTE   1				
Dispositional   Disposition   Disposition   Dispositional				
DigicalParial, National Pierro Cent M, Uge				
Disposition   Nacional Country   Multiple   0   0   0   0   0   0   0   0   0				
DigicalPaint, RevolversalEarry Cntt, M. Jos   DigicalPaint, RevolversalEarry Cntt, M. Jos   DigicalPaint, Sprucht, Spruchts Daily Cntt, M. Jos   DigicalPaint, Spruchts Daily Cntt, M. Jos   DigicalPaint, Teaseaston Cntt, Teaseaston Cntt, M. Jos   DigicalPaint, Teaseaston Cntt, Teaseaston Cntt, M. Jos   DigicalPaint, Teaseaston Cntt, Teaseast		0	0	<b>~</b>
Disposition RecordularTypes, Crift, Mus98  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		0	0	~
DipoCaPaint_TransportConf_Cnt_Mur8		0	0	•
DigCoPPAIN_Tanasachonom_CoL_M_U_08		0	0	~
	DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	~
target, I.Z., GenStopCond, I.Z.RegiPtr, Chil, T. str. STR         66         66           target, I.Z., GenStopCond, I.Z.RegiPtr, Chil, T. str. STR         556         556           target, I.Z., GenStopCond, I.Z.RegiPtr, Chil, T. str. CkRI         2309         2309           target, I.Z., GenStopCond, I.Z.RegiPtr, Chil, T. str. CkRI         1204         1204           target, I.Z., GenStopCond, I.Z.RegiPtr, Chil, T. str. CkRI         7         67           target, I.Z., GenStopCond, I.Z.RegiPtr, Chil, T. str. DKR         67         67           target, I.Z., GenStopCond, I.Z.RegiPtr, Chil, T. str. DKR         66         66           target, I.Z., GenStopCond, I.Z.RegiPtr, Chil, T. str. DKR         5         55           target, I.Z., GenStopCond, I.Z.RegiPtr, Chil, T. str. DKR         5         5           target, I.Z., GenStopCond, I.Z.RegiPtr, Chil, T. str. DKR         3         3         3           target, I.Z., GenStopCond, I.Z.RegiPtr, Chil, T. str. DKR         3         3         3         4           target, I.Z., GenStopCond, I.Z.RegiPtr, Chil, T. str. DKR         3         3         3         4           target, I.Z., GenStopCond, I.Z.RegiPtr, Chil, T. str. DKR         3         3         3         4           target, I.Z., GenStopCond, I.Z.RegiPtr, Chil, T. str. DKR         3         3         3         4 <td>DigColPsInt_TransactionCnt_Cnt_M_u08</td> <td>10</td> <td>10</td> <td>~</td>	DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	~
Isingell L2c GenStopCond   JeRegPIP_CntT_strClkL.   2009   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309   2309	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target   Zo_GenStopCond   ZeRegPr_Cnt_T_str_CLKt	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	~
Integel_12C_GenStopCond_12ReRepPr_Cnt_T_str.CLKH   1204   1204   1204   1204   1204   1204   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target_Ize_GenStopCond_IzeRegPtr_Cnt_T_str.SAR         57           target_Ize_GenStopCond_IzeRegPtr_Cnt_T_str.DXR         66           defenStopCond_IzeRegPtr_Cnt_T_str.DXR         66           defenStopCond_IzeRegPtr_Cnt_T_str.DXR         66           defenStopCond_IzeRegPtr_Cnt_T_str.DXR         66           defenStopCond_IzeRegPtr_Cnt_T_str.DXR         5           defenStopCond_IzeRegPtr_Cnt_T_str.DXR         5           defenStopCond_IzeRegPtr_Cnt_T_str.DXR         3           defenStopCond_IzeRegPtr_Cnt_T_str.DXR         3           defen_Ize_Ize_GenStopCond_IzeRegPtr_Cnt_T_str.DIDIT         1204           darget_Ize_GenStopCond_IzeRegPtr_Cnt_T_str.DIDIT         66           defen_Ize_Ize_GenStopCond_IzeRegPtr_Cnt_T_str.DINAC         3           darget_Ize_GenStopCond_IzeRegPtr_Cnt_T_str.DIN         1           darget_Ize_GenStopCond_IzeRegPtr_Cnt_T_str.DIN         1           darget_Ize_GenStopCond_IzeRegPtr_Cnt_T_str.DIDIT         1           darget_Ize_GenStopCond_IzeRegPtr_Cnt_T_str.DOUT         3           darget_Ize_GenStopCond_IzeRegPtr_Cnt_T_str.DOUT         3           darget_Ize_GenStopCond_IzeRegPtr_Cnt_T_str.DOUT         3           darget_Ize_GenStopCond_IzeRegPtr_Cnt_T_str.DUT         3           darget_Ize_GenStopCond_IzeRegPtr_Cnt_T_str.DUT         3           darget_Ize_GenStopCo				
target_I2e_GenStopCond_I2eRegPtr_Cnt_T_str.SAR         55         55           target_I2e_GenStopCond_I2eRegPtr_Cnt_T_str.DNR         66         66           target_I2e_GenStopCond_I2eRegPtr_Cnt_T_str.WR         5         5           target_I2e_GenStopCond_I2eRegPtr_Cnt_T_str.WR         5         5           target_I2e_GenStopCond_I2eRegPtr_Cnt_T_str.PIDTR         3         3           target_I2e_GenStopCond_I2eRegPtr_Cnt_T_str.PIDTR         1204         1204           target_I2e_GenStopCond_I2eRegPtr_Cnt_T_str.PIDTR         1204         1204           target_I2e_GenStopCond_I2eRegPtr_Cnt_T_str.PIDTR         66         66           target_I2e_GenStopCond_I2eRegPtr_Cnt_T_str.DIDR         3         3           target_I2e_GenStopCond_I2eRegPtr_Cnt_T_str.DIDR         1         1           target_I2e_GenStopCond_I2eRegPtr_Cnt_T_str.DIDR         1         1           target_I2e_GenStopCond_I2eRegPtr_Cnt_T_str.DIDT         3         3           target_I2e_GenStopCond_I2eRegPtr_Cnt_T_str.DIT         2         2           target_I2e_GenStopCond_I2eRegPtr_Cnt_T_str.Str.CIR         1         1           target_I2e_GenStopCond_I2eRegPtr_Cnt_T_str.DIR         3         3           target_I2e_GenStopCond_I2eRegPtr_Cnt_T_str.DIR         3         3           target_I2e_GenStopCond_I2eRegPtr_Cnt_T_str.DIR				
target   Ze_GenStopCond   22RegPtr_Cnt_T_str.DXR				
target_IZo_GenStopCond_IZoRegPtr_Cnt_T_str.NDR         2309           target_IZo_GenStopCond_IZoRegPtr_Cnt_T_str.NVR         5           target_IZo_GenStopCond_IZoRegPtr_Cnt_T_str.NVR         5           target_IZo_GenStopCond_IZoRegPtr_Cnt_T_str.NDR         3           target_IZo_GenStopCond_IZoRegPtr_Cnt_T_str.NDD11         1204           target_IZo_GenStopCond_IZoRegPtr_Cnt_T_str.NDD12         66           de         66           target_IZo_GenStopCond_IZoRegPtr_Cnt_T_str.NDN         3           target_IZo_GenStopCond_IZoRegPtr_Cnt_T_str.NDN         1           target_IZo_GenStopCond_IZoRegPtr_Cnt_T_str.NDN         1           target_IZo_GenStopCond_IZoRegPtr_Cnt_T_str.NDN         1           target_IZo_GenStopCond_IZoRegPtr_Cnt_T_str.NDN         2           target_IZo_GenStopCond_IZoRegPtr_Cnt_T_str.NDN         2           target_IZo_GenStopCond_IZoRegPtr_Cnt_T_str.NDN         3           target_IZo_GenStopCond_IZoRegPtr_Cnt_T_str.Clr.         1           target_IZo_GenStopCond_IZoRegPtr_Cnt_T_str.Clr.         1           target_IZo_GenStopCond_IZoRegPtr_Cnt_T_str.ODR         2           target_IZo_GenStopCond_IZoRegPtr_Cnt_T_str.NDR         3           target_IZo_Send_IZoRegPtr_Cnt_T_str.NDR         5           target_IZo_Send_IZoRegPtr_Cnt_T_str.NDR         66           target_IZo_Send_IZoRegPtr_				
target   2c. GenStopCond   2cRegPtr_Cnt_T str.NPR   5				
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.EMDR   3   3   3   3   3   3   3   3   3				
larget   2c   GenStopCond   2cRegPtr_Cnt_T_str.PSC   66   66   66   66   66   66   66				
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11         1204         1204           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12         66         66           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC         1         1           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DN         1         1           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DN         2         2           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DNU         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CtR         1         1           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DD         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DD         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DAR         5         5           target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR         5         5           target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR         66         66           target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR         66         66           target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR         67         67 <td></td> <td></td> <td></td> <td></td>				
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DMAC         3         3         3           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DMAC         3         3         3           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DIN         1         1         1           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DIN         2         2         4           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DUT         3         3         4           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DUT         3         3         4           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DLR         1         1         4           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DLR         1         1         4           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DLR         2         2         2           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DLR         3         3         3         4           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DLR         3         3         3         4         4           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DLR         3         3         3         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4 <td< td=""><td></td><td></td><td></td><td></td></td<>				
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DNN         1         1           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN         1         1           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN         2         2           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DUT         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.Str.ET         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DUR         1         1           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DDR         2         2           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DDR         2         2           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DR         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DAR         5         5           target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR         5         5           target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR         66         4           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL         2309         2309           target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR         67         67           target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR         67         67           target_l2c_Send_l2cRegPtr_Cnt_T_str.DAR         66         66				~
larget_ 2c_GenStopCond_!2cRegPtr_Cnt_T_str.DNR		3	3	~
target_ 2c_GenStopCond_ 2cRegPtr_Cnt_T_str.DIN   2   2   2   2   2   2   3   3   3   3		1	1	•
target_12e_GenStopCond_12cRegPtr_Cnt_T_str.DOUT         3         3           target_12e_GenStopCond_12cRegPtr_Cnt_T_str.SET         3         3           target_12e_GenStopCond_12cRegPtr_Cnt_T_str.CLR         1         1           target_12e_GenStopCond_12cRegPtr_Cnt_T_str.DDR         2         2           target_12e_GenStopCond_12cRegPtr_Cnt_T_str.PD         3         3           target_12e_GenStopCond_12cRegPtr_Cnt_T_str.DRL         3         3           target_12e_GenStopCond_12cRegPtr_Cnt_T_str.DRL         3         3           target_12e_GenStopCond_12cRegPtr_Cnt_T_str.DRL         3         3           target_12e_GenStopCond_12cRegPtr_Cnt_T_str.DRL         3         3           target_12e_Gend_12cRegPtr_Cnt_T_str.Dat_Str.CLR         55         55           target_12e_Send_12cRegPtr_Cnt_T_str.CLKL         2309         2309           target_12e_Send_12cRegPtr_Cnt_T_str.CLKL         2309         2309           target_12e_Send_12cRegPtr_Cnt_T_str.DRR         67         67           target_12e_Send_12cRegPtr_Cnt_T_str.DRR         67         67           target_12e_Send_12cRegPtr_Cnt_T_str.DXR         66         66           target_12e_Send_12cRegPtr_Cnt_T_str.DRR         5         55           target_12e_Send_12cRegPtr_Cnt_T_str.DRR         3         3	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.SET         3         3           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLR         1         1           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DDR         2         2           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.PD         3         3           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.PSL         3         3           target_12c_Send_12cRegPtr_Cnt_T_str.DAR         55         55           target_12c_Send_12cRegPtr_Cnt_T_str.DAR         66         66           target_12c_Send_12cRegPtr_Cnt_T_str.DIMR         66         66           target_12c_Send_12cRegPtr_Cnt_T_str.CLKL         2309         2309           target_12c_Send_12cRegPtr_Cnt_T_str.CLKL         2309         2309           target_12c_Send_12cRegPtr_Cnt_T_str.CNT         87         87           target_12c_Send_12cRegPtr_Cnt_T_str.DAR         67         67           target_12c_Send_12cRegPtr_Cnt_T_str.DAR         66         66           target_12c_Send_12cRegPtr_Cnt_T_str.DAR         66         66           target_12c_Send_12cRegPtr_Cnt_T_str.DAR         5         5           target_12c_Send_12cRegPtr_Cnt_T_str.DAR         5         5           target_12c_Send_12cRegPtr_Cnt_T_str.DAR         5         5           target_12c_Send_12cReg	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_12c_GenStopCond_12cRegPtr_CntT_str.ODR         2         2           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.ODR         2         2           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.PD         3         3           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.PSL         3         3           target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DAR         55         55           target_12c_Send_12cRegPtr_Cnt_T_str.MMR         66         66           target_12c_Send_12cRegPtr_Cnt_T_str.Str.Str.         556         556           target_12c_Send_12cRegPtr_Cnt_T_str.CLK.         2309         2309           target_12c_Send_12cRegPtr_Cnt_T_str.CLK.         2309         2309           target_12c_Send_12cRegPtr_Cnt_T_str.DAR         87         87           target_12c_Send_12cRegPtr_Cnt_T_str.DRR         67         67           target_12c_Send_12cRegPtr_Cnt_T_str.DAR         66         66           target_12c_Send_12cRegPtr_Cnt_T_str.DAR         66         66           target_12c_Send_12cRegPtr_Cnt_T_str.DAR         55         55           target_12c_Send_12cRegPtr_Cnt_T_str.DAR         66         66           target_12c_Send_12cRegPtr_Cnt_T_str.DAR         5         5           target_12c_Send_12cRegPtr_Cnt_T_str.DAR         3         3           target_12c_Se	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD         3         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD         3         3         3           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL         3         3         3           target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR         55         55         55           target_l2c_Send_l2cRegPtr_Cnt_T_str.DMR         66         66         4           target_l2c_Send_l2cRegPtr_Cnt_T_str.Str.R         556         556         556           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL         2309         2309         2309           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH         1204         1204         1204           target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT         87         87         87           target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR         67         67         4           target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR         66         66         4           target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR         66         66         4           target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR         5         5         5           target_l2c_Send_l2cRegPtr_Cnt_T_str.DNR         3         3         3           target_l2c_Send_l2cRegPtr_Cnt_T_str.DNR         3         3         3 <td>target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET</td> <td>3</td> <td>3</td> <td>~</td>	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD         3         3         v           target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL         3         3         3           target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR         55         55         4           target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR         66         66         4           target_l2c_Send_l2cRegPtr_Cnt_T_str.STR         556         556         4           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL         2309         2309         4           target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH         1204         1204         1204           target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT         87         87         4           target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR         67         67         67           target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR         66         66         4           target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR         66         66         4           target_l2c_Send_l2cRegPtr_Cnt_T_str.WDR         2309         2309         2309           target_l2c_Send_l2cRegPtr_Cnt_T_str.DNR         5         5         4           target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR         3         3         3           target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR         5         5         4	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR			~
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRL         3         3           target_12c_Send_12cRegPtr_Cnt_T_str.DAR         55         55           target_12c_Send_12cRegPtr_Cnt_T_str.IMR         66         66           target_12c_Send_12cRegPtr_Cnt_T_str.STR         556         556           target_12c_Send_12cRegPtr_Cnt_T_str.CLKL         2309         2309           target_12c_Send_12cRegPtr_Cnt_T_str.CLKH         1204         1204           target_12c_Send_12cRegPtr_Cnt_T_str.DRR         67         87           target_12c_Send_12cRegPtr_Cnt_T_str.DRR         67         67           target_12c_Send_12cRegPtr_Cnt_T_str.DXR         66         66           target_12c_Send_12cRegPtr_Cnt_T_str.DXR         66         66           target_12c_Send_12cRegPtr_Cnt_T_str.DXR         66         66           target_12c_Send_12cRegPtr_Cnt_T_str.MDR         2309         2309           target_12c_Send_12cRegPtr_Cnt_T_str.PID         5         5           target_12c_Send_12cRegPtr_Cnt_T_str.PID         3         3           target_12c_Send_12cRegPtr_Cnt_T_str.PID         1         104           target_12c_Send_12cRegPtr_Cnt_T_str.DIN         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DIN         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DI				~
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR       55       55         target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR       66       66         target_l2c_Send_l2cRegPtr_Cnt_T_str.STR       556       556         target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL       2309       2309         target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH       1204       1204         target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT       87       87         target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR       67       67         target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR       55       55         target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR       66       66         target_l2c_Send_l2cRegPtr_Cnt_T_str.DNR       66       66         target_l2c_Send_l2cRegPtr_Cnt_T_str.DNR       2309       2309         varget_l2c_Send_l2cRegPtr_Cnt_T_str.DNR       5       5         target_l2c_Send_l2cRegPtr_Cnt_T_str.BNDR       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.DNC       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.DNC       66       66         target_l2c_Send_l2cRegPtr_Cnt_T_str.DNAC       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.DNAC       1       1         target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN       1       1         target_l2c_Send_l2cRegPtr_Cn				~
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR       66       66         target_l2c_Send_l2cRegPtr_Cnt_T_str.STR       556       556         target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL       2309       2309         target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH       1204       1204         target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT       87       87         target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR       67       67         target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR       55       55         target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR       66       66         target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR       2309       2309         target_l2c_Send_l2cRegPtr_Cnt_T_str.WR       5       5         target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.ENDR       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.ENDL       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11       1204       1204         target_l2c_Send_l2cRegPtr_Cnt_T_str.DNAC       3       3         target_l2c_Send_l2cRegPtr_Cnt_T_str.DNA       1       1         target_l2c_Send_l2cRegPtr_Cnt_T_str.DNA       1       1         target_l2c_Send_l2cRegPtr				
target_!2c_Send_!2cRegPtr_Cnt_T_str.STR       556       556         target_!2c_Send_!2cRegPtr_Cnt_T_str.CLKL       2309       2309         target_!2c_Send_!2cRegPtr_Cnt_T_str.CLKH       1204       1204         target_!2c_Send_!2cRegPtr_Cnt_T_str.CNT       87       87         target_!2c_Send_!2cRegPtr_Cnt_T_str.DRR       67       67         target_!2c_Send_!2cRegPtr_Cnt_T_str.SAR       55       55         target_!2c_Send_!2cRegPtr_Cnt_T_str.DXR       66       66         target_!2c_Send_!2cRegPtr_Cnt_T_str.DXR       66       66         target_!2c_Send_!2cRegPtr_Cnt_T_str.WR       2309       2309         target_!2c_Send_!2cRegPtr_Cnt_T_str.BMDR       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.PID11       1204       1204         target_!2c_Send_!2cRegPtr_Cnt_T_str.PID12       66       66         target_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       1       1         target_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       1       1         target_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       2       2         target_!2c_Send_!2cRegPtr_Cnt_T_str.DOUT       3       3				
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL       2309       2309         target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH       1204       1204         target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT       87       87         target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR       67       67         target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR       55       55         target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR       66       66         target_I2c_Send_I2cRegPtr_Cnt_T_str.DMR       2309       2309         target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC       66       66         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11       1204       1204         target_I2c_Send_I2cRegPtr_Cnt_T_str.DID12       66       66         target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       3       3				
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH       1204       1204         target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT       87       87         target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR       67       67         target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR       55       55         target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR       66       66         target_I2c_Send_I2cRegPtr_Cnt_T_str.NDR       2309       2309         target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.PNDR       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC       66       66         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11       1204       1204         target_I2c_Send_I2cRegPtr_Cnt_T_str.DNAC       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT       3       3				
target   2c Send   12cRegPtr_Cnt_T str.CNT       87       87         target   12c Send   12cRegPtr_Cnt_T str.DRR       67       67         target   12c Send   12cRegPtr_Cnt_T str.DAR       55       55         target   12c Send   12cRegPtr_Cnt_T str.DXR       66       66         target   12c Send   12cRegPtr_Cnt_T str.MDR       2309       2309         target   12c Send   12cRegPtr_Cnt_T str.IVR       5       5         target   12c Send   12cRegPtr_Cnt_T str.EMDR       3       3         target   12c Send   12cRegPtr_Cnt_T str.PSC       66       66         target   12c Send   12cRegPtr_Cnt_T str.PID11       1204       1204         target   12c Send   12cRegPtr_Cnt_T str.PID12       66       66         target   12c Send   12cRegPtr_Cnt_T str.DMAC       3       3         target   12c Send   12cRegPtr_Cnt_T str.DIN       1       1         target   12c Send   12cRegPtr_Cnt_T str.DIR       1       1         target   12c Send   12cRegPtr_Cnt_T str.DIN       2       2         target   12c Send   12cRegPtr_Cnt_T str.DOUT       3       3				
target   2c Send   12cRegPtr_Cnt_T str.DRR       67       67         target   12c Send   12cRegPtr_Cnt_T str.SAR       55       55         target   12c Send   12cRegPtr_Cnt_T str.DXR       66       66         target   12c Send   12cRegPtr_Cnt_T str.MDR       2309       2309         target   12c Send   12cRegPtr_Cnt_T str.IVR       5       5         target   12c Send   12cRegPtr_Cnt_T str.EMDR       3       3         target   12c Send   12cRegPtr_Cnt_T str.PSC       66       66         target   12c Send   12cRegPtr_Cnt_T str.PID11       1204       1204         target   12c Send   12cRegPtr_Cnt_T str.PID12       66       66         target   12c Send   12cRegPtr_Cnt_T str.DMAC       3       3         target   12c Send   12cRegPtr_Cnt_T str.DMAC       3       3         target   12c Send   12cRegPtr_Cnt_T str.DIR       1       1         target   12c Send   12cRegPtr_Cnt_T str.DIR       1       1         target   12c Send   12cRegPtr_Cnt_T str.DIN       2       2         target   12c Send   12cRegPtr_Cnt_T str.DOUT       3       3				
target   2c Send   12cRegPtr_Cnt_T str.SAR       55       55         target   12c Send   12cRegPtr_Cnt_T str.DXR       66       66         target   12c Send   12cRegPtr_Cnt_T str.MDR       2309       2309         target   12c Send   12cRegPtr_Cnt_T str.IVR       5       5         target   12c Send   12cRegPtr_Cnt_T str.EMDR       3       3         target   12c Send   12cRegPtr_Cnt_T str.PSC       66       66         target   12c Send   12cRegPtr_Cnt_T str.PID11       1204       1204         target   12c Send   12cRegPtr_Cnt_T str.PID12       66       66         target   12c Send   12cRegPtr_Cnt_T str.DMAC       3       3         target   12c Send   12cRegPtr_Cnt_T str.DMAC       3       3         target   12c Send   12cRegPtr_Cnt_T str.DIR       1       1         target   12c Send   12cRegPtr_Cnt_T str.DIR       1       1         target   12c Send   12cRegPtr_Cnt_T str.DIN       2       2         target   12c Send   12cRegPtr_Cnt_T str.DOUT       3       3				
target   2c Send   2cRegPtr_Cnt_T str.DXR       66       66         target   2c Send   2cRegPtr_Cnt_T str.MDR       2309       2309         target   2c Send   2cRegPtr_Cnt_T str.IVR       5       5         target   2c Send   2cRegPtr_Cnt_T str.EMDR       3       3         target   2c Send   2cRegPtr_Cnt_T str.PSC       66       66         target   2c Send   2cRegPtr_Cnt_T str.PID11       1204       1204         target   2c Send   2cRegPtr_Cnt_T str.PID12       66       66         target   12c Send   2cRegPtr_Cnt_T str.DMAC       3       3         target   12c Send   2cRegPtr_Cnt_T str.DMAC       3       3         target   12c Send   2cRegPtr_Cnt_T str.DIR       1       1         target   12c Send   2cRegPtr_Cnt_T str.DIR       1       1         target   12c Send   2cRegPtr_Cnt_T str.DIN       2       2         target   12c Send   2cRegPtr_Cnt_T str.DOUT       3       3				
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR       2309       2309         target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR       5       5         target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC       66       66         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11       1204       1204         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12       66       66         target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT       3       3				~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR       5       5         target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC       66       66         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11       1204       1204         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12       66       66         target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT       3       3				<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC       66       66         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11       1204       1204         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12       66       66         target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT       3       3				~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC       66       66       ✓         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11       1204       1204       ✓         target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12       66       66       ✓         target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC       3       3       ✓         target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN       1       1       ✓         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR       1       1       ✓         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       2       2       ✓         target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT       3       3       ✓		3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12       66       66         target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT       3       3		66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT       3       3	target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT       3       3	target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR       1       1       ✓         target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN       2       2       ✓         target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT       3       3       ✓	target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN 2 2 2 2 4 2 4 2 4 2 4 2 4 2 4 2 4 2 4				~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT 3 3				~
target_izc_Seno_izckegrtr_cnt_i_str.SE1 3				
	target_120_5e110_120RegPti_ORt_1_Str.5E1	٥	S.	

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Name	Actual Value	Expected Value	Result
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	1	1	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	2	2	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3 55	<b>*</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55 66	66	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	556	556	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1 2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	3	3	<b>*</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL	3	3	
	55	55	-
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR target_l2c SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~

T				V
Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	~
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	<b>✓</b>
I2c_SetRecv	1	I2c_SetRecv	1	<b>✓</b>

Test Step 3.22 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADDATREG_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32

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DigColPsini_interruptiNotinication		, , , , ,
Name	Input Value	
T DataRegisters Cnt u08[2]	30	
Γ_DataRegisters_Cnt_u08[3]	36	
T_DataRegisters_Cnt_u08[4]	38	
 Γ_DataRegisters_Cnt_u08[5]	34	
Γ_DataRegisters_Cnt_u08[6]	10	
T_DataRegisters_Cnt_u08[7]	12	
T_DataRegisters_Cnt_u08[8]	14	
2cREG1_temp	target_i2cREG1_temp	
<_ColSensorI2CAddress_Cnt_u08	9	
	10	
C_SpurSensorI2CAddress_Cnt_u08 Careat I2a_CarStanCand_I2aDagDtr_Cat_T_atr_OAD		
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT	87	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR	67	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	
	2309	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	55	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
arget I2c Send I2cRegPtr Cnt T str.PSL	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	
irget_12c_SetRecv_12cRegPtr_Cnt_T_str.CLKL	2309	
	1204	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	

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Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target I2c SetRecv I2cRegPtr Cnt T str.DIR	1
· ·	2
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target I2c SetStatus I2cRegPtr Cnt T str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target I2c SetupMasterReceive I2cRegPtr Cnt T str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	1204
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	1
target I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
$target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SAR$	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5



Name			
INAIIIE	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	55		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	556		
target_i2cREG1_temp.CLKL	2309 1204		
target_i2cREG1_temp.CLKH target_i2cREG1_temp.CNT	87		
target i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target i2cREG1 temp.MDR	2309		
target i2cREG1 temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target i2cREG1 temp.PID11	1204		
target i2cREG1 temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
	2		
target_i2cREG1_temp.ODR			
target_i2cREG1_temp.ODR target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PD	3	Expected Value	Result
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL	3 3 Actual Value	1	Result
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0]	3 3 Actual Value 1 10	1 10	Result
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]	3 3 Actual Value 1 10 20	1 10 20	~
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]	3 3 Actual Value 1 10 20 30	1 10 20 30	Result
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc	3 3 Actual Value 1 10 20 30 0	1 10 20 30 0	***
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc	3 3 Actual Value 1 10 20 30 0 1	1 10 20 30 0	~
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc	3 3 Actual Value 1 10 20 30 0 1	1 10 20 30 0 1	
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16	3 3 Actual Value 1 10 20 30 0 1 1 1 2309	1 10 20 30 0 1 1 2309	
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08	3 3 Actual Value 1 10 20 30 0 1 1 1 2309 123	1 10 20 30 0 1 1 1 2309	
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum	3 3 Actual Value 1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_REAL	1 10 20 30 0 1 1 2309 123 L INIT_SENSOR2_EXTREADDATREG_READ	0
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16	3 3 Actual Value 1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1	1 10 20 30 0 1 1 1 2309 123 L INIT_SENSOR2_EXTREADDATREG_READ	0
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	3 3 Actual Value 1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2	1 10 20 30 0 1 1 1 2309 123 E INIT_SENSOR2_EXTREADDATREG_READ 1 2	0
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_I12CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc	3 3 Actual Value 1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0	1 10 20 30 0 1 1 1 2309 123 E INIT_SENSOR2_EXTREADDATREG_READ 1 2 0	
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_I1itFailedOnce_Cnt_M_lgc  DigColPsInt_InitFailedOnce_Cnt_M_lgc	3 3 Actual Value 1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0	1 10 20 30 0 1 1 1 2309 123 E INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0	
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_I1tFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc	3 3 Actual Value 1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0	1 10 20 30 0 1 1 1 2309 123 E INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0	
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_i2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_I12CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvODataType_Cnt_M_u08	3 3 Actual Value 1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_REAL 1 2 0 0 0 0 0	1 10 20 30 0 1 1 1 2309 123 E INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0	
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target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColFustData_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_l12CHwCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvdDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	3 3 Actual Value 1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0 87 10 55	1 10 20 30 0 1 1 1 2309 123 E INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0 0 87 10 55	
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_enum  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_12CHwCustData_Uls_M_u16  DigColPsInt_litFailedOnce_Cnt_M_lgc  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_SpurCustDataTound_Cnt_M_lgc  DigColPsInt_SpurCustDataTound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR	3 3 Actual Value 1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0 87 10 55 66	1 10 20 30 0 1 1 1 2309 123 E INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0 0 0 87 10 55 66	
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustDatA_ulls_M_u16  DigColPsInt_I2CHwCustDatA_ulls_M_u16  DigColPsInt_I2CHwCustDatA_ulls_M_u16  DigColPsInt_I2CHwCustDatA_ulls_M_u16  DigColPsInt_I3CHwCustDatA_ulls_M_u16  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvdDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.JMR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	3 3 Actual Value 1 10 20 30 0 1 1 12309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0 87 10 55 66 556	1 10 20 30 0 1 1 1 2309 123 C INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0 87 10 55 66 556	
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustDatA_ulls_M_u16  DigColPsInt_I2CHwCustDatA_ulls_M_u16  DigColPsInt_I2CHwCustDatA_ulls_M_u16  DigColPsInt_I3CHwCustData_Ulls_M_u16  DigColPsInt_I3CHwCustData_Ulls_M_u16  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_u08  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	3 3 Actual Value 1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0 87 10 55 66 556 2309	1 10 20 30 0 1 1 1 2309 123 C INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0 0 87 10 55 66 556 2309	
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u18  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustDatA_ulis_M_u16  DigColPsInt_I2CHwCustDatA_ulis_M_u16  DigColPsInt_I2CHwCustDatA_ulis_M_u16  DigColPsInt_I3CHwIncompleteCustData_Ulis_M_u16  DigColPsInt_I3CHwIncompleteCustData_Ulis_M_u16  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL  target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	3 3 Actual Value 1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0 87 10 55 66 556 2309 1204	1 10 20 30 0 1 1 1 2309 123 E INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0 0 87 10 55 66 556 2309 1204	
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u18  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_I3chInitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_u08  DigColPsInt_SpurCustDataTound_Cnt_M_lgc  DigColPsInt_SpurCustDataTound_Cnt_M_lgc  DigColPsInt_SpurCustDateTound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.OAR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL	3 3 Actual Value 1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0 0 87 10 55 66 556 2309 1204 87	1 10 20 30 0 1 1 1 2309 123 E INIT_SENSOR2_EXTREADDATREG_READ 0 0 0 0 0 0 0 0 55 66 556 2309 1204	
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u18  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStave_Cnt_M_u08  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_I3cHailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustData_Ond_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.OAR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR	3 3 Actual Value 1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0 87 10 55 66 556 2309 1204 87 67	1 10 20 30 0 1 1 1 2309 123 LINIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0 0 87 10 55 66 556 2309 1204 87 67	
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u18  DigColPsInt_CurrentStave_Cnt_M_u08  DigColPsInt_CurrentStave_Cnt_M_u08  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_I3cHailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustData_Cnt_M_u16  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.OAR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CNT  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR	3 3 Actual Value 1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0 0 87 10 55 66 556 2309 1204 87 67 55	1 10 20 30 0 1 1 1 2309 123 LINIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0 0 87 10 55 66 556 2309 1204 87 67 55	
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurSnsrData_Cnt_M_u16  DigColPsInt_TransactionCnt_Cnt_M_u08  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DAR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CNT  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DAR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DAR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DAR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DAR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DAR	3 3 Actual Value 1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0 87 10 55 66 556 2309 1204 87 67 55 66	1 10 20 30 0 1 1 1 2309 123 LINIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0 0 87 10 55 66 556 2309 1204 87 67 55 66	
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDetatType_Cnt_M_u08  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.UKL  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR  target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR	3 3 Actual Value 1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0 87 10 55 66 556 2309 1204 87 67 55 66 2309	1 10 20 30 0 1 1 1 2309 123 LINIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0 0 0 87 10 55 66 556 2309 1204 87 67 55 66 2309	
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_u08  DigColPsInt_ColSnsrData_Cnt_M_u08  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwCustData_Uls_M_u16  DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_SpurCustDatFound_Cnt_M_lgc  DigColPsInt_TransactionCnt_Cnt_M_u08  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.OAR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.UKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CLKL  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.CNT  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DRR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR  target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DXR	3 3 Actual Value 1 10 20 30 0 1 1 1 2309 123 INIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0 87 10 55 66 556 2309 1204 87 67 55 66 2309 5	1 10 20 30 0 1 1 1 2309 123 LINIT_SENSOR2_EXTREADDATREG_READ 1 2 0 0 0 0 0 0 0 0 87 10 55 66 556 2309 1204 87 67 55 66 2309 5	

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN	1 2	1 2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DUT	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	2309	2309	
target_I2c_Send_I2cRegPtr_Cnt_1_str.IVR  target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
target I2c Send I2cRegPtr Cnt T str.PID12	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target I2c Send I2cRegPtr Cnt T str.FUN	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	55	55	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	66 2309	66 2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	
	3	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
target I2c SetRecv I2cRegPtr Cnt T str.PID12	66	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	•
	0.0		
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	•
	66 2309 5	2309	

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.lVR	5	5	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FMDR	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR		1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	556	556	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>→</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>→</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>-</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	-
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	3	3	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	3	3	-
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	

T .				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	~
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	<b>✓</b>
I2c SetRecv	1	I2c SetRecv	1	_



Test Step 3.23 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_Igc DigColPsInt_ColSnsrData_Cnt_M_u16	1 2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ SENSOR1 SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0 97
DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08	87 10
Flags_Cnt_T_b16	4
I2c GenStopCond(I2cRegPtr Cnt T str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34 10
T_DataRegisters_Cnt_u08[6] T_DataRegisters_Cnt_u08[7]	10
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	9
k_SpurSensorl2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	55 66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target I2c GenStopCond I2cRegPtr Cnt T str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR	1
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
LOI GOL LEO CONCLOPCIONA (ECITORI II CIRL I BILLED	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	55
	55 66
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	66
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	66 556

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Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
	1
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target I2c SetStatus I2cRegPtr Cnt T str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	
	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	

DigColPsInt\_InterruptNotification

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Input Value target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKH 1204 87  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.CNT$ target I2c SetupMasterReceive I2cRegPtr Cnt T str.DRR 67 target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.SAR 55 target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.DXR 66 target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.MDR 2309 target I2c SetupMasterReceive I2cRegPtr Cnt T str.IVR 5  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.EMDR$ 3 target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.PSC 66  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.PID11$ 1204 target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.PID12 66  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.DMAC$ 3 target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.FUN 1 target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.DIR 2 target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.DIN 3 target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.DOUT target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.SET 3  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.CLR$ 1  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.ODR$ 2 target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.PD 3 target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.PSL 3 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.OAR 55  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IMR$ 66 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.STR 556 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKL 2309  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKH$ 1204 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CNT 87 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DRR 67 55 target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DXR$ 66 target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR 2309 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IVR 5 target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR 3 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSC 66 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID11 1204  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID12$ 66  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DMAC$ 3  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.FUN$ 1  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIR$ 2 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIN target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DOUT 3  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SET$ 3  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLR$ target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.ODR 2  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PD$ 3 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSL 3 target i2cREG1 temp.OAR 55 target\_i2cREG1\_temp.IMR 66 target i2cREG1 temp.STR 556 target\_i2cREG1\_temp.CLKL 2309 target i2cREG1 temp.CLKH 1204 target\_i2cREG1\_temp.CNT 87 target i2cREG1 temp.DRR 67 target\_i2cREG1\_temp.SAR 55 target i2cREG1 temp.DXR 66 target\_i2cREG1\_temp.MDR 2309 target\_i2cREG1\_temp.IVR 5 target\_i2cREG1\_temp.EMDR 3 target\_i2cREG1\_temp.PSC 66 target\_i2cREG1\_temp.PID11 1204 target\_i2cREG1\_temp.PID12 66 3 target i2cREG1 temp.DMAC target\_i2cREG1\_temp.FUN 1 target\_i2cREG1\_temp.DIR 1 target\_i2cREG1\_temp.DIN 2 3 target i2cREG1 temp.DOUT target\_i2cREG1\_temp.SET 3 target i2cREG1 temp.CLR 1 target\_i2cREG1\_temp.ODR 2 target\_i2cREG1\_temp.PD 3 target\_i2cREG1\_temp.PSL 3 **Expected Value** Actual Value Name Result

 $DigColPsInt\_AttempOccurForCustDatRead\_Cnt\_M\_u08$ 

1

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Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	•
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	•
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	•
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1 2309	2309	
DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_GETDATA	READ_SENSOR1_GETDATA	
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	
DigColPsInt NackOccured Cnt M Igc	0	0	
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	•
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	•
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	3	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	2	2	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.SE1 target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	1	1	
	2	2	
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	3	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	3	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	55	55	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	66	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	
target 120 Octivedy 1201/eyrti Olit I Sti.STK	330		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>*</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3 66	3 66	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	1204	1204	
target I2c SetRecv I2cRegPtr Cnt T str.PID12	66	66	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target I2c SetRecv I2cRegPtr Cnt T str.PD	3	3	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target I2c SetStatus I2cRegPtr Cnt T str.STR	556	556	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>✓</b>
target I2c SetStatus I2cRegPtr Cnt T str.CLKH	1204	1204	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1	1	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	1	1	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	2	2	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	3	3	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	~
	. 0	3	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3		
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3 55	3 55	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	3	3	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \



Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~

T			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	~
I2c_SetupMasterReceive	1	l2c_SetupMasterReceive	1	~
I2c_SetRecv	1	I2c_SetRecv	1	~

Test Step 3.24 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt ColSnsrData Cnt M u16	2309
DigColPsInt CurrentSlave Cnt M u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt RecvOverrunError Cnt M Igc	0
DigColPsInt RecvdDataType Cnt M u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	9

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Name	Input Value
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.DIR	1
	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR	1
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPti_Cnt_T_str.CNT	87
	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1

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Name	Input Value
	·
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target I2c SetStatus I2cRegPtr Cnt T str.SAR	55
	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target I2c SetStatus I2cRegPtr Cnt T str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
	66
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target I2c SetupMasterReceive I2cRegPtr Cnt T str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	3
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	2
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	1204
	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3



Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	55		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	556		
target_i2cREG1_temp.CLKL	2309		
target_i2cREG1_temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result

target_I2CREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	<b>~</b>
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	<b>✓</b>
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	<b>✓</b>
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	<b>✓</b>
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	<b>✓</b>
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_GETDATA	READ_SENSOR2_GETDATA	<b>✓</b>
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	<b>✓</b>
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	2	2	<b>✓</b>
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	<b>✓</b>
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	<b>✓</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	<b>✓</b>
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	<b>✓</b>
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	<b>✓</b>
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	<b>✓</b>
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	<b>✓</b>
I2c_SetRecv(Length_Cnt_T_u32)	2	2	<b>✓</b>
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	2	2	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	~

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Name	Actual Value	Expected Value	Result
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2 3	3	
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.PSL	3	3	_
target I2c Send I2cRegPtr Cnt T str.OAR	55	55	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67 55	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	55 66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2 3	3	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87 67	<b>*</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	67 55	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	_
target I2c SetRecv I2cRegPtr Cnt T str.MDR	2309	2309	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>V</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	1 2	1 2	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>v</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	<b>V</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL	2309	2309 1204	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	1204 87	87	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR	67	67	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	1	1	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_120_octotatus_12011cgr tr_ont_1_str.Dilly	-		



Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.MDR	2309	2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DMAC	3	3	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.FUN	1	1	·
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIR	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	<u> </u>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	<u> </u>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	<u> </u>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
	1204	1204	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	87	87	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	67	67	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55 66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	66	66	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	3	3	<b>~</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	1	1	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	1	1	-
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	<b>Y</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	

T			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	~
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	•
I2c_SetRecv	1	I2c_SetRecv	1	•

Test Step 3.25 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0



DigColPsInt_InterruptNotification	TAACILAU
Name	Input Value
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_SENDCMD
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_Igc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPoint_SpurCustDatFound_Cnt_M_lgc	0 87
DigColPoint_SpurSnsrData_Cnt_M_u16	10
DigColPsInt_TransactionCnt_Cnt_M_u08 Flags_Cnt_T_b16	4
l2c_GenStopCond(l2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target I2c SetRecv I2cRegPtr Cnt T str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target I2c SetupMasterReceive I2cRegPtr Cnt T str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	9
k_SpurSensorl2CAddress_Cnt_u08	10
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT	87
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55 66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target I2c GenStopCond I2cRegPtr Cnt T str.PID11	1204
target I2c GenStopCond I2cRegPtr Cnt T str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target I2c GenStopCond I2cRegPtr Cnt T str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	3
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	66

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Name	Input Value	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	
target I2c Send I2cRegPtr Cnt T str.PID12	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	
target I2c SetRecv I2cRegPtr Cnt T str.PID11	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	
	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	2	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR		
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR	556	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.DIN	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	
	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD		
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	

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DigColPsInt\_InterruptNotification

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Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	2309		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	2309		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	5		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3		
target_i2cREG1_temp.OAR	55		
target i2cREG1 temp.IMR	66		
target_i2cREG1_temp.STR	556		
target i2cREG1 temp.CLKL	2309		
target i2cREG1 temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target i2cREG1 temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target i2cREG1 temp.MDR	2309		
target i2cREG1 temp.IVR	5		
target i2cREG1 temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target i2cREG1 temp.PID12	66		
target i2cREG1 temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target i2cREG1 temp.DIR	1		
target i2cREG1 temp.DIN	2		
target i2cREG1_temp.DOUT	3		
target i2cREG1 temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
		Francis d Malica	D
Name  DisColleget Attempolecus ForCustDetDeed, Cet M, v00	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	~
DigColPsInt_Buffer_Cnt_M_u08[0]	32	32	~
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	•
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	<u> </u>
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	•
DigColPsInt ColCustDatFound Cnt M lgc	1	1.3	I 📦

2309

DigColPsInt\_ColCustDatFound\_Cnt\_M\_lgc

DigColPsInt\_ColSnsrData\_Cnt\_M\_u16

1 2309

2014-10-14, 23:42:41+0530



MacCoPart Committee Crit No St.   Marco   Ma	M	A -41 V-1	Form a set of Malions	D14
Displace  Commissions   Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions  Displace  Commissions	Name	Actual Value	Expected Value	Result
Dipolar Public Deline (Content of March 1997)   1		-		-
Digital Part   Digi				
Digits   Principate   Company   Co				
Digita Perint Neudocured On M. 192   0   0   0   V   Digita Perint Recordinality or CM M. 100   0   0   0   0   0   0   0   0   0				
Disputable Recolorumations C.M. May   Disputable Recolorumations C.M				
Digitability Special Project (MLAUS)  Digitability Special Special Project (MLAUS)  Digitability Special Special Project (MLAUS)  Digitability Special Special Project (MLAUS)  To ST				
Digits   D			0	<b>✓</b>
Disposition   Transaction of Cold   Miles   10   10   10   10   10   10   10   1		0	0	~
Image   Dec.   GenShapeCond   DeckeyPr. Cell   Jan Folks   196   196   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197   197	DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	<b>✓</b>
	DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	~
Langer, I.E.C. Gent StopCoot, I.E.Regin TO. 11, 181-STR  1899   E.C. Gent StopCoot, I.E.Regin TO. 11, 181-CRL  1909   E.C. Gent StopCoot, I.E.Regin TO. 11,	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	•
Imaged   Dec.   Centifortion   December   Cent   T. set C.H.H.   2004   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205   1205	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	~
September   Sept	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	~
### STATES	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	-
Second Second Control (1)   18 m	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	
	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT			-
Imaged   120, Centification   120, Personal Process	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR			
### Internal Life Centrological Centrologica				
Section   Sect				
Image   120   GenStonCond   Zelengh PC of T, set PEND R				
Image   120   Cents   150				
Image LPD, CeeStopCond, Josephy Cott, J. str PD11				_
Single   120   GenSingCond   2648pg PC on   1   Sing PD12				
target_Lize_GenSiopCond_LizeRegPT_Cnt_T at PLUN         1           target_Lize_GenSiopCond_LizeRegPT_Cnt_T at PLUN         1           target_Lize_GenSiopCond_LizeRegPT_Cnt_T at PLUN         1           target_Lize_GenSiopCond_LizeRegPT_Cnt_T at PLUN         1           target_Lize_GenSiopCond_LizeRegPT_Cnt_T at PLUN         2           target_Lize_GenSiopCond_LizeRegPT_Cnt_T at PLUN         3           target_Lize_GenSiopCond_LizeRegPT_Cnt_T at PLUN         1           target_Lize_GenSiopCond_LizeRegPT_Cnt_T at PLUN         1           target_Lize_GenSiopCond_LizeRegPT_Cnt_T at PLUN         3           target_Lize_GenSiopCond_LizeRegPT_Cnt_T at PLUN         55           target_Lize_GenSiopCond_LizeRegPT_Cnt_T at PLUN         55           target_Lize_GenSiopCond_LizeRegPT_Cnt_T at PLUN         55           target_Lize_GenSiopCond_LizeRegPT_Cnt_T at PLUN         55           target_Lize_GenSiopCond_LizeRegPT_Cnt_T at PLUN         66           target_Lize_GenSionCond_LizeRegPT_Cnt_T at PLUN         67           target_Lize_GendPT_Cnt_T at PLUN         67				-
target_Lize_GenStopCond_E2Releght_Cont_T sit PIN         1         1           target_Lize_GenStopCond_E2Releght_Cont_T sit DIN         2         2           target_Re_GenStopCond_E2Releght_Cont_T sit DIN         2         2           target_Re_GenStopCond_E2Releght_Cont_T sit DIN         3         3           target_Re_GenStopCond_E2Releght_Cont_T sit DONT         3         3           target_Lize_GenStopCond_E2Releght_Cont_T sit DONT         1         1           target_Lize_GenStopCond_E2Releght_Cont_T sit DONT         3         3           target_Lize_GenStopCond_E2Releght_Cont_T sit DONT         3         3           target_Lize_GenStopCond_E2Releght_Cont_T sit DONT         3         3           target_Lize_GenStopCond_E2Releght_Cont_T sit DONT         55         55           target_Lize_Send_E2Releght_Cont_T sit DONT         66         6           target_Lize_Send_E2Releght_Cont_T sit DONT         66         6           target_Lize_Send_E2Releght_Cont_T sit DONT         66         6           target_Lize_Send_E2Releght_Cont_T sit DONT         67         87           target_Lize_Send_E2Releght_Cont_T sit DONT         67         67           target_Lize_Send_E2Releght_Cont_T sit DONT         66         66           varget_Lize_Send_E2Releght_Cont_T sit DONT         66				
Engel   Dec GenStepCond   ZeRegPt Cnt   T at DIR   1   1   1   1   1   1   1   1   1				_
			· ·	
target_12e_GenStopCond_12eRegPtr_Cntstr_SET 3 3 3 3 4				
surget_L2c_GenSlopCond_L2cRepPt_Cnt_T_str.CLR				
target L2c. GenStopCond, L2cRegPtr, Cnt.T, str CDR 2 2 2 2 3 3 3 4 4 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1				-
singel 12c, GenStopCond, 12cRepPtr, Cnt, T, str. PDR         2         2           singel 12c, GenStopCond, 12cRepPtr, Cnt, T, str. PDR         3         3           singel 12c, GenStopCond, 12cRepPtr, Cnt, T, str. PDR         3         3           singel 12c, Send, 12cRepPtr, Cnt, T, str. ARR         55         55           singel 12c, Send, 12cRepPtr, Cnt, T, str. ALR         66         66           singel 12c, Send, 12cRepPtr, Cnt, T, str. CLKI         2309         2309           singel 12c, Send, 12cRepPtr, Cnt, T, str. CLKI         1204         1204           singel 12c, Send, 12cRepPtr, Cnt, T, str. CLKI         1204         1204           singel 12c, Send, 12cRepPtr, Cnt, T, str. CLKI         1204         1204           singel 12c, Send, 12cRepPtr, Cnt, T, str. CLKI         1204         1204           singel 12c, Send, 12cRepPtr, Cnt, T, str. CLKI         67         67           singel 12c, Send, 12cRepPtr, Cnt, T, str. ARR         67         67           singel 12c, Send, 12cRepPtr, Cnt, T, str. ARR         55         55           singel 12c, Send, 12cRepPtr, Cnt, T, str. ARR         55         55           singel 12c, Send, 12cRepPtr, Cnt, T, str. ARR         56         66           singel 12c, Send, 12cRepPtr, Cnt, T, str. ARR         56         66           singel 12c, Send, 12cRepPtr, C				
target L2c, GenStopCond, L2cRegPtr, Cnt, T., str. PD         3         3         3           target L2c, GenStopCond, L2cRegPtr, Cnt, T., str. PSL         3         3         3           target L2c, GenStopCond, L2cRegPtr, Cnt, T., str. PSL         55         55         55           target L2c, Send, L2cRegPtr, Cnt, T., str. LSR         566         66         66           target L2c, Send, L2cRegPtr, Cnt, T., str. CNL         2309         2308         7           target L2c, Send, L2cRegPtr, Cnt, T., str. CNL         1204         1204         7           target L2c, Send, L2cRegPtr, Cnt, T., str. CNR         67         67         87           target L2c, Send, L2cRegPtr, Cnt, T., str. CNR         67         67         67         47           target L2c, Send, L2cRegPtr, Cnt, T., str. CNR         67         67         67         47           target L2c, Send, L2cRegPtr, Cnt, T., str. CNR         66         66         66         47           target L2c, Send, L2cRegPtr, Cnt, T., str. CNR         55         55         55         55           target L2c, Send, L2cRegPtr, Cnt, T., str. CNR         66         66         66         47           target L2c, Send, L2cRegPtr, Cnt, T., str. CNR         5         5         4           target L2c, Send, L2cRegPtr, Cnt, T., str. CNR				•
singet   12c   Send   12cRepPr   Cnt   T str PSL   3   3   3   4   4   4   4   4   4   4				~
target_ 2c_Send_!2cRegPtr_Cntstr.DAR    farget_ 2c_Send_!2cRegPtr_Cntstr.STRR    566   66   66   √     target_ 2c_Send_!2cRegPtr_Cntstr.STRR    556   556   556   ✓     target_ 2c_Send_!2cRegPtr_Cntstr.STRR    556   556   556   ✓     target_ 2c_Send_!2cRegPtr_Cntstr.CLKL    2309   2309   2309   ✓     target_ 2c_Send_!2cRegPtr_Cntstr.CLKL    1204   1204   1204   ✓     target_ 2c_Send_!2cRegPtr_Cntstr.CKNT    87   87   87   ✓     target_ 2c_Send_!2cRegPtr_Cntstr.CKNT    87   67   67   67   ✓     target_ 2c_Send_!2cRegPtr_Cntstr.DKR    55   55   55     target_ 2c_Send_!2cRegPtr_Cntstr.DKR    66   66   66   ✓     target_ 2c_Send_!2cRegPtr_Cntstr.DKR    75   75   75   75     target_ 2c_Send_!2cRegPtr_Cntstr.DKR    80   2309   2309   ✓     target_ 2c_Send_!2cRegPtr_Cntstr.DKR    81   82   309   2309   ✓     target_ 2c_Send_!2cRegPtr_Cntstr.DKR    82   309   2309   ✓     target_ 2c_Send_!2cRegPtr_Cntstr.DKR    83   3   ✓     target_ 2c_Send_!2cRegPtr_Cntstr.DKR    84   30   3   3   ✓     target_ 2c_Send_!2cRegPtr_Cntstr.DKR    85   66   66   ✓     target_ 2c_Send_!2cRegPtr_Cntstr.DMAC    80   30   30   ✓     target_ 2c_Send_!2cRegPtr_Cntstr.DMAC    80   30   30   ✓     target_ 2c_Send_!2cRegPtr_Cntstr.DMAC    80   30   30   ✓     target_ 2c_Send_!2cRegPtr_Cntstr.DMAC    81   1   1   ✓     target_ 2c_Send_!2cRegPtr_Cntstr.DMAC    81   1   1   ✓     target_ 2c_Send_!2cRegPtr_Cntstr.DMAC    81   3   3   ✓     target_ 2c_Send_!2cRegPtr_Cntstr.DMAC    81   3   3   ✓     target_ 2c_Send_!2cRegPtr_Cntstr.DMAC    82   2   2   ✓     target_ 2c_Send_!2cRegPtr_Cntstr.DMAC    83   3   3   ✓     target_ 2c_Send_!2cRegPtr_Cntstr.DMAC    81   3   3   3   ✓     target_ 2c_Send_!2cRegPtr_Cntstr.DMAC    82   3   3   3   ✓     target_ 2c_Send_!2cRegPtr_Cntstr.DMAC    83   3   3   ✓     target_ 2c_Send_!2cRegPtr_Cntstr.DMAC    84   3   3   3   ✓     target_ 2c_Send_!2cRegPtr_Cntstr.DMAC    85   3   3   3   ✓     target_ 2c_Send_!2cRegPtr_Cntstr.DMAC    85   3   3   3   ✓			3	<b>✓</b>
target_12c_Send_12cRegPtr_CntT_str.STR  556  556  556  556  556  556  556  5	target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_ Zc_Send_ ZcRegPtr_Cnt_T str.CLK    1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204   1204	target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_12c_Send_12cRegPtr_Cnt_Tstr.CNT         1204           target_12c_Send_12cRegPtr_Cnt_Tstr.CNT         87           target_12c_Send_12cRegPtr_Cnt_Tstr.CNR         67           target_12c_Send_12cRegPtr_Cnt_Tstr.DNR         66           target_12c_Send_12cRegPtr_Cnt_Tstr.DNR         66           def         46           target_12c_Send_12cRegPtr_Cnt_Tstr.DNR         66           def         46           def         47           target_12c_Send_12cRegPtr_Cnt_Tstr.DNR         5           target_12c_Send_12cRegPtr_Cnt_Tstr.DNR         5           target_12c_Send_12cRegPtr_Cnt_Tstr.ENDR         3           target_12c_Send_12cRegPtr_Cnt_Tstr.DD11         1204           target_12c_Send_12cRegPtr_Cnt_Tstr.DD12         66           de         66	target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_[2c_Send_ 2cRegPir_Cnt_T_str.DRR	target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_[2c_Send_]2cRegPtr_Cnt_T_str.DRR         67         67           target_[2c_Send_]2cRegPtr_Cnt_T_str.SAR         55         55           target_[2c_Send_]2cRegPtr_Cnt_T_str.MDR         66         66           target_[2c_Send_]2cRegPtr_Cnt_T_str.MDR         2309         2309           target_[2c_Send_]2cRegPtr_Cnt_T_str.MDR         5         5           target_[2c_Send_]2cRegPtr_Cnt_T_str.DNR         3         3           target_[2c_Send_]2cRegPtr_Cnt_T_str.DNDR         3         3           target_[2c_Send_]2cRegPtr_Cnt_T_str.DDT         66         66           target_[2c_Send_]2cRegPtr_Cnt_T_str.DDT2         66         66           target_[2c_Send_]2cRegPtr_Cnt_T_str.DMAC         3         3           target_[2c_Send_]2cRegPtr_Cnt_T_str.DNAC         3         3           target_[2c_Send_]2cRegPtr_Cnt_T_str.DNT         1         1           target_[2c_Send_]2cRegPtr_Cnt_T_str.DNT         1         1           target_[2c_Send_]2cRegPtr_Cnt_T_str.DNT         2         2           target_[2c_Send_]2cRegPtr_Cnt_T_str.DOUT         3         3           target_[2c_Send_]2cRegPtr_Cnt_T_str.DDR         2         2           target_[2c_Send_]2cRegPtr_Cnt_T_str.DR         2         2           target_[2c_Send_]2cRegPtr_Cnt_T_str.DR         3	target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
Larget_12c_Send_12cRegPtr_Cnt_T_str.DAR   55   55   55   55   55   55   55	target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_12c_Send_12cRegPtr_Cnt_T_str.DXR         66         66           target_12c_Send_12cRegPtr_Cnt_T_str.MDR         2309         2309           varget_12c_Send_12cRegPtr_Cnt_T_str.WR         5         5           target_12c_Send_12cRegPtr_Cnt_T_str.EMDR         3         3           varget_12c_Send_12cRegPtr_Cnt_T_str.PDC1         66         66           target_12c_Send_12cRegPtr_Cnt_T_str.PD11         1204         1204           target_12c_Send_12cRegPtr_Cnt_T_str.DMAC         3         3           target_12c_Send_12cRegPtr_Cnt_T_str.DMAC         3         3           target_12c_Send_12cRegPtr_Cnt_T_str.DIN         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DIN         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DIN         2         2           target_12c_Send_12cRegPtr_Cnt_T_str.DOUT         3         3           target_12c_Send_12cRegPtr_Cnt_T_str.SET         3         3           target_12c_Send_12cRegPtr_Cnt_T_str.DOR         2         2           target_12c_Send_12cRegPtr_Cnt_T_str.DOR         2         2           target_12c_Send_12cRegPtr_Cnt_T_str.DOR         3         3           target_12c_Send_12cRegPtr_Cnt_T_str.MR         66         66           varget_12c_SenRecv_12cRegPtr_Cnt_T_str.MR         66 </td <td>target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR</td> <td>67</td> <td>67</td> <td>~</td>	target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.NDR         2309         2309         ✓           target_I2c_Send_I2cRegPtr_Cnt_T_str.NDR         5         5         ✓           target_I2c_Send_I2cRegPtr_Cnt_T_str.NDR         3         3         3           target_I2c_Send_I2cRegPtr_Cnt_T_str.PDC         66         66         66         ✓           target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12         66         66         66         ✓           target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC         3         3         3         ✓           target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC         3         3         3         ✓           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN         1         1         1         ✓         ✓           target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN         2         2         2         ✓         ✓           ✓                ✓            ✓	target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_!2c_Send_!2cRegPtr_Cnt_T_str.IVR				~
target_!2c_Send_!2cRegPtr_Cnt_T_str.EMDR         3         3           target_!2c_Send_!2cRegPtr_Cnt_T_str.PiD11         1204         1204           target_!2c_Send_!2cRegPtr_Cnt_T_str.PiD11         1204         1204           target_!2c_Send_!2cRegPtr_Cnt_T_str.DID12         66         66           target_!2c_Send_!2cRegPtr_Cnt_T_str.DMAC         3         3           target_!2c_Send_!2cRegPtr_Cnt_T_str.DIN         1         1           target_!2c_Send_!2cRegPtr_Cnt_T_str.DIN         1         1           target_!2c_Send_!2cRegPtr_Cnt_T_str.DIN         2         2           target_!2c_Send_!2cRegPtr_Cnt_T_str.DOUT         3         3           target_!2c_Send_!2cRegPtr_Cnt_T_str.SET         3         3           target_!2c_Send_!2cRegPtr_Cnt_T_str.CR         1         1           target_!2c_Send_!2cRegPtr_Cnt_T_str.OR         1         1           target_!2c_Send_!2cRegPtr_Cnt_T_str.DOR         2         2           target_!2c_Send_!2cRegPtr_Cnt_T_str.PD         3         3           target_!2c_Send_!2cRegPtr_Cnt_T_str.DAR         5           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR         5           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.STR         56           target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CNT         87           target_!2c_SetRe				
target 12c_Send_12cRegPtr_Cnt_T_str.PSC       66       66         target 12c_Send_12cRegPtr_Cnt_T_str.PID11       1204       1204         target 12c_Send_12cRegPtr_Cnt_T_str.PID12       66       66         target 12c_Send_12cRegPtr_Cnt_T_str.PIDAC       3       3         target 12c_Send_12cRegPtr_Cnt_T_str.DMAC       3       3         target 12c_Send_12cRegPtr_Cnt_T_str.DIN       1       1         target 12c_Send_12cRegPtr_Cnt_T_str.DIN       2       2         target 12c_Send_12cRegPtr_Cnt_T_str.DOUT       3       3         target 12c_Send_12cRegPtr_Cnt_T_str.SET       3       3         target 12c_Send_12cRegPtr_Cnt_T_str.DOUT       3       3         target 12c_Send_12cRegPtr_Cnt_T_str.DOR       1       1         target 12c_Send_12cRegPtr_Cnt_T_str.DOR       2       2         target 12c_Send_12cRegPtr_Cnt_T_str.DD       3       3         target 12c_Send_12cRegPtr_Cnt_T_str.DAR       3       3         target 12c_Send_12cRegPtr_Cnt_T_str.DAR       55       55         target 12c_SelRecv_12cRegPtr_Cnt_T_str.DAR       55       55         target 12c_SelRecv_12cRegPtr_Cnt_T_str.DAR       66       66         target 12c_SelRecv_12cRegPtr_Cnt_T_str.CLK       200       200         target 12c_SelRecv_12cRegPtr_Cnt_T				
target_12c_Send_12cRegPtr_Cnt_T_str.PID11         1204         1204           target_12c_Send_12cRegPtr_Cnt_T_str.PID12         66         66           target_12c_Send_12cRegPtr_Cnt_T_str.DIMAC         3         3           target_12c_Send_12cRegPtr_Cnt_T_str.DIN         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DIR         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DIN         2         2           target_12c_Send_12cRegPtr_Cnt_T_str.DUT         3         3           target_12c_Send_12cRegPtr_Cnt_T_str.DUT         3         3           target_12c_Send_12cRegPtr_Cnt_T_str.DET         3         3           target_12c_Send_12cRegPtr_Cnt_T_str.DDR         1         1           target_12c_Send_12cRegPtr_Cnt_T_str.DDR         2         2           target_12c_Send_12cRegPtr_Cnt_T_str.DDR         3         3           target_12c_Send_12cRegPtr_Cnt_T_str.PSL         3         3           target_12c_Send_12cRegPtr_Cnt_T_str.DAR         55         55           target_12c_SetRecv_12cRegPtr_Cnt_T_str.DAR         55         55           target_12c_SetRecv_12cRegPtr_Cnt_T_str.DAR         66         66           target_12c_SetRecv_12cRegPtr_Cnt_T_str.CLKI         2309         2309           target_12c_SetRecv_12cRegPtr_Cnt_T_str.DAR				
target_12c_Send_12cRegPtr_Cnt_T_str.PID12       66       66         target_12c_Send_12cRegPtr_Cnt_T_str.DMAC       3       3         target_12c_Send_12cRegPtr_Cnt_T_str.PIDN       1       1         target_12c_Send_12cRegPtr_Cnt_T_str.DIR       1       1         target_12c_Send_12cRegPtr_Cnt_T_str.DIN       2       2         target_12c_Send_12cRegPtr_Cnt_T_str.DUT       3       3         target_12c_Send_12cRegPtr_Cnt_T_str.DUT       3       3         target_12c_Send_12cRegPtr_Cnt_T_str.DET       3       3         target_12c_Send_12cRegPtr_Cnt_T_str.DDR       1       1         target_12c_Send_12cRegPtr_Cnt_T_str.DDR       2       2         target_12c_Send_12cRegPtr_Cnt_T_str.DDR       2       2         target_12c_Send_12cRegPtr_Cnt_T_str.DDR       3       3         target_12c_Send_12cRegPtr_Cnt_T_str.DAR       3       3         target_12c_Send_12cRegPtr_Cnt_T_str.DAR       55       55         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DAR       66       66         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DAR       66       66         target_12c_SetRecv_12cRegPtr_Cnt_T_str.CLK       2309       2309         target_12c_SetRecv_12cRegPtr_Cnt_T_str.DAR       67       67         target_12c_SetRecv_12cRegPtr_Cnt_T_str.				
target_ 2c_Send_ 2cRegPtr_Cnt_T_str.DMAC         3         3           target_ 2c_Send_ 2cRegPtr_Cnt_T_str.FUN         1         1           target_ 2c_Send_ 2cRegPtr_Cnt_T_str.DIR         1         1           target_ 2c_Send_ 2cRegPtr_Cnt_T_str.DIN         2         2           target_ 2c_Send_ 2cRegPtr_Cnt_T_str.DOUT         3         3           target_ 2c_Send_ 2cRegPtr_Cnt_T_str.SET         3         3           target_ 2c_Send_ 2cRegPtr_Cnt_T_str.CLR         1         1           target_ 2c_Send_ 2cRegPtr_Cnt_T_str.DOR         2         2           target_ 2c_Send_ 2cRegPtr_Cnt_T_str.DOR         2         2           target_ 2c_Send_ 2cRegPtr_Cnt_T_str.DOR         3         3           target_ 2c_Send_ 2cRegPtr_Cnt_T_str.DAR         3         3           target_ 2c_Send_ 2cRegPtr_Cnt_T_str.DAR         3         3           target_ 2c_SetRecv_ 2cRegPtr_Cnt_T_str.OAR         55         55           target_ 2c_SetRecv_ 2cRegPtr_Cnt_T_str.STR         56         66           target_ 2c_SetRecv_ 2cRegPtr_Cnt_T_str.CLKL         2309         2309           target_ 2c_SetRecv_ 2cRegPtr_Cnt_T_str.CLKL         2309         2309           target_ 2c_SetRecv_ 2cRegPtr_Cnt_T_str.DAR         67         67           target_ 2c_SetRecv_ 2cRegPtr_Cnt_T_str.DAR				
target_12c_Send_12cRegPtr_Cnt_T_str.FUN       1       1       4         target_12c_Send_12cRegPtr_Cnt_T_str.DIR       1       1       4         target_12c_Send_12cRegPtr_Cnt_T_str.DIN       2       2       2         target_12c_Send_12cRegPtr_Cnt_T_str.DOUT       3       3       3         target_12c_Send_12cRegPtr_Cnt_T_str.SET       3       3       3         target_12c_Send_12cRegPtr_Cnt_T_str.DLR       1       1       4         target_12c_Send_12cRegPtr_Cnt_T_str.DDR       2       2       2         target_12c_Send_12cRegPtr_Cnt_T_str.DD       3       3       3         target_12c_Send_12cRegPtr_Cnt_T_str.DAR       3       3       3         target_12c_Send_12cRegPtr_Cnt_T_str.OAR       3       3       3         target_12c_Send_12cRegPtr_Cnt_T_str.OAR       55       55       55         target_12c_Send_12cRegPtr_Cnt_T_str.MR       66       66       4         target_12c_Send_12cRegPtr_Cnt_T_str.CLKL       2309       2309       4         target_12c_Send_12cRegPtr_Cnt_T_str.CLKL       2309       2309       4         target_12c_Send_12cRegPtr_Cnt_T_str.DAR       67       67       67         target_12c_Send_12cRegPtr_Cnt_T_str.DAR       67       67       67				
target_!2c_Send_!2cRegPtr_Cnt_T_str.DIR       1       1         target_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       2       2         target_!2c_Send_!2cRegPtr_Cnt_T_str.DOUT       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.DUT       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.CLR       1       1         target_!2c_Send_!2cRegPtr_Cnt_T_str.ODR       2       2         target_!2c_Send_!2cRegPtr_Cnt_T_str.PD       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.DAR       3       3         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.OAR       55       55         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IMR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.STR       556       556         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKL       2309       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKL       2309       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CNT       87       87         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       67       67         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.SAR       55       55         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.MDR       66       66         target_!2				
target_!2c_Send_!2cRegPtr_Cnt_T_str.DIN       2       2         target_!2c_Send_!2cRegPtr_Cnt_T_str.DOUT       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.SET       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.CLR       1       1         target_!2c_Send_!2cRegPtr_Cnt_T_str.ODR       2       2         target_!2c_Send_!2cRegPtr_Cnt_T_str.PD       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.PD       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.PSL       3       3         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.OAR       55       55         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IMR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.STR       556       556         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKL       2309       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKH       1204       1204         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       67       67         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       67       67         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.MDR       2309       2309         target				
target_!2c_Send_!2cRegPtr_Cnt_T_str.DOUT       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.SET       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.CLR       1       1         target_!2c_Send_!2cRegPtr_Cnt_T_str.DDR       2       2         target_!2c_Send_!2cRegPtr_Cnt_T_str.PD       3       3         target_!2c_Send_ergPtr_Cnt_T_str.PSL       3       3         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.OAR       55       55         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IMR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.STR       556       556         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKL       2309       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKH       1204       1204         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       67       67         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       67       67         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66       66         ta				
target_!2c_Send_!2cRegPtr_Cnt_T_str.SET       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.CLR       1       1         target_!2c_Send_!2cRegPtr_Cnt_T_str.ODR       2       2         target_!2c_Send_!2cRegPtr_Cnt_T_str.PD       3       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.PSL       3       3         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.OAR       55       55         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.OAR       55       55         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.NIR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.STR       556       556         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKL       2309       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKH       1204       1204         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DKT       87       87         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       67       67         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.MDR       2309       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       55       55				
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR       1       1         target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR       2       2         target_I2c_Send_I2cRegPtr_Cnt_T_str.PD       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL       3       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR       55       55         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR       66       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR       556       556         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL       2309       2309         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH       1204       1204         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT       87       87         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR       67       67         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR       66       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR       66       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR       66       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR       2309       2309         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR       5       5				
target_!2c_Send_!2cRegPtr_Cnt_T_str.ODR       2       2         target_!2c_Send_!2cRegPtr_Cnt_T_str.PD       3         target_!2c_Send_!2cRegPtr_Cnt_T_str.PSL       3         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.OAR       55         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IMR       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.STR       556         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKL       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKH       1204         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CNT       87         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       67         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR       67         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DAR       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.MDR       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IVR       5				
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD       3       3         target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR       55         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR       556         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL       2309         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH       1204         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT       87         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR       67         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR       55         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR       2309         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.NDR       5         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR       5				
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL       3       3         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR       55       55         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR       66       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR       556       556         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL       2309       2309         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH       1204       1204         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT       87       87         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR       67       67         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR       55       55         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR       66       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DAR       66       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR       2309       2309         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.NDR       5       5				
target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.OAR       55       55         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IMR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.STR       556       556         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKL       2309       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKH       1204       1204         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CNT       87       87         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       67       67         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.SAR       55       55         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.MDR       2309       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IVR       5       5				
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR       66       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR       556       556         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL       2309       2309         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH       1204       1204         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT       87       87         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR       67       67         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR       55       55         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR       66       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR       2309       2309         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR       5       5				•
target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.STR       556       556         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKL       2309       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKH       1204       1204         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CNT       87       87         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       67       67         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.SAR       55       55         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.MDR       2309       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IVR       5       5				_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL       2309       2309         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH       1204       1204         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT       87       87         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR       67       67         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR       55       55         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR       66       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR       2309       2309         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR       5       5				
target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CLKH       1204       1204         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.CNT       87       87         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DRR       67       67         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.SAR       55       55         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.DXR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.MDR       2309       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IVR       5       5				
target_!2c_SetRecv_!2cRegPtr_Cntstr.CNT       87       87         target_!2c_SetRecv_!2cRegPtr_Cntstr.DRR       67       67         target_!2c_SetRecv_!2cRegPtr_Cntstr.SAR       55       55         target_!2c_SetRecv_!2cRegPtr_Cntstr.DXR       66       66         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.MDR       2309       2309         target_!2c_SetRecv_!2cRegPtr_Cnt_T_str.IVR       5       5				
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR       67       67         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR       55       55         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR       66       66         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR       2309       2309         target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR       5       5				~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR       55       55         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR       66       66         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR       2309       2309         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR       5       5				<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR       66       66       ✓         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR       2309       2309       ✓         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR       5       5       ✓			55	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR       2309       2309         target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR       5       5			66	~
- 3-12 - 12-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1		2309	2309	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR 3	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	5	5	~
	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	~

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	66	66	
target I2c SetRecv I2cRegPtr Cnt T str.FUN	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target I2c SetRecv I2cRegPtr Cnt T str.SET	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2 3	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT		3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	
target I2c SetStatus I2cRegPtr Cnt T str.PSL	3	3	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	55	55	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.IMR	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKH	1204	1204	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DRR	67	67	•
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SAR	55	55	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DXR	66	66	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	•
	LEE	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	66 2309	2309	•

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSL

DigColPsInt\_InterruptNotification

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c_Send	1	I2c_Send	1	~

3

3

Test Step 3.26 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt CmdFailOccurred Cnt M Igc	1
DigColPsInt ColCustDatFound Cnt M Igc	1
DigColPsInt ColSnsrData Cnt M u16	2309
DigColPsInt CurrentSlave Cnt M u08	123
DigColPsInt CurrentStepNo Cnt M enum	INIT SENSOR2 SENDCMD
DigColPsInt I2CHwCustData Uls M u16	1
DigColPsInt I2CHwIncompleteCustData Uls M u16	2
DigColPsInt InitFailedOnce Cnt M Igc	0
DigColPsInt NackOccured Cnt M Igc	0
DigColPsInt PrevRegDataType Cnt M u08	1
DigColPsInt RecvOverrunError Cnt M Igc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt SkipRegisterWrite Cnt M lgc	0
DigColPsInt SpurCustDatFound Cnt M Igc	0
DigColPsInt SpurSnsrData Cnt M u16	87
DigColPsInt TransactionCnt Cnt M u08	10
Flags_Cnt_T_b16	4
l2c_GenStopCond(l2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c SetupMasterReceive(I2cRegPtr Cnt T str)	target I2c SetupMasterReceive I2cRegPtr Cnt T str
I2c SetupMasterTransmit(I2cRegPtr Cnt T str)	target I2c SetupMasterTransmit I2cRegPtr Cnt T str
T DataRegisters Cnt u08[0]	0
	32
T_DataRegisters_Cnt_u08[1]	30
T_DataRegisters_Cnt_u08[2]	36
T_DataRegisters_Cnt_u08[3]	38
T_DataRegisters_Cnt_u08[4]	34
T_DataRegisters_Cnt_u08[5]	
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	9
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87

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		- 100
Name	Input Value	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	
target I2c GenStopCond I2cRegPtr Cnt T str.MDR	2309	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	
target I2c GenStopCond I2cRegPtr Cnt T str.FUN	1	
target I2c GenStopCond I2cRegPtr Cnt T str.DIR	1	
· · · · · · · · · · · · · · · · · · ·	2	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN	3	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	
target I2c Send I2cRegPtr Cnt T str.SET	3	
· ·	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR		
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	
	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR		
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	2	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	

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Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target I2c SetStatus I2cRegPtr Cnt T str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target I2c SetStatus I2cRegPtr Cnt T str.DIN	2
	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	556
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66



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Name	Input Value		
target_i2cREG1_temp.STR	556		
target_i2cREG1_temp.CLKL	2309		
target_i2cREG1_temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67 55		
target_i2cREG1_temp.SAR target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target i2cREG1 temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	~
DigColPsInt_Buffer_Cnt_M_u08[0]	32	32	~
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	~
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	_
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	•
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1 2309	1	-
DigColPoint_ColSnsrData_Cnt_M_u16	123	2309	
DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_SETREG	INIT_SENSOR2_CHECKSTAT_SETREG	
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	•
DigColPsInt RecvOverrunError Cnt M Igc	0	0	-
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	-
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	-
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	-
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	-
I2c_Send(Length_Cnt_T_u32)	1	1	•
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC	66	66	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11		1204	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12	1204		
	1204	66	<b>₩</b>
target 12c GenStonCond 12cRegPtr Cnt T str DMAC	66	66	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC	66	3	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	66		•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	66 3 1	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	66 3 1 1	3 1 1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	66 3 1 1 2	3 1 1 2	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FUN target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT	66 3 1 1 2 3	3 1 1 2 3	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FUN target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR	66 3 1 1 2 3 3	3 1 1 2 3 3	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	66 3 1 1 2 3 3	3 1 1 2 3 3 1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DDR	66 3 1 1 1 2 3 3 1 1	3 1 1 2 3 3 1 1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DDR	66 3 1 1 1 2 3 3 1 1 2 3	3 1 1 2 3 3 1 1 2 3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	66 3 1 1 1 2 3 3 1 1 2 3 3	3 1 1 2 3 3 3 1 2 3 3 3	

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	87	87	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66 2309	66 2309	
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2C_Send_I2CRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3 55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55		
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66 556	66 556	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target_lzc_SetStatus_lzcRegPtr_Cnt_1_str.CLKL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH	1204	1204	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	87	87	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	•
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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	•
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	•
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	•
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	•
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	•
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	•
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
rarget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	
arget I2c SetupMasterReceive I2cRegPtr Cnt T str.DIR	1	1	
arget I2c SetupMasterReceive I2cRegPtr Cnt T str.DIN	2	2	•
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	
arget I2c SetupMasterReceive I2cRegPtr Cnt T str.SET	3	3	
arget I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	1	1	
arget I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	2	2	
arget I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	3	3	
arget I2c SetupMasterReceive I2cRegPtr Cnt T str.PSL	3	3	
arget I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	55	55	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	
arget I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	556	556	
arget I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	2309	2309	
arget I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	1204	1204	
arget I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	87	87	
arget I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	67	67	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	55	55	
arget I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	66	66	
arget I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	2309	2309	
arget I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	5	5	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FMDR	3	3	
arget I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	66	66	
	1204	1204	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	66	66	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	3	3	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC		1	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT		· ·	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	•
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	•
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	•

T .				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c Send	1	I2c Send	1	_

Test Step 3.27 (Repeat Count = 1)		<b>~</b>
Name	Input Value	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	
DigColPsInt_Buffer_Cnt_M_u08[0]	10	
DigColPsInt_Buffer_Cnt_M_u08[1]	20	
DigColPsInt_Buffer_Cnt_M_u08[2]	30	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	
DigColPsInt_CurrentSlave_Cnt_M_u08	123	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADADDRREG_SENDCMD	
DigColPsInt_I2CHwCustData_Uls_M_u16	1	
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	

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Name	Input Value
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags Cnt T b16	4
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
2c Send(I2cRegPtr Cnt T str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
_DataRegisters_Cnt_u08[0]	0
	32
_DataRegisters_Cnt_u08[1]	30
_DataRegisters_Cnt_u08[2]	
_DataRegisters_Cnt_u08[3]	36
_DataRegisters_Cnt_u08[4]	38
_DataRegisters_Cnt_u08[5]	34
_DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
_DataRegisters_Cnt_u08[8]	14
2cREG1_temp	target_i2cREG1_temp
_ColSensorl2CAddress_Cnt_u08	9
_SpurSensorl2CAddress_Cnt_u08	10
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
arget I2c GenStopCond I2cRegPtr Cnt T str.PSC	66
arget I2c GenStopCond I2cRegPtr Cnt T str.PID11	1204
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
arget I2c GenStopCond I2cRegPtr Cnt T str.FUN	1
	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
arget_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
	3

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DigColPSIIIL_Interruptivotilication	
Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
arget I2c Send I2cRegPtr Cnt T str.CLR	1
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
	66
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	556
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	66
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
arget I2c SetRecv I2cRegPtr Cnt T str.CLR	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
	66
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	556
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
rarget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
rarget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR	67
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
arget I2c SetStatus I2cRegPtr Cnt T str.SET	3
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
arget I2c SetStatus I2cRegPtr Cnt T str.ODR	2
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
arget_12c_SetStatus_12cRegPtr_Cnt_T_str.PSL	3
arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	55
	66
arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	
arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	556
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
	66
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	
arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PID12 arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMAC arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.FUN	66 3 1

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Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SET	3		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	3		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSL	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	556		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	1		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.ODR	2		
	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL			
target_i2cREG1_temp.OAR	55		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	556		
target_i2cREG1_temp.CLKL	2309		
target_i2cREG1_temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target i2cREG1 temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target i2cREG1 temp.SET	3		
target i2cREG1 temp.CLR	1		
0 =	2		
target_i2cREG1_temp.ODR			
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	~
DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	~
DigColPsInt_Buffer_Cnt_M_u08[1]	128	128	~
DigColPsInt_Buffer_Cnt_M_u08[2]	0	0	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	~
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1 EXTREADCTRLREG SEN	INIT_SENSOR1_EXTREADCTRLREG_SEN	~
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	~
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	~
DigColPsInt InitFailedOnce Cnt M Igc	0	0	-
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	-

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Name	Actual Value	Expected Value	Result
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	<b>~</b>
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	
DigColPoint_SpurSnsrData_Cnt_M_u16	87 10	87 10	
DigColPsInt_TransactionCnt_Cnt_M_u08 target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	
target I2c GenStopCond I2cRegPtr Cnt T str.STR	556	556	·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target I2c GenStopCond I2cRegPtr Cnt T str.CLKH	1204	1204	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>v</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET	3	3	<b>v</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3 55	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	55 66	-
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	556	556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.IVR	5	5	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3	3	<b>Y</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	55	55	<b>Y</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>V</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	556	556	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	· ·
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87 67	87 67	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	55	55	
target_l2c_SetRecv_l2cRegPtr_Cnt_1_str.5AR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	66	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	·
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	J
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>

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Name	Actual Value	Expected Value	Result
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	3	3	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	1	1	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.IMR	66	66	
target I2c SetStatus I2cRegPtr Cnt T str.STR	556	556	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>Y</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3		
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN target_l2c SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	1	1	- J
	2	1 2	Ž
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN target_l2c SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	3	3	- J
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_1_str.DOUT target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	- V
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SE1 target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	2	2	
target I2c SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	2309	2309	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	_
target 12c Setupiviaster Haristilit 12cRegFti Citt I Str.DiviAC			

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~

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Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET	3
target I2c GenStopCond I2cRegPtr Cnt T str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target I2c GenStopCond I2cRegPtr Cnt T str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target I2c Send I2cRegPtr Cnt T str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target I2c SetRecv I2cRegPtr Cnt T str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target I2c SetRecv I2cRegPtr Cnt T str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	55 66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55

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Nome	Innut Value
Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target I2c SetStatus I2cRegPtr Cnt T str.PID12	66
·	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target I2c SetStatus I2cRegPtr Cnt T str.DIR	1
	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target I2c SetupMasterReceive I2cRegPtr Cnt T str.EMDR	3
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
	1
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
	3
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	2309
target I2c SetupMasterTransmit I2cReqPtr Cnt T str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
	2
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target i2cREG1 temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target i2cREG1 temp.SAR	55
target_izertEo1_temp.oArt	
target i2cREG1 temp.DXR	66



Name	Input Value		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Namo	Actual Value	Expected Value	Result

target_i2cREG1_temp.PD	3	3		
target_i2cREG1_temp.PSL	3	3		
Name	Actual Value	Expected Value	Result	
DigColPsInt AttempOccurForCustDatRead Cnt M u08	1	1	~	
DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	<b>~</b>	
DigColPsInt_Buffer_Cnt_M_u08[1]	128	128	-	
DigColPsInt_Buffer_Cnt_M_u08[2]	0	0	-	
DigColPsInt BusBusySeqError Cnt M Igc	0	0	-	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	-	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	-	
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	-	
DigColPsInt CurrentSlave Cnt M u08	123	123	-	
DigColPsInt CurrentStepNo Cnt M enum		N INIT SENSOR2 EXTREADCTRLREG SEN	·	
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1		
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	-	
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0		
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	-	
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0		
DigColPsInt RecvdDataType Cnt M u08	0	0	-	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	,	
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	-	
DigColPsInt TransactionCnt Cnt M u08	10	10	j	
I2c_Send(Length_Cnt_T_u32)	3	3	-	
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	,	
target I2c GenStopCond I2cRegPtr Cnt T str.OAR	55	55	-	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	,	
target I2c GenStopCond I2cRegPtr Cnt T str.STR	556	556		
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	2309	2309	J	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH	1204	1204	-	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT	87	87		
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR	67	67	-	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	-	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	-	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	-	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	-	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	-	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	,	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	j	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	-	
target I2c GenStopCond I2cRegPtr Cnt T str.DIR	1	1		
target I2c GenStopCond I2cRegPtr Cnt T str.DIN	2	2		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3		
target I2c GenStopCond I2cRegPtr Cnt T str.SET	3	3		
target I2c GenStopCond I2cRegPtr Cnt T str.CLR	1	1		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2		
target I2c GenStopCond I2cRegPtr Cnt T str.PD	3	3	j	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3		
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	J	
target_12c_Send_12cRegPtr_Cnt_T_str.IMR	66	66		
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	556	556		
target_12c_Send_12cRegPtr_Cnt_T_str.CLKL	2309	2309		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204		
target_12c_Send_12cRegPtr_Cnt_T_str.CNT	87	87		
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	- 4	
target I2c Send I2cRegPtr Cnt T str.SAR	55	55		
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	66	66		
	2309	2309	· ·	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309		

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Name	Actual Value	Expected Value	Result
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	· ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	<i>y</i>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204 66	1204 66	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12 target_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target I2c Send I2cRegPtr Cnt T str.ODR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	55	55	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	66	66	<b>Y</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>Y</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	1204	1204	<i>-</i>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	66	66	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.DIN	2	2	_
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	·
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>Y</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12	66	66	<b>V</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1 2	1 2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_Setotatus_izcivegrit_Crit_1_str.PGL target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.UMR	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	_

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3	3	<b>✓</b>

T .				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteData	1	SetupWriteData	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c Send	1	I2c Send	1	_

Test Step 3.29 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_SENDCMD
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0

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Name	Input Value
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str) I2c Send(I2cRegPtr Cnt T str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target I2c SetupMasterTransmit I2cRegPtr Cnt T str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	9
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR	66
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR	556
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	1204 87
target_l2c_GenStopCond_l2cRegPtr_Cnt_1_str.CN1 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR	67
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR	55
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	55 66
	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	1204
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3 3
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3 55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
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lame	Input Value
arget I2c SetRecv I2cRegPtr Cnt T str.STR	556
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
arget I2c SetRecv I2cRegPtr Cnt T str.CNT	87
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
arget I2c SetRecv I2cRegPtr Cnt T str.PSC	66
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
arget_12c_SetRecv_12cRegPtr_Cnt_T_str.PID12	66
	3
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	1
irget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
rget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	3
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
irget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
irget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
arget I2c SetStatus I2cRegPtr Cnt T str.PID12	66
	3
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
irget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	
irget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR	1
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
irget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
rget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	3
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
rget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.MDR	2309
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
	3
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
	3
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt T str.SET	
	1
rget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1 2
rrget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET  rrget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR  rrget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR  rrget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	

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Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	1204		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	87		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	1204		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.FUN	1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR	1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	2		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	3		
	3		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	55		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	556		
target_i2cREG1_temp.CLKL	2309		
target_i2cREG1_temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result

target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	~
DigColPsInt_Buffer_Cnt_M_u08[0]	32	32	•
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	~
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	•
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_DUMMY_SEND	INIT_SENSOR1_DUMMY_SEND	•
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	~
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	2	2	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	~
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	~
I2c_Send(Length_Cnt_T_u32)	1	1	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	-

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Name	Actual Value	Expected Value	Resul
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	· ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	
target I2c Send I2cRegPtr Cnt T str.PID11	1204	1204	
target I2c Send I2cRegPtr Cnt T str.PID12	66	66	
target I2c Send I2cRegPtr Cnt T str.DMAC	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	
target I2c Send I2cRegPtr Cnt T str.DIR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	
target I2c Send I2cRegPtr Cnt T str.ODR	2	2	
	3	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL			
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	556	556	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	
		2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	

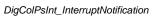
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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	-
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR	55	55	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204 66	1204 66	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	
	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD	3	3	
	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.NRR	556	556	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.EMDR	3	3	
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID12	66	66	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.FUN	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SET	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSL	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	2309	2309	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PUN target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DUT	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOT target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	
target 120 Octupinastor Franklin 1201/Cyfti Oll I St.SET	l o	٦	

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✓
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3	3	<b>✓</b>

Т				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	l2c_Send	1	~

Nome	Innut Value
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_DUMMY_SEND
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target I2c GenStopCond I2cRegPtr Cnt T str
I2c_Send(I2cRegPtr_Cnt_T_str)	target I2c Send I2cRegPtr Cnt T str
I2c SetRecv(I2cRegPtr Cnt T str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
	34
T_DataRegisters_Cnt_u08[5]	
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	9
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1

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Name	Input Value	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	
	1	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	
target I2c Send I2cRegPtr Cnt T str.PSC	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	
target I2c Send I2cRegPtr Cnt T str.SET	3	
· · · · ·	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR		
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	
target I2c SetRecv I2cRegPtr Cnt T str.EMDR	3	
target I2c SetRecv I2cRegPtr Cnt T str.PSC	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
target I2c SetRecv I2cRegPtr Cnt T str.DIR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	
target I2c SetRecv I2cRegPtr Cnt T str.DOUT	3	
	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_SetStatus_I2cRegPti_Cnt_T_str.EMDR	66	
	1204	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11		
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12	66	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DMAC	3	

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Name	Input Value
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
	2309
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
	66
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	67
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target i2cREG1 temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target i2cREG1 temp.CNT	87
target i2cREG1 temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target i2cREG1 temp.EMDR	3
target i2cREG1 temp.PSC	66
	100
target i2cREG1 temp.PID11	1204

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Input Value target\_i2cREG1\_temp.PID12 66 target\_i2cREG1\_temp.DMAC 3 target\_i2cREG1\_temp.FUN target\_i2cREG1\_temp.DIR target\_i2cREG1\_temp.DIN 2 target\_i2cREG1\_temp.DOUT 3 target\_i2cREG1\_temp.SET 3 target\_i2cREG1\_temp.CLR 1 et i2cREG1 temp.ODR

target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	~
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	~
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	~
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	~
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_DUMMY_READ	INIT_SENSOR1_DUMMY_READ	•
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	~
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	<b>*</b>
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	
DigColPsInt_TransactionCnt_Cnt_M_u08	10 2	10	-
I2c_SetRecv(Length_Cnt_T_u32)	2	2 2	
I2c_SetupMasterReceive(DataLength_Cnt_T_u16) target I2c GenStopCond I2cRegPtr Cnt T str.OAR	55	55	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.NRC	556	556	
target I2c GenStopCond I2cRegPtr Cnt T str.CLKL	2309	2309	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC	66	66	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	1204 87	1204 87	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	55	55	
target_lzc_Send_lzcRegPtr_Cnt_I_str.SAR target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	66	66	
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	2309	2309	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	V
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	-
	1	1	

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**Actual Value Expected Value** Result target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DMAC target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.FUN target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DIN target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DOUT target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.SET target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLR  $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.ODR$ target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PD target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.PSL target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.OAR  $target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.IMR$ target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.STR V target I2c SetRecv I2cRegPtr Cnt T str.CLKL target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.CLKH target I2c SetRecv I2cRegPtr Cnt T str.CNT target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DRR target I2c SetRecv I2cRegPtr Cnt T str.SAR target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DXR target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.MDR target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.IVR target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.EMDR target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.PSC target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.PID11 target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.PID12 target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DMAC target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.FUN  $target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DIR$ **~** target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DIN  $target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.DOUT$ target I2c SetRecv I2cRegPtr Cnt T str.SET target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.CLR V target I2c SetRecv I2cRegPtr Cnt T str.ODR ~ target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.PD target\_I2c\_SetRecv\_I2cRegPtr\_Cnt\_T\_str.PSL • target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.OAR  $target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.IMR$ target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.STR target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.CLKL target I2c SetStatus I2cRegPtr Cnt T str.CLKH target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.CNT target I2c SetStatus I2cRegPtr Cnt T str.DRR target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.SAR target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.DXR  $target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.MDR$ target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.IVR  $target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.EMDR$ target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.PSC target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.PID11 target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.PID12 target I2c SetStatus I2cRegPtr Cnt T str.DMAC target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.FUN **~** target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.DIR target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.DIN target I2c SetStatus I2cRegPtr Cnt T str.DOUT target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.SET target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.CLR •  $target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.ODR$ target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.PD **~** target\_I2c\_SetStatus\_I2cRegPtr\_Cnt\_T\_str.PSL  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.OAR$ target I2c SetupMasterReceive I2cRegPtr Cnt T str.IMR  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.STR$ target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.CLKL target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.CLKH target I2c SetupMasterReceive I2cRegPtr Cnt T str.CNT target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.DRR target I2c SetupMasterReceive I2cRegPtr Cnt T str.SAR target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.DXR  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.MDR$  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.IVR$ target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.EMDR  $target\_I2c\_SetupMasterReceive\_I2cRegPtr\_Cnt\_T\_str.PSC$ 

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	

Т				V
Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	~
I2c_SetupMasterReceive	1	l2c_SetupMasterReceive	1	~
I2c_SetRecv	1	l2c_SetRecv	1	~

Test Step 3.31 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_SENDCMD
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str

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Name	Input Value
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp k_ColSensorl2CAddress_Cnt_u08	target_i2cREG1_temp
k SpurSensori2CAddress Cnt u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target I2c GenStopCond I2cRegPtr Cnt T str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target I2c GenStopCond I2cRegPtr Cnt T str.DRR	67
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR	55
target I2c GenStopCond I2cRegPtr Cnt T str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87 67
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	66 2309
target_l2c_Send_l2cRegPtr_Cnt_I_str.WDR target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	5
target_l2c_Send_l2cRegPtr_Cnt_T_str.FMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target I2c Send I2cRegPtr Cnt T str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target I2c Send I2cRegPtr Cnt T str.DMAC	3
target I2c Send I2cRegPtr Cnt T str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
	67

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Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target I2c SetRecv I2cRegPtr Cnt T str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target I2c SetupMasterReceive I2cRegPtr Cnt T str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target I2c SetupMasterReceive I2cRegPtr Cnt T str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	1204
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DigColPsInt\_InterruptNotification

DigCoiPsint_interruptivotilication			Signo
Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3		
target i2cREG1 temp.OAR	55		
target_i2cREG1_temp.IMR	66		
target i2cREG1 temp.STR	556		
target i2cREG1 temp.CLKL	2309		
target i2cREG1 temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
	66		
target_i2cREG1_temp.DXR	2309		
target_i2cREG1_temp.MDR	5		
target_i2cREG1_temp.IVR			
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	0	0	•
DigColPsInt_Buffer_Cnt_M_u08[0]	32	32	•
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	•
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	•
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	•
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	•
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	•
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	•
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	•
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_DUMMY_SEND	INIT_SENSOR2_DUMMY_SEND	•
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	•
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	•
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	•
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	

I2c\_SetupMasterTransmit(DataLength\_Cnt\_T\_u16)

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.OAR$ 

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.IMR

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.STR

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKL

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKH$ 

 ${\tt DigColPsInt\_RecvOverrunError\_Cnt\_M\_lgc}$ 

DigColPsInt\_RecvdDataType\_Cnt\_M\_u08

DigColPsInt\_SpurSnsrData\_Cnt\_M\_u16

DigColPsInt\_TransactionCnt\_Cnt\_M\_u08

I2c\_Send(Length\_Cnt\_T\_u32)

DigColPsInt\_SpurCustDatFound\_Cnt\_M\_lgc

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<b>Y</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✓
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✓
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	2	2	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	66	66	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>v</b>

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Image   170,   Imag	Name	Actual Value	Expected Value	Result
bargor   Dec.   Sessionane   Deckerger   Cut	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
September   Defendence   Defendence   Coll   1 st 5588   50   50   50   50   50   50   50	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	~
Image:     Description:     Description:	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	~
Segret   1965   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966   1966	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
Sept   12,5	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	~
baggs   126, Sestiman, 2008.ppf   Coll   126 PM		2309	2309	<b>✓</b>
Segret   Dec.   SesSimes,   DecRept   Coll   Tes PRIOR				_
Image: Dec. Sections.   DecRept Pot Coll T. or POCI				<b>✓</b>
Image: Page: Self-States, 12-Registry Cont.   Tast PO11   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994   1994				
Impair   D. SalSahan   Deficial Port   Sat DNACE				
Image: Light   Light				
Image: Dec. Selfstein, 2/Rep@Pc, CHT, 1st DIN   2   2   2				
Image   Dec. SerSahus   22ReptPr CNT_set DION   2   2   2   3   3   3   4   4   4   4   4   4   4				-
Image: Lipe Self-Status   JeRospith Cot.   T. str. SET   3   3   3   4   4   4   4   4   4   4	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR			
Improl. 12. SetSetSette, Dicheptin Cot.   1 st 55F   1   1   1   1   1   1   1   1   1	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN			
Image: Res. Selfstates. Dickerpit: Cost. T. art. Col. Rev.   1   2   2   2   3   3   3   3   3   3   3	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
Langer   Line   Selfstatus   Exchanger   Cont.   Jack 2008	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	~
	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✓
Image   DC   Serbish   Defaulty   Cent   List PSE	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	•
Image   Dr. SetSabus   ScReppP; Ont   str PSI	target I2c SetStatus I2cRegPtr Cnt T str.PD	3	3	<b>✓</b>
singel LS, SetupMasterRecove J2CRepft* CNT_str DAR         55           singel LS, SetupMasterRecove J2CRepft* CNT_str DAR         66           singel LS, SetupMasterRecove J2CRepft* CNT_str DAR         56           singel LS, SetupMasterRecove J2CRepft* CNT_str CLKI         2299           singel LS, SetupMasterRecove J2CRepft* CNT_str CLKI         2299           singel LS, SetupMasterRecove J2CRepft* CNT_str CLKI         2299           singel LS, SetupMasterRecove J2CRepft* CNT_str CNT         87           stragel LS, SetupMasterRecove J2CRepft* CNT_str CNT         87           stragel LS, SetupMasterRecove J2CRepft* CNT_str CNT         85           stragel LS, SetupMasterRecove J2CRepft* CNT_str CNT         85           stragel LS, SetupMasterRecove J2CRepft* CNT_str CNT         86           stragel LS, SetupMasterRecove J2CRepft* CNT_str CNT         85           stragel LS, SetupMasterRecove J2CRepft* CNT_str CNT         87           stragel LS, SetupMasterRecove J2CRepft* CNT_str CNT         87           stragel LS, SetupMasterRecove J2CRepft* CNT_str DNT         5           stragel LS, SetupMasterRecove J2CRepft* CNT_str DNT         120           stragel LS, SetupMasterRecove J2Crepft* CNT_str DNT         120           stragel LS, SetupMasterRecove J2Crepft* CNT_str DNT         1           stragel LS, SetupMasterRecove J2Crepft* CNT_str DNT         1				_
singel 20: SetuphiasterReceive J2Regift Cet T_str ENR         66           singel 20: SetuphiasterReceive J2Regift Cet T_str STR         556           singel 20: SetuphiasterReceive J2Regift Cet T_str STR         556           singel 20: SetuphiasterReceive J2Regift Cet T_str CHR         204           singel 20: SetuphiasterReceive J2Regift Cet T_str CHR         1204           singel 20: SetuphiasterReceive J2Regift Cet T_str CHR         1204           singel 20: SetuphiasterReceive J2Regift Cet T_str DRR         67           singel 20: SetuphiasterReceive J2Regift Cet T_str DRR         67           singel 20: SetuphiasterReceive J2Regift Cet T_str DRR         66           singel 20: SetuphiasterReceive J2Regift Cet T_str DRR         66           singel 20: SetuphiasterReceive J2Regift Cet T_str DRR         5           singel 20: SetuphiasterReceive J2Regift Cet T_str DRR         5           singel 20: SetuphiasterReceive J2Regift Cet T_str DRY         5           singel 20: SetuphiasterReceive J2Regift Cet T_str DRY         66           singel 20: SetuphiasterReceive J2Regift Cet T_str DRY         66           singel 20: SetuphiasterReceive J2Regift Cet T_str DRY         1           singel 20: SetuphiasterReceive J2Regift Cet T_str DRY         1           singel 20: SetuphiasterReceive J2Regift Cet T_str DRY         1           singel 20: SetuphiasterReceive J2Regift Ce				-
Image LPD   SemphasterRecoins   ZerRegPt CNT   3 to CLNL   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   2399   239				
Image   126_SetuphsterfReceive   126RegPtr_CRLT_str.CLK				
Integral   120   SetuphidasterReceive   2cRegiPtr_CRLT_str.CNT   87   87   87   87   87   87   87   8				
target_12s_SetuphotasterReceive_12cRegittr_CRLT_str.DRR         67           druget_12s_SetuphotasterReceive_12cRegittr_CRLT_str.DRR         67           druget_12s_SetuphotasterReceive_12cRegittr_CRLT_str.DRR         65           druget_12s_SetuphotasterReceive_12cRegittr_CRLT_str.DRR         66           druget_12s_SetuphotasterReceive_12cRegittr_CRLT_str.DRR         2009           druget_12s_SetuphotasterReceive_12cRegittr_CRLT_str.DRR         5           druget_12s_SetuphotasterReceive_12cRegittr_CRLT_str.DRR         3           druget_12s_SetuphotasterReceive_12cRegittr_CRLT_str.DRR         3           druget_12s_SetuphotasterReceive_12cRegittr_CRLT_str.DRR         3           druget_12s_SetuphotasterReceive_12cRegittr_CRLT_str.DRR         3           druget_12s_SetuphotasterReceive_12cRegittr_CRLT_str.DRR         1           druget_12s_SetuphotasterReceive_12cRegittr_CRLT_str.DRR         3           druget_12s_SetuphotasterReceive_12cRegittr_CRLT_str.DRR         1           druget_12s_SetuphotasterReceive_12cRegittr_CRLT_str.DRR         1           druget_12s_SetuphotasterReceive_12cRegittr_CRLT_str.DRR         1           druget_12s_SetuphotasterReceive_12cRegittr_CRLT_str.DRR         3           druget_12s_SetuphotasterReceive_12cRegittr_CRLT_str.DRR         3           druget_12s_SetuphotasterReceive_12cRegittr_CRLT_str.DRR         3           druget_12s_Setupho				
Engel   Ze_SelupMasterReceive   J20RegPtr_Cnt_T str.DRR	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>~</b>
target 12e, SetupMasterReceive (2RepPtr. Cnt.T. str. SAR         55         55           target 12e, SetupMasterReceive (2RepPtr. Cnt.T. str. DXR         68         68           target 12e, SetupMasterReceive (2RepPtr. Cnt.T. str. DXR         5         5           target 12e, SetupMasterReceive (2RepPtr. Cnt.T. str. DXR         5         5           target 12e, SetupMasterReceive (2RepPtr. Cnt.T. str. EMR         3         3           target 12e, SetupMasterReceive (2RepPtr. Cnt.T. str. PDI11         1204         1204           target 12e, SetupMasterReceive (2RepPtr. Cnt.T. str. PDI11         1204         1204           target 12e, SetupMasterReceive (2RepPtr. Cnt.T. str. DI01         66         66           target 12e, SetupMasterReceive (2RepPtr. Cnt.T. str. DIN         3         3           target 12e, SetupMasterReceive (2RepPtr. Cnt.T. str. DIN         1         1           target 12e, SetupMasterReceive (2RepPtr. Cnt.T. str. DIR         1         1           target 12e, SetupMasterReceive (2RepPtr. Cnt.T. str. DIR         1         1           target 12e, SetupMasterReceive (2RepPtr. Cnt.T. str. DIR         1         1           target 12e, SetupMasterReceive (2RepPtr. Cnt.T. str. DIT         3         3         3           target 12e, SetupMasterReceive (2RepPtr. Cnt.T. str. DIT         3         3         3           <	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	~
Larget   Ze_SetupMasterReceive   26RegPtr_Cnt_T_str.NDR	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
Earget   22_SetupMasterReceive   22-RegPtr_Cnt_strUNR   5	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_12c_SetupMasterReceive_12cRegitr_CntT_str.NDR         2309           target_12c_SetupMasterReceive_12cRegitr_CntT_str.NDR         5           target_12c_SetupMasterReceive_12cRegitr_CntT_str.DDR         3           target_12c_SetupMasterReceive_12cRegitr_CntT_str.DDR         3           target_12c_SetupMasterReceive_12cRegitr_CntT_str.DDR         66           target_12c_SetupMasterReceive_12cRegitr_CntT_str.DDR         66           target_12c_SetupMasterReceive_12cRegitr_CntT_str.DDR         3           target_12c_SetupMasterReceive_12cRegitr_CntT_str.DDR         1           target_12c_SetupMasterReceive_12cRegitr_CntT_str.DDR         1           target_12c_SetupMasterReceive_12cRegitr_CntT_str.DDR         1           target_12c_SetupMasterReceive_12cRegitr_CntT_str.DDR         1           target_12c_SetupMasterReceive_12cRegitr_CntT_str.DDR         3           target_12c_SetupMasterReceive_12cRegitr_CntT_str.Str.DDR         3           target_12c_SetupMasterReceive_12cRegitr_CntT_str.DDR         3           target_12c_SetupMasterReceive_12cRegitr_CntT_str.DDR         1           target_12c_SetupMasterReceive_12cRegitr_CntT_str.DDR         3           target_12c_SetupMasterReceive_12cRegitr_CntT_str.DDR         3           target_12c_SetupMasterTargetr_12c_Regitr_CntT_str.DDR         3           target_12c_SetupMasterTargetr_12c_Regitr_CntT_str.DDR <t< td=""><td>target I2c SetupMasterReceive I2cRegPtr Cnt T str.DXR</td><td>66</td><td>66</td><td><b>✓</b></td></t<>	target I2c SetupMasterReceive I2cRegPtr Cnt T str.DXR	66	66	<b>✓</b>
starget   2c. SetupMasterReceive   2cRegPtr_Cnt_T str_ENDR			2309	_
larget_12e_SetupMasterReceive_12cRegiPt_CntT_strENDR         3           farget_12e_SetupMasterReceive_12cRegiPt_CntT_strPD11         1204           farget_12e_SetupMasterReceive_12cRegiPt_CntT_strPD12         66           farget_12e_SetupMasterReceive_12cRegiPt_CntT_strDNAC         3           farget_12e_SetupMasterReceive_12cRegiPt_CntT_strDNAC         3           farget_12e_SetupMasterReceive_12cRegiPt_CntT_strDNA         1           farget_12e_SetupMasterReceive_12cRegiPt_CntT_strDNA         1           farget_12e_SetupMasterReceive_12cRegiPt_CntT_strDNA         1           farget_12e_SetupMasterReceive_12cRegiPt_CntT_strDNA         2           farget_12e_SetupMasterReceive_12cRegiPt_CntT_strDNA         3           farget_12e_SetupMasterReceive_12cRegiPt_CntT_strDNA         3           farget_12e_SetupMasterReceive_12cRegiPt_CntT_strDNA         3           farget_12e_SetupMasterReceive_12cRegiPt_CntT_strDNA         1           farget_12e_SetupMasterReceive_12cRegiPt_CntT_strDNA         2           farget_12e_SetupMasterReceive_12cRegiPt_CntT_strDNA         3           farget_12e_SetupMasterReceive_12cRegiPt_CntT_strDNA         5           farget_12e_SetupMasterTransmt_12cRegiPt_CntT_strDNA         55           farget_12e_SetupMasterTransmt_12cRegiPt_CntT_strDNA         56           farget_12e_SetupMasterTransmt_12cRegiPt_CntT_strDNA         66				-
target   2c. SetupMasterReceive   12cRegPtr   Cnt   T str   PSC   66   66   66   4   4   4   4   4   4				
target J2c SetupMasterReceive J2cRegPtr Cnt_T str.PID11				
target   2c. SetupMasterReceive   2cRegPtr_Cnt_T_str.DID12         66         66           target   2c. SetupMasterReceive   2cRegPtr_Cnt_T_str.DIMC         3         3           target   2c. SetupMasterReceive   2cRegPtr_Cnt_str.UN         1         1           target   2c. SetupMasterReceive   2cRegPtr_Cnt_str.DIN         1         1           target   2c. SetupMasterReceive   2cRegPtr_Cnt_T_str.DIN         2         2           target   2c. SetupMasterReceive   2cRegPtr_Cnt_T_str.DIV         3         3           target   2c. SetupMasterReceive   2cRegPtr_Cnt_T_str.DIV         3         3           target   2c. SetupMasterReceive   2cRegPtr_Cnt_T_str.DIV         1         1           target   2c. SetupMasterReceive   2cRegPtr_Cnt_T_str.DIV         3         3           target   2c. SetupMasterReceive   2cRegPtr_Cnt_T_str.DIV         5         55           target   2c. SetupMasterTransmit   2cRegPtr_Cnt_T_str.DIV         66         66           target   2c. SetupMasterTransmit   2cRegPtr_Cnt_T_str.				
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMAC         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DN         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DN         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DN         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDUT         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDUT         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DD         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDR         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDR         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDR         2           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         3           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         66           66         66           varget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CtxL         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CtxL         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CtxL         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         66           66         66           varget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         66           for         67				-
target_ 2c_SetupMasterReceive_ 2cRegPtr_Cnt_T_str.DIR	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66		
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIR         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         2         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOR         2         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOR         2         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DAR         3         3           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         55         55           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.Ctr.DAR         55         556           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.Ctr.DAR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.Ctr.DAR         67         67           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         67         67           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         <	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	-
target_ 2c_SetupMasterReceive_ 2cRegPtr_Cnt_T_str.DIN   2	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DOUT         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.SET         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.CDR         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DDR         2         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T str.DD         3         3           target_12c_SetupMasterTeceive_12cRegPtr_Cnt_T str.DAR         5         5           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T str.DAR         55         55           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T str.DAR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T str.CLKL         2309         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T str.CLKL         2309         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T str.DAR         67         87           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T str.DAR         67         67           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T str.DAR         66         66           varget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T str.DAR         67         67           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T str.DAR         66         66           varget_12c_SetupMasterTransmit_12cRegPtr_Cnt_T str.DAR	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CRT         1         1         1         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4	target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIN	2	2	<b>✓</b>
target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.CRT         1         1         1         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4	target I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	3	3	~
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.Ctr         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.Dtr         2         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PD         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.Dtr         3         3           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.OAR         55         55           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.Dtr         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.Ctr         2309         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.Ctr         1204         1204           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.Ctr         87         87           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DT         87         87           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         67         67           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         5         5           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         5         5           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR				<b>~</b>
target_lzc_SetupMasterReceive_lzcRegPtr_CntT_str.ODR				_
target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PD         3         3           target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PSL         3           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR         55           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR         66           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL         2009           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKL         2009           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLKH         1204           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT         87           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT         87           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.SAR         67           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.SAR         55           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR         2309           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR         3           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR         3           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR         3           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PiD11         1204           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PiD12         66           da         66           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T				
target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PSL         3           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR         55           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.IMR         66           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.STR         556           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CkL         2309           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CkL         2309           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CkL         2309           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CkL         87           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CkR         67           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DkR         67           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DkR         66           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR         2309           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR         3           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PiD11         1204           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PiD12         66           66         4           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DkAC         3           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.Din         1           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_Tstr.Din				
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.OAR         55         55           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.IMR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         2309         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         2309         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH         1204         1204           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         67         87           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         67         67           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         5         5           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.BMDR         3         3           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSC         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DD12         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DD12         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DD12         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cn				
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.IMR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         2309         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH         1204         1204           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT         87         87           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         67         67           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         67         67           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNR         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.NR         2309         2309           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNR         5         5           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSC         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID11         1204         1204           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID12         66         66           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIR         1         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIR         1         1           target_12c_SetupMasterTransmit_12cRegPtr_Cn				
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL       2309       2309         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL       1204       1204         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT       87       87         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT       87       87         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR       67       67         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       5       5         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       5       5         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR       3       3         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PBC       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC       3       3         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR       1       1         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR       1       1         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN       2       2         target_l2c_Setu				-
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL       2309       2309         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH       1204       1204         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRT       87       87         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       67       67         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR       55       55         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR       66       66         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR       5       5         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MDR       2309       2309         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR       3       3         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PMDR       3       3         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID11       1204       1204         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DMAC       3       3         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DMAC       3       3         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN       1       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN       2       2         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN       3       3         target_				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH       1204       1204         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       87         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       67       67         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       55       55         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       2309       2309         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       5       5         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PBC       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PBC       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       1204       1204         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DUT       3       3         target_I2c_SetupMasterTrans	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT       87       87         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR       67       67         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       55       55         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR       2309       2309         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.WR       5       5         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR       3       3         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PDC       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PDI11       1204       1204         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PDI12       66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DINAC       3       3         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN       1       1         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT       3       3         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET       3       3         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET       3       3         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR       2       2         target_l2c_Setup	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT       87         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR       67         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR       55         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       66         66       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR       2309         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.WR       5         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR       3         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11       1204         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12       66         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PUN       1         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR       1         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT       3         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT       3         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET       3         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUR       3         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR       2         target_l2c_SetupMasterTransmit_	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DRR       67       67         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.SAR       55       55         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       66       66         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR       2309       2309         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PNR       5       5         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       3       3         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PNSC       66       66         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID11       1204       1204         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID12       66       66         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DMAC       3       3         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN       1       1         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIR       1       1         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DOUT       3       3         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLR       1       1         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLR       1       1         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CDR       2       2         target_!2c_SetupM		87	87	<b>✓</b>
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.SAR       55       55         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DXR       66       66         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MDR       2309       2309         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.VR       5       5         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       3       3         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSC       66       66         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID11       1204       1204         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID12       66       66         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DMAC       3       3         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN       1       1         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIR       1       1         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DOUT       3       3         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DOUT       3       3         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLR       1       1         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLR       1       1         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DDR       2       2         target_!2c_SetupMast				-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       2309       2309         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       5       5         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       1204       1204         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIAC       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOR       2       2         target_I2c_SetupMasterTr				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       2309       2309         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       5       5         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       1204       1204         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PUN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DET       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DLR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR       2       2         target_I2c_SetupMasterTr				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       5       5         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       1204       1204         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DLR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DLR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DLR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DDR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DDR       3       3				
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.EMDR       3       3         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSC       66       66         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID11       1204       1204         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PID12       66       66       4         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DMAC       3       3       3         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIR       1       1       1         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN       2       2       2         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DOUT       3       3       3         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DET       3       3       3         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DET       3       3       3         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DER       1       1       1         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DDR       2       2       2         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DDR       2       2       2         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DDR       2       2       2         target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DDR       2       2<				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC       66       66       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       1204       1204       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       66       66       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       3       3       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       2       2       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       3       3       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       3       3       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR       1       1       1       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR       2       2       ✓       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR       2       2       ✓       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD       3       3       ✓				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11       1204       1204         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       66       66         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DET       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DER       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DER       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DER       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DDR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DDR       3       3				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12       66       66       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       3       3       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       1       1       1       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       2       2       ✓       ✓         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       3       3       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓       ✓<	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DDR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD       3       3	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DD       3       3	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DD       3       3	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DD       3       3				-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET       3       3         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR       1       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR       2       2         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DD       3       3				-
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT  3 3 3  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET  3 3 3  vtarget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR  1 1 1  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR  2 2 2  target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD  3 3 3 4 4				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET 3 3 3 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1				
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR 2 2 2 4 2 4 2 4 4 2 4 4 2 4 4 2 4 4 2 4 4 2 4 4 2 4 4 2 4 4 2 4 4 2 4 4 4 2 4 4 4 2 4 4 4 2 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD 3 3				
	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR			~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL 3 3	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~



Τ				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c Send	1	I2c Send	1	-

Test Step 3.32 (Repeat Count = 1)	Innut Value
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_DUMMY_SEND
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
lags_Cnt_T_b16	4
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target I2c Send I2cRegPtr Cnt T str
2c SetRecv(I2cRegPtr Cnt T str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target I2c SetStatus I2cRegPtr Cnt T str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
DataRegisters_Cnt_u08[0]	0
DataRegisters_Cnt_u08[1]	32
_DataRegisters_Crit_u08[2]	30
	36
DataRegisters_Cnt_u08[3]	38
_DataRegisters_Cnt_u08[4]	
_DataRegisters_Cnt_u08[5]	34
_DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
_DataRegisters_Cnt_u08[8]	14
2cREG1_temp	target_i2cREG1_temp
_ColSensorI2CAddress_Cnt_u08	9
_SpurSensorI2CAddress_Cnt_u08	10
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET	3
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR	1

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Name	Input Value	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	
target I2c GenStopCond I2cRegPtr Cnt T str.PD	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	
	556	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309 1204	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
target I2c Send I2cRegPtr Cnt T str.PSL	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
	556	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR		
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	2309	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	1204	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	87	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	
target I2c SetRecv I2cRegPtr Cnt T str.PD	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	
target I2c SetStatus I2cRegPtr Cnt T str.IMR	66	
	556	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR		
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	
	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN		
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	

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Name	Input Value
target I2c SetStatus I2cRegPtr Cnt T str.SET	3
target I2c SetStatus I2cRegPtr Cnt T str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target I2c SetStatus I2cRegPtr Cnt T str.PD	3
target I2c SetStatus I2cRegPtr Cnt T str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target I2c SetupMasterReceive I2cRegPtr Cnt T str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	55
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	66
	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	66
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target I2c SetupMasterTransmit I2cReqPtr Cnt T str.DMAC	3
target I2c SetupMasterTransmit I2cReqPtr Cnt T str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
	66
target i2cREG1 temp.PSC	
	1204
target_i2cREG1_temp.PID11	1204 66
target_i2cREG1_temp.PID11 target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.PID11	

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Name	Input Value		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	✓
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✓
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✓
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✓
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✓
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✓
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	✓
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_DUMMY_READ	INIT_SENSOR2_DUMMY_READ	✓
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	✓
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	2	2	✓
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✓
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✓
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✓
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	✓
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✓
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	✓
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	~
I2c_SetRecv(Length_Cnt_T_u32)	2	2	<b>✓</b>
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	2	2	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR	55	55	

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	2 3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	·
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>v</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	3	3	· ·
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	87	87	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11	66 1204	66 1204	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.DMAC	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>→</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	3	3	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD	3	3	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66 556	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	556 2309	2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	1204	1204	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>V</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	· ·
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	66	66	· ·
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	3	3	· ·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~

T				V
Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	~
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	<b>✓</b>
I2c_SetRecv	1	I2c_SetRecv	1	<b>✓</b>

Test Step 3.33 (Repeat Count = 1)	✓ ·
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADDATREG_READ
DigColPsInt_I2CHwCustData_UIs_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str

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Name	Input Value	
T_DataRegisters_Cnt_u08[0]	0	
T_DataRegisters_Cnt_u08[1]	32	
T_DataRegisters_Cnt_u08[2]	30	
T_DataRegisters_Cnt_u08[3]	36	
T_DataRegisters_Cnt_u08[4]	38	
T_DataRegisters_Cnt_u08[5]	34	
Γ_DataRegisters_Cnt_u08[6]	10	
T_DataRegisters_Cnt_u08[7]	12	
T DataRegisters Cnt u08[8]	14	
2cREG1_temp	target_i2cREG1_temp	
ColSensorI2CAddress Cnt u08	9	
k_SpurSensorI2CAddress_Cnt_u08	10	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	
rarget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	2309	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	
	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT		
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR	2	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	3	
	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.STR	556	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	

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Name	Input Value
arget I2c SetRecv I2cRegPtr Cnt T str.EMDR	3
arget I2c SetRecv I2cRegPtr Cnt T str.PSC	66
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
arget I2c SetRecv I2cRegPtr Cnt T str.PID12	66
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
rarget_12c_SetRecv_12cRegPtr_Cnt_T_str.DIN	2
rarget_12c_SetRecv_12cRegPtr_Cnt_T_str.DOUT	3
target I2c SetRecv I2cRegPtr Cnt T str.SET	3
	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
arget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR	55
arget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR	66
arget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR	556
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
arget I2c SetStatus I2cRegPtr Cnt T str.PSC	66
arget I2c SetStatus I2cRegPtr Cnt T str.PID11	1204
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
	3
rarget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
rarget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
rarget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	
rarget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
rarget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	55
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
arget I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	1204
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.FUN	1
arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIR	1
arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN	2
	3
arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
	1204
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt T str.CLKH	
	87
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87 67
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	

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Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3		
target_i2cREG1_temp.OAR	55		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	556		
target_i2cREG1_temp.CLKL	2309		
target_i2cREG1_temp.CLKH	1204		
target_i2cREG1_temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target_i2cREG1_temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	2		
target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT	3		
target i2cREG1 temp.SET	3		
target_i2cREG1_temp.CLR	1		
target i2cREG1 temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt AttempOccurForCustDatRead Cnt M u08	1	1	-
DigColPsInt Buffer Cnt M u08[0]	10	10	•
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	-
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	-
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	-
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	-
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	-
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	•
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	•
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADDATREG_READ	INIT_SENSOR1_EXTREADDATREG_READ	•
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	~
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	_
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	•
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	<b>•</b>
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	<b>V</b>
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	· ·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	Ž
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	556	556	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKI	2309	2309	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	1204		~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH	1204 87	1204 87	Ž
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR	67	67	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR	55	55	J
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	-
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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target I2c GenStopCond I2cRegPtr Cnt T str.FUN	1	1	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target I2c GenStopCond I2cRegPtr Cnt T str.PD	3	3	_
target I2c GenStopCond I2cRegPtr Cnt T str.PSL	3	3	·
target I2c Send I2cRegPtr Cnt T str.OAR	55	55	Ţ
target_12e_ochd_12ertegr tr_ont_1_str.oArt	66	66	·
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	<b>63</b> 6	j
target_i2c_send_i2cRegPtr_Cnt_T_str.CLKL	2309	2309	Ž
	1204	1204	Ž
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	87	87	Ž
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT			Ţ
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	Ž
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
target I2c SetRecv I2cRegPtr Cnt T str.CLKL	2309	2309	<b>✓</b>
target I2c SetRecv I2cRegPtr Cnt T str.CLKH	1204	1204	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	_
	67	67	

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>V</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	1	1	<b>Y</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR	1 2	2	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	3	3	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.SET	3	3	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309 5	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR target_I2c SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2C_SetupMasterReceive_I2CRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>V</b>
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR	55	55	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	556	556	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	2	2	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>V</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3 1	3	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	2	2	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	
	1-	i -	

T .				V
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~



Input Value
3
123
145
200
1
1
1
566
30
INIT_SENSOR1_EXTREADDATREG_SETREG
67
68
1
1
4
1
4
1
1
129
100
2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
target_I2c_Send_I2cRegPtr_Cnt_T_str
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
0
32
30
36
38
36
10
12
14
target_i2cREG1_temp
0
120
567
44
4444
566
4466
129
6
567
44
566
554
1
44
4466
44
1
1
2
0
1
1
2
0
3
3 3
3
3 567
3 567 44
3 567 44 4444
3 567 44 4444 566
3 567 44 4444

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Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129
arget I2c SetRecv I2cRegPtr Cnt T str.DRR	6
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
arget I2c SetRecv I2cRegPtr Cnt T str.DXR	44
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566
	554
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	44
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
arget I2c SetRecv I2cRegPtr Cnt T str.CLR	2
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44
	4444
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44
arget_12c_SetStatus_12cRegPtr_Cnt_T_str.DMAC	1
arget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	1
	2
arget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
	567
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	
arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	44 4444

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Name	Input Value		
	•		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SAR	567		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2		
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2		
	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR			
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	567		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	0		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3		
target_i2cREG1_temp.OAR	567		
target_i2cREG1_temp.IMR	44		
target_i2cREG1_temp.STR	4444		
target i2cREG1 temp.CLKL	566		
target i2cREG1 temp.CLKH	4466		
target_i2cREG1_temp.CNT	129		
target_i2cREG1_temp.DRR	6		
target_i2cREG1_temp.SAR	567		
target i2cREG1 temp.DXR	44		
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target_i2cREG1_temp.MDR	566		
target_i2cREG1_temp.IVR	554		
target_i2cREG1_temp.EMDR	1		
target i2cREG1 temp.PSC	44		
target i2cREG1 temp.PID11	4466		
·			
target_i2cREG1_temp.PID12	44		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	1		
target i2cREG1 temp.DIR	2		
target_i2cREG1_temp.DIN	0		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target i2cREG1 temp.CLR	2		
target i2cREG1 temp.ODR	0		
target_i2cREG1_temp.PD	3		
	3		
target_i2cREG1_temp.PD		Expected Value	Result

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Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	123	123	<b>~</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	~
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	<b>~</b>
DigColPoint_BusBusySeqError_Cnt_M_lgc	1	1	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	
DigColPsInt ColSnsrData Cnt M u16	566	566	
DigColPsInt_CurrentSlave_Cnt_M_u08	30	30	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT COMPLETE	INIT COMPLETE	<b>✓</b>
DigColPsInt_I2CHwCustData_Uls_M_u16	67	67	
DigColPsInt I2CHwIncompleteCustData UIs M u16	68	68	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1	1	~
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	~
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt_SpurSnsrData_Cnt_M_u16	129	129	<b>✓</b>
DigColPsInt_TransactionCnt_Cnt_M_u08	100	100	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129	129	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>Y</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	44	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554 1	554	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	44	44	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11	4466	4466	
target I2c GenStopCond I2cRegPtr Cnt T str.PID12	44	44	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>*</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	44	44	<b>Y</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	<b>Y</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466 44	4466	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	2	2	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DUT	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	·
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>✓</b>

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	<u> </u>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	44	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	554	554 1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	
target I2c SetRecv I2cRegPtr Cnt T str.PID12	44	44	·
target I2c SetRecv I2cRegPtr Cnt T str.DMAC	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target I2c SetRecv I2cRegPtr Cnt T str.DIR	2	2	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	✓
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	<b>v</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>V</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	44	44	<i>y</i>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR	566	566 554	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	554	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	
target_I2C_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
target I2c SetStatus I2cRegPtr Cnt T str.DIN	0	0	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>~</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	129	129	<b>•</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	6	6	· ·
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	567	567	· ·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566 554	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	554	1	
target_I2C_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID12	44	44	·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	~

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c_GenStopCond	1	I2c_GenStopCond	1	~

Test Sten 2.25 (Panest Count = 4)	
Test Step 3.35 (Repeat Count = 1) Name	Input Value
DigColPsInt AttempOccurForCustDatRead Cnt M u08	3
	123
DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	145
	200
DigColPoint_Buffer_Cnt_M_u08[2]	1
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_Igc	·
DigColPsInt_ColSnsrData_Cnt_M_u16	566
DigColPsInt_CurrentSlave_Cnt_M_u08	30
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG
DigColPsInt_I2CHwCustData_UIs_M_u16	67
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	68
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	4
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	129
DigColPsInt_TransactionCnt_Cnt_M_u08	100
Flags_Cnt_T_b16	2
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	0
k_SpurSensorl2CAddress_Cnt_u08	120
target I2c GenStopCond I2cRegPtr Cnt T str.OAR	567

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Name	Input Value
target I2c GenStopCond I2cRegPtr Cnt T str.IMR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466
target I2c GenStopCond I2cRegPtr Cnt T str.CNT	129
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR	6
	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	44
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	3
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	567
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	44
arget_12c_Send_12cRegPtr_Cnt_T_str.Nrt	4444
arget_12c_Send_12cRegPtr_Cnt_T_str.CtKL	566
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
arget_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	6
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
target I2c Send I2cRegPtr Cnt T str.DMAC	1
target I2c Send I2cRegPtr Cnt T str.FUN	1
target I2c Send I2cRegPtr Cnt T str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
arget_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	1
arget_12c_Send_12cRegPtr_Cnt_T_str.SET	1
	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FMDR	1
	44
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
	0
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	
	1
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR  target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	1

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Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target I2c SetStatus I2cRegPtr Cnt T str.OAR	567
	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target I2c SetStatus I2cRegPtr Cnt T str.DIN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1 2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	1
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	4444
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	566
target I2c SetupMasterTransmit I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	1
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	2
target_120_0etupiviaster framsmit_126/tegFtt_Offt_1_5tf.OLR	L



DigColPsInt_InterruptNotification			VALCITAG
Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR target_i2cREG1_temp.IMR	567 44		
target i2cREG1 temp.STR	4444		
target i2cREG1 temp.CLKL	566		
target_i2cREG1_temp.CLKH	4466		
target_i2cREG1_temp.CNT	129		
target_i2cREG1_temp.DRR	6		
target_i2cREG1_temp.SAR	567		
target_i2cREG1_temp.DXR	44		
target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR	566 554		
target i2cREG1_temp.FMC	1		
target_i2cREG1_temp.PSC	44		
target_i2cREG1_temp.PID11	4466		
target_i2cREG1_temp.PID12	44		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN target_i2cREG1_temp.DOUT	1		
target i2cREG1 temp.SET	1		
target i2cREG1 temp.CLR	2		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3	3	•
DigColPsInt_Buffer_Cnt_M_u08[0]	123	123	•
DigColPoint_Buffer_Cnt_M_u08[1]	145 200	145 200	
DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	•
DigColPsInt_ColSnsrData_Cnt_M_u16	566	566	•
DigColPsInt_CurrentSlave_Cnt_M_u08	30	30	•
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE	READ_COMPLETE	•
DigColPsInt_I2CHwCustData_UIs_M_u16	67	67	•
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt InitFailedOnce Cnt M lgc	68	68	
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	
DigColPsInt RecvOverrunError Cnt M Igc	1	1	
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	•
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	•
DigColPsInt_SpurSnsrData_Cnt_M_u16	129	129	•
DigColPsInt_TransactionCnt_Cnt_M_u08	100	100	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	567	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	4444	44	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	566	4444 566	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129	129	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	6	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	567	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	44	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	566	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	554	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC	1 44	1 44	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	4466	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	44	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	0	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0 1 1	0 1 1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0 1 1 2	0 1 1 2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0 1 1	0 1 1	

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	· ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6 567	
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	567	44	- J
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44 566	566	
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	554	554	
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	44	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	4466	4466	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11 target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	
target_12c_Send_12cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	2	2	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	0	0	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	1	1	
	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	0	0	
target I2c Send I2cRegPtr_Cnt_T_str.ODR	3	3	
target I2c Send I2cRegPtr_Cnt_T_str.PD	3	3	
target I2c SetRecv I2cRegPtr_Cnt_T_str.PSL target I2c SetRecv I2cRegPtr Cnt T str.OAR	567	567	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	44	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	566	566	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	4466	4466	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	567	567	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	
target I2c SetRecv I2cRegPtr Cnt T str.DMAC	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	<u> </u>
target I2c SetRecv I2cRegPtr Cnt T str.DOUT	1	1	
target I2c SetRecv I2cRegPtr Cnt T str.SET	1	1	<u> </u>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>✓</b>
target I2c SetRecv I2cRegPtr Cnt T str.PD	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	·
target I2c SetStatus I2cRegPtr Cnt T str.OAR	567	567	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	-
target I2c SetStatus I2cRegPtr Cnt T str.DRR	6	6	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	
	1.	ļ.	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target I2c SetStatus I2cRegPtr Cnt T str.PSL	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>✓</b>
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	566	566	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	_
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DXR	44	44	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	
target_I2C_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.FUN	1	1	•
	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT		1	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	0	0	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	4444	4444	<b>Y</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
I2c_GenStopCond	1	I2c_GenStopCond	1	~

Test Step 3.36 (Repeat Count = 1)		~
Name	Input Value	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3	
DigColPsInt_Buffer_Cnt_M_u08[0]	123	
DigColPsInt_Buffer_Cnt_M_u08[1]	145	
DigColPsInt_Buffer_Cnt_M_u08[2]	200	
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	
DigColPsInt_ColSnsrData_Cnt_M_u16	566	
DigColPsInt_CurrentSlave_Cnt_M_u08	30	
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_READ	
DigColPsInt_I2CHwCustData_Uls_M_u16	67	



Name	Input Value
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	68
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	4
	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	129
DigColPsInt_TransactionCnt_Cnt_M_u08	100
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
	32
T_DataRegisters_Cnt_u08[1]	
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	0
k_SpurSensorl2CAddress_Cnt_u08	120
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466
target I2c GenStopCond I2cRegPtr Cnt T str.PID12	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target I2c Send I2cRegPtr Cnt T str.OAR	567
• •	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	129
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN	1
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0

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Name	Input Value	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	
	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET		
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	
target I2c SetRecv I2cRegPtr Cnt T str.CNT	129	
· · - · · · · · · · · · · · · · · · · ·		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	
	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	
target I2c SetStatus I2cRegPtr Cnt T str.SAR	567	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.MDR	566	
	554	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR		
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	
target I2c SetStatus I2cRegPtr Cnt T str.DOUT	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	
	129	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	

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DigColPsInt\_InterruptNotification

Name	Input Value		
110000	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR			
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	567		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSC	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0		
	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	567		
target_i2cREG1_temp.IMR	44		
target_i2cREG1_temp.STR	4444		
target_i2cREG1_temp.CLKL	566		
target_i2cREG1_temp.CLKH	4466		
target_i2cREG1_temp.CNT	129		
target_i2cREG1_temp.DRR	6		
target i2cREG1 temp.SAR	567		
target i2cREG1 temp.DXR	44		
target_i2cREG1_temp.MDR	566		
target_i2cREG1_temp.IVR	554		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	44		
target_i2cREG1_temp.PID11	4466		
target_i2cREG1_temp.PID12	44		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	1		
target i2cREG1 temp.DIR	2		
target i2cREG1 temp.DIN	0		
	1		
target_i2cREG1_temp.DOUT			
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3	3	<b>✓</b>
DigColPsInt_Ruffer_Cnt_M_u08[0]	30	30	
	7	7	
DigColPsInt_Buffer_Cnt_M_u08[1]			
DigColPsInt_Buffer_Cnt_M_u08[2]	70	70	<b>~</b>
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	~
DigColPsInt_CmdFailOccurred_Cnt_M_Igc	1	1	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc		1	<b>✓</b>
3 * * * 2 * * * * * * * * * * * * * * *	1		
DigColPsInt_ColSnsrData_Cnt_M_u16	1 566	566	
		566 30	*
DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08	566 30	30	<b>✓</b>
DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum	566 30 INIT_SENSOR1_SENDCMD	30 INIT_SENSOR1_SENDCMD	<b>✓</b>
DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16	566 30 INIT_SENSOR1_SENDCMD 67	30 INIT_SENSOR1_SENDCMD 67	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum	566 30 INIT_SENSOR1_SENDCMD	30 INIT_SENSOR1_SENDCMD	· ·

DigColPsInt\_NackOccured\_Cnt\_M\_lgc

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Name	Actual Value	Expected Value	Result
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	<b>*</b>
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	
DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt TransactionCnt Cnt M u08	129 100	129 100	
I2c_Send(Length_Cnt_T_u32)	3	3	
l2c SetupMasterTransmit(DataLength Cnt T u16)	3	3	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR	567	567	
target I2c GenStopCond I2cRegPtr Cnt T str.IMR	44	44	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>*</b>
target I2c GenStopCond I2cRegPtr Cnt T str.CLKL	566	566	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129	129	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	554	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	44	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	44	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	0	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>V</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD	3	3	<b>~</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	· ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44 4444	44 4444	
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	566	566	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	4466	4466	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	<b>*</b>
target I2c Send I2cRegPtr Cnt T str.DRR	6	6	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>~</b>
target I2c Send I2cRegPtr Cnt T str.DXR	44	44	
target I2c Send I2cRegPtr Cnt T str.MDR	566	566	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>v</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3	3	<b>V</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	567	567	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444 566	4444 566	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	4466	4466	_
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	129	129	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.IVR	554	554	·
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	1	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	44	44	<b>v</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
	<u> </u>		



margin Line   Service   Contempt   1   1   1   1   1   1   1   1   1	Name	Actual Value	Expected Value	Result
Image: Los Seffero, DeSeptero, Col. T. and DOM	0 =			
Section   Company   Comp				
				•
Barger   Dis.   Series   Discourage   Disc	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	
Sept   10.5 Serious   Debugs   10.5 CH_   10.5 CH_   10.5 CH_	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	•
	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD			•
Secret   12, Secretary   12, Secretary   13,			i i	•
Langer   12   SerSalasis   12   Care   Part   12   Care   14   C				•
Barger   12.6 SesSibus   12.6 Rep   Part   17.5 Col.   14.0				
Marging   12, SerSibus   2004grip* Cmt   1 st Cmt   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129				
				•
James, I.P.S. Selfshah, 200eg/Pr. Cot. T. pt. DNR  44  44  44  440  440  440  440  440				
Langel, I.E., Selfshate, J.Cofegiff, Crit. T. jart. NNR  554  1879, J.C., Selfshate, J.Cofegiff, Crit. T. jart. PNR  554  1879, J.C., Selfshate, J.Cofegiff, Crit. T. jart. PNR  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		567	567	•
	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	•
Image   IZC Selfstate   Zelfstate   Zelf	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	•
target_12c_SelStatus_12cReptpt_Coll_T_str.PDC         44         4466           larget_12c_SelStatus_12cReptpt_Coll_T_str.PDD11         4466         4466           larget_12c_SelStatus_12cReptpt_Coll_T_str.PDD12         44         44           larget_12c_SelStatus_12cReptpt_Coll_T_str.DNA         1         1           larget_12c_SelStatus_12cReptpt_Coll_T_str.DNN         1         1           larget_12c_SelStatus_12cReptpt_Coll_T_str.DNN         0         0           larget_12c_Selstatus_12cReptpt_Coll_T_str.DNN         3         3           larget_12c_Selstatus_12cReptpt_Coll_T_str.DNN         3         3           larget_12c_Selstatus_12cReptpt_Coll_T_str.DNN         444         444	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	•
tanget I.2. Selfstatus JoRheght Cont T. str PIDI1         4466           target I.2. Selfstatus JoRheght Cont T. str PIDI2         44           tanget I.2. Selfstatus JoRheght Cont T. str DIMAC         1           tanget J.2. Selfstatus JoRheght Cont T. str DIMAC         1           tanget J.2. Selfstatus JoRheght Cont T. str DIM         2           tanget J.2. Selfstatus JoRheght Cont T. str DIM         0           tanget J.2. Selfstatus JoRheght Cont T. str DIM         0           tanget J.2. Selfstatus JoRheght Cont T. str DIM         1           tanget J.2. Selfstatus JoRheght Cont T. str DIM         0           tanget J.2. Selfstatus JoRheght Cont T. str DIM         1           tanget J.2. Selfstatus JoRheght Cont T. str DIM         0           tanget J.2. Selfstatus JoRheght Cont T. str DIM         0           tanget J.2. Selfstatus JoRheght Cont T. str DIM         3           tanget J.2. Selfstatus JoRheght Cont T. str DIM         3           tanget J.2. Selfstatus JoRheght Cont T. str DIM         44           tanget J.2. Selfstatus JoRheght Cont T. str DIM         44           tanget J.2. Selfstatus JoRheght Cont T. str DIM         44           tanget J.2. Selfstatus JoRheght Cont T. str DIM         44           tanget J.2. Selfstatus JoRheght Cont T. str DIM         44           tanget J.2. Selfstatus JoRheght Cont T. str DIM </td <td></td> <td></td> <td></td> <td>•</td>				•
tagent J.C., Selfstatus, J.C. Reppit C. Ont. 1. str. DIAC         1           target J.C., Selfstatus, J.C. Reppit C. Ont. 1. str. DIAC         1           target J.C., Selfstatus, J.C. Reppit C. Ont. 1. str. DIAC         1           target J.C., Selfstatus, J.C. Reppit C. Ont. 1. str. DIAC         1           target J.C., Selfstatus, J.C. Reppit C. Ont. 1. str. DIAC         0           target J.C., Selfstatus, J.C. Reppit C. Ont. 1. str. DIAC         1           target J.C., Selfstatus, J.C. Reppit C. Ont. 1. str. DIAC         1           target J.C., Selfstatus, J.C. Reppit C. Ont. 1. str. DIAC         0           target J.C., Selfstatus, J.C. Reppit C. Ont. 1. str. DIAC         0           target J.C., Selfstatus, J.C. Reppit C. Ont. 1. str. DIAC         0           target J.C., Selfstatus, J.C. Reppit C. Ont. 1. str. DIAC         3           target J.C., Selfstatus, J.C. Reppit C. Ont. 1. str. DIAC         3           target J.C., Selfstatus, J.C. Reppit C. Ont. 1. str. DIAC         3           target J.C., Selfstatus, J.C. Reppit C. Ont. 1. str. DIAC         444           target J.C., Selfstatus, J.C. Reppit C. Ont. 1. str. DIAC         567           target J.C., Selfstatus, J.C. Reppit C. Ont. 1. str. DIAC         567           target J.C., Selfstatus, J.C. Reppit C. Ont. 1. str. DIAC         566           target J.C., Selfstatus, J.C. Reppit C. Ont. 1. str. DIAC         567				•
Images   125, Selfsblaus   126,Pept   Cut   T. str.DMC   1				•
Larget_Lize_SetStatus_JezRepPt_Cnt_T st_FUN         1           Larget_Lize_SetStatus_JezRepPt_Cnt_T st_DIR         2           Larget_Lize_SetStatus_JezRepPt_Cnt_T st_DIN         0           Larget_Lize_SetStatus_JezRepPt_Cnt_T st_DIN         1           Larget_Lize_SetStatus_JezRepPt_Cnt_T st_DINT         1           Larget_Lize_SetStatus_JezRepPt_Cnt_T st_DIT_St_DINT         1           Larget_Lize_SetStatus_JezRepPt_Cnt_T st_DIT_St_DINT         0           Larget_Lize_SetStatus_JezRepPt_Cnt_T st_DIT_DIT_St_DINT         0           Larget_Lize_SetStatus_JezRepPt_Cnt_T st_DIT_DIT_St_DINT         3           Larget_Lize_SetStatus_JezRepPt_Cnt_T st_DIT_DIT_St_DINT         3           Larget_Lize_SetUpMasterRecove_JezRepPt_Cnt_T st_DINT         44           Larget_Lize_SetUpMasterRecove_JezRepPt_Cnt_T st_DINT         44           Larget_Lize_SetUpMasterRecove_JezRepPt_Cnt_T st_DINT         444           Larget_Lize_SetUpMasterRecove_JezRepPt_Cnt_T st_DINT         444           Larget_Lize_SetUpMasterRecove_JezRepPt_Cnt_T st_DINT         446           Larget_Lize_SetUpMasterRecove_JezRepPt_Cnt_T st_DINT         446           Larget_Lize_SetUpMasterRecove_JezRepPt_Cnt_T st_DINT         446           Larget_Lize_SetUpMasterRecove_JezRepPt_Cnt_T st_DINT         457           Larget_Lize_SetUpMasterRecove_JezRepPt_Cnt_T st_DINT         566				·
Images   Lots   Selfstatus   JeRegPtr Cnt T_str DIN				
larget_Re_SelSatus_ReapPtr_Cont_str.DOUT         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1				
target_IZe_SelStatus_IZeRepPtr_Cnt_T_str.SET         1         1           target_IZe_SelStatus_IZeRepPtr_Cnt_T_str.CLR         2         2           target_IZe_SelStatus_IZeRepPtr_Cnt_T_str.DDR         0         0           target_IZe_SelStatus_IZeRepPtr_Cnt_T_str.DDR         3         3           target_IZe_Selstatus_IZeRepPtr_Cnt_T_str.DDR         3         3           target_IZe_Selstatus_IZeRepPtr_Cnt_T_str.DL         3         3           target_IZe_Selstatus_IZeRepPtr_Cnt_T_str.DL         44         44           target_IZe_Selstatus_IZeRepPtr_Cnt_T_str.DL         567         567           target_IZe_Selstatus_IZeRepPtr_Cnt_T_str.DL         566         567           target_IZe_Selstatus_IZERepPtr_Cnt_T_str.DL         566         566           target_IZe_Selstatus_IZERepPtr_Cnt_T_str.CLKI         444         444           target_IZe_Selstatus_IZERepPtr_Cnt_T_str.CLKI         4466         4466           target_IZe_Selstatus_IZERepPtr_Cnt_T_str.DL         446         4466           target_IZe_Selstatus_IZERepPtr_Cnt_T_str.DL         6         6           target_IZe_Selstatus_IZERepPtr_Cnt_T_str.DL         6         6           target_IZe_Selstatus_IZERepPtr_Cnt_T_str.DL         567         567           target_IZe_Selstatus_IZERepPtr_Cnt_T_str.DL         6         6 </td <td></td> <td>1</td> <td>1</td> <td>•</td>		1	1	•
target J2e_SetStatus_J2cRepPir_CntT_str.PD         3         3           target_SetStatus_J2cRepPir_CntT_str.PD         3         3           target_SetStatus_J2cRepPir_CntT_str.PD         3         3           target_SetStatus_J2cRepPir_CntT_str.PD         567         567           target_Set_SetUpMasterReceive_J2cRepPir_CntT_str.MR         44         44           target_J2e_SetUpMasterReceive_J2cRepPir_CntT_str.Lst.STR         444         444           target_J2e_SetUpMasterReceive_J2cRepPir_CntT_str.CtxL         566         566           target_J2e_SetUpMasterReceive_J2cRepPir_CntT_str.CtxL         466         4466           target_J2e_SetUpMasterReceive_J2cRepPir_CntT_str.CtxT         129         129           target_J2e_SetUpMasterReceive_J2cRepPir_CntT_str.DtxT         129         129           target_J2e_SetUpMasterReceive_J2cRepPir_CntT_str.DtxT         44         44           target_J2e_SetUpMasterReceive_J2cRepPir_CntT_str.DtxT         44         44           target_J2e_SetUpMasterReceive_J2cRepPir_CntT_str.DtxT         56         56           target_J2e_SetUpMasterReceive_J2cRepPir_CntT_str.DtxT         554         554           target_J2e_SetUpMasterReceive_J2cRepPir_CntT_str.DtxT         44         44           target_J2e_SetUpMasterReceive_J2cRepPir_CntT_str.DtxT         44         44		1	1	•
target 12c SetStatus 12cRegPtr Cnt_Tst.PD         3         3           target 12c SetStatus 12cRegPtr Cnt_Tst.PD         3         3           target 12c SetUpMasterReceive 12cRegPtr Cnt_Tst.DAR         567         567           target 12c SetupMasterReceive 12cRegPtr Cnt_Tst.DAR         44         44           target 12c SetupMasterReceive 12cRegPtr Cnt_Tst.DAR         44         444           target 12c SetupMasterReceive 12cRegPtr Cnt_Tst.CLKI         566         566           target 12c SetupMasterReceive 12cRegPtr Cnt_Tst.CLKI         4466         4466           target 12c SetupMasterReceive 12cRegPtr Cnt_Tst.CNT         129         129           target 12c SetupMasterReceive 12cRegPtr Cnt_Tst.DAR         6         6           target 12c SetupMasterReceive 12cRegPtr Cnt_Tst.DAR         6         6           target 12c SetupMasterReceive 12cRegPtr Cnt_Tst.DAR         44         44           target 12c SetupMasterReceive 12cRegPtr Cnt_Tst.DAR         44         44           target 12c SetupMasterReceive 12cRegPtr Cnt_Tst.DAR         1         1           target 12c SetupMasterReceive 12cRegPtr Cnt_Tst.DAR         4         44           target 12c SetupMasterReceive 12cRegPtr Cnt_Tst.DAT         44         44           target 12c SetupMasterReceive 12cRegPtr Cnt_Tst.DAT         1         1	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	•
larget   2c_Setslatus   2cRegPtr_Cnt_T_str.PSL   3   3   3   3   3   3   3   3   3	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	•
larget   2e   SetupMasterReceive   12eRegPtr_Cnt_T_str.NRR	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.NMR         44         44           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.STR         444         444           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CNL         566         566           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CNT         129         129           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CNT         129         129           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR         6         6           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR         6         6           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR         567         567           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRD         566         566           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRD         566         566           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRD         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRD         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRD         44         44           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRD         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRD         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRD				•
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CtXL         556         556           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CtXL         556         556           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CtXL         466         4466           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CtXT         129         129           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR         6         6           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DXR         44         44           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DXR         44         44           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         566         566           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNR         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PSC         44         44           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNAC         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMAC         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNC         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNC         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNC         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNC <td< td=""><td></td><td></td><td></td><td>•</td></td<>				•
target_12c_SetupMasterReceive_12cRegPtr_Cnt_str.CLKL         566         566           target_12c_SetupMasterReceive_12cRegPtr_Cnt_str.CNtH         4466         4466           target_12c_SetupMasterReceive_12cRegPtr_Cnt_str.CNT         129         129           target_12c_SetupMasterReceive_12cRegPtr_Cnt_str.CNR         6         6           target_12c_SetupMasterReceive_12cRegPtr_Cnt_str.DRR         6         6           target_12c_SetupMasterReceive_12cRegPtr_Cnt_str.DNR         44         44           target_12c_SetupMasterReceive_12cRegPtr_Cnt_str.DNR         556         566           target_12c_SetupMasterReceive_12cRegPtr_Cnt_str.DNR         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_str.DNR         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_str.DND         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_str.DND         44         44           target_12c_SetupMasterReceive_12cRegPtr_Cnt_str.DNDC         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_str.DNDC         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_str.DND         0         0           target_12c_SetupMasterReceive_12cRegPtr_Cnt_str.DND         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_str.DND         0         0				
larget   12c   SetupMasterReceive   12cRegPtr Cnt_T   str.CNT   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129   129				
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRT         129         129           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR         6         6           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR         567         567           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR         44         44           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR         566         566           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR         554         554           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRC         44         44           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNC         44         44           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DNAC         1         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DN         1         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         1         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         1         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRC         2         2         2 <tr< td=""><td></td><td></td><td></td><td></td></tr<>				
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR         6         6           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.SAR         567         567           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.MDR         44         44           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.MDR         566         566           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.MDR         554         554           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PDRDR         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PDRDR         44         44           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PDRDR         4466         4466           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMAC         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMR         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOT         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.ODR         0         0           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.ODR         3<				•
target_J2_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DXR         44         44           target_J2_SetupMasterReceive_J2cRegPtr_Cnt_T_str.MDR         566         566           target_J2_SetupMasterReceive_J2cRegPtr_Cnt_T_str.WR         554         554           target_J2_SetupMasterReceive_J2cRegPtr_Cnt_T_str.EMDR         1         1           target_J2_SetupMasterReceive_J2cRegPtr_Cnt_T_str.PSC         44         44           target_J2_SetupMasterReceive_J2cRegPtr_Cnt_T_str.PID11         4466         4466           target_J2_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DMAC         1         1           target_J2_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DMAC         1         1           target_J2_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DIR         2         2           target_J2_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DIR         2         2           target_J2_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DIN         0         0           target_J2_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DOUT         1         1           target_J2_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DR         0         0           target_J2_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DR         0         0           target_J2_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DR         3         3         3           target_J2_SetupMasterTransmit_J2cRegPtr_Cnt_T_str.DAR         44				•
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.NDR         566         566           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.NR         554         554           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.EMDR         1         1           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PDC         44         44           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12         44         44           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC         1         1           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC         1         1           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC         1         1           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC         1         1           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN         0         0           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN         0         0           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT         1         1         1           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR         2         2         2           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DDR         0         0         0           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         3         3         3           target_	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR         554         554           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.BMDR         1         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC         44         44           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11         4466         4466           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12         44         44           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DINC         1         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN         1         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN         0         0           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT         1         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT         1         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT         1         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT         1         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT         3         3           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT         3         3           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT         4         4           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MIN         4 <td>target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR</td> <td>44</td> <td>44</td> <td>•</td>	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	•
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.ENDR         1         44         44         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	•
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PSC         44         44           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PID11         4466         4466           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PID12         44         44           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMAC         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMAC         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIR         2         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         0         0           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOUT         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOUT         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DOR         2         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DR         0         0           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DR         3         3         3           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         567         567           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.Str.R         444         444           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         4466         4466           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_st				•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11         4466         4466           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12         44         44           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC         1         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC         1         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR         2         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN         0         0           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT         1         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DUT         1         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DR         2         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DR         0         0           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DR         0         0           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DAR         3         3           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         567         567           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CtkL         566         566           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CtkL         4466         4466           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR	0 = = 1 = 0 = ==			·
target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIM2         44         44           target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIM2         1         1           target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN         1         1           target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR         2         2           target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIN         0         0           target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DUT         1         1           target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DUT         1         1           target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DR         2         2           target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DR         0         0           target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DR         0         0           target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DA         3         3           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR         567         567           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.MR         44         444           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLK         566         566           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CNT         129         129           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DAR         6				•
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC         1         1           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN         1         1           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN         2         2           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN         0         0           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT         1         1           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET         1         1           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT         1         1           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOR         0         0           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOR         0         0           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DD         3         3           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DAR         567         567           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         44         44           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         566         566           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         4466         4466           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         6         6           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DAR         44				•
target_I2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DIN         1           target_I2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DIN         2           target_I2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DIN         0           target_I2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DUT         1           target_I2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.SET         1           target_I2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.CLR         2           target_I2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.ODR         0           0         0           target_I2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DDR         0           0         0           target_I2c_SetupMasterReceive_J2cRegPtr_Cnt_T_str.DAR         3           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         567           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         44           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL         566           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL         566           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL         4466           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         6           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         6           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR         44           target_I2c_SetupMasterTransmit_I2c				
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIR         2         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DIN         0         0           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DUT         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.SET         1         1           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLR         2         2           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDR         0         0           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DD         3         3           target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DDR         3         3           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DAR         567         567           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MR         44         44           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.STR         4444         444           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL         566         566           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLK         4466         4466           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         6         6           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         6         6           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR         44 </td <td></td> <td></td> <td></td> <td></td>				
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN         0         0           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT         1         1           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SET         1         1           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR         2         2           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR         0         0           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD         3         3           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD         3         3           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL         3         3           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.OAR         567         567           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR         444         44           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL         566         566           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT         129         129           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         6         6           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         6         6           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         6         6           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR         566				
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR         1           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR         2           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR         0           0         0           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DD         3           target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DL         3           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR         567           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR         444           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR         4444           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL         566           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH         4466           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT         129           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR         6           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR         567           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR         44           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR         44           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.NDR         566           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.NDR         566           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.NDR         566 <td></td> <td>0</td> <td>0</td> <td>•</td>		0	0	•
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLR       2       2         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.ODR       0       0         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PD       3       3         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PSL       3       3         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.OAR       567       567         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.STR       44       44         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.STR       4444       444         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL       566       566         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL       4466       4466         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT       129       129         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       6       6         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       6       6         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR       44       44         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR       44       44         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR       566       566         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR       554       554         target_12c_Se	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target   2c SetupMasterReceive   2cRegPtr_Cnt_T_str.ODR         0         0           target   2c SetupMasterReceive   2cRegPtr_Cnt_T_str.PD         3         3           target   2c SetupMasterReceive   2cRegPtr_Cnt_T_str.PSL         3         3           target   2c SetupMasterTransmit_  2cRegPtr_Cnt_T_str.OAR         567         567           target   2c SetupMasterTransmit_  2cRegPtr_Cnt_T_str.IMR         44         44           target   2c SetupMasterTransmit_  2cRegPtr_Cnt_T_str.STR         4444         4444           target   2c SetupMasterTransmit_  2cRegPtr_Cnt_T_str.CLKL         566         566           target   2c SetupMasterTransmit_  2cRegPtr_Cnt_T_str.CLKH         4466         4466           target   2c SetupMasterTransmit_  2cRegPtr_Cnt_T_str.CNT         129         129           target   2c SetupMasterTransmit_  2cRegPtr_Cnt_T_str.DRR         6         6           target   12c SetupMasterTransmit_  12cRegPtr_Cnt_T_str.DXR         44         44           target   12c SetupMasterTransmit_  12cRegPtr_Cnt_T_str.DXR         44         44           target   12c SetupMasterTransmit_  12cRegPtr_Cnt_T_str.MDR         566         566           target   12c SetupMasterTransmit_  12cRegPtr_Cnt_T_str.IMDR         554         554           target   12c SetupMasterTransmit_  12cRegPtr_Cnt_T_str.EMDR         1         1	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	•
target   2c SetupMasterReceive   2cRegPtr_Cnt_T str.PD       3       3         target   2c SetupMasterReceive   2cRegPtr_Cnt_T str.PSL       3       3         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T str.OAR       567       567         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T str.IMR       44       44         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T str.STR       4444       4444         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T str.CLKL       566       566         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T str.CLKH       4466       4466         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T str.CNT       129       129         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T str.DRR       6       6         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T str.DAR       44       44         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T str.DXR       44       44         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T str.DXR       44       44         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T str.IVR       566       566         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T str.IVR       554       554         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T str.EMDR       1       1	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	•
target   2c SetupMasterReceive   2cRegPtr_Cnt_T_str.PSL       3         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T_str.OAR       567         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T_str.IMR       44         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T_str.STR       4444         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T_str.CLKL       566         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T_str.CLKH       4466         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T_str.CNT       129         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T_str.DRR       6         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T_str.SAR       567         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T_str.DXR       44         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T_str.DXR       44         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T_str.MDR       566         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T_str.NDR       566         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T_str.IVR       554         target   2c SetupMasterTransmit   2cRegPtr_Cnt_T_str.EMDR       1	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR		· · · · · · · · · · · · · · · · · · ·	•
target   2c SetupMasterTransmit   2cRegPtr Cnt T_str.OAR       567       567         target   2c SetupMasterTransmit   2cRegPtr Cnt T_str.IMR       44       44         target   2c SetupMasterTransmit   2cRegPtr Cnt T_str.STR       4444       4444         target   2c SetupMasterTransmit   2cRegPtr Cnt T_str.CLKL       566       566         target   2c SetupMasterTransmit   2cRegPtr Cnt T_str.CLKH       4466       4466         target   2c SetupMasterTransmit   2cRegPtr Cnt T_str.CNT       129       129         target   12c SetupMasterTransmit   12cRegPtr Cnt T_str.DRR       6       6         target   12c SetupMasterTransmit   12cRegPtr Cnt T_str.DXR       44       44         target   12c SetupMasterTransmit   12cRegPtr Cnt T_str.DXR       44       44         target   12c SetupMasterTransmit   12cRegPtr Cnt T_str.MDR       566       566         target   12c SetupMasterTransmit   12cRegPtr Cnt T_str.IVR       554       554         target   12c SetupMasterTransmit   12cRegPtr Cnt T_str.EMDR       1       1				•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR       4444       4444         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL       566       566         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH       4466       4466         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT       129       129         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       6       6         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DAR       567       567         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       566       566         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       554       554         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       1       1				•
target   2c SetupMasterTransmit   2cRegPtr Cnt T str.STR       4444       4444         target   2c SetupMasterTransmit   2cRegPtr Cnt T str.CLKL       566       566         target   2c SetupMasterTransmit   2cRegPtr Cnt_T str.CLKH       4466       4466         target   2c SetupMasterTransmit   2cRegPtr Cnt_T str.CNT       129       129         target   2c SetupMasterTransmit   2cRegPtr Cnt_T str.DRR       6       6         target   12c SetupMasterTransmit   12cRegPtr Cnt_T str.DAR       567       567         target   12c SetupMasterTransmit   12cRegPtr Cnt_T str.DXR       44       44         target   12c SetupMasterTransmit   12cRegPtr Cnt_T str.MDR       566       566         target   12c SetupMasterTransmit   12cRegPtr Cnt_T str.IVR       554       554         target   12c SetupMasterTransmit   12cRegPtr Cnt_T str.EMDR       1       1				•
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKL       566       566         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLKH       4466       4466         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT       129       129         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       6       6         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.SAR       567       567         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR       44       44         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MDR       566       566         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.IVR       554       554         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR       1       1				
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH       4466       4466         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT       129       129         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR       6       6         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR       567       567         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR       44       44         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR       566       566         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IVR       554       554         target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR       1       1				
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CNT       129       129         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR       6       6         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.SAR       567       567         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR       44       44         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MDR       566       566         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.IVR       554       554         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR       1       1				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR       6       6         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR       567       567         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       566       566         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       554       554         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       1       1				
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR       567       567         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR       44       44         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR       566       566         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR       554       554         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR       1       1				
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DXR       44       44         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.MDR       566       566         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.IVR       554       554         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.EMDR       1       1				•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR 554 554 target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR 1 1		44	44	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR 1	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	•
				•
				·
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC 44 44 4466 4466 4466				

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~

T				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteData	1	SetupWriteData	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c_Send	1	I2c_Send	1	<b>✓</b>

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3
DigColPsInt Buffer Cnt M u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
	200
DigColPsInt_Buffer_Cnt_M_u08[2]	1
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	566
DigColPsInt_CurrentSlave_Cnt_M_u08	30
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READEXTERR_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	67
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	68
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	4
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	129
DigColPsInt_TransactionCnt_Cnt_M_u08	100
Flags_Cnt_T_b16	32
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Γ_DataRegisters_Cnt_u08[0]	0
Γ_DataRegisters_Cnt_u08[1]	32
「_DataRegisters_Cnt_u08[2]	30
Γ_DataRegisters_Cnt_u08[3]	36
Γ_DataRegisters_Cnt_u08[4]	38
Γ_DataRegisters_Cnt_u08[5]	34
Γ_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
C_DataRegisters_Cnt_u08[8]	14
2cREG1_temp	target_i2cREG1_temp
c_ColSensorl2CAddress_Cnt_u08	0
C_SpurSensorI2CAddress_Cnt_u08	120
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44
arget I2c GenStopCond I2cRegPtr Cnt T str.STR	4444
arget I2c GenStopCond I2cRegPtr Cnt T str.CLKL	566
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466
arget I2c GenStopCond I2cRegPtr Cnt T str.CNT	129
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567
	44
<pre>carget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DXR carget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR</pre>	566

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Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR	1 44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44
target I2c GenStopCond I2cRegPtr Cnt T str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD	3
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	129 6
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	567
target I2c Send I2cRegPtr Cnt T str.DXR	44
target I2c Send I2cRegPtr Cnt T str.MDR	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_l2c_Send_l2cRegPtr_Cnt_T_str.FUN target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3 567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44
target I2c SetRecv I2cRegPtr Cnt T str.STR	4444
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DUT	0
target_l2c_SetRecv_l2cRegPtr_Cnt_i_str.DOU1 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	1
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH	4466 129
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	129
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR	567
O	111

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	(
Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466
target I2c SetStatus I2cRegPtr Cnt T str.PID12	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target I2c SetStatus I2cRegPtr Cnt T str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
	1
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	567
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	6
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	4466
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	567
target i2cREG1 temp.IMR	44
target_i2cREG1_temp.STR	4444
	566
target_i2cREG1_temp.CLKL	
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129



Nome	Input Value		
Name target_i2cREG1_temp.DRR	Input Value		
target i2cREG1 temp.SAR	567		
target_i2cREG1_temp.DXR	44		
target_i2cREG1_temp.MDR	566		
target_i2cREG1_temp.IVR	554		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	44		
target_i2cREG1_temp.PID11	4466		
target_i2cREG1_temp.PID12	44		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DUN target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target i2cREG1 temp.CLR	2		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3	3	~
DigColPsInt_Buffer_Cnt_M_u08[0]	30	30	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	7	7	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[2]	70	70	<b>✓</b>
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	566	566	~
DigColPsInt_CurrentSlave_Cnt_M_u08	30	30	<b>~</b>
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_SENDCMD	INIT_SENSOR2_SENDCMD	· ·
DigColPsInt_I2CHwCustData_Uls_M_u16	67 68	67 68	
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt InitFailedOnce Cnt M lgc	1	1	
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	<b>✓</b>
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	129	129	<b>✓</b>
DigColPsInt_TransactionCnt_Cnt_M_u08	100	100	~
I2c_Send(Length_Cnt_T_u32)	3	3	<b>✓</b>
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	4444	· ·
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT	4466 129	4466 129	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	6	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	567	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	554	<b>✓</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	<b>✓</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN	0	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>*</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	129	129	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	6	6	

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.DOUT	1	1	✓
target I2c Send I2cRegPtr Cnt T str.SET	1	1	~
target I2c Send I2cRegPtr Cnt T str.CLR	2	2	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target I2c SetRecv I2cRegPtr Cnt T str.STR	4444	4444	<b>~</b>
target I2c SetRecv I2cRegPtr Cnt T str.CLKL	566	566	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target I2c SetRecv I2cRegPtr Cnt T str.DRR	6	6	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>✓</b>
target I2c SetRecv I2cRegPtr Cnt T str.MDR	566	566	~
target I2c SetRecv I2cRegPtr Cnt T str.IVR	554	554	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	<b>~</b>
target I2c SetRecv I2cRegPtr Cnt T str.PID11	4466	4466	~
target I2c SetRecv I2cRegPtr Cnt T str.PID12	44	44	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target I2c SetRecv I2cRegPtr Cnt T str.DIR	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	<b>~</b>
target I2c SetRecv I2cRegPtr Cnt T str.PSL	3	3	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	✓
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3	3	<b>✓</b>

T			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
SetupWriteData	1	SetupWriteData	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c Send	1	I2c Send	1	<b>✓</b>

Test Step 3.38 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	566
DigColPsInt_CurrentSlave_Cnt_M_u08	30
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADDATREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	67
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	68
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	4
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1

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Name	Input Value	
DigColPsInt_RecvdDataType_Cnt_M_u08	4	
DigColPsInt SkipRegisterWrite Cnt M lgc	1	
DigColPsInt SpurCustDatFound Cnt M lgc	1	
DigColPsInt_SpurSnsrData_Cnt_M_u16	129	
DigColPsInt TransactionCnt Cnt M u08	100	
Flags_Cnt_T_b16	32	
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str	
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str	
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target I2c SetRecv I2cRegPtr Cnt T str	
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target I2c SetStatus I2cRegPtr Cnt T str	
	target I2c SetupMasterReceive I2cRegPtr Cnt T str	
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)		
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str	
「_DataRegisters_Cnt_u08[0]	0	
「_DataRegisters_Cnt_u08[1]	32	
_DataRegisters_Cnt_u08[2]	30	
_DataRegisters_Cnt_u08[3]	36	
_DataRegisters_Cnt_u08[4]	38	
「_DataRegisters_Cnt_u08[5]	34	
_DataRegisters_Cnt_u08[6]	10	
_DataRegisters_Cnt_u08[7]	12	
_DataRegisters_Cnt_u08[8]	14	
2cREG1_temp	target_i2cREG1_temp	
ColSensorl2CAddress_Cnt_u08	0	
SpurSensorI2CAddress Cnt u08	120	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566	
	4466	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH		
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	
arget I2c GenStopCond I2cRegPtr Cnt T str.DIR	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	
	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR		
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	
	1	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	44	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
argor_reo_ocna_reorrogr tl_OHL_1_3tt.FD	<del>'</del>	

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	(
Name	Input Value
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
target I2c SetRecv I2cRegPtr Cnt T str.CNT	129
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44
	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target I2c SetRecv I2cRegPtr Cnt T str.CLR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129
	6
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target I2c SetStatus I2cRegPtr Cnt T str.PSC	44
target I2c SetStatus I2cRegPtr Cnt T str.PID11	4466
	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target I2c SetStatus I2cRegPtr Cnt T str.SET	1
target I2c SetStatus I2cRegPtr Cnt T str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	566
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKH	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2

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Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSL	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	566		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	6		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3		
target i2cREG1 temp.OAR	567		
target_i2cREG1_temp.IMR	44		
target i2cREG1 temp.STR	4444		
target i2cREG1_temp.CLKL	566		
target i2cREG1 temp.CLKH	4466		
	129		
target_i2cREG1_temp.CNT	6		
target_i2cREG1_temp.DRR	567		
target_i2cREG1_temp.SAR			
target_i2cREG1_temp.DXR	44		
target_i2cREG1_temp.MDR	566		
target_i2cREG1_temp.IVR	554		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	44		
target_i2cREG1_temp.PID11	4466		
target_i2cREG1_temp.PID12	44		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	2		
target_i2cREG1_temp.DIN	0		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3	3	~
DigColPsInt_Buffer_Cnt_M_u08[0]	14	14	~
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	~
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	566	566	~
DigColPsInt_CurrentSlave_Cnt_M_u08	120	120	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADDATREG_SETR	INIT_SENSOR2_EXTREADDATREG_SETR	~
DigColPsInt_I2CHwCustData_Uls_M_u16	67	67	~
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	9	9	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1	1	~
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	~
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	129	129	<b>✓</b>
DigColPsInt_TransactionCnt_Cnt_M_u08	100	100	~

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Name	Actual Value	Expected Value	Result
I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.OAR	567	567	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	44	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR	567 44	567 44	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	566	J
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	2 0	-
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT	1	1	Ž
target I2c GenStopCond I2cRegPtr Cnt T str.SET	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.STR target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	4444 566	4444 566	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	J
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	44 4466	44 4466	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	J
target I2c Send I2cRegPtr Cnt T str.DMAC	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	· ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	Ž
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	129	129	V
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	6 567	6 567	<i>J</i>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	1 2	1 2	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	3	3 3	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR	567	567	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	
target I2c SetStatus I2cRegPtr Cnt T str.STR	4444	4444	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR	566	566	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	44	1 44	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11	4466	4466	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	4444	4444	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	566	566	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKH	4466	4466	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12 target_I2c SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.FUN	1	1	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIR	2	2	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIN	0	0	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	1	1	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	566	566	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129 6	129 6	j
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	567	567	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	44	44	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	566	566	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	•
<u> </u>		4	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC			

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DigColPsInt_	InterruptNotification
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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3	3	<b>✓</b>

Т			V	
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	l2c_Send	1	~

Test Step 3.39 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	11
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	2767
DigColPsInt_CurrentSlave_Cnt_M_u08	45
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	76
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	77
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt SkipRegisterWrite Cnt M Igc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt SpurSnsrData Cnt M u16	564
DigColPsInt_TransactionCnt_Cnt_M_u08	130
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target I2c GenStopCond I2cRegPtr Cnt T str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target I2c SetRecv I2cRegPtr Cnt T str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_12c_SetStatus_12cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
	30
T_DataRegisters_Cnt_u08[2]	36
T_DataRegisters_Cnt_u08[3]	
T_DataRegisters_Cnt_u08[4]	38 34
T_DataRegisters_Cnt_u08[5]	
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	7
k_SpurSensorI2CAddress_Cnt_u08	123
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556
target I2c GenStopCond I2cRegPtr Cnt T str.PID12	100

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	(
Name	Input Value
	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100
	2767
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788
	2767
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767
	9
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100
target I2c SetRecv I2cRegPtr Cnt T str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
	1
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target I2c SetRecv I2cRegPtr Cnt T str.ODR	3
	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767
target_12c_SetStatus_12cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2767
target_12c_SetStatus_12cRegPtr_Cnt_T_str.IVR	9
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100

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Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2 0
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR	3 100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	2767
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	9
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSC	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	556 564
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	556 100
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_[2c_SetupMasterTransmit_[2cRegPtr_Cnt_T_str.CLR	1
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	3
target_i2cREG1_temp.IMR	100
target_i2cREG1_temp.STR	7788
target_i2cREG1_temp.CLKL	2767
target_i2cREG1_temp.CLKH	556
target_i2cREG1_temp.CNT	564
target_i2cREG1_temp.DRR	88
target_i2cREG1_temp.SAR	3 100
target_i2cREG1_temp.DXR target_i2cREG1_temp.MDR	2767
target i2cREG1_temp.IVR	9
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TEST DETAILS REPORT  DigColPsInt_InterruptNotification	2014-10-14, 23:42:41+0530	9	Razorcat
Name	Input Value		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	100		
target_i2cREG1_temp.PID11	556		
target_i2cREG1_temp.PID12	100		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	1		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	1		
target_i2cREG1_temp.ODR	3		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	12	12	~
DigColPsInt_Buffer_Cnt_M_u08[0]	123	123	✓
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	✓
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	✓
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✓
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✓
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	✓
DigColPsInt_ColSnsrData_Cnt_M_u16	2767	2767	<b>✓</b>
DigColPsInt_CurrentSlave_Cnt_M_u08	45	45	<b>✓</b>
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE	INIT_COMPLETE	<b>✓</b>
DigColPsInt_I2CHwCustData_Uls_M_u16	76	76	<b>✓</b>
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	77	77	<b>✓</b>
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	✓
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	<b>~</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	<b>~</b>
DigColPsInt_RecvdDataType_Cnt_M_u08	2	2	<b>✓</b>
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	564	564	<b>✓</b>
DigColPsInt_TransactionCnt_Cnt_M_u08	130	130	<b>✓</b>
I2c_Send(Length_Cnt_T_u32)	1	1	<b>✓</b>

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I2c\_SetupMasterTransmit(DataLength\_Cnt\_T\_u16)

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.OAR$ 

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.IMR$ 

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.STR$ 

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKL

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLKH$ 

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CNT

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DRR$ 

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.SAR$ 

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DXR

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.MDR$ 

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.IVR

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.EMDR$ 

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PSC

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PID11$ 

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PID12

target I2c GenStopCond I2cRegPtr Cnt T str.DMAC

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.FUN

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DIR

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DIN

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.SET$ 

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.CLR  $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.ODR$ 

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PD

 $target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.PSL$ 

 $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.OAR$ 

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IMR target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.STR

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKL

 $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CLKH$ 

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.CNT

 $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DRR$ 

target I2c Send I2cRegPtr Cnt T str.SAR

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.DXR

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.MDR

 $target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.IVR$ 

target\_I2c\_Send\_I2cRegPtr\_Cnt\_T\_str.EMDR

target\_I2c\_GenStopCond\_I2cRegPtr\_Cnt\_T\_str.DOUT

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	100	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	556	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	<u> </u>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	<u> </u>
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT	2	2	
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	0	0	- V
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	100	100	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.STR	7788	7788	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.CLKL	2767	2767	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.CLKH	556	556	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564	564	
target I2c SetRecv I2cRegPtr Cnt T str.DRR	88	88	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	100	100	
target I2c SetRecv I2cRegPtr Cnt T str.MDR	2767	2767	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.IVR	9	9	
target I2c SetRecv I2cRegPtr Cnt T str.EMDR	0	0	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.PSC	100	100	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	556	556	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100	100	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	
target I2c SetRecv I2cRegPtr Cnt T str.PSL	3	3	•
target I2c SetStatus I2cRegPtr Cnt T str.OAR	3	3	
target I2c SetStatus I2cRegPtr Cnt T str.IMR	100	100	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788	7788	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	
target I2c SetStatus I2cRegPtr Cnt T str.CLKH	556	556	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564	564	•
target I2c SetStatus I2cRegPtr Cnt T str.DRR	88	88	
target I2c SetStatus I2cRegPtr Cnt T str.SAR	3	3	•
target I2c SetStatus I2cRegPtr Cnt T str.DXR	100	100	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2767	2767	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9	9	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100	100	
target I2c SetStatus I2cRegPtr Cnt T str.PID11	556	556	·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100	100	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3	3	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100	100	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788	7788	
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLKL	2767	2767	
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLKH	556	556	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT	564	564	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR	88	88	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	100	
0			

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	9	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	100	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556	556	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	100	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	100	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	556	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	88	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100	100	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767	2767	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	100	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556	556	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	100	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>

T				V
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 3.40 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8
DigColPsInt_Buffer_Cnt_M_u08[0]	1
DigColPsInt_Buffer_Cnt_M_u08[1]	1
DigColPsInt_Buffer_Cnt_M_u08[2]	100
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	20
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	22
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	23
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	80
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str



Name	Input Value
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	44
k_SpurSensorI2CAddress_Cnt_u08	127
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target I2c GenStopCond I2cRegPtr Cnt T str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target I2c GenStopCond I2cRegPtr Cnt T str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target I2c Send I2cRegPtr Cnt T str.PID12	66
target I2c Send I2cRegPtr Cnt T str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target I2c Send I2cRegPtr Cnt T str.DIR	1
target_i2c_Send_i2cRegPtr_Cnt_T_str.DIN	2
target_i2c_Send_i2cRegPtr_Cnt_T_str.DOUT	3
target_i2c_Send_i2cRegPtr_Cnt_T_str.SET	3
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	1
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	2
	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87

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Name	Input Value	
target I2c SetRecv I2cRegPtr Cnt T str.DRR	67	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	
target_i2c_SetRecv_i2cRegPtr_Cnt_T_str.MDR	2309	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.IVR	5	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR	3	
	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC		
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	3	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DXR	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.IVR	5	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FMDR	3	
	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC		
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	1204	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	
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target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	2309	

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Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3		
target_i2cREG1_temp.OAR	55		
target_i2cREG1_temp.IMR	66		
target i2cREG1 temp.STR	556		
target i2cREG1 temp.CLKL	2309		
target_i2cREG1_temp.CLKH	1204		
target i2cREG1 temp.CNT	87		
target_i2cREG1_temp.DRR	67		
target i2cREG1 temp.SAR	55		
target_i2cREG1_temp.DXR	66		
target i2cREG1 temp.MDR	2309		
target_i2cREG1_temp.IVR	5		
target i2cREG1 temp.EMDR	3		
target i2cREG1 temp.PSC	66		
target_i2cREG1_temp.PID11	1204		
target_i2cREG1_temp.PID12	66		
target i2cREG1 temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target i2cREG1 temp.DIR	1		
target_i2cREG1_temp.DIN	2		
target i2cREG1 temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target i2cREG1 temp.CLR	1		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Resul
DigColPsInt AttempOccurForCustDatRead Cnt M u08	8	8	Resul
DigColPsInt_AttempoccurrorCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	
DigColPsInt_Buffer_Cnt_M_u08[1]	1	1	
DigColPsInt_Buffer_Cnt_M_u08[2]	100	100	
DIGOON SINT_DUNCI_ONT_W_UOO[2]	100	100	

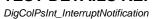
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8	8	•
DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	•
DigColPsInt_Buffer_Cnt_M_u08[1]	1	1	~
DigColPsInt_Buffer_Cnt_M_u08[2]	100	100	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	~
DigColPsInt_CmdFailOccurred_Cnt_M_Igc	1	1	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	~
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_SET	INIT_SENSOR2_EXTREADCTRLREG_SET	~
DigColPsInt_I2CHwCustData_Uls_M_u16	22	22	~
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	23	23	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	~
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	~
DigColPsInt_RecvdDataType_Cnt_M_u08	2	2	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	~
DigColPsInt_TransactionCnt_Cnt_M_u08	80	80	~
I2c_Send(Length_Cnt_T_u32)	1	1	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~

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Name	Actual Value 87	Expected Value 87	Result
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR	67	67	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11	1204	1204	<b>*</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID12 target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC	66 3	66 3	
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD	3	3	<b>V</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	3	3	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR	55 66	55 66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.NRR target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	
target_12c_Send_12cRegPtr_Cnt_T_str.STR  target_12c_Send_12cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	66	66	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11 target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	1204 66	1204 66	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>*</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3	3	Ž
target_12c_SetRecv_12cRegPtr_Cnt_T_str.P3L	55	55	~
target I2c SetRecv I2cRegPtr Cnt T str.IMR	66	66	_
target I2c SetRecv I2cRegPtr Cnt T str.STR	556	556	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>V</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	2309	2309 5	~
target_12c_SetRecv_12cRegPtr_Cnt_T_str.FMDR	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	1	1	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>*</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3 1	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.PSL	3	3	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR	55	55	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	~

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>-</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87 67	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67 55	55	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.IVR	5	5	
target I2c SetStatus I2cRegPtr Cnt T str.EMDR	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	
target I2c SetStatus I2cRegPtr Cnt T str.PID11	1204	1204	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID12	66	66	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	•
target I2c SetStatus I2cRegPtr Cnt T str.DIN	2	2	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	<u> </u>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.FUN	1	1	<u> </u>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	2	2	<b>Y</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR			
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.ODR	3	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	556	556	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKL	2309	2309	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH	1204	1204	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	87	87	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	67	67	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	2309	2309	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	-
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	66	66	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>



T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c_Send	1	I2c_Send	1	<b>✓</b>

Test Step 3.41 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8
DigColPsInt_Buffer_Cnt_M_u08[0]	28
DigColPsInt_Buffer_Cnt_M_u08[1]	200
DigColPsInt_Buffer_Cnt_M_u08[2]	250
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	7846
DigColPsInt_CurrentSlave_Cnt_M_u08	10
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR2 CHECKSTAT READ
DigColPsInt I2CHwCustData Uls M u16	40
DigColPsInt I2CHwIncompleteCustData UIs M u16	41
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
ligColPsInt_RecvOverrunError_Cnt_M_lgc	1
ligColPsInt_Recvoverruit_Hor_Cit_M_igc	3
ligColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
bigColPsInt_SkipRegisterwrite_Crit_ivi_igc	1
bigColPsint_SpurCustDatround_Cnt_wi_gc	98
DigColPsInt_TransactionCnt_Cnt_M_u08	12
Clags_Cnt_T_b16	32
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str
_DataRegisters_Cnt_u08[0]	0
_DataRegisters_Cnt_u08[1]	32
_DataRegisters_Cnt_u08[2]	30
_DataRegisters_Cnt_u08[3]	36
_DataRegisters_Cnt_u08[4]	38
_DataRegisters_Cnt_u08[5]	34
_DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
_DataRegisters_Cnt_u08[8]	14
2cREG1_temp	target_i2cREG1_temp
_ColSensorl2CAddress_Cnt_u08	74
_SpurSensorl2CAddress_Cnt_u08	100
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974
arget I2c GenStopCond I2cRegPtr Cnt T str.CNT	98
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10
arget I2c GenStopCond I2cRegPtr Cnt T str.MDR	7846
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	55
irget_12c_GenStopCond_12cRegPtr_Cnt_T_str.FMDR	1
rget I2c GenStopCond I2cRegPtI_Cnt_T_str.EMDR	10
riget_12c_GeristopCond_12cRegPtr_Cnt_1_str.P3C	8974
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	10
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2

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Name	Input Value	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	
target I2c GenStopCond I2cRegPtr Cnt T str.PD	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	10	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	
target I2c Send I2cRegPtr Cnt T str.FUN	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	
target I2c Send I2cRegPtr Cnt T str.DOUT	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	1	
target I2c Send I2cRegPtr Cnt T str.PD	1	
	1	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	10	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR		
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	
target I2c SetRecv I2cRegPtr Cnt T str.DIR	2	
target I2c SetRecv I2cRegPtr Cnt T str.DIN	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	
target I2c SetRecv I2cRegPtr Cnt T str.PD	1	
	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL		
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR	10	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	1223	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	8974	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	98	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	10	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	10	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7846	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	55	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC	10	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN		
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	

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DigColPSIIIL_InterruptiNotification	
Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	8974
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	2
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SET	1
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	10
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DXR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	10
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	8974
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	10
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	1
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	1
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtt_Cnt_T_str.DIN	1
	1
arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	1
arget_I2c_SetupMasterTransmit_I2cRegPti_Cnt_T_str.SET  arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
	1
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1 10
arget_i2cREG1_temp.OAR	
arget_i2cREG1_temp.IMR	10
arget_i2cREG1_temp.STR	1223
arget_i2cREG1_temp.CLKL	7846
arget_i2cREG1_temp.CLKH	8974
rarget_i2cREG1_temp.CNT	98
arget_i2cREG1_temp.DRR	12
arget_i2cREG1_temp.SAR	10
larget_i2cREG1_temp.DXR	10
target_i2cREG1_temp.MDR	7846
arget_i2cREG1_temp.IVR	55
target_i2cREG1_temp.EMDR	1
arget_i2cREG1_temp.PSC	10
target_i2cREG1_temp.PID11	8974
target_i2cREG1_temp.PID12	10
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_izertEGT_temp.r GN	·

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Name	Input Value		
target_i2cREG1_temp.DIN	1		
target i2cREG1 temp.DOUT	1		
target i2cREG1 temp.SET	1		
·	2		
target_i2cREG1_temp.CLR			
target_i2cREG1_temp.ODR			
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	1		
Name	Actual Value	Expected Value	Result
DigColPsInt AttempOccurForCustDatRead Cnt M u08	8	8	~
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	3	3	_
DigColPsInt_Buffer_Cnt_M_u08[2]	7	7	<b>✓</b>
	1	1	
DigColPsInt_BusBusySeqError_Cnt_M_lgc			~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	7846	7846	~
DigColPsInt_CurrentSlave_Cnt_M_u08	74	74	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR1 EXTREADADDRREG SEN	INIT SENSOR1 EXTREADADDRREG SEN	~
DigColPsInt_I2CHwCustData_Uls_M_u16	40	40	~
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	41	41	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt NackOccured Cnt M Igc	1	1	<b>~</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	~
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	98	98	~
DigColPsInt_TransactionCnt_Cnt_M_u08	12	12	~
I2c_Send(Length_Cnt_T_u32)	3	3	~
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223	1223	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
			J
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98	98	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12	12	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7846	7846	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	55	55	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target I2c GenStopCond I2cRegPtr Cnt T str.PSC	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	8974	8974	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR			
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	10	<b>~</b>
target_12c_Send_12cRegPtr_Cnt_T_str.STR	1223	1223	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	7846	7846	· ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98	98	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846	7846	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55	55	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10	10	_
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	8974	8974	
	10	10	Ž
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12			
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10	10	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10	10	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223	1223	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98	98	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	12	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10	10	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10	10	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846	7846	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55	55	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10	10	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974	8974	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10	10	

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Name	Actual Value	Expected Value	Result
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223	1223	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98	98	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10	10	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846	7846	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974	8974	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	~

T			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
SetupWriteData	1	SetupWriteData	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	•
I2c_Send	1	I2c_Send	1	-

Test Step 3.42 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	6
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	2767
DigColPsInt_CurrentSlave_Cnt_M_u08	45
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	37
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	38
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	564
DigColPsInt_TransactionCnt_Cnt_M_u08	130
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str

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DigColPsini_interruptivotilication		
Name	Input Value	
T_DataRegisters_Cnt_u08[0]	0	
T_DataRegisters_Cnt_u08[1]	32	
T_DataRegisters_Cnt_u08[2]	30	
T DataRegisters Cnt u08[3]	36	
T DataRegisters Cnt u08[4]	38	
T_DataRegisters_Cnt_u08[5]	34	
T_DataRegisters_Cnt_u08[6]	10	
T_DataRegisters_Cnt_u08[7]	12	
T_DataRegisters_Cnt_u08[8]	14	
i2cREG1_temp	target_i2cREG1_temp	
k_ColSensorl2CAddress_Cnt_u08	69	
k_SpurSensorI2CAddress_Cnt_u08	123	
	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR		
rarget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100	
rarget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR	7788	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767	
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH	556	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100	
arget I2c GenStopCond I2cRegPtr Cnt T str.DMAC	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	
	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	
rarget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD		
rarget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL	3	
rarget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	
arget I2c Send I2cRegPtr Cnt T str.EMDR	0	
arget I2c Send I2cRegPtr Cnt T str.PSC	100	
arget I2c Send I2cRegPtr Cnt T str.PID11	556	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	
	2	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.DMAC	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556	
	564	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100	
arget 12a CotPoor 12aPagPtr Cpt T atr MDP	2767	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	9	

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Name	Input Value	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100	
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	
arget I2c SetRecv I2cRegPtr Cnt T str.PD	0	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88	
arget I2c SetStatus I2cRegPtr Cnt T str.SAR	3	
arget I2c SetStatus I2cRegPtr Cnt T str.DXR	100	
arget I2c SetStatus I2cRegPtr Cnt T str.MDR	2767	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100	
	556	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	100	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12		
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	
rarget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	
rarget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	
arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	3	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	
arget I2c SetupMasterReceive I2cRegPtr Cnt T str.FUN	0	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	
arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	3	
arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	2	
arget I2c SetupMasterReceive I2cRegPtr_Cnt_1_str.bOUT	0	
	1	
arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLR	3	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	
arget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD		
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	
	00	
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	
arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR  arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	3	



	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1 3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET	0		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3		
target_i2cREG1_temp.OAR	3		
target_i2cREG1_temp.IMR	100		
target_i2cREG1_temp.STR	7788		
target_i2cREG1_temp.CLKL	2767		
target_i2cREG1_temp.CLKH	556		
target_i2cREG1_temp.CNT	564		
target_i2cREG1_temp.DRR	88		
target_i2cREG1_temp.SAR	3		
target_i2cREG1_temp.DXR	100		
target_i2cREG1_temp.MDR	2767		
target_i2cREG1_temp.IVR	9		
target_i2cREG1_temp.EMDR	0		
target_i2cREG1_temp.PSC	100		
target_i2cREG1_temp.PID11	556		
target_i2cREG1_temp.PID12	100		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	3		
target_i2cREG1_temp.DIII	2		
target_i2cREG1_temp.DOUT target_i2cREG1_temp.SET	0		
target_i2cREG1_temp.CLR	1		
target_izcred1_temp.oerv			
target i2cREG1 temp ODR			
target_i2cREG1_temp.ODR	3		
target_i2cREG1_temp.PD	0		
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL	0 3	Expected Value	Result
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL Name	0 3 Actual Value	Expected Value	Result
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	0 3 Actual Value 6	6	Result
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]	0 3 Actual Value 6 36	6 36	-
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]	0 3 Actual Value 6 36 145	6 36 145	-
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]	0 3 Actual Value 6 36	6 36	7
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	0 3 Actual Value 6 36 145 200	6 36 145 200	~
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc	0 3 Actual Value 6 36 145 200 0	6 36 145 200 0	~
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0 3 Actual Value 6 36 145 200 0	6 36 145 200 0	•
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc	0 3 Actual Value 6 36 145 200 0 1	6 36 145 200 0 1	
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16	0 3 Actual Value 6 36 145 200 0 1 0 2767	6 36 145 200 0 1 0 2767	
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08	0 3 Actual Value 6 36 145 200 0 1 0 2767 123	6 36 145 200 0 1 0 2767	
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum	0 3  Actual Value 6 36 145 200 0 1 0 2767 123 INIT_SENSOR2_READERROR_SETREG	6 36 145 200 0 1 0 2767 123 INIT_SENSOR2_READERROR_SETREG	0
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_UIs_M_u16	0 3  Actual Value 6 36 145 200 0 1 0 2767 123 INIT_SENSOR2_READERROR_SETREG 37 38 0	6 36 145 200 0 1 0 2767 123 INIT_SENSOR2_READERROR_SETREG 37 38 0	
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target_i2cREG1_temp.PD target_i2cREG1_temp.PSL.  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_laitFailedOnce_Cnt_M_lgc DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvdDataType_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_u08 DigColPsInt_TransactionCnt_Cnt_M_u08 DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	0 3  Actual Value 6 36 145 200 0 1 0 2767 123 INIT_SENSOR2_READERROR_SETREG 37 38 0 0 0 0 1 1 1 1 3 100 7788 2767 556	6 36 145 200 0 1 1 0 2767 123 IINIT_SENSOR2_READERROR_SETREG 37 38 0 0 0 0 1 1 1 1 3 100 7788 2767 5556	
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL.  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CndFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_lactHwCustData_Uls_M_u16 DigColPsInt_lackOccured_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL	0 3  Actual Value 6 36 145 200 0 1 0 2767 123 INIT_SENSOR2_READERROR_SETREG 37 38 0 0 0 0 1 1 1 1 3 100 7788 2767 556 564	6 36 145 200 0 1 1 0 2767 123 IINIT_SENSOR2_READERROR_SETREG 37 38 0 0 0 0 1 1 1 1 3 100 7788 2767 556 564	
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL.  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvOverunError_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_u08 DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL	0 3  Actual Value 6 36 145 200 0 1 1 0 2767 123 INIT_SENSOR2_READERROR_SETREG 37 38 0 0 0 0 1 1 1 1 3 100 7788 2767 556 564 88	6 36 145 200 0 1 0 2767 123 IINIT_SENSOR2_READERROR_SETREG 37 38 0 0 0 0 2 0 564 130 1 1 1 3 100 7788 2767 556 564 88	
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL.  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CndFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_lactHwCustData_Uls_M_u16 DigColPsInt_lackOccured_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CkL	0 3  Actual Value 6 36 145 200 0 1 0 2767 123 INIT_SENSOR2_READERROR_SETREG 37 38 0 0 0 0 1 1 1 1 3 100 7788 2767 556 564	6 36 145 200 0 1 1 0 2767 123 IINIT_SENSOR2_READERROR_SETREG 37 38 0 0 0 0 1 1 1 1 3 100 7788 2767 556 564	

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9	9	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100	100	<b>✓</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PID11	556	556	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100	100	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>Y</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	1	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	100	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	7788	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	556	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	564	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	88	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	3	<b>v</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	100	<b>Y</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	2767	
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	9	9	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	100	100	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC target_l2c_Send_l2cRegPtr_Cnt_T_str.PID11	556	556	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>→</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>→</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3	3	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100	100	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	7788	<b>V</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	2767	2767	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	556 564	556 564	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	88	88	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3	3	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100	100	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767	2767	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9	9	·
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	100	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556	556	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100	100	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLR	1	1	<b>~</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	3	3	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3	3	<b>y</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR	100	100 7788	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788 2767	2767	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH	556	556	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKn	564	564	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.DRR	88	88	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3	3	<b>→</b>
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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100	100	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2767	2767	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9	9	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100	100	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556	556	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100	100	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	0	0	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIR	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3 2	3 2	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	0	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	3	3	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL	3	3	
	3	3	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	100	100	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	7788	7788	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR target_I2c SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKH	556	556	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564	564 88	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3	3	
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DXR	100	100	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	2767	Ž
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	9	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	100	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556	556	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	100	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	<b>v</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	<b>Y</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	<b>Y</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>Y</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	100	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	<b>Y</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	556	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	88	<b>Y</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100	100	<b>v</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767	2767	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	100	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556	556	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	100	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	<b>✓</b>



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Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c Send	1	I2c Send	1	_

est Step 3.43 (Repeat Count = 1)	Invest Value
ame	Input Value
igColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8
igColPsInt_Buffer_Cnt_M_u08[0]	100
igColPsInt_Buffer_Cnt_M_u08[1]	200
igColPsInt_Buffer_Cnt_M_u08[2]	250
igColPsInt_BusBusySeqError_Cnt_M_lgc	1
igColPsInt_CmdFailOccurred_Cnt_M_lgc	1
igColPsInt_ColCustDatFound_Cnt_M_lgc	1
igColPsInt_ColSnsrData_Cnt_M_u16	7846
igColPsInt_CurrentSlave_Cnt_M_u08	10
igColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_READ
igColPsInt_I2CHwCustData_Uls_M_u16	40
igColPsInt_I2CHwIncompleteCustData_Uls_M_u16	41
igColPsInt_InitFailedOnce_Cnt_M_Igc	0
igColPsInt_NackOccured_Cnt_M_lgc	1
igColPsInt_PrevReqDataType_Cnt_M_u08	3
igColPsInt_RecvOverrunError_Cnt_M_lgc	1
igColPsInt_RecvdDataType_Cnt_M_u08	3
igColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
igColPsInt_SpurCustDatFound_Cnt_M_lgc	1
igColPsInt_SpurSnsrData_Cnt_M_u16	98
igColPsInt_TransactionCnt_Cnt_M_u08	12
ags_Cnt_T_b16	32
c_GenStopCond(I2cRegPtr_Cnt_T_str)	target I2c GenStopCond I2cRegPtr Cnt T str
c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
c SetStatus(I2cRegPtr Cnt T str)	target I2c SetStatus I2cRegPtr Cnt T str
c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
_DataRegisters_Cnt_u08[0]	0
_DataRegisters_Cnt_u08[1]	32
_DataRegisters_Cnt_u08[2]	30
_DataRegisters_Cnt_u08[3]	36
_DataRegisters_Cnt_u08[4]	38
_DataRegisters_Cnt_u08[5]	34
_DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
_DataRegisters_Cnt_u08[8]	14
cREG1_temp	target_i2cREG1_temp
_ColSensorl2CAddress_Cnt_u08	74
_SpurSensorI2CAddress_Cnt_u08	100
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98
rget I2c GenStopCond I2cRegPtr Cnt T str.DRR	12
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7846
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	55
rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR	1
rget I2c GenStopCond I2cRegPtr Cnt T str.PSC	10
	8974
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	10
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	•
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DOUT rget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SET	1

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Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10
target I2c Send I2cRegPtr Cnt T str.STR	1223
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target I2c Send I2cRegPtr Cnt T str.PSC	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10
	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223
	7846
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1.
target I2c SetRecv I2cRegPtr Cnt T str.PSC	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	1223
target_12c_SetStatus_12cRegPtr_Cnt_T_str.CLKL	7846
target_12c_SetStatus_12cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	98
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR	12
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR	10
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_12c_SetStatus_12cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1

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Name   December   De		
barget (Dec.) Servicement (Dec.) Type CORN         2           barget (Dec.) Servicement (Dec.) Type CORN         1           barget (Dec.) Servicement (Dec.) Type CORN         1           barget (Dec.) Servicement (Dec.) Proc.) Type CORN (Dec.) Type CORN         1           barget (Dec.) Servicement (Dec.) Proc.) Type CORN (Dec.) Type CORN         1           barget (Dec.) Servicement (Dec.) Proc.) Type CORN (Dec.) Type CORN         1           barget (Dec.) Servicement (Dec.) Proc.) Type CORN (Dec.) Type CORN         1           barget (Dec.) Servicement (Dec.) Proc.) Type CORN (Dec.) Ty	Name	Input Value
barget (Dec.) Servicement (Dec.) Type CORN         2           barget (Dec.) Servicement (Dec.) Type CORN         1           barget (Dec.) Servicement (Dec.) Type CORN         1           barget (Dec.) Servicement (Dec.) Proc.) Type CORN (Dec.) Type CORN         1           barget (Dec.) Servicement (Dec.) Proc.) Type CORN (Dec.) Type CORN         1           barget (Dec.) Servicement (Dec.) Proc.) Type CORN (Dec.) Type CORN         1           barget (Dec.) Servicement (Dec.) Proc.) Type CORN (Dec.) Type CORN         1           barget (Dec.) Servicement (Dec.) Proc.) Type CORN (Dec.) Ty	target I2c SetStatus I2cRegPtr Cnt T str.SET	1
Sept   10.5 Sept   1.5 Sept   1		
Image   12   Selfabus   Exclosify Cut   T set PD		
	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
barger ID, Selaphysterifectore, Discipling CLT, profiled         10           barger, ID, Selaphysterifectore, Discipling CLT, profiled         10           barger, ID, Selaphysterifectore, Discipling CLT, profiled         1223           barger, ID, Selaphysterifectore, Discipling CLT, profiled         374           barger, ID, Selaphysterifectore, Discipling CLT, profiled         10           barger, ID, Selaphysterifectore, Discipling CLT, profiled         10           barger, ID, Selaphysterifectore, Discipling CLT, profiled         1           barger, ID, Selaphysterifectore, Discipling CLT, profiled         1 </td <td>target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD</td> <td>1</td>	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
tages   D. S. Sanukharis Receive   2016-php   Cm   _ ser DAR	target I2c SetStatus I2cRegPtr Cnt T str.PSL	1
Image   Dr. Schnekharricheone   Driebergh Cort   _ met NR	v v	
Larget, D.C., Satushbarte Receive Dischaptor C.T., and D.T.R.         1221           Larget, D.C., Satushbarte Receive Dischaptor C.T., and D.R.R.         1974           Larget, D.C., Satushbarte Receive Dischaptor, C.T., and D.R.R.         1974           Larget, D.C., Satushbarte Receive Dischaptor, C.T., and D.R.R.         19           Larget, D.C., Satushbarte Receive Dischaptor, C.T., and D.R.R.         10           Larget, D.C., Satushbarte Receive Dischaptor, C.T., and D.R.R.         10           Larget, D.C., Satushbarte Receive Dischaptor, C.T., and D.R.R.         10           Larget, D.C., Satushbarte Receive Dischaptor, C.T., and D.R.R.         7684           Larget, D.C., Satushbarte Receive Dischaptor, C.T., and D.R.R.         1           Larget, D.C., Satushbarte Receive Dischaptor, C.T., and D.R.R.         1           Larget, D.C., Satushbarte Receive Dischaptor, C.T., and D.R.R.         1           Larget, D.C., Satushbarte Receive Dischaptor, C.T., and D.R.R.         1           Larget, D.C., Satushbarte Receive Dischaptor, C.T., and D.R.R.         1           Larget, D.C., Satushbarte Receive Dischaptor, C.T., and D.R.R.         1           Larget, D.C., Satushbarte Receive Dischaptor, C.T., and D.R.R.         1           Larget, D.C., Satushbarte Receive Dischaptor, C.T., and D.R.R.         1           Larget, D.C., Satushbarte Receive Dischaptor, C.M.R.R.         1           Larget, D.C		
Biology E.P., Selephatericone p. Discipler C.P., 19 C. I. 101         8974           Biology E.P., Selephatericone p. Discipler C.P., 19 C. I. 101         8974           Biology E.P., Selephatericone p. Discipler C.P., 19 C. I. 101         12           Biology E.P., Selephatericone p. Discipler C.P., 19 C. II 101         10           Biology E.P., Selephatericone p. Discipler C.P., 19 C. II 101         10           Biology E.P., Selephatericone p. Discipler C.P., 19 D. II 101         10           Biology E.P., Selephatericone p. Discipler C.P., 19 D. II 101         10           Biology E.P., Selephatericone p. Discipler C.P., 19 D. II 101         10           Biology E.P., Selephatericone p. Discipler C.P., 19 D. II 101         10           Biology E.P., Selephatericone p. Discipler C.P., 19 D. II 101         10           Biology E.P., Selephatericone p. Discipler C.P., 19 D. II 101         10           Biology E.P., Selephatericone p. Discipler C.P., 19 D. II 101         10           Biology E.P., Selephatericone p. Discipler C.P., 19 D. II 101         10           Biology E.P., Selephatericone p. Discipler C.P., 19 D. II 101         1           Biology E.P., Selephatericone p. Discipler C.P., 19 D. II 101         1           Biology E.P., Selephatericone p. Discipler C.P., 19 D. II 101         1           Biology E.P., Selephatericone p. Discipler C.P., 19 D. II 101         1           Biology E.P., Sel	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	10
togst_DR_Selsylvateriscone_Disciple_Cststrict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Strict_Str	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223
taggst Dr. Sesphyterinforceus, Dickley Dr. Chr. Law CH 1997   taggst Dr. Sesphyterinforceus, Dickley Dr. Chr. Law CH 1998   taggst Dr. Sesphyterinforceus, Dickley Dr. Chr. Law CH 1998   taggst Dr. Sesphyterinforceus, Dickley Dr. Chr. Law CH 1998   taggst Dr. Sesphyterinforceus, Dickley Dr. Chr. Law CH 1998   taggst Dr. Sesphyterinforceus, Dickley Dr. Chr. Law CH 1998   taggst Dr. Sesphyterinforceus, Dickley Dr. Chr. Law CH 1998   taggst Dr. Sesphyterinforceus, Dickley Dr. Chr. Law CH 1998   taggst Dr. Sesphyterinforceus, Dickley Dr. Chr. Law CH 1998   taggst Dr. Sesphyterinforceus, Dickley Dr. Chr. Law CH 1998   taggst Dr. Sesphyterinforceus, Dickley Dr. Chr. Law CH 1998   taggst Dr. Sesphyterinforceus, Dickley Dr. Chr. Law CH 1998   taggst Dr. Sesphyterinforceus, Dickley Dr. Chr. Law CH 1998   taggst Dr. Sesphyterinforceus, Dickley Dr. Chr. Law CH 1998   taggst Dr. Sesphyterinforceus, Dickley Dr. Chr. Law CH 1998   taggst Dr. Sesphyterinforceus, Dickley Dr. Chr. Law CH 1998   taggst Dr. Sesphyterinforceus, Dickley Dr. Chr. Law CH 1998   taggst Dr. Sesphyterinforceus, Dickley Dr. Chr. Law CH 1998   taggst Dr. Sesphyterinforceus, Dickley Dr. Chr. Law CH 1998   taggst Dr. Sesphyterinforceus, Dickley Dr. Chr. Law CH 1998   taggst Dr. Sesphyterinforceus, Dickley Dr. Chr. Law CH 1998   taggst Dr. Sesphyterinforceus, Dickley Dr. Chr. Law CH 1998   taggst Dr. Sesphyterinforceus, Dickley Dr. Chr. Law CH 1998   taggst Dr. Sesphyterinforceus, Dickley Dr. Chr. Law CH 1998   taggst Dr. Sesphyterinforceus, Dickley Dr. Chr. Law CH 1998   taggst Dr. Sesphyterinforceus, Dickley Dr. Chr. Law CH 1998   taggst Dr. Sesphyterinforceus, Dickley Dr. Chr. Law CH 1998   taggst Dr. Sesphyterinforceus, Dickley Dr. Chr. Law CH 1998   taggst Dr. Sesphyterinforceus, Dickley Dr. Chr. Law CH 1998   taggst Dr. Sesphyterinforceus, Dickley Dr. Chr. Law CH 1998   taggst Dr. Sesphyterinforceus, Dickley Dr. Chr. Law CH 1998   taggst Dr. Sesphyterinforceus, Dr. Chr. Law CH 1998   taggst Dr. Sesphyterinforceus, Dr. Chr. Law CH 1998   taggst Dr. Sesph	target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	7846
		8074
Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         10           Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         10           Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         10           Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         10           Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         11           Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         1           Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         1           Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         1           Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         1           Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         1           Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         1           Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         1           Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         1           Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         1           Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         1           Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         1           Langer, D.C., Sestphanter Roceue, Discripting, Dull. 2 at SAR         1           Langer, D.C., Sestphanter Roc		
Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         10           Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         786           Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         786           Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         786           Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         1           Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         10           Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         10           Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         1           Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         1           Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         1           Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         1           Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         1           Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         1           Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         1           Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         1           Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         1           Langer, D.C., Sentphater Recover, Discoppin, Cort. Jan JAN R         1           Langer, D.C., Sentphater Recover, Discoppi		
torget Dic, SestphanterRorow, DicRegNpt, Coll. T. at JNDR   19   19   19   19   19   19   19   1	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12
Larget 12: SetupMaterinReceive 12: DRISEQPU CNT_str XVIN         55           Larget 12: SetupMaterinReceive 20: DRISEQPU CNT_str XVIN         55           Larget 12: SetupMaterinReceive 20: DRISEQPU CNT_str XVINC         10           Larget 12: SetupMaterinReceive 20: DRISEQPU CNT_str XVINC         1           Larget 12: SetupMaterinReceive 20: DRISEQPU CNT_str XVINC         1 <t< td=""><td>target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR</td><td>10</td></t<>	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10
Larget 12: SetupMaterinReceive 12: DRISEQPU CNT_str XVIN         55           Larget 12: SetupMaterinReceive 20: DRISEQPU CNT_str XVIN         55           Larget 12: SetupMaterinReceive 20: DRISEQPU CNT_str XVINC         10           Larget 12: SetupMaterinReceive 20: DRISEQPU CNT_str XVINC         1           Larget 12: SetupMaterinReceive 20: DRISEQPU CNT_str XVINC         1 <t< td=""><td>target I2c SetupMasterReceive I2cRegPtr Cnt T str.DXR</td><td>10</td></t<>	target I2c SetupMasterReceive I2cRegPtr Cnt T str.DXR	10
Image: 1.2. SetupAnterReceive; DERRepPIC CNT _ SETURNER		
target 102. SetupMater Receive (2Relegif Cost 1_pt PID1)  target 102. SetupMater Transmit (2Relegif Cost 1_pt PID1)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_I_str.IVR	
Impel 12. SebupMasterRecous (Enterlight Cost. 1 pt/1011) Impel 12. SebupMasterRecous (Enterlight Cost. 1 pt/1012) Impel 12. SebupMasterRecous (Enterlight Cost. 1 pt/1014) Impel 12. SebupMasterRecous (Enterlight Cost. 1 pt/1014) Impel 12. SebupMasterRecous (Enterlight Cost. 1 pt/1014) Impel 12. SebupMasterRecous, (Enterlight Cost. 1 pt/1018) Impel 12. SebupMasterTrammil (Enterlight Cost. 1 pt/1018) Impel 12. SebupMaster	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
	target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSC	10
target (J.C. SchepMasterRocene) (2cRopPt Cont_tail DMAG target (J.C. SchepMasterRocene) (2cRopPt Cont_tail Schep target (J.C. SchepMaster Target) (2cropPt		
large_LD_S_SelupMasterRecoles_120RegPtr_CNT_Ist_INUN         1           large_LD_S_SelupMasterRecoles_120RegPtr_CNT_Ist_INUN         2           large_LD_S_SelupMasterRecoles_120RegPtr_CNT_Ist_INUN         2           large_LD_S_SelupMasterRecoles_120RegPtr_CNT_Ist_INUN         1           large_LD_S_SelupMasterRecoles_120RegPtr_CNT_Ist_INUN         1           large_LD_S_SelupMasterRecoles_120RegPtr_CNT_Ist_INUN         1           large_LD_S_SelupMasterRecoles_120RegPtr_CNT_Ist_INUN         2           large_LD_S_SelupMasterRecoles_120RegPtr_CNT_Ist_INUN         1           large_LD_S_SelupMasterRecoles_120RegPtr_CNT_Ist_INUN         1           large_LD_S_SelupMasterRecoles_120RegPtr_CNT_Ist_INUN         1           large_LD_S_SelupMasterTrainer_LDREGPTr_CNT_Ist_INUN         1           large_LD_S_SelupMasterTrainer_LDREGPTr_CNT_Ist_INUN         1           large_LD_S_SelupMasterTrainer_LDREGPTr_CNT_Ist_INUN         1           large_LD_S_SelupMasterTrainer_LDREGPTr_CNT_Ist_INUN         1           large_LD_S_SelupMasterTrainer_LDREGPTr_CNT_Ist_INUN         1           large_LD_S_SelupMasterTrainer_LDREGPTr_CNT_Ist_Inut_INUN         1           large_LD_S_SelupMasterTrainer_LDREGPTr_CNT_Ist_Inut_INUN         1           large_LD_S_SelupMasterTrainer_LDREGPTr_CNT_Ist_Inut_INUN         1           large_LD_S_SelupMasterTrainer_LDREGPTr_CNT_Ist_Inut_INUN <t< td=""><td></td><td></td></t<>		
target, I.C. SetupMasterTacenou, 12cReptPr. Cont. I. str DIN togget, I.C. SetupMasterTacenou, 12cReptPr. Cont. I. str DIN togget, I.C. SetupMasterTacenou, 12cReptPr. Cont. I. str DIN togget, I.C. SetupMasterTacenou, 12cReptPr. Cont. I. str DINI tog	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_I_str.PID12	
Lingel, E.D., SelephiasterReceive, 120Reptpt, Cort. T. str. DIN         1           Lingel, E.D., SelephiasterReceive, 120Reptpt, Cort. T. str. DIN         1           Lingel, E.D., SelephiasterReceive, 120Reptpt, Cort. T. str. DIN         1           Lingel, E.D., SelephiasterReceive, 120Reptpt, Cort. T. str. SET         1           Lingel, E.D., SelephiasterReceive, 120Reptpt, Cort. T. str. CUR         2           Lingel, E.D., SelephiasterReceive, 120Reptpt, Cort. T. str. CUR         2           Lingel, E.D., SelephiasterReceive, 120Reptpt, Cort. T. str. CUR         1           Lingel, E.D., SelephiasterReceive, 120Reptpt, Cort. T. str. CUR         1           Lingel, E.D., SelephiasterTrainell, 120Reptp, Cort. T. str. CUR         1           Lingel, E.D., SelephiasterTrainell, 120Reptp, Cort. T. str. CUR         10           Lingel, E.D., SelephiasterTrainell, 120Reptp, Cort. T. str. CUR         10           Lingel, E.D., SelephiasterTrainell, 120Reptp, Cort. T. str. CUR         10           Lingel, E.D., SelephiasterTrainell, 120Reptp, Cort. T. str. CUR         894           Lingel, E.D., SelephiasterTrainell, 120Reptp, Cort. T. str. CUR         98           Lingel, E.D., SelephiasterTrainell, 120Reptp, Cort. T. str. SUR         10           Lingel, E.D., SelephiasterTrainell, 120Reptp, Cort. T. str. SUR         10           Lingel, E.D., SelephiasterTrainell, 120Reptp, Cort. T. str. SUR         10	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
tigget_IDS_SebupMasterFacebus_IDS-Reptr_ On_T_ ist DIN         1           tigget_IDS_SebupMasterFacebus_IDS-Reptr_ On_T_ ist DIN         2           tigget_IDS_SebupMasterFacebus_IDS-Reptr_ On_T_ ist DIN         2           tigget_IDS_SebupMasterFacebus_IDS-Reptr_ On_T_ ist DIN         1           tigget_IDS_SebupMasterFacebus_IDS-Reptr_ On_T_ ist DIN         1           tigget_IDS_SebupMasterFacebus_IDS-Reptr_ On_T_ ist DIN         1           tigget_IDS_SebupMasterFacebus_IDS-Reptr_ On_T_ ist DIN         10           tigget_IDS_SebupMasterFacebus_IDS-	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
targer L.D. Schuphater Fraceric Lord Schoph Cot I, 3 at DOVT 1 targer L.D. Schuphater Fraceric Lord Schoph Cot I, 3 at DOVT 1 targer L.D. Schuphater Fraceric Lord Schoph Cot I, 3 at DOVT 1 targer L.D. Schuphater Fraceric Lord Schoph Cot I, 3 at DOVT 1 targer L.D. Schuphater Fraceric Lord Schoph Cot I, 3 at DOV 1 targer L.D. Schuphater Fraceric Lord Schoph Cot I, 3 at DOV 1 targer L.D. Schuphater Fraceric Lord Schoph Cot I, 3 at DOV 1 targer L.D. Schuphater Fraceric Lord Schoph Cot I, 3 at DOV 1 targer L.D. Schuphater Fraceric Lord Schoph Cot I, 3 at DOV 1 targer L.D. Schuphater Fraceric Lord Schoph Cot I, 3 at DOV 1 targer L.D. Schuphater Fraceric Lord Schoph Cot I, 3 at DOV 1 targer L.D. Schuphater Fraceric Lord Schoph Cot I, 3 at DOV 1 targer L.D. Schuphater Fraceric Lord Schoph Cot I, 3 at DOV 1 targer L.D. Schuphater Fraceric Lord Schoph Cot I, 3 at DOV 1 targer L.D. Schuphater Fraceric Lord Schoph Cot I, 3 at DOV 1 targer L.D. Schuphater Fraceric Lord Schoph Cot I, 3 at DOV 1 targer L.D. Schuphater Fraceric Lord Schoph Cot I, 3 at DOV 1 targer L.D. Schuphater Fraceric Lord Schoph Cot I, 3 at DOV 1 targer L.D. Schuphater Fraceric Lord Schoph Cot I, 3 at DOV 1 targer L.D. Schuphater Fraceric Lord Schoph Cot I, 3 at DOV 1 targer L.D. Schuphater Fraceric Lord Schoph Cot I, 3 at DOV 1 targer L.D. Schuphater Fraceric Lord Schoph Cot I, 3 at DOV 1 targer L.D. Schuphater Fraceric Lord Schoph Cot I, 3 at DOV 1 targer L.D. Schuphater Fraceric Lord Schoph Cot I, 3 at DOV 1 targer L.D. Schuphater Fraceric Lord Schoph Cot I, 3 at DOV 1 targer L.D. Schuphater Fraceric Lord Schoph Cot I, 3 at DOV 1 targer L.D. Schuphater Fraceric Lord Schoph Cot I, 3 at DOV 1 targer L.D. Schuphater Fraceric Lord Schoph Cot I, 3 at DOV 1 targer L.D. Schuphater Fraceric Lord Schoph Cot II, 3 at DOV 1 targer L.D. Schuphater Fraceric Lord Schoph Cot II, 3 at DOV 1 targer L.D. Schuphater Fraceric Lord Schoph Cot II, 3 at DOV 1 targer L.D. Schuphater Fraceric Lord Schoph Cot II, 3 at DOV 1 targer L.D. Schophater Fraceric Lord Schoph Cot II, 3		2
large_L2_SebuphasterFaceev_L2CRepPt_COT_Tat DUT         1           large_L2_SebuphasterFaceev_L2CRepPt_COT_Tat DUT         2           large_L2_SebuphasterFaceev_L2CRepPt_COT_Tat Dut COR         1           large_L2_SebuphasterFamami_L2CRepPt_COT_Tat Dut COR         1           large_L2_SebuphasterFamami_L2CRepPt_COT_Tat Dut COR         1           large_L2_SebuphasterFamami_L2CRepPt_COT_Tat Dut COR         1           large_L2_SebuphasterFamami_L2CRepPt_COT_Tat Dut COR         8874           large_L2_SebuphasterFamami_L2CRepPt_COT_Tat Dut COR         98           large_L2_SebuphasterFamami_L2CRepPt_COT_Tat Dut COR         1           large_L2_SebuphasterTamami_L2CRepPt_COT_Tat Dut COR         1           large_L2_SebuphasterTamami_L2CRepPt_COT_Tat Dut COR         1           large_L2_SebuphasterTamami_L2CRepPt_COT_Tat Dut COR         5           large_L2_SebuphasterTamami_L2CRepPt_COT_Tat Dut COR         1           large_L2_SebuphasterTamami_L2CRepPt_COT_Tat Dut COR         1           large_L2_SebuphasterTamami_L2CRepPt_COT_Tat Dut COR         1		
target_Dz. SehuphdasterReceive_IzcReght_Cott_I str.CIR         2           target_Dz. SehuphdasterReceive_IzcReght_Cott_I str.CIR         2           target_Dz. SehuphdasterReceive_IzcReght_Cott_I str.CIR         1           target_Dz. SehuphdasterReceive_IzcReght_Cott_I str.DIL         1           target_Dz. SehuphdasterReceive_IzcReght_Cott_I str.DIL         1           target_Dz. SehuphdasterTarenin_IzcReght_Cott_I str.DIL         10           target_Dz. SehuphdasterTarenin_IzcReght_Cott_I str.DIL         10           target_Dz. SehuphdasterTarenin_IzcReght_Cott_I str.DIL         7846           target_Dz. SehuphdasterTarenin_IzcReght_Cott_I str.CIK         7846           target_Dz. SehuphdasterTarenin_IzcReght_Cott_I str.DIR         12           target_Dz. SehuphdasterTarenin_IzcReght_Cott_I str.DIR         12           target_Dz. SehuphdasterTarenin_IzcReght_Cott_I str.DIR         10           target_Dz. SehuphdasterTarenin_IzcReght_Cott_I str.DIR         7846           target_Dz. SehuphdasterTarenin_IzcReght_Cott_I str.DIR         7846           target_Dz. SehuphdasterTarenin_IzcReght_Cott_I str.DIR         7846           target_Dz. SehuphdasterTarenin_IzcReght_Cott_I str.DIR         1           target_Dz. SehuphdasterTarenin_IzcReght_Cott_I str.DIR         1           target_Dz. SehuphdasterTarenin_IzcReght_Cott_I str.DIR         1           target_Dz. Sehuphdaster		
larget_L2b. SchupMasterRoceive_L2cRegPtr_Cnt_1 at CNR         2           larget_L2b. SchupMasterRoceive_L2cRegPtr_Cnt_1 at CNR         1           larget_L2b. SchupMasterRoceive_L2cRegPtr_Cnt_1 at CNR         1           larget_L2b. SchupMasterRoceive_L2cRegPtr_Cnt_1 at CNR         1           larget_L2b. SchupMasterRoceive_L2cRegPtr_Cnt_1 at CNR         10           larget_L2b. SchupMasterTransmit_L2cRegPtr_Cnt_1 at CNR         10           larget_L2b. SchupMasterTransmit_L2cRegPtr_Cnt_1 at CNR         10           larget_L2b. SchupMasterTransmit_L2cRegPtr_Cnt_1 at CNR         1223           larget_L2b. SchupMasterTransmit_L2cRegPtr_Cnt_1 at CNR         8974           larget_L2b. SchupMasterTransmit_L2cRegPtr_Cnt_1 at CNR         98           larget_L2b. SchupMasterTransmit_L2cRegPtr_Cnt_1 at CNR         12           larget_L2b. SchupMasterTransmit_L2cRegPtr_Cnt_1 at XDR         10           larget_L2b. SchupMasterTransmi		
target_12e_SetupMaster Receive_12eRegPtr_Cntstr.PD  target_12e_SetupMaster Receive_12eRegPtr_Cntstr.PD  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.PSL  1  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.PSL  10  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.PSL  10  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.PSR  1223  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.Ctt.M  1364  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.Ctt.M  1364  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.Ctt.M  1364  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.Ctt.M  1364  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.DXR  1365  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.DXR  1465  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.DXR  1565  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.DXR  1666  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.DXR  1766  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.DXR  1766  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.DXR  1767  target_12e_Setu	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_12e_SetupMaster Receive_12eRegPtr_Cntstr.PD  target_12e_SetupMaster Receive_12eRegPtr_Cntstr.PD  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.PSL  1  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.PSL  10  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.PSL  10  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.PSR  1223  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.Ctt.M  1364  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.Ctt.M  1364  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.Ctt.M  1364  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.Ctt.M  1364  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.DXR  1365  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.DXR  1465  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.DXR  1565  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.DXR  1666  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.DXR  1766  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.DXR  1766  target_12e_SetupMaster Transmit_12eRegPtr_Cntstr.DXR  1767  target_12e_Setu	target I2c SetupMasterReceive I2cReqPtr Cnt T str.CLR	2
Image   122_SetupMaster   124RegPt   CRI   T. str PD		1
target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DAR         1           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DAR         10           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DAR         10           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DLT_str U.RL         1223           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DLT_str U.RL         748           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DAR         12           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DAR         12           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DAR         12           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DAR         12           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DAR         10           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DAR         10           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DAR         7846           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DAR         10           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DAR         11           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DAR         11           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DAR         11           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DAR         11           target_12e_SebupMasterTransmit_IzRepPri_Ont_T_str DAR         12           target_12e_SebupMaste		
Isrget   2c. SetupMasterTransmit   2cRepPtr_Cnt_TstMR   10	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_I_str.PD	
target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_NMR         10           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_CLKL         7846           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_CLKH         8974           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_CLKH         8974           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_CKH         98           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_Str_AR         10           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_Str_AR         10           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_Str_AR         10           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_MRR         7846           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_MRR         7846           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_MRR         1           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_MRR         1           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_D1D1         8974           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_D1D1         1           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_D1D1         1           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_D1D1         1           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_D1D1         1           target_12e_SetupMasterTransmit_L2cRegPtr_CntT_str_D1D1         1           target_12e_SetupMast	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1
target_12e_SetupMasterTransmit_J2cRagePtr_CntT_str.NR         10           target_12e_SetupMasterTransmit_J2cRagePtr_CntT_str.CLK1         7846           target_12e_SutupMasterTransmit_J2cRagePtr_CntT_str.CLK1         8974           target_12e_SetupMasterTransmit_J2cRagePtr_CntT_str.CLK1         98           target_12e_SetupMasterTransmit_J2cRagePtr_CntT_str.DKR         12           target_12e_SetupMasterTransmit_J2cRagePtr_CntT_str.DKR         10           target_12e_SetupMasterTransmit_J2cRagePtr_CntT_str.DKR         10           target_12e_SetupMasterTransmit_J2cRagePtr_CntT_str.DKR         10           target_12e_SetupMasterTransmit_J2cRagePtr_CntT_str.DKR         7846           target_12e_SetupMasterTransmit_J2cRagePtr_CntT_str.DKR         1           target_12e_SetupMasterTransmit_J2cRagePtr_CntT_str.DKR         2           target_12e_SetupMasterTransmit_J2cRagePtr_CntT_str.DKR         1           target_12e_SetupMasterTran	target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	10
large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_CLK.         7846           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_CLK.         7846           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_CNLT         8874           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_DNLT         98           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_DNR         10           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_DNR         10           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_DNR         10           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_DNR         7846           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_DNR         55           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_DNDR         1           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_DDID1         8974           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_DDID1         8974           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_DDID1         10           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_DDID2         10           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_DDID3         1           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_DDID3         1           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_DDID4         2           large_Lize_SetupMasterTransmit_L2cRegPtr_CnLT_str_DDID4         1           large_Lize_REGI		
Lorge Lize: SetupMasterTransmit JacRepPtr_Cnt_T_str.CLKI         7846           Lize: SetupMasterTransmit JacRepPtr_Cnt_T_str.CNT         8874           Lize: SetupMasterTransmit JacRepPtr_Cnt_T_str.CNT         98           Lize: Lize: SetupMasterTransmit JacRepPtr_Cnt_T_str.DNR         10           Lize: Lize: SetupMasterTransmit JacRepPtr_Cnt_T_str.DNR         11           Lize: Lize: SetupMasterTransmit JacRepPtr_Cnt_T_str.DNR         11           Lize: Lize: SetupMasterTransmit JacRepPtr_Cnt_T_str.DNR         1           Lize: Lize: SetupMasterTransmit JacRepPtr_Cnt_T_str.DNR         1           Lize: Lize: SetupMasterTransmit JacRepPtr_Cnt_T_str.DNA         1           Lize: Lize: SetupMaster		
larget Lize. SetupMasterTransmit JazRepPtr_Cnt_T_str.CNT         897           target Lize. SetupMasterTransmit JazRepPtr_Cnt_T_str.DRT         12           target Lize. SetupMasterTransmit JazRepPtr_Cnt_T_str.DRR         12           target Lize. SetupMasterTransmit JazRepPtr_Cnt_T_str.DRR         10           target Lize. SetupMasterTransmit JazRepPtr_Cnt_T_str.DRN         10           target Lize. SetupMasterTransmit JazRepPtr_Cnt_T_str.DNR         7846           target Lize. SetupMasterTransmit JazRepPtr_Cnt_T_str.DNR         5           target Lize. SetupMasterTransmit JazRepPtr_Cnt_T_str.DNR         1           target Lize. SetupMasterTransmit JazRepPtr_Cnt_T_str.DNR         1           target Lize. SetupMasterTransmit JazRepPtr_Cnt_T_str.DNAC         10           target Lize. SetupMasterTransmit JazRepPtr_Cnt_T_str.DNAC         11           target Lize. SetupMasterTransmit JazRepPtr_Cnt_T_str.DNAC         1           target Lize. SetupMasterTransmit JazRepPtr_Cnt_T_str.DNAC         1           target Lize. SetupMasterTransmit JazRepPtr_Cnt_T_str.DNA         1		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         12           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         10           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         10           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         10           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         10           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         11           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRR         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DRC         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DD12         10           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DD12         10           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDAC         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDAC         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDA         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDA         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDA         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDA         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDA         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDA         1           target_12c_SetupMasterTransmit_	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846
larget   2c. SetupMaster Transmit   2cRegPtr_Cnt_T_str.SAR	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974
larget   2c. SetupMaster Transmit   2cRegPtr_Cnt_T_str.SAR	target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR         10           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR         7846           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR         7846           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR         55           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC         10           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC         10           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11         8974           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID12         10           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID1         10           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID1         2           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID1         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID1         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID1         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID1         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID2         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID2         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DID2         1           target_I2c_Setu		
Larget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR         7846           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC         10           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PDC         10           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PDD1         8974           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN         2           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DUT         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DUT         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DUT         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIT         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIT         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIT         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIT         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIT         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIT         1           target_I2c_SetupMasterTransmit_I		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ENDR         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ENDR         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PDC         10           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PDD11         8974           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR         2           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR         2           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR         2           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CDR         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOR         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PDL         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PDL         1           target_I2c_REGI_temp_DAR         10           target_I2c_REGI_temp_DAR         10           target_I2c_REGI_temp_DAR         10           target_I2c_REGI_temp_DAR         10           target_I2c_REGI_temp_DAR	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.ENDR         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PDC1         10           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PD11         8974           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PD12         10           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNAC         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNAC         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIR         2           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIT         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.ClR         2           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIT         1           target_12c_Set_1 tarnp_NIR	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ENDR         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PDC         10           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11         8974           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12         10           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMC         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR         2           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR         2           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL         1           target_I2c_Set_I tamp_IMR         10           target_I2c_Set_I tamp_IMR         10           target_I2c_REG_I tamp_IDR         12           target_I2c_REG_I tamp_IDR         12           target_I2c_REG_I tamp_IDNR	target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC         10           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11         8974           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR         2           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD         1           target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD         1           target_I2c_REG1_temp_OAR         10           target_I2c_REG1_temp_DAR         10           target_I2c_REG1_temp_DAR         12           target_I2c_REG1_temp_DAR         12           target_I2c_REG1_temp_DAR         10           target_I2c_REG1_temp_DAR         10 <tr< td=""><td></td><td></td></tr<>		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID11         8974           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PID12         10           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNAC         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DN         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DNR         2           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DOUT         1           target_12c_REG1_temp_CLKH         8974           target_12c_REG1_temp_DUT         1		
target_l2c_SetupMasterTransmit_l2cRegPtr_CntT_str.PID12         10           target_l2c_SetupMasterTransmit_l2cRegPtr_CntT_str.DNAC         1           target_l2c_SetupMasterTransmit_l2cRegPtr_CntT_str.DNN         1           target_l2c_SetupMasterTransmit_l2cRegPtr_CntT_str.DIR         2           target_l2c_SetupMasterTransmit_l2cRegPtr_CntT_str.DIN         1           target_l2c_SetupMasterTransmit_l2cRegPtr_CntT_str.DOUT         1           target_l2c_SetupMasterTransmit_l2cRegPtr_CntT_str.DQT         1           target_l2c_SetupMasterTransmit_l2cRegPtr_CntT_str.CLR         2           target_l2c_SetupMasterTransmit_l2cRegPtr_CntT_str.DQT         1           target_l2c_Set_lemp_DAR         10           target_l2c_REG1_temp_DAR         10           target_l2c_REG1_temp_DLR         12           target_l2c_REG1_temp_DAR         10           target_l2c_REG1_temp_DAR         1		
target_!2e_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.FUN         1           target_!2e_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.FUN         1           target_!2e_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN         2           target_!2e_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN         1           target_!2e_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DUT         1           target_!2e_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.SET         1           target_!2e_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.CLR         2           target_!2e_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DDR         1           target_!2e_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DDR         1           target_!2e_SetupMasterTransmit_!2eRegPtr_Cnt_T_str.PD         1           target_!2e_SetupMasterTransmit_!2eRegPtr_Cnt_T_str.PSL         1           target_!2e_SetupMasterTransmit_!2eRegPtr_Cnt_T_str.PSL         1           target_!2e_SetupMasterTransmit_!2eRegPtr_Cnt_T_str.PSL         1           target_!2e_SetupMasterTransmit_!2eRegPtr_Cnt_T_str.PSL         1           target_!2e_SetupMasterTransmit_!2eRegPtr_Cnt_T_str.PSL         1           target_!2e_SetupMasterTransmit_!2eRegPtr_Cnt_T_str.PSL         1           target_!2e_RegG1_temp.STR         10           target_!2e_RegG1_temp.DRR         1           target_!2e_RegG1_temp.PSC         10           target_!2e_RegG1_te	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974
target_!2e_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN         1           target_!2e_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN         2           target_!2e_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DUT         1           target_!2e_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL         1           target_!2e_REG1_temp_OAR         10           target_!2e_REG1_temp_DAR         10           target_!2e_REG1_temp_CLKL         7846           target_!2e_REG1_temp_CLKH         8974           target_!2e_REG1_temp_DRR         12           target_!2e_REG1_temp_DRR         12           target_!2e_REG1_temp_DRR         10           target_!2e_REG1_temp_NAR         10           target_!2e_REG1_temp_NDR         55           target_!2e_REG1_temp_NDR         1           target_!2e_REG1_temp_PDDR         1           target_!2e_REG1_temp_PDID12	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.FUN         1           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIR         2           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DIN         1           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DOUT         1           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DOUT         1           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DOR         1           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.DOR         1           target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PD         1           target_!2c_RetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL         1           target_!2c_REG1_temp_OAR         10           target_!2c_REG1_temp_DAR         10           target_!2c_REG1_temp_CLKL         7846           target_!2c_REG1_temp_CLKH         8974           target_!2c_REG1_temp_DRR         12           target_!2c_REG1_temp_DRR         12           target_!2c_REG1_temp_DRR         10           target_!2c_REG1_temp_DRR         10           target_!2c_REG1_temp_DRR         10           target_!2c_REG1_temp_DRR         10           target_!2c_REG1_temp_DRDR         1           target_!2c_REG1_temp_PDDR         1           target_!2c_REG1_temp_PDDR         1	target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	1
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIR         2           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DUT         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR         2           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR         2           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DD         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL         1           target_l2c_REG1_temp.OAR         10           target_l2c_REG1_temp.DAR         10           target_l2c_REG1_temp.CLKL         7646           target_l2c_REG1_temp.DAR         10           target_l2c_REG1_temp.DAR         10           target_l2c_REG1_temp.DAR         10           target_l2c_REG1_temp.DNR         1           target_l2c_REG1_temp.PDNR         1           target_l2c_REG1_temp.PDNAC         1		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DIN         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DOUT         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLR         2           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CDR         2           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DDR         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DD         1           target_12c_REG1_temp.DAR         10           target_12c_REG1_temp.SAR         12           target_12c_REG1_temp.DAR         10           target_12c_REG1_temp.DAR         10           target_12c_REG1_temp.DMD         7646           target_12c_REG1_temp.PDND         1           target_12c_REG1_temp.PDND         1           target_12c_REG1_temp.PDNA         10           target_12c_REG1_temp.PDNA         1 <td></td> <td></td>		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DOUT         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.SET         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.CLR         2           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.ODR         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PD         1           target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSL         1           target_12c_REG1_temp_OAR         10           target_12cREG1_temp_IMR         10           target_12cREG1_temp_STR         1223           target_12cREG1_temp_CLKL         7846           target_12cREG1_temp_CLKH         8974           target_12cREG1_temp_CNT         98           target_12cREG1_temp_DRR         12           target_12cREG1_temp_DRR         12           target_12cREG1_temp_DAR         10           target_12cREG1_temp_DNR         10           target_12cREG1_temp_IVR         55           target_12cREG1_temp_DRDR         1           target_12cREG1_temp_PBDR         1           target_12cREG1_temp_PDD1         10           target_12cREG1_temp_PDD12         10           target_12cREG1_temp_PDMAC         1           target_12cREG1_temp_FUNA         1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR         2           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL         1           target_l2cREG1_temp.OAR         10           target_l2cREG1_temp.BMR         10           target_l2cREG1_temp.STR         1223           target_l2cREG1_temp.CLKL         7846           target_l2cREG1_temp.CLKH         8974           target_l2cREG1_temp.DNR         12           target_l2cREG1_temp.DNR         12           target_l2cREG1_temp.DNR         10           target_l2cREG1_temp.DNR         10           target_l2cREG1_temp.MDR         7846           target_l2cREG1_temp.BMDR         1           target_l2cREG1_temp.PSC         10           target_l2cREG1_temp.PSC         10           target_l2cREG1_temp.PID11         8974           target_l2cREG1_temp.PID12         10           target_l2cREG1_temp.FUN         1           target_l2cREG1_temp.FUN         1	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SET         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR         2           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.ODR         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL         1           target_l2cREG1_temp.OAR         10           target_l2cREG1_temp.BMR         10           target_l2cREG1_temp.STR         1223           target_l2cREG1_temp.CLKL         7846           target_l2cREG1_temp.CLKH         8974           target_l2cREG1_temp.DNR         12           target_l2cREG1_temp.DNR         12           target_l2cREG1_temp.DNR         10           target_l2cREG1_temp.DNR         10           target_l2cREG1_temp.MDR         7846           target_l2cREG1_temp.BMDR         1           target_l2cREG1_temp.PSC         10           target_l2cREG1_temp.PSC         10           target_l2cREG1_temp.PID11         8974           target_l2cREG1_temp.PID12         10           target_l2cREG1_temp.FUN         1           target_l2cREG1_temp.FUN         1	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T str.CDR         2           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T str.ODR         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD         1           target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL         1           target_l2cREG1_temp.OAR         10           target_l2cREG1_temp.BTR         10           target_l2cREG1_temp.STR         1223           target_l2cREG1_temp.CLKL         7846           target_l2cREG1_temp.CKT         8974           target_l2cREG1_temp.DRR         12           target_l2cREG1_temp.DRR         12           target_l2cREG1_temp.DRR         10           target_l2cREG1_temp.DRR         10           target_l2cREG1_temp.MDR         10           target_l2cREG1_temp.MDR         7846           target_l2cREG1_temp.EMDR         1           target_l2cREG1_temp.EMDR         1           target_l2cREG1_temp.PBDG         10           target_l2cREG1_temp.PID11         8974           target_l2cREG1_temp.PID12         10           target_l2cREG1_temp.PID12         10           target_l2cREG1_temp.PIDNAC         1           target_l2cREG1_temp.EVDN         1		
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DD       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PD       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSL       1         target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.PSL       1         target_12c_REG1_temp.JRR       10         target_12c_REG1_temp.JMR       10         target_12c_REG1_temp.STR       1223         target_12c_REG1_temp.CLKL       7846         target_12c_REG1_temp.CLKH       8974         target_12c_REG1_temp.DNR       12         target_12c_REG1_temp.SAR       10         target_12c_REG1_temp.DXR       10         target_12c_REG1_temp.DNR       7846         target_12c_REG1_temp.MDR       7846         target_12c_REG1_temp.BMDR       1         target_12c_REG1_temp.BMDR       1         target_12c_REG1_temp.PBDC       10         target_12c_REG1_temp.PID11       8974         target_12c_REG1_temp.PID42       10         target_12c_REG1_temp.DMAC       1         target_12c_REG1_temp.DMAC       1         target_12c_REG1_temp.FUN       1	· ·	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD       1         target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL       1         target_i2cREG1_temp.OAR       10         target_i2cREG1_temp.IMR       10         target_i2cREG1_temp.STR       1223         target_i2cREG1_temp.CLKL       7846         target_i2cREG1_temp.CNT       8974         target_i2cREG1_temp.CNT       98         target_i2cREG1_temp.DRR       12         target_i2cREG1_temp.DXR       10         target_i2cREG1_temp.DXR       10         target_i2cREG1_temp.MDR       7846         target_i2cREG1_temp.IVR       55         target_i2cREG1_temp.BMDR       1         target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1		
target_!2c_SetupMasterTransmit_!2cRegPtr_Cnt_T_str.PSL       1         target_!2cREG1_temp.OAR       10         target_!2cREG1_temp.IMR       10         target_!2cREG1_temp.STR       1223         target_!2cREG1_temp.CLKL       7846         target_!2cREG1_temp.CLKH       8974         target_!2cREG1_temp.DRR       12         target_!2cREG1_temp.DRR       12         target_!2cREG1_temp.DXR       10         target_!2cREG1_temp.DXR       10         target_!2cREG1_temp.MDR       7846         target_!2cREG1_temp.MDR       55         target_!2cREG1_temp.EMDR       1         target_!2cREG1_temp.PBC       10         target_!2cREG1_temp.PID11       8974         target_!2cREG1_temp.PID12       10         target_!2cREG1_temp.PID12       10         target_!2cREG1_temp.DMAC       1         target_!2cREG1_temp.DMAC       1         target_!2cREG1_temp.FUN       1		
target_i2cREG1_temp.OAR       10         target_i2cREG1_temp.IMR       10         target_i2cREG1_temp.STR       1223         target_i2cREG1_temp.CLKL       7846         target_i2cREG1_temp.CLKH       8974         target_i2cREG1_temp.CNT       98         target_i2cREG1_temp.DRR       12         target_i2cREG1_temp.SAR       10         target_i2cREG1_temp.DXR       10         target_i2cREG1_temp.MDR       7846         target_i2cREG1_temp.IVR       55         target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
target_i2cREG1_temp.OAR       10         target_i2cREG1_temp.IMR       10         target_i2cREG1_temp.STR       1223         target_i2cREG1_temp.CLKL       7846         target_i2cREG1_temp.CLKH       8974         target_i2cREG1_temp.CNT       98         target_i2cREG1_temp.DRR       12         target_i2cREG1_temp.SAR       10         target_i2cREG1_temp.DXR       10         target_i2cREG1_temp.MDR       7846         target_i2cREG1_temp.IVR       55         target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1
target_i2cREG1_temp.IMR       10         target_i2cREG1_temp.STR       1223         target_i2cREG1_temp.CLKL       7846         target_i2cREG1_temp.CNT       8974         target_i2cREG1_temp.DNR       12         target_i2cREG1_temp.DRR       12         target_i2cREG1_temp.SAR       10         target_i2cREG1_temp.DXR       10         target_i2cREG1_temp.MDR       7846         target_i2cREG1_temp.IVR       55         target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1		
target_i2cREG1_temp.CLKL       7846         target_i2cREG1_temp.CLKH       8974         target_i2cREG1_temp.CNT       98         target_i2cREG1_temp.DRR       12         target_i2cREG1_temp.SAR       10         target_i2cREG1_temp.DXR       10         target_i2cREG1_temp.MDR       7846         target_i2cREG1_temp.IVR       55         target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1		
target_i2cREG1_temp.CLKL       7846         target_i2cREG1_temp.CLKH       8974         target_i2cREG1_temp.CNT       98         target_i2cREG1_temp.DRR       12         target_i2cREG1_temp.SAR       10         target_i2cREG1_temp.DXR       10         target_i2cREG1_temp.MDR       7846         target_i2cREG1_temp.IVR       55         target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1		
target_i2cREG1_temp.CLKH       8974         target_i2cREG1_temp.CNT       98         target_i2cREG1_temp.DRR       12         target_i2cREG1_temp.SAR       10         target_i2cREG1_temp.DXR       10         target_i2cREG1_temp.MDR       7846         target_i2cREG1_temp.IVR       55         target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1	target_i2cREG1_temp.STR	1223
target_i2cREG1_temp.CLKH       8974         target_i2cREG1_temp.CNT       98         target_i2cREG1_temp.DRR       12         target_i2cREG1_temp.SAR       10         target_i2cREG1_temp.DXR       10         target_i2cREG1_temp.MDR       7846         target_i2cREG1_temp.IVR       55         target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1	target_i2cREG1_temp.CLKL	7846
target_i2cREG1_temp.CNT       98         target_i2cREG1_temp.DRR       12         target_i2cREG1_temp.SAR       10         target_i2cREG1_temp.DXR       10         target_i2cREG1_temp.MDR       7846         target_i2cREG1_temp.IVR       55         target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1		8974
target_i2cREG1_temp.DRR       12         target_i2cREG1_temp.SAR       10         target_i2cREG1_temp.DXR       10         target_i2cREG1_temp.MDR       7846         target_i2cREG1_temp.IVR       55         target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1	·	
target_i2cREG1_temp.SAR       10         target_i2cREG1_temp.DXR       10         target_i2cREG1_temp.MDR       7846         target_i2cREG1_temp.IVR       55         target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1		
target_i2cREG1_temp.DXR       10         target_i2cREG1_temp.MDR       7846         target_i2cREG1_temp.IVR       55         target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1		
target_i2cREG1_temp.MDR       7846         target_i2cREG1_temp.IVR       55         target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1	target_i2cREG1_temp.SAR	10
target_i2cREG1_temp.MDR       7846         target_i2cREG1_temp.IVR       55         target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1	target_i2cREG1_temp.DXR	10
target_i2cREG1_temp.IVR       55         target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1		7846
target_i2cREG1_temp.EMDR       1         target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1		
target_i2cREG1_temp.PSC       10         target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1		
target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1	target_i2cREG1_temp.EMDR	
target_i2cREG1_temp.PID11       8974         target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1	target_i2cREG1_temp.PSC	10
target_i2cREG1_temp.PID12       10         target_i2cREG1_temp.DMAC       1         target_i2cREG1_temp.FUN       1		8974
target_i2cREG1_temp.DMAC 1 target_i2cREG1_temp.FUN 1		
target_i2cREG1_temp.FUN 1		
L L'O DEGLI L DID	target_i2cREG1_temp.FUN	1
target_izckeg1_temp.DIR 2	target_i2cREG1_temp.DIR	2

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3			
Name	Input Value		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	1		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8	8	~
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	~
DigColPsInt_Buffer_Cnt_M_u08[1]	200	200	<b>*</b>
DigColPoint_Buffer_Cnt_M_u08[2]	250 1	250	7
DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	-
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	-
DigColPsInt_ColSnsrData_Cnt_M_u16	7846	7846	~
DigColPsInt_CurrentSlave_Cnt_M_u08	10	10	-
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_SETREG	INIT_SENSOR2_READERROR_SETREG	<b>~</b>
DigColPsInt_I2CHwCustData_Uls_M_u16	40	40	~
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	41	41	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	~
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	~
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	98	98	~
DigColPsInt_TransactionCnt_Cnt_M_u08	12	12	~
I2c_Send(Length_Cnt_T_u32)	1	1	<b>V</b>
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	<b>V</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223	1223	-
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	7846	7846	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98	98	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12	12	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7846	7846	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	55	55	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	8974	8974	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	10	10	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1 2	1 2	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR	1	1	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	
target_12c_GenStopCond_12cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223	1223	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98	98	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10	10	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	10	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	7846	7846	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	55 1	55	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	10	1 10	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974	8974	<b>V</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.PID12	10	10	
target_12c_Send_12cRegPtr_Cnt_T_str.DMAC	1	1	V
target_12c_Send_12cRegPtr_Cnt_T_str.FUN	1	1	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10	10	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10	10	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223	1223	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98	98	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	12	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10	10	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10	10	

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Name	Actual Value	Expected Value	Result
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223	1223	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98	98	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10	10	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846	7846	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55	55	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974	8974	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10	10	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	~

T				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c_Send	1	I2c_Send	1	-

Test Step 3.44 (Repeat Count = 1)	<u> </u>
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2
DigColPsInt_Buffer_Cnt_M_u08[0]	255
DigColPsInt_Buffer_Cnt_M_u08[1]	255
DigColPsInt_Buffer_Cnt_M_u08[2]	255
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	7
DigColPsInt_CurrentSlave_Cnt_M_u08	35
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	31
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	32
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	88
DigColPsInt_TransactionCnt_Cnt_M_u08	110
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str

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Input Value  0 32 30 36 38 34
32 30 36 38 34
30 36 38 34
36 38 34
38 34
34
10
IO
12
14
target_i2cREG1_temp
59
5
65
89
67
7
577
88
23
65
89
7
44
2
89
577
89
2
0
0
1
2
2
0
1
2
0
65
89
67
7
577
88
23
65
89
7
44
2
89
577
89
2
0
0
1
2
2
0
1
2
0
65
89
67
7
577
88
88 23
23
23 65

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Name	Input Value
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2
arget I2c SetRecv I2cRegPtr Cnt T str.PSC	89
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89
arget I2c SetRecv I2cRegPtr Cnt T str.DMAC	2
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
	0
rarget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
arget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR	65
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	88
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44
arget I2c SetStatus I2cRegPtr Cnt T str.EMDR	2
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89
	577
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0
arget I2c SetupMasterReceive I2cRegPtr Cnt T str.OAR	65
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7
arget I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKH	577
arget I2c SetupMasterReceive I2cRegPtr Cnt T str.CNT	88
	23
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
arget I2c SetupMasterReceive I2cRegPtr Cnt T str.SET	2
rget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLR	0
arget_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.ODR	1
	2
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	
arget_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67
rget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	7
	577
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	
	88
arget_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	
arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH  arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT  arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR  arget_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	88



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Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2 89		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	577		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	2		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	0		
target_i2cREG1_temp.OAR	65		
target_i2cREG1_temp.IMR	89		
target_i2cREG1_temp.STR	67 7		
target_i2cREG1_temp.CLKL	577		
target_i2cREG1_temp.CLKH target_i2cREG1_temp.CNT	88		
target_i2cREG1_temp.DRR	23		
target i2cREG1 temp.SAR	65		
target_i2cREG1_temp.DXR	89		
target_i2cREG1_temp.MDR	7		
target_i2cREG1_temp.IVR	44		
target_i2cREG1_temp.EMDR	2		
target_i2cREG1_temp.PSC	89		
target_i2cREG1_temp.PID11	577		
target_i2cREG1_temp.PID12	89		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1 2		
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt AttempOccurForCustDatRead Cnt M u08	2	2	Nesuit
DigColPsInt_Buffer_Cnt_M_u08[0]	38	38	
DigColPsInt_Buffer_Cnt_M_u08[1]	255	255	-
DigColPsInt_Buffer_Cnt_M_u08[2]	255	255	•
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	-
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	-
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	-
DigColPsInt_ColSnsrData_Cnt_M_u16	7	7	•
DigColPsInt_CurrentSlave_Cnt_M_u08	35	35	-
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_SETREG	INIT_SENSOR1_READEXTERR_SETREG	•
DigColPsInt_I2CHwCustData_Uls_M_u16	31	31	•
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	32	32	•
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	•
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	_
DigColPsInt_RecvdDataType_Cnt_M_u08	5	5	•
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	<b>V</b>
DigColPoInt_SpurSnsrData_Cnt_M_u16	88	88	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
DigColPsInt_TransactionCnt_Cnt_M_u08	110	110	~
I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65	65	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89	89	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67	67	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7	7	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	577	577	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88	88	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23	23	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65	65	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	89	89	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7	7	~

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44	44	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89 577	89 577	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11 target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89	89	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	65 89	65 89	
target_I2c_Send_I2cRegPtr_Cnt_T_str.NTR	67	67	
target I2c Send I2cRegPtr Cnt T str.CLKL	7	7	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65	65	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89	89	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67	67	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7	7	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	577 88	577 88	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	23	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	65	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89	89	
target I2c SetRecv I2cRegPtr Cnt T str.MDR	7	7	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44	44	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89	89	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577	577	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89	89	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2 2	2 2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65	65	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89	89	•
	67	67	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR		7	
	7	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577	577	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	577 88	577 88	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLKH	577	577	

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7	7	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	2	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	577	577	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89	89	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>*</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	65	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23	23	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65	65	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89	89	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89	89	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577	577	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89	89	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	_
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	577	577	<b>✓</b>
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID12	89	89	
target_12c_SetupMasterTransmit_12cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	0	0	·
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	-
	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	U	U	



T			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c Send	1	I2c Send	1	<b>✓</b>

Fest Step 3.45 (Repeat Count = 1)	Input Volue
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	11
DigColPsInt_Buffer_Cnt_M_u08[0]	255
DigColPsInt_Buffer_Cnt_M_u08[1]	255
DigColPsInt_Buffer_Cnt_M_u08[2]	255
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	65535
DigColPsInt_CurrentSlave_Cnt_M_u08	127
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE
DigColPsInt_I2CHwCustData_Uls_M_u16	511
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	255
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
igColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	5
igColPsInt_SkipRegisterWrite_Cnt_M_Igc	1
igColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	65535
DigColPsInt_TransactionCnt_Cnt_M_u08	255
Flags_Cnt_T_b16	64
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
	0
 _DataRegisters_Cnt_u08[1]	32
	30
	36
C_DataRegisters_Cnt_u08[4]	38
	34
bataRegisters_Cnt_u08[6]	10
catalogsettetri	12
bataRegisters_Cnt_u08[8]	14
	target_i2cREG1_temp
c_ColSensorI2CAddress_Cnt_u08	127
SpurSensorI2CAddress Cnt u08	127
	1023
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	255
· ·	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	32767
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	65535
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	65535
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	65535
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	255
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	1023
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	255
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	65535
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	4095
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	255
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	65535
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	255
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
arget I2c GenStopCond I2cRegPtr Cnt T str.CLR	3

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DigColPSint_Interruptivotilication		
Name	Input Value	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	255	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	32767	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	65535	
arget I2c Send I2cRegPtr Cnt T str.CNT	65535	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	255	
arget I2c Send I2cRegPtr Cnt T str.SAR	1023	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	255	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	65535	
	4095	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	255	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	65535	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	255	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	1023	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	255	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	32767	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	65535	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	65535	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	65535	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	255	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	1023	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	255	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	65535	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	4095	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	255	
arget I2c SetRecv I2cRegPtr Cnt T str.PID11	65535	
· ·	255	
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12 arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	3	
arget I2c SetRecv I2cRegPtr Cnt T str.FUN	1	
·		
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	1023	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	255	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	32767	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	65535	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	65535	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	65535	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	255	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	1023	
irget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	255	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	65535	
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	4095	
	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	255	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC		
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	65535	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	255	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	

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Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	1023
target I2c SetupMasterReceive I2cRegPtr Cnt T str.IMR	255
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	32767
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	65535
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	65535
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	65535
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	255
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	1023
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	255
target I2c SetupMasterReceive I2cRegPtr Cnt T str.MDR	65535
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IVR	4095
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	255
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	65535
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	255
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	1023
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	255
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	32767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	1023
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	4095
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	1023
target_i2cREG1_temp.IMR	255
target i2cREG1 temp.STR	32767
target i2cREG1 temp.CLKL	65535
target i2cREG1_temp.CLKH	65535
· ·	
target_i2cREG1_temp.CNT	65535
target_i2cREG1_temp.DRR	255
target_i2cREG1_temp.SAR	1023
target_i2cREG1_temp.DXR	255
target i2cREG1 temp.MDR	65535
target i2cREG1 temp.IVR	4095
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	255
target_i2cREG1_temp.PID11	65535
target_i2cREG1_temp.PID12	255
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target i2cREG1 temp.DIR	3
	1

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Name	Input Value		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target i2cREG1 temp.CLR	3		
target i2cREG1 temp.ODR	3		
target i2cREG1 temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
	11	11	Result
DigColPoint_AttempOccurForCustDatRead_Cnt_M_u08	255	255	
DigColPoint_Buffer_Cnt_M_u08[0]		255	
DigColPoint_Buffer_Cnt_M_u08[1]	255		
DigColPsInt_Buffer_Cnt_M_u08[2]	255	255	
DigColPsInt_BusBusySeqError_Cnt_M_Igc	1	1	
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	<b>*</b>
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	<b>Y</b>
DigColPsInt_ColSnsrData_Cnt_M_u16	65535	65535	<b>✓</b>
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE	READ_COMPLETE	<b>✓</b>
DigColPsInt_I2CHwCustData_Uls_M_u16	511	511	~
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	255	255	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1	1	~
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	<b>✓</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✓
DigColPsInt_RecvdDataType_Cnt_M_u08	5	5	<b>✓</b>
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	•
DigColPsInt_SpurSnsrData_Cnt_M_u16	65535	65535	<b>✓</b>
DigColPsInt_TransactionCnt_Cnt_M_u08	255	255	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	1023	1023	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	255	255	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	32767	32767	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	<b>v</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	65535	65535	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	255	255	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	1023	1023	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	255	255	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	65535	65535	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	4095	4095	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	255	255	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	65535	65535	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	255	255	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target I2c GenStopCond I2cRegPtr Cnt T str.DIR	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	3	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023	1023	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	255	255	·
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	32767	32767	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	65535	65535	
	255	255	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	1023	1023	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR			
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	255	255	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	65535	65535	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	4095	4095	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	255	255	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	65535	65535	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	255	255	· ·
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	<b>Y</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	<b>Y</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	

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The part of the	Nama	A stud Value	Even acts of Volum	Daguit
	Name	Actual Value	Expected Value	Result
Sept   Description   Control   Con				
Target Die, Senter Content of the Co				-
Togst Dipt. Spellings. Dipt. Spellings. Dipt.				
Target Etz Serfiero (2014/98/ph CH 1 than MS				_
September   Description   De				
angel 20, Serfece 2, Jeschegh C. T., and C.M.  angel 20, Serfece 2, Jeschegh C. T., and C.M.  angel 20, Serfece 2, Jeschegh C. T., and C.M.  angel 20, Serfece 2, Jeschegh C. T., and C.M.  angel 20, Serfece 2, Jeschegh C. T., and C.M.  angel 20, Serfece 2, Jeschegh C. T., and C.M.  angel 20, Serfece 2, Jeschegh C. T., and C.M.  angel 20, Serfece 2, Jeschegh C. T., and C.M.  angel 20, Serfece 2, Jeschegh C. T., and C.M.  angel 20, Serfece 2, Jeschegh C. T., and C.M.  angel 20, Serfece 2, Jeschegh C. T., and C.M.  angel 20, Serfece 2, Jeschegh C. T., and C.M.  angel 20, Serfece 2, Jeschegh C. T., and C.M.  angel 20, Serfece 2, Jeschegh C. T., and C.M.  angel 20, Serfece 2, Jeschegh C. T., and C.M.  angel 20, Serfece 2, Jeschegh C.T., and C.M.  angel 2				•
Barger   12. Serifice   12. Serifi				~
Image   126, Sentence   December   11   1   1   1   1   1   1   1   1		65535	65535	•
	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	65535	65535	~
	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	255	255	~
	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	1023	1023	•
Burger   12.5. SerRevo   12.5. Regiver   10.1. Test PAR	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	255	255	~
	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	65535	65535	~
	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	4095	4095	•
Image   125   Series   126   Regir   Put   1   1   1   1   1   1   1   1   1	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR			
Image   12.5 Serbies   12.5 Serbie	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC			
Image: 120 Selface; 120 Regift: CHT_SELFEN   1				
Seption   Discipling Cont_   Discipli				
Image:   Description   Celt   Table   Description   Desc				
Langer   12.5. Selfisco   2.6Regin   Cont   T. att DND			•	
Langer   12.5 Selfston   12.6 Selfston   12.				_
Integral   22. Self-Serio   26RegPP   Cont.   1 str CER				
Image:   22. SetRiescy   226Reg/Pt   Cnt.   T. str. CDR				
Image   125, Self-Recy   Diche pipts   Cont   T. str. PDD				
target_LZc_SetRecv_LZcRegPtr_Cnt_Tst_PD  3				
Image: 1.25. Self-Rocy   Lock Purple; Cott   T. Str. PAR   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023   1023				
target LZe, SelStatus, J2cRegPtr, Cnt, T, str. OAR         1023         1023         V           target LZe, SelStatus, J2cRegPtr, Cnt, T, str. MR         255         256         V           target LZe, SelStatus, J2cRegPtr, Cnt, T, str. CNR         65935         65535         V           target LZe, SelStatus, J2cRegPtr, Cnt, T, str. CNR         65935         65535         V           target LZe, SelStatus, J2cRegPtr, Cnt, T, str. CNT         65535         65535         C           target LZe, SelStatus, J2cRegPtr, Cnt, T, str. CNT         65535         65535         V           target LZe, SelStatus, J2cRegPtr, Cnt, T, str. CNT         255         255         V           target LZe, SelStatus, J2cRegPtr, Cnt, T, str. CNR         255         255         V           target LZe, SelStatus, J2cRegPtr, Cnt, T, str. CNR         4096         4093         4093           target LZe, SelStatus, J2cRegPtr, Cnt, T, str. PDIT         4096         4096         4096           target LZe, SelStatus, J2cRegPtr, Cnt, T, str. PDIT         65535         525         25           target LZe, SelStatus, J2cRegPtr, Cnt, T, str. PDIT         65535         525         25           target LZe, SelStatus, J2cRegPtr, Cnt, T, str. PDIT         65535         525         25           target LZe, SelStatus, J2cRegPtr, Cnt, T, str. PDIT				
singel_De_SelSatus_2  22-RegPtr_Cnt_T str.NRR   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255				
target   Ze_SetStatus   ZeRegPr   Cnit_T str.STR   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   32767   3				_
Integel   Zo   SelStatus   ZoRegPtr Cnt   T str CLK    65535   65535   V   target   Zo   SelStatus   ZoRegPtr Cnt   T str CLKH   65535   65535   V   target   Zo   SelStatus   ZoRegPtr Cnt   T str CLKH   65535   65535   V   target   Zo   SelStatus   ZoRegPtr Cnt   T str CNT   65535   65535   V   target   Zo   SelStatus   ZoRegPtr Cnt   T str CNT   65535   C   ZoS   Target   Zo   ZoS   ZoS   V   target   Zo   ZoS   ZoS   V   target   Zo   ZoS   ZoS   V   Target   Zo   ZoS   ZoS   ZoS   V   Target   Zo   ZoS   ZoS   ZoS   ZoS   V   Target   Zo   ZoS   ZoS   ZoS   ZoS   V   Target   Zo   ZoS   Z				
target 120_SetStatus_12cRegPt_Cnt_Tstr.CNT         65535         65535         ✓           target 126_SetStatus_12cRegPt_Cnt_Tstr.CNT         65535         65535         ✓           target 126_SetStatus_12cRegPt_Cnt_Tstr.DRR         255         255         ✓           target 126_SetStatus_12cRegPt_Cnt_Tstr.DMR         3         3         ✓           target 126_SetStatus_12cRegPt_Cnt_Tstr.DBR         3         3         ✓           target 126_SetStatus_12cRegPt_Cnt_Tstr.DD11         65535         65535         65535            target 126_SetStatus_12cRegPt_Cnt_Tstr.DD12         255         225         225          ✓           target 126_SetStatus_12cRegPt_Cnt_Tstr.DNC         3         3         3         ✓				
larget L2c, SelStatus   J2cRepPr Cnt T_str CNT   5555   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   2				
target_12e_SetStatus_12cRepPtr_Cnt_T_str.DRR         255         255         ✓           target_12e_SetStatus_12cRepPtr_Cnt_T_str.DRR         1023         1023         ✓           target_12e_SetStatus_12cRepPtr_Cnt_T_str.DRR         255         255         ✓           target_12e_SetStatus_12cRepPtr_Cnt_T_str.DMDR         65535         65535         ✓           target_12e_SetStatus_12cRepPtr_Cnt_T_str.DNDR         3         3         3           target_12e_SetStatus_12cRepPtr_Cnt_T_str.DNDR         3         3         3           target_12e_SetStatus_12cRepPtr_Cnt_T_str.DDT1         65535         255         255           target_12e_SetStatus_12cRepPtr_Cnt_T_str.DDT1         65535         65535         ✓           target_12e_SetStatus_12cRepPtr_Cnt_T_str.DDT2         25         255         255            target_12e_SetStatus_12cRepPtr_Cnt_T_str.DDT2         25         255         255         ✓           target_12e_SetStatus_12cRepPtr_Cnt_T_str.DDT2         3         3         3         ✓           target_12e_SetStatus_12cRepPtr_Cnt_T_str.DDT2         3         3         3         3           target_12e_SetStatus_12cRepPtr_Cnt_T_str.DDT2         3         3         3         3           target_12e_SetStatus_12cRepPtr_Cnt_T_str.DDT3         3				~
large   122. SelfStatus   22RepPtr_Cnt_T sir. DXR   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255   255			255	~
target_12c_SetStatus_12cRegPtr_Cnt_T_str.NDR		1023	1023	•
target_12c_SelStatus_12cRegPtr_Cnt_Tstr.IVR	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	255	255	~
target   Zo, SelSiatus   2cRegPtr_Cnt_T str.EMDR         3         3         V           target   Zo, SelSiatus   2cRegPtr_Cnt_T str.PSC         255         255         V           target   Zo, SelSiatus   2cRegPtr_Cnt_T str.PID11         65535         S         V           target   Zo, SelSiatus   2cRegPtr_Cnt_T str.DID12         255         255         V           target   Zo, SelSiatus   2cRegPtr_Cnt_T str.DIN         3         3         V           target   Zo, SelSiatus   2cRegPtr_Cnt_T str.DIN         1         1         1         V           target   Zo, SelSiatus   2cRegPtr_Cnt_T str.DIN         3         3         3         V           target   Zo, SelSiatus   2cRegPtr_Cnt_T str.DIN         3         3         3         V           target   Zo, SelSiatus   2cRegPtr_Cnt_T str.DOT         3         3         3         V           target   Zo, SelSiatus   2cRegPtr_Cnt_T str.CLR         3         3         3         V           target   Zo, SelSiatus   2cRegPtr_Cnt_T str.DOR         3         3         3         V           target   Zo, SelSiatus   2cRegPtr_Cnt_T str.PSL         3         3         3         V         target   Zo, Selsiatus   2cRegPtr_Cnt_T str.PSL         3         3         3         V         target   Zo, Selsiatus   2cRegPtr_Cnt_T str.PSL	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	65535	65535	~
target_[2c_SetStatus_!2cRegPtr_Cnt_T_str.PBC         255         255           target_[2c_SetStatus_!2cRegPt_Cnt_T_str.PD11         65535         65355           target_[2c_SetStatus_!2cRegPt_Cnt_T_str.DD12         255         255           target_[2c_SetStatus_!2cRegPt_Cnt_T_str.DMAC         3         3           target_[2c_SetStatus_!2cRegPt_Cnt_T_str.DNAC         3         3      <	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	4095	4095	~
target   2c. SetStatus   ZcRegPtr_Cnt_T.str.PID11         65535         65535         ✓           target   2c. SetStatus   ZcRegPtr_Cnt_T.str.DNAC         3         3         ✓           target   2c. SetStatus   ZcRegPtr_Cnt_T.str.DNAC         3         3         ✓           target   2c. SetStatus   ZcRegPtr_Cnt_T.str.DNAC         3         3         ✓           target   2c. SetStatus   ZcRegPtr_Cnt_T.str.DNA         1         1         1           target   2c. SetStatus   ZcRegPtr_Cnt_T.str.DNA         3         3         ✓           target   2c. SetStatus   ZcRegPtr_Cnt_T.str.DNA         3         3         ✓           target   2c. SetStatus   ZcRegPtr_Cnt_T.str.Str.CLR         3         3         3         ✓           target   2c. SetStatus   ZcRegPtr_Cnt_T.str.DCLR         3         3         3         ✓         target   2c. SetStatus   ZcRegPtr_Cnt_T.str.DCLR         3         3         3         ✓         target   2c. SetStatus   ZcRegPtr_Cnt_T.str.DACR         3         3         3         ✓         target   2c. SetStatus   ZcRegPtr_Cnt_T.str.DACR         3         3         3         ✓         target   2c. SetStatus   ZcRegPtr_Cnt_T.str.DACR         1023         1023         1023         1023         1023         1023         1023         1023         1023         1023         1023<	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_ 2c_SetSlatus_ 2cRegPtr_Cnt_T_str.PID12	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	255	255	~
target_ 2c_SetStatus_ 2cRegPtr_Cnt_T_str.PUN         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         1         2         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4 <td>target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11</td> <td>65535</td> <td></td> <td>~</td>	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	65535		~
target_l2c_SetStatus_l2cRegPr_Cnt_T_str.FUN         1         1         1         4           target_l2c_SetStatus_l2cRegPr_Cnt_T_str.DIR         3         3         3         3         3         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4			255	~
target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DIR         3         3			3	~
target_2c_SetStatus_2cRegPtr_CnLT_str.DIN         3         3           target_12c_SetStatus_12cRegPtr_CnLT_str.DOUT         3         3           target_12c_SetStatus_12cRegPtr_CnLT_str.SET         3         3           target_12c_SetStatus_12cRegPtr_CnLT_str.CIR         3         3           target_12c_SetStatus_12cRegPtr_CnLT_str.DDR         3         3           target_12c_SetStatus_12cRegPtr_CnLT_str.DDR         3         3           target_12c_SetStatus_12cRegPtr_CnLT_str.DDL         3         3           target_12c_SetUpMasterReceive_12cRegPtr_CnLT_str.DAR         1023         3           target_12c_SetupMasterReceive_12cRegPtr_CnLT_str.DAR         1023         1023           target_12c_SetupMasterReceive_12cRegPtr_CnLT_str.DAR         255         255           target_12c_SetupMasterReceive_12cRegPtr_CnLT_str.CLKL         65535         65535           target_12c_SetupMasterReceive_12cRegPtr_CnLT_str.CLKL         65535         65535           target_12c_SetupMasterReceive_12cRegPtr_CnLT_str.DAR         255         255           target_12c_SetupMasterReceive_12cRegPtr_CnLT_str.DAR         255         255           target_12c_SetupMasterReceive_12cRegPtr_CnLT_str.DAR         255         255           target_12c_SetupMasterReceive_12cRegPtr_CnLT_str.DAR         3         3           target_12c_S				
target_l2c_SetStatus_l2cRegPtr_Cnt_Tstr.DOUT         3         3           target_l2c_SetStatus_l2cRegPtr_Cnt_Tstr.SET         3         3           target_l2c_SetStatus_l2cRegPtr_Cnt_Tstr.CLR         3         3           target_l2c_SetStatus_l2cRegPtr_Cnt_Tstr.ODR         3         3           target_l2c_SetStatus_l2cRegPtr_Cnt_Tstr.PD         3         3           target_l2c_SetStatus_l2cRegPtr_Cnt_Tstr.PD         3         3           target_l2c_SetspMasterReceive_l2cRegPtr_Cnt_Tstr.OAR         1023         1023           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.IMR         255         255           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.STR         32767         32767           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.CLKL         65535         65535           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.CLKL         65535         65535           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.CNT         65635         65535           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.DRR         255         255           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.DRR         255         255           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.DXR         255         255           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_Tstr.DXR         3         3				~
target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.CLR         3         3            target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.CDR         3         3             target_!2c_SetStatus_!2cRegPtr_Cnt_T_str.DDR         3         3 </td <td></td> <td></td> <td></td> <td></td>				
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OLR         3         3           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR         3         3           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DD         3         3           target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DD         3         3           target_l2c_SetUpMasterReceive_l2cRegPtr_Cnt_T_str.OAR         1023         1023           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DAR         255         255           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CKL         65535         65535           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CKLH         65535         65535           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CKT         65535         65535           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DAR         255         255           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DAR         3         3           target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DAR         3				¥
target_12c_SetStatus_12cRegPtr_Cnt_T_str.DDR         3         3         4           target_12c_SetStatus_12cRegPtr_Cnt_T_str.DD         3         3         3         4           target_12c_SetStatus_12cRegPtr_Cnt_T_str.DAR         3         3         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4         4				
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD       3       3          target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL       3       3          target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR       1023       1023          target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR       255            target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR       32767				
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL       3       3       V         target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DAR       1023       1023       V         target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.IMR       255       255       255         target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR       32767       32767       32767         target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL       65535       65535       65535       V         target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CNT       65535       65535       65535       V         target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR       255       255       255       V         target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR       255       255       V         target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR       255       255       V         target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.MDR       65535       65535       V         target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.NDR       4095       4095       V         target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11       65535       65535       V         target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12       255       255       V         target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIAC       3 </td <td></td> <td></td> <td></td> <td></td>				
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.OAR       1023       1023         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.IMR       255       255         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.STR       32767       32767         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLKL       65535       65535         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLKH       65535       65535         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CKNT       65535       65535         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CNT       65535       65535         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DRR       255       255         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DXR       255       255         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DXR       255       255         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.MDR       65535       65535         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.BMDR       3       3         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PNC       255       255         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PID11       65535       65535         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.PID12       255       255         target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.DMAC       3       3 <td></td> <td></td> <td></td> <td></td>				
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR       255       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR       32767       32767         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL       65535       65535         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH       65535       65535         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT       65535       65535         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR       255       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.AAR       1023       1023         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR       255       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR       65535       65535         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR       65535       65535         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR       65535       65535         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PDC       255       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11       65535       65535         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC       3       3				
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR       32767         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL       65535         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH       65535         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT       65535         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR       65535         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR       65535         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR       4095         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11       65535         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR       3				
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL       65535       65535         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT       65535       65535         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT       65535       65535         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR       255       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR       255       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR       255       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR       65535       65535         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR       4095       4095         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC       255       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11       65535       65535         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12       255       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR       3       3				
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH       65535       65535         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT       65535       65535         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR       255       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR       1023       1023         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR       255       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR       65535       65535         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR       4095       4095         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC       255       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11       65535       65535         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12       255       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR       3       3				
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT       65535       65535         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR       255       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR       1023       1023         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR       255       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR       65535       65535         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR       4095       4095         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC       255       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11       65535       65535         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12       255       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIAC       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIAC       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN       1       1         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR       3       3          target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR       3       3				
target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DRR       255       255         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.SAR       1023       1023         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DXR       255       255         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.MDR       65535       65535         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.IVR       4095       4095         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.EMDR       3       3         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PSC       255       255         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID11       65535       65535         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.PID12       255       255         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DMAC       3       3         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DMAC       3       3         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.FUN       1       1         target_!2c_SetupMasterReceive_!2cRegPtr_Cnt_T_str.DIR       3       3				
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR       1023       1023         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR       255       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR       65535       65535         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR       4095       4095         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC       255       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11       65535       65535         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12       255       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR       3       3				~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR       255       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR       65535       65535         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR       4095       4095         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC       255       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11       65535       65535         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12       255       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR       3       3		1023	1023	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR       65535       4095         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR       4095       4095         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC       255       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11       65535       65535         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12       255       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR       3       3			255	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR       4095       4095         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC       255       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11       65535       65535         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12       255       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR       3       3				~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC       255       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11       65535       65535         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12       255       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR       3       3		4095	4095	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11       65535       65535         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12       255       255         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC       3       3         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN       1       1         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN       3       3         v       4       4         target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR       3       3		3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12 255 255   target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC 3 3 3   target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN 1 1 1 2   target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR 3 3 3	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	255	255	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC  target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN  target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR  3  v  target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR  3	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	65535	65535	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID12	255		~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIR 3	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC			~
				~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN 3 3				~
	target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN	3	3	~

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	1023	1023	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	255	255	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	32767	32767	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	65535	65535	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	255	255	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	1023	1023	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	255	255	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	65535	65535	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	4095	4095	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	255	255	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	65535	65535	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	255	255	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Test Step 3.46 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	7
DigColPsInt_Buffer_Cnt_M_u08[0]	1
DigColPsInt_Buffer_Cnt_M_u08[1]	5
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_BusBusySeqError_Cnt_M_Igc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	847
DigColPsInt_CurrentSlave_Cnt_M_u08	15
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_DUMMY_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	19
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	20
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	487
DigColPsInt_TransactionCnt_Cnt_M_u08	70
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36

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Digoon ont_interruptivotineation		
Name	Input Value	
T_DataRegisters_Cnt_u08[4]	38	
T DataRegisters Cnt u08[5]	34	
T_DataRegisters_Cnt_u08[6]	10	
T_DataRegisters_Cnt_u08[7]	12	
T_DataRegisters_Cnt_u08[8]	14	
i2cREG1_temp	target_i2cREG1_temp	
	39	
k_ColSensorl2CAddress_Cnt_u08	0	
k_SpurSensorI2CAddress_Cnt_u08		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	34	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	24	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	455	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	847	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	987	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	487	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	34	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	34	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	24	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	847	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	56	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	24	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	987	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	24	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	
target I2c GenStopCond I2cRegPtr Cnt T str.DIR	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	
	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR		
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PD	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24	
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	
target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	2	
	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLR	3	
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR		
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	2	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	34	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	24	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	455	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	847	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	987	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	487	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	34	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	34	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	24	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	847	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	56	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	24	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	987	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	24	
0		

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Name	Input Value
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2
target I2c SetRecv I2cRegPtr Cnt T str.CLR	3
·	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	24
target I2c SetStatus I2cRegPtr Cnt T str.STR	455
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	847
	987
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	56
	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	24
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	34
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SAR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	24
target I2c SetupMasterReceive I2cRegPtr Cnt T str.MDR	847
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIN	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSL	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34
	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24



Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	3		
	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2		
target_i2cREG1_temp.OAR	34		
target_i2cREG1_temp.IMR	24		
target_i2cREG1_temp.STR	455		
target_i2cREG1_temp.CLKL	847		
target_i2cREG1_temp.CLKH	987		
target_i2cREG1_temp.CNT	487		
target_i2cREG1_temp.DRR	34		
target i2cREG1 temp.SAR	34		
target i2cREG1 temp.DXR	24		
target_i2cREG1_temp.MDR	847		
target i2cREG1 temp.IVR	56		
target i2cREG1 temp.EMDR	2		
target i2cREG1_temp.PSC	24		
	987		
target_i2cREG1_temp.PID11	11		
target_i2cREG1_temp.PID12	24		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	3		
target_i2cREG1_temp.DIN	3		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.CLR	3		
target_i2cREG1_temp.ODR	3		
target i2cREG1 temp.PD	2		
target_i2cREG1_temp.PSL	2		
target_i2cREG1_temp.PSL  Name	2 Actual Value	Expected Value	Result
		Expected Value	Result
Name	Actual Value	•	
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	Actual Value	7	~
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	Actual Value 7 10	7 10	<b>~</b>
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2]	Actual Value 7 10 3	7 10 3	* *
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc	Actual Value 7 10 3 7 0	7 10 3 7 0	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc	Actual Value 7 10 3 7 0	7 10 3 7 0 0	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc	Actual Value 7 10 3 7 0 0	7 10 3 7 0 0	· · · · · · · · · · · · · · · · · · ·
Name DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_igc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16	Actual Value 7 10 3 7 0 0 847	7 10 3 7 0 0 0 0 847	· · · · · · · · · · · · · · · · · · ·
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08	Actual Value 7 10 3 7 0 0 0 847	7 10 3 7 0 0 0 847	· · · · · · · · · · · · · · · · · · ·
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum	Actual Value 7 10 3 7 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN	7 10 3 7 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN	· · · · · · · · · · · · · · · · · · ·
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16	Actual Value 7 10 3 7 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19	7 10 3 7 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19	· · · · · · · · · · · · · · · · · · ·
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_igc DigColPsInt_CmdFailOccurred_Cnt_M_igc DigColPsInt_ColCustDatFound_Cnt_M_igc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	Actual Value 7 10 3 7 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20	7 10 3 7 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20	· · · · · · · · · · · · · · · · · · ·
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc	Actual Value 7 10 3 7 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20 0	7 10 3 7 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20 0	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc	Actual Value 7 10 3 7 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20 0 0	7 10 3 7 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20 0 0	· · · · · · · · · · · · · · · · · · ·
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc	Actual Value 7 10 3 7 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20 0 0 0	7 10 3 7 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20 0 0 0	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_12CHwCustData_UIs_M_u16  DigColPsInt_12CHwIncompleteCustData_UIs_M_u16  DigColPsInt_InitFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvdDataType_Cnt_M_u08	Actual Value 7 10 3 7 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20 0 0 1	7 10 3 7 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20 0 0 0 1	
Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08  DigColPsInt_Buffer_Cnt_M_u08[0]  DigColPsInt_Buffer_Cnt_M_u08[1]  DigColPsInt_Buffer_Cnt_M_u08[2]  DigColPsInt_BusBusySeqError_Cnt_M_lgc  DigColPsInt_CmdFailOccurred_Cnt_M_lgc  DigColPsInt_ColCustDatFound_Cnt_M_lgc  DigColPsInt_ColSnsrData_Cnt_M_u16  DigColPsInt_CurrentSlave_Cnt_M_u08  DigColPsInt_CurrentStepNo_Cnt_M_enum  DigColPsInt_I2CHwCustData_UIs_M_u16  DigColPsInt_12CHwIncompleteCustData_UIs_M_u16  DigColPsInt_initFailedOnce_Cnt_M_lgc  DigColPsInt_NackOccured_Cnt_M_lgc  DigColPsInt_RecvOverrunError_Cnt_M_lgc  DigColPsInt_RecvdDataType_Cnt_M_u08  DigColPsInt_RecvdDataType_Cnt_M_u08  DigColPsInt_SpurCustDatFound_Cnt_M_lgc	Actual Value 7 10 3 7 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20 0 0 0 1	7 10 3 7 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20 0 0 1 0 0	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_12CHwIncompleteCustData_UIs_M_u16 DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvdDataType_Cnt_M_u08 DigColPsInt_RecvdDataType_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16	Actual Value 7 10 3 7 0 0 0 10 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20 0 0 1 0 487	7 10 3 7 0 0 0 0 NINIT_SENSOR2_EXTREADADDRREG_SEN 19 20 0 0 1 0 487	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_enum DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I13cHdOnce_Cnt_M_lgc DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_u08 DigColPsInt_RecvDataType_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurSnsrData_Cnt_M_u16 DigColPsInt_TransactionCnt_Cnt_M_u08	Actual Value 7 10 3 7 0 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20 0 0 0 1 0 487 70	7 10 3 7 0 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20 0 0 0 1 0 487 70	· · · · · · · · · · · · · · · · · · ·
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DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 DigColPsInt_IntFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_u08 DigColPsInt_SpurCustDatCnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	Actual Value 7 10 3 7 0 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20 0 0 1 0 0 1 0 3 3 3 3 3 4 24 455 847 987 487 34	7 10 3 7 0 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20 0 0 1 0 0 1 1 0 487 70 3 3 3 34 24 455 847 987 487 34	
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DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16 DigColPsInt_IntFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvDataType_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	Actual Value 7 10 3 7 0 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20 0 0 1 0 0 1 0 3 3 3 3 4 24 455 847 987 487 34 34 24 847	7 10 3 7 0 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20 0 0 1 0 487 70 3 3 3 34 24 455 847 987 487 34 34 24	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_latificatiedOnce_Cnt_M_lgc DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Lengtn_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	Actual Value 7 10 3 7 0 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20 0 0 1 1 0 487 70 3 3 3 34 24 455 847 987 487 34 34 34 24 847 56	7 10 3 7 0 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20 0 0 1 0 487 70 3 3 3 34 24 455 847 987 487 34 34 24 847 56	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentStepNo_Cnt_M_enum DigColPsInt_I2CHwCustData_UIs_M_u16 DigColPsInt_I13tHoccurred_Cnt_M_lgc DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_u08 DigColPsInt_RecvOverrunError_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Length_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DAR	Actual Value 7 10 3 7 0 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20 0 0 0 1 0 487 70 3 3 3 34 24 455 847 987 487 34 34 24 847 56	7 10 3 7 0 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20 0 0 1 0 487 70 3 3 3 34 24 455 847 987 487 34 34 24 847 56	
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColCustDatFound_Cnt_M_lgc DigColPsInt_ColSnsrData_Cnt_M_u16 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_CurrentSlave_Cnt_M_u08 DigColPsInt_I2CHwCustData_Uls_M_u16 DigColPsInt_latificatiedOnce_Cnt_M_lgc DigColPsInt_InitFailedOnce_Cnt_M_lgc DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_u08 DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_SpurCustDatFound_Cnt_M_lgc DigColPsInt_TransactionCnt_Cnt_M_u08 I2c_Send(Lengtn_Cnt_T_u32) I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	Actual Value 7 10 3 7 0 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20 0 0 1 1 0 487 70 3 3 3 34 24 455 847 987 487 34 34 34 24 847 56	7 10 3 7 0 0 0 0 847 0 INIT_SENSOR2_EXTREADADDRREG_SEN 19 20 0 0 1 0 487 70 3 3 3 34 24 455 847 987 487 34 34 24 847 56	

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	24	24	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	0 3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34	34	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.IMR target_l2c_Send_l2cRegPtr_Cnt_T_str.STR	24 455	24 455	
target_12c_Send_12cRegPtr_Cnt_T_str.CLKL	847	847	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987	987	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487	487	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34	34	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34	34	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24	24	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847	847	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56	56	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.EMDR	2	2 24	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC target_I2c Send_I2cRegPtr_Cnt_T str.PID11	24 987	987	- V
target I2c Send I2cRegPtr Cnt T str.PID12	24	24	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target I2c Send I2cRegPtr Cnt T str.FUN	0	0	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	<b>~</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.PD	2	2 2	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	2 34	34	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	24	24	
target I2c SetRecv I2cRegPtr Cnt T str.STR	455	455	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	847	847	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	987	987	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	487	487	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	34	34	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	34	34	<b>~</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	24	24	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	847 56	847 56	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	2	2	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.PSC	24	24	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	987	987	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	24	24	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	2	2	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.PSL	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	34	34	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	24	24	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	455	455	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	847	847	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	987	987	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	487	487	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	34	34	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR	34	34	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR	24	24	<b>→</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR	847 56	847 56	
iaigot_izo_ocioiaiao_izoNGyFil_OHt_1_5tt.fVR	50	J0	

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	24	24	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	987	987	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	24	24	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2	34	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	24	24	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	455	455	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	847	847	
target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLKH	987	987	~
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CNT	487	487	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	34	34	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	34	34	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	24	24	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	847	847	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	56	56	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	24	24	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	987	987	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	24	24	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34	34	~
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.IMR	24	24	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.STR	455	455	- 4
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847	987	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	987 487	487	-
	34	34	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34	34	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24	24	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.MDR	847	847	~
target I2c SetupMasterTransmit I2cReqPtr Cnt T str.IVR	56	56	_
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24	24	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987	987	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24	24	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	~

T				V
Actual Function	Count	Expected Function	Count	Result
SetupWriteData	1	SetupWriteData	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	~
I2c Send	1	I2c Send	1	_



Test Step 3.47 (Repeat Count = 1)	Input Value
Name DigColPelat AttempOccurForCustDatPead Cat M u08	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	10
DigColPsInt_Buffer_Cnt_M_u08[0]	20
DigColPsInt_Buffer_Cnt_M_u08[1]	30
DigColPsInt_Buffer_Cnt_M_u08[2] DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_DusbusySeqEnot_Cnt_M_igc	1
DigColPsInt ColCustDatFound Cnt M Igc	1
DigColPsInt_ColCustDatFound_Cnt_M_igc	554
DigColPsInt_ColoristData_Crit_W_u10	40
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR2 READERROR READ
DigColPsInt_I2CHwCustData_Uls_M_u16	34
DigColPsInt I2CHwlncompleteCustData Uls M u16	35
	1
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_Igc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	123
DigColPsInt_TransactionCnt_Cnt_M_u08	120
Flags_Cnt_T_b16	32
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Γ_DataRegisters_Cnt_u08[0]	0
Γ_DataRegisters_Cnt_u08[1]	32
Γ_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
2cREG1_temp	target_i2cREG1_temp
<_ColSensorl2CAddress_Cnt_u08	64
<_SpurSensorI2CAddress_Cnt_u08	10
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	54
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
rarget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554
arget I2c GenStopCond I2cRegPtr Cnt T str.IVR	788
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
arget I2c GenStopCond I2cRegPtr Cnt T str.PSC	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
arget I2c GenStopCond I2cRegPtr Cnt T str.DMAC	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3
arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR arget_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR	2
	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKL	554
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123

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DigColPsini_interruptivotilication	
Name	Input Value
arget I2c Send I2cRegPtr Cnt T str.DRR	45
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344
arget I2c Send I2cRegPtr Cnt T str.PID12	66
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554
rget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	123
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
arget_12c_SetRecv_12cRegPtr_Cnt_T_str.PID11	344
	66
arget_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	3
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554
irget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	123
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45
urget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
rget I2c SetStatus I2cRegPtr Cnt T str.MDR	554
rget_12c_SetStatus_12cRegPtr_Cnt_T_str.IVR	788
irget I2c SetStatus I2cRegPti_Cnt_1_str.tvk	3
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
irget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
irget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
rget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
	3
rrget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1 2
rget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR  rget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.ODR  rget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PD  rget_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PSL  rget_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.OAR	1 2 54
arget_ 2c_SetStatus_ 2cRegPtr_Cnt_T_str.CLR arget_ 2c_SetStatus_ 2cRegPtr_Cnt_T_str.ODR arget_ 2c_SetStatus_ 2cRegPtr_Cnt_T_str.PD arget_ 2c_SetStatus_ 2cRegPtr_Cnt_T_str.PSL arget_ 2c_SetStatus_ 2cRegPtr_Cnt_T_str.PSL arget_ 2c_SetupMasterReceive_ 2cRegPtr_Cnt_T_str.OAR arget_ 2c_SetupMasterReceive_ 2cRegPtr_Cnt_T_str.IMR arget_ 2c_SetupMasterReceive_ 2cRegPtr_Cnt_T_str.STR	1 2

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Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DIR	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DOUT	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.ODR	2		
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PD	1		
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PSL	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLR	3		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.ODR	2		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	2		
target_i2cREG1_temp.OAR			
	54		
target_i2cREG1_temp.IMR	66		
target_i2cREG1_temp.STR	8		
target_i2cREG1_temp.CLKL	554		
target_i2cREG1_temp.CLKH	344		
target_i2cREG1_temp.CNT	123		
target_i2cREG1_temp.DRR	45		
target_i2cREG1_temp.SAR	54		
target_i2cREG1_temp.DXR	66		
target_i2cREG1_temp.MDR	554		
target_i2cREG1_temp.IVR	788		
target_i2cREG1_temp.EMDR	3		
target_i2cREG1_temp.PSC	66		
target_i2cREG1_temp.PID11	344		
target_i2cREG1_temp.PID12	66		
target_i2cREG1_temp.DMAC	3		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	3		
target_i2cREG1_temp.DIN	2		
target_i2cREG1_temp.DOUT	3		
target_i2cREG1_temp.SET	3		
target_i2cREG1_temp.CLR	3		
target_i2cREG1_temp.ODR	2		
target_i2cREG1_temp.PD	1		
target_i2cREG1_temp.PSL	2		
	4		
Name	Actual Value	Expected Value	Resu

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Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	38	38	~
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	<b>V</b>
DigColPoint_Buffer_Cnt_M_u08[2]	30	30	
DigColPsInt_BusBusySeqError_Cnt_M_Igc DigColPsInt CmdFailOccurred Cnt M Igc	1	1	-
DigColPsInt ColCustDatFound Cnt M Igc	1	1	,
DigColPsInt ColSnsrData Cnt M u16	554	554	~
DigColPsInt_CurrentSlave_Cnt_M_u08	40	40	-
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READEXTERR_SETREG	INIT_SENSOR2_READEXTERR_SETREG	•
DigColPsInt I2CHwCustData Uls M u16	34	34	~
DigColPsInt I2CHwIncompleteCustData UIs M u16	35	35	<b>~</b>
DigColPsInt_InitFailedOnce_Cnt_M_Igc	1	1	~
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	~
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	~
DigColPsInt_RecvdDataType_Cnt_M_u08	1	1	~
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	123	123	~
DigColPsInt_TransactionCnt_Cnt_M_u08	120	120	~
I2c_Send(Length_Cnt_T_u32)	1	1	~
l2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54	54	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8	8	_
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	554	554	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344	123	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DRR	123 45	45	<b>V</b>
target I2c GenStopCond I2cRegPtr Cnt T str.SAR	54	54	J
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	-
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554	554	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788	788	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344	344	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	54	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	<b>*</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8	8	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554	554	¥
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	344	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123 45	123 45	-
target_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	54	54	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR target_l2c_Send_l2cRegPtr_Cnt_T_str.DXR	66	66	
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR	554	554	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	788	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target I2c Send I2cRegPtr Cnt T str.PSC	66	66	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344	344	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	~
0 0			
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	54	54	~
	54 66 8	54 66 8	7

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554	554	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344	344	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123	123	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45	45	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54	54	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554	554	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788	788	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344	344	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	1	1	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	3 2	3 2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SET	3	3	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.ODR	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	
target I2c SetRecv I2cRegPtr Cnt T str.PSL	2	2	· ·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54	54	
target_12c_SetStatus_12cRegPtr_Cnt_T_str.IMR	66	66	<b>V</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8	8	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554	554	~
target I2c SetStatus I2cRegPtr Cnt T str.CLKH	344	344	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	123	123	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45	45	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54	54	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554	554	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	788	788	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344	344	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3 2	3	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	<del>-</del>	_	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	54	2 54	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	66	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	8	8	-
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	554	554	
target_12c_SetupMasterReceive_12cRegPti_Cnt_T_str.CLKL target_12c_SetupMasterReceive_12cRegPtr_Cnt_T_str.CLKH	344	344	-
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CNT	123	123	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45	45	•
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SAR	54	54	_
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554	554	-
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788	788	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344	344	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54	54	

target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSL

DigColPsInt\_InterruptNotification

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**Actual Value Expected Value**  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IMR$ 66 66  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.STR$  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKL$ 554 554  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLKH$ 344 344  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CNT$ 123 123  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DRR$ 45 45 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SAR 54 54  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DXR$ 66 66 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.MDR 554 554  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.IVR$ 788 788 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.EMDR 3 3  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PSC$ 66 66 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID11 344 344 66  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PID12$ 66  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DMAC$ 3 3 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.FUN 1  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIR$ 3 3 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DIN 2 2  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.DOUT$ 3 3 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.SET 3 3  $target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.CLR$ 3 3 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.ODR 2 2 1 target\_I2c\_SetupMasterTransmit\_I2cRegPtr\_Cnt\_T\_str.PD 1

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c Send	1	I2c Send	1	_

2

Test Step 3.48 (Repeat Count = 1)	
Name	Input Value
DigColPsInt AttempOccurForCustDatRead Cnt M u08	4
DigColPsInt Buffer Cnt M u08[0]	100
DigColPsInt Buffer Cnt M u08[1]	200
DigColPsInt Buffer Cnt M u08[2]	250
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt CmdFailOccurred Cnt M Igc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt ColSnsrData Cnt M u16	7
DigColPsInt CurrentSlave Cnt M u08	35
DigColPsInt CurrentStepNo Cnt M enum	INIT SENSOR2 DUMMY READ
DigColPsInt I2CHwCustData Uls M u16	70
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	71
DigColPsInt InitFailedOnce Cnt M Igc	0
DigColPsInt NackOccured Cnt M Igc	0
DigColPsInt PrevRegDataType Cnt M u08	5
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt RecvdDataType Cnt M u08	5
DigColPsInt SkipRegisterWrite Cnt M Igc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt SpurSnsrData Cnt M u16	88
DigColPsInt_TransactionCnt_Cnt_M_u08	110
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_l2c_SetStatus_l2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14

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	( 14 17 10 10
Name	Input Value
i2cREG1 temp	target_i2cREG1_temp
k_ColSensorl2CAddress_Cnt_u08	127
	5
k_SpurSensorI2CAddress_Cnt_u08	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65
target I2c GenStopCond I2cRegPtr Cnt T str.DXR	89
	7
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target I2c GenStopCond I2cRegPtr Cnt T str.DIR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CNT	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89
torget 12e CetPoor 12ePooPt- Cet T et CTD	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	01
target_I2c_SetRecv_I2cRegPtr_Cnt_I_str.STR target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	7
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	7 577 88
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	7 577 88 23
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	7 577 88 23 65
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	7 577 88 23 65 89
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	7 577 88 23 65 89 7
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	7 577 88 23 65 89 7
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR	7 577 88 23 65 89 7
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	7 577 88 23 65 89 7
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR	7 577 88 23 65 89 7 44
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	7 577 88 23 65 89 7 44 2
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DAR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12	7 577 88 23 65 89 7 44 2 89 577
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DAR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	7 577 88 23 65 89 7 44 2 89 577 89
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DAR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	7 577 88 23 65 89 7 44 2 89 577 89 2
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DAR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIAC target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIAC target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DIR	7 577 88 23 65 89 7 44 2 89 577 89 2 0 0
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DAR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.MDR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.EMDR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	7 577 88 23 65 89 7 44 2 89 577 89 2

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Name	Innut Value
	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89
	67
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89
	577
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89
	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89
target I2c SetupMasterReceive I2cRegPtr Cnt T str.MDR	7
· · - · · · · · · · · · · · · · · · · ·	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSC	89
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PID11	577
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SET	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	89
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	67
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89
	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	
target up Setupiageter (ranemit 12cDegDtr Cht Cetr DID12	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	2
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	
	2 0 0

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Name	Input Value		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0		
target_i2cREG1_temp.OAR	65		
target_i2cREG1_temp.IMR	89		
target_i2cREG1_temp.STR	67		
target_i2cREG1_temp.CLKL	7		
target_i2cREG1_temp.CLKH	577		
target_i2cREG1_temp.CNT	88		
target_i2cREG1_temp.DRR	23		
target_i2cREG1_temp.SAR	65		
target_i2cREG1_temp.DXR	89		
target_i2cREG1_temp.MDR	7		
target_i2cREG1_temp.IVR	44		
target_i2cREG1_temp.EMDR	2		
target_i2cREG1_temp.PSC	89		
target_i2cREG1_temp.PID11	577		
target_i2cREG1_temp.PID12	89		
target_i2cREG1_temp.DMAC	2		
target_i2cREG1_temp.FUN	0		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	2		
target_i2cREG1_temp.SET	2		
target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.ODR	1		
target_i2cREG1_temp.PD	2		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result

target_izerteer_temp.r D	L		
target_i2cREG1_temp.PSL	0		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	4	4	~
DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	•
DigColPsInt_Buffer_Cnt_M_u08[1]	200	200	~
DigColPsInt_Buffer_Cnt_M_u08[2]	250	250	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	~
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt_ColSnsrData_Cnt_M_u16	7	7	•
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_SET	INIT_SENSOR1_EXTREADCTRLREG_SET	<b>✓</b>
DigColPsInt_I2CHwCustData_Uls_M_u16	70	70	~
DigColPsInt_I2CHwIncompleteCustData_UIs_M_u16	71	71	~
DigColPsInt_InitFailedOnce_Cnt_M_Igc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	<b>✓</b>
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	~
DigColPsInt_RecvdDataType_Cnt_M_u08	5	5	<b>✓</b>
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	88	88	<b>✓</b>
DigColPsInt_TransactionCnt_Cnt_M_u08	110	110	~
I2c_Send(Length_Cnt_T_u32)	1	1	<b>✓</b>
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65	65	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67	67	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	577	577	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88	88	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23	23	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	89	89	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44	44	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89	89	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	•

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	2	✓
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.ODR	1	1	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSL target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	65	65	- J
target_12c_Send_12cRegPtr_Cnt_T_str.IMR	89	89	<u> </u>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	<b>~</b>
target_l2c_Send_l2cRegPtr_Cnt_T_str.SAR	65	65	<b>V</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89 7	89 7	×
target_l2c_Send_l2cRegPtr_Cnt_T_str.MDR target_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	44	44	Ž
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	<u> </u>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DIR	0	0	<b>v</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	1 2	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.DOUT target_l2c_Send_l2cRegPtr_Cnt_T_str.SET	2	2	- J
target I2c Send I2cRegPtr Cnt T str.CLR	0	0	<u> </u>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	✓
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65	65	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89	89	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67	67	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7 577	7 577	<u> </u>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CNT	88	88	Ž
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DRR	23	23	<u> </u>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	65	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89	89	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7	7	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44	44	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC	89	89	<b>~</b>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	577	577	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID12 target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	89 2	89 2	Ž
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.FUN	0	0	·
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	2	✓
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0 65	0 65	<b>*</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IMR	89	89	Ž
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67	67	Ž
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7	7	·
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	88	88	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23	23	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65	65	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89	89	<b>✓</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR	7	7	<b>✓</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.IVR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.EMDR	44 2	44	~
target_I2c_SetStatus_I2cRegPtr_Cnt_I_str.EMDR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89	2 89	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	577	577	<u> </u>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	~



Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	✓
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	65	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	89	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67	67	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577	577	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88	88	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23	23	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65	65	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	✓
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✓
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	<b>✓</b>

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	~
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	<b>✓</b>
I2c_Send	1	I2c_Send	1	•

Test Step 3.49 (Repeat Count = 1)	✓
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2
DigColPsInt_Buffer_Cnt_M_u08[0]	1
DigColPsInt_Buffer_Cnt_M_u08[1]	5

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DigColPsini_interruptivotilication	
Name	Input Value
igColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
igColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	56
DigColPsInt_CurrentSlave_Cnt_M_u08	90
higColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_GETDATA
igColPsInt_I2CHwCustData_Uls_M_u16	64
igColPsInt_I2CHwIncompleteCustData_Uls_M_u16	65
igColPsInt_InitFailedOnce_Cnt_M_lgc	0
igColPsInt_NackOccured_Cnt_M_lgc	1
igColPsInt_PrevReqDataType_Cnt_M_u08	3
igColPsInt_RecvOverrunError_Cnt_M_lgc	1
igColPsInt_RecvdDataType_Cnt_M_u08	1
igColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
igColPsInt_SpurCustDatFound_Cnt_M_lgc	1
igColPsInt_SpurSnsrData_Cnt_M_u16	7878
igColPsInt_TransactionCnt_Cnt_M_u08	100
ags_Cnt_T_b16	32
c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
tc_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
tc_SetRecv(I2cRegPtr_Cnt_T_str)	target_l2c_SetRecv_l2cRegPtr_Cnt_T_str
tc_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
_DataRegisters_Cnt_u08[0]	0
_DataRegisters_Cnt_u08[1]	32
_DataRegisters_Cnt_u08[2]	30
_DataRegisters_Cnt_u08[3]	36
_DataRegisters_Cnt_u08[4]	38
_DataRegisters_Cnt_u08[5]	34
_DataRegisters_Cnt_u08[6]	10
_DataRegisters_Cnt_u08[7]	12
_DataRegisters_Cnt_u08[8]	14
2cREG1_temp	target_i2cREG1_temp
_ColSensorI2CAddress_Cnt_u08	114
_SpurSensorl2CAddress_Cnt_u08	30
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	678
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	45
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	66
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	56
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	6788
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	7878
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12
urget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	678
urget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	45
rget I2c GenStopCond I2cRegPtr Cnt T str.MDR	56
	778
urget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	45
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	6788
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	45
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2
rget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1
rget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	678
rget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	45
rget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	66
rget_l2c_send_l2cRegPtr_Cnt_T_str.CLKL	56
irget_12c_send_12cRegPtr_Cnt_T_str.CLKH	6788
irget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	7878
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12
irget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	678
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	45
want IOn Cond IOnDorDtr Cot T ats MDD	56
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	778

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Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	6788
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target I2c Send I2cRegPtr Cnt T str.CLR	0
	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	678
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	45
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	56
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKH	6788
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	7878
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	678
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	45
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	778
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	45
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	6788
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	45
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	678
target 12c SetStatus 12cRegPtr Cnt T str.IMR	45
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	6788
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	7878
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR	12
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR	678
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	45
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	778
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	45
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	6788
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	45
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	678
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	45
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.STR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	6788
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	7878
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	678
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	45

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Name	Input Value		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.MDR	56		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	778		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	45		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	6788		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	45		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1		
target I2c SetupMasterReceive I2cRegPtr Cnt T str.SET	1		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1		
	2		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD			
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	678		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	45		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	66		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	6788		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	7878		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	678		
	45		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR target_l2c SetupMasterTransmit_l2cRegPtr_Cnt_T str.MDR	56		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	778		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.EMDR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	45		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	6788		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	45		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1		
	1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DOUT			
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1		
target_i2cREG1_temp.OAR	678		
target_i2cREG1_temp.IMR	45		
target i2cREG1 temp.STR	66		
target_i2cREG1_temp.CLKL	56		
target_i2cREG1_temp.CLKH	6788		
target i2cREG1 temp.CNT	7878		
target_i2cREG1_temp.DRR	12		
target_i2cREG1_temp.SAR	678		
target_i2cREG1_temp.DXR	45		
target_i2cREG1_temp.MDR	56		
target_i2cREG1_temp.IVR	778		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	45		
target i2cREG1 temp.PID11	6788		
target i2cREG1 temp.PID12	45		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN	1		
target_i2cREG1_temp.DIR	0		
target_i2cREG1_temp.DIN	1		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.SET target_i2cREG1_temp.CLR	0		
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD	0 1 2		
target_i2cREG1_temp.CLR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL	0 1 2 1	Evenanted Value	Barrit
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL Name	0 1 2 1 Actual Value	Expected Value	
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	0 1 2 1 Actual Value 2	2	•
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0]	0 1 2 1 <b>Actual Value</b> 2	•	•
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	0 1 2 1 Actual Value 2	2	Ž
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0]	0 1 2 1 <b>Actual Value</b> 2	2	Result
target_i2cREG1_temp.CLR target_i2cREG1_temp.ODR target_i2cREG1_temp.PD target_i2cREG1_temp.PSL  Name  DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 DigColPsInt_Buffer_Cnt_M_u08[0] DigColPsInt_Buffer_Cnt_M_u08[1]	0 1 2 1 <b>Actual Value</b> 2 1 5	2 1 5	~

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Name	Actual Value	Expected Value	Result
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt_ColSnsrData_Cnt_M_u16	56	56	~
DigColPsInt_CurrentSlave_Cnt_M_u08	90	90	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE	READ_COMPLETE	~
DigColPsInt_I2CHwCustData_Uls_M_u16	64	64	
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	65	65	~
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	<b>V</b>
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	· ·
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	Ž
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_SpurSnsrData_Cnt_M_u16	261	261	
DigColPsInt_TransactionCnt_Cnt_M_u08	101	101	Ž
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	678	678	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IMR	45	45	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.STR	66	66 56	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	56		
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT	7878	7878	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12	12	· ·
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.SAR	678	678	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	45	45	· ·
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	56	56	<b>•</b>
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR	778	778	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.EMDR	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	45	45	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	6788	6788	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	45	45	~
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DMAC	1	1	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.FUN	1	1	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIR	0	0	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	·
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLR	0	0	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	678	678	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	45	45	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	66	66	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	56	56	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	7878	7878	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	678	678	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	45	45	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	56	56	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	778	778	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSC	45	45	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	6788	6788	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	45	45	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	678	678	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	45	45	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	66	66	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	56	56	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	7878	7878	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	12	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	678	678	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	45	45	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	56	56	<b>✓</b>

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Name	Actual Value	Expected Value	Result
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IVR	778	778	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1 45	1 45	· ·
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSC target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	6788	6788	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	45	45	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DOUT	1	1	<b>~</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	<b>Y</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	· ·
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.ODR target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PD	2	2	
target_12c_SetRecv_12cRegPtr_Cnt_T_str.PSL	1	1	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	678	678	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	45	45	<b>✓</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.STR	66	66	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	56	56	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	7878	7878	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12	12	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	678	678	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DXR target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.MDR	45 56	45 56	
target_I2c_SetStatus_I2cRegPtr_Cnt_I_str.MDR target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	778	778	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>~</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	45	45	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	6788	6788	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	45	45	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	<b>~</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DIN	1	1	<b>Y</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	0	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	678	678	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	45	45	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	66	66	<b>~</b>
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.CLKL	56	56	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	· ·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	7878 12	7878 12	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.SAR	678	678	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.DXR	45	45	
target I2c SetupMasterReceive I2cRegPtr Cnt T str.MDR	56	56	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	778	778	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	45	45	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	6788	6788	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	45	45	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DMAC	1	1	· ·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	· ·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.DIN target_l2c SetupMasterReceive_l2cRegPtr_Cnt_T_str.DOUT	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1	1	<b>~</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	678	678	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	45	45	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	66	66	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	56 6788	56 6788	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CLKH target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.CNT	7878	7878	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	678	678	·
0			

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	45	45	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	56	56	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	778	778	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	45	45	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	6788	6788	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	45	45	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	-
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3
DigColPsInt_Buffer_Cnt_M_u08[0]	10
igColPsInt_Buffer_Cnt_M_u08[1]	15
bigColPsInt_Buffer_Cnt_M_u08[2]	16
DigColPsInt BusBusySegError Cnt M Igc	0
DigColPsInt CmdFailOccurred Cnt M Igc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	566
digColPsInt_CurrentSlave_Cnt_M_u08	110
igColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_SETREG
pigColPsInt I2CHwCustData Uls M u16	7
igColPsInt I2CHwIncompleteCustData Uls M u16	8
DigColPsInt InitFailedOnce Cnt M Igc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
bigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
ligColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt SpurSnsrData Cnt M u16	129
igColPsInt_TransactionCnt_Cnt_M_u08	30
lags Cnt T b16	32
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
DataRegisters Cnt u08[0]	0
DataRegisters Cnt u08[1]	32
DataRegisters Cnt u08[2]	30
DataRegisters_Cnt_u08[3]	36
	38
DataRegisters_Cnt_u08[5]	34
	10
aataRegisters_Cnt_u08[7]	12
DataRegisters Cnt u08[8]	14
2cREG1 temp	target i2cREG1 temp
ColSensorI2CAddress Cnt u08	19
_SpurSensorI2CAddress_Cnt_u08	30
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.Nink	4444
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466
arget I2c GenStopCond I2cRegPtr Cnt T str.CNT	129

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Name	Input Value
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	·
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
arget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566 4466
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	129
arget_l2c_Send_l2cRegPtr_Cnt_T_str.CNT arget_l2c_Send_l2cRegPtr_Cnt_T_str.DRR	6
arget_l2c_send_l2cRegPtr_Cnt_T_str.brR arget_l2c_send_l2cRegPtr_Cnt_T_str.sAR	567
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
arget_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
arget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
arget_l2c_Send_l2cRegPtr_Cnt_T_str.DIN	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
arget_l2c_Send_l2cRegPtr_Cnt_T_str.SET	1
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
arget_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
	3
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL arget_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567
arget_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	

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Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566
target I2c SetStatus I2cRegPtr Cnt T str.IVR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target I2c SetStatus I2cRegPtr Cnt T str.DIN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PD	3
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	129
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44

DigColPsInt\_InterruptNotification

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Input Value target\_i2cREG1\_temp.STR 4444 target\_i2cREG1\_temp.CLKL 566 target\_i2cREG1\_temp.CLKH 4466 target\_i2cREG1\_temp.CNT 129 target\_i2cREG1\_temp.DRR 6 target\_i2cREG1\_temp.SAR 567 target\_i2cREG1\_temp.DXR 44 target\_i2cREG1\_temp.MDR 566 target\_i2cREG1\_temp.IVR 554  $target\_i2cREG1\_temp.EMDR$ 1 target\_i2cREG1\_temp.PSC 44 target\_i2cREG1\_temp.PID11 4466 target\_i2cREG1\_temp.PID12 44 target\_i2cREG1\_temp.DMAC 1 target\_i2cREG1\_temp.FUN target\_i2cREG1\_temp.DIR 2 target\_i2cREG1\_temp.DIN 0 target\_i2cREG1\_temp.DOUT 1 target\_i2cREG1\_temp.SET 1 target\_i2cREG1\_temp.CLR 2 target\_i2cREG1\_temp.ODR 0 target i2cPEG1 temp PD

target_i2cREG1_temp.PD	3		
target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3	3	~
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	<b>✓</b>
DigColPsInt Buffer Cnt M u08[1]	15	15	~
DigColPsInt_Buffer_Cnt_M_u08[2]	16	16	<b>✓</b>
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	~
DigColPsInt CmdFailOccurred Cnt M Igc	1	1	<b>✓</b>
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	~
DigColPsInt_ColSnsrData_Cnt_M_u16	566	566	<b>✓</b>
DigColPsInt CurrentSlave Cnt M u08	110	110	~
DigColPsInt CurrentStepNo Cnt M enum	INIT SENSOR1 READEXTERR SETREG	INIT SENSOR1 READEXTERR SETREG	<b>✓</b>
DigColPsInt I2CHwCustData Uls M u16	7	7	~
DigColPsInt I2CHwIncompleteCustData UIs M u16	8	8	<b>✓</b>
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	~
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	<b>✓</b>
DigColPsInt RecvOverrunError Cnt M Igc	0	0	~
DigColPsInt RecvdDataType Cnt M u08	2	2	<b>~</b>
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	~
DigColPsInt SpurSnsrData Cnt M u16	129	129	<b>~</b>
DigColPsInt TransactionCnt Cnt M u08	30	30	
target I2c GenStopCond I2cRegPtr Cnt T str.OAR	567	567	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566	566	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>V</b>
target I2c GenStopCond I2cRegPtr Cnt T str.CNT	129	129	_
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	567	
target I2c GenStopCond I2cRegPtr Cnt T str.DXR	44	44	<b>~</b>
target I2c GenStopCond I2cRegPtr Cnt T str.MDR	566	566	
target I2c GenStopCond I2cRegPtr Cnt T str.IVR	554	554	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	44	<b>~</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	4466	~
target I2c GenStopCond I2cRegPtr Cnt T str.PID12	44	44	<b>~</b>
target I2c GenStopCond I2cRegPtr Cnt T str.DMAC	1	1	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>~</b>
target I2c GenStopCond I2cRegPtr Cnt T str.DIR	2	2	~
target I2c GenStopCond I2cRegPtr Cnt T str.DIN	0	0	<b>✓</b>
target I2c GenStopCond I2cRegPtr Cnt T str.DOUT	1	1	~
target I2c GenStopCond I2cRegPtr Cnt T str.SET	1	1	<b>✓</b>
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	<b>✓</b>
target I2c GenStopCond I2cRegPtr Cnt T str.PD	3	3	~
target I2c GenStopCond I2cRegPtr Cnt T str.PSL	3	3	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>~</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.CLKH	4466	4466	~
<u> </u>	1	1	

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	<b>✓</b>
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	-
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	_
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
target I2c Send I2cRegPtr Cnt T str.SET	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	
	0	0	
target_l2c_Send_l2cRegPtr_Cnt_T_str.ODR			
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	<u> </u>
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	567	567	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	
	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	44	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC			
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	4466	4466	-
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	<b>✓</b>
target I2c SetRecv I2cRegPtr Cnt T str.CLR	2	2	<b>✓</b>
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	_
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	_
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	
	4444	4444	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	566	4444 566	Ž
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL			
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	<b>✓</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DRR	6	6	
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	-
target I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	-
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.Pib12	1	1	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	
	2	2	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR			
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	•
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.DOUT	1	1	<u> </u>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.SET	1	1	~
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>✓</b>

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	•
target I2c SetupMasterReceive I2cRegPtr Cnt T str.PSL	3	3	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.OAR	567	567	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	44	44	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.STR	4444	4444	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CLKH	4466	4466	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.CNT	129	129	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DRR	6	6	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SAR	567	567	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IVR	554	554	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.EMDR	1	1	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSC	44	44	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PID11	4466	4466	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DMAC	1	1	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.FUN	1	1	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIR	2	2	•
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DIN	0	0	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.DOUT	1	1	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.SET	1	1	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PD	3	3	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	

T				V
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	<b>✓</b>

Test Step 3.51 (Repeat Count = 1)	
Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	15
DigColPsInt_Buffer_Cnt_M_u08[2]	16
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	566
DigColPsInt_CurrentSlave_Cnt_M_u08	50
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADDATREG_READ
DigColPsInt_I2CHwCustData_UIs_M_u16	91
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	0
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1



DigColPSITI_Interruptivotilication		
Name	Input Value	
DigColPsInt_RecvdDataType_Cnt_M_u08	2	
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1	
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	
)igColPsInt_SpurSnsrData_Cnt_M_u16	129	
DigColPsInt_TransactionCnt_Cnt_M_u08	7	
Flags_Cnt_T_b16	32	
2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str	
2c_Send(I2cRegPtr_Cnt_T_str)	target_l2c_Send_l2cRegPtr_Cnt_T_str	
2c SetRecv(I2cRegPtr Cnt T str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str	
2c SetStatus(I2cRegPtr Cnt T str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str	
_ , , , , , , , , , , , , , , , , , , ,		
2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str	
2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str	
_DataRegisters_Cnt_u08[0]	0	
_DataRegisters_Cnt_u08[1]	32	
_DataRegisters_Cnt_u08[2]	30	
_DataRegisters_Cnt_u08[3]	36	
_DataRegisters_Cnt_u08[4]	38	
_DataRegisters_Cnt_u08[5]	34	
_DataRegisters_Cnt_u08[6]	10	
_DataRegisters_Cnt_u08[7]	12	
_DataRegisters_Cnt_u08[8]	14	
2cREG1_temp	target_i2cREG1_temp	
ColSensorl2CAddress_Cnt_u08	27	
SpurSensorI2CAddress Cnt u08	10	
arget I2c GenStopCond I2cRegPtr Cnt T str.OAR	567	
arget I2c GenStopCond I2cRegPtr Cnt T str.IMR	44	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	
arget I2c GenStopCond I2cRegPtr Cnt T str.PID12	44	
arget I2c GenStopCond I2cRegPtr Cnt T str.DMAC	1	
arget I2c GenStopCond I2cRegPtr Cnt T str.FUN	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	
arget I2c GenStopCond I2cRegPtr Cnt T str.DOUT	1	
	1	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET		
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	
arget_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	
rget_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	
arget I2c Send I2cRegPtr Cnt T str.DRR	6	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	
rget_I2c_send_I2cRegPtr_Cnt_T_str.MDR	566	
	554	
arget_l2c_Send_l2cRegPtr_Cnt_T_str.IVR	1	
urget_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR		
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	
irget_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	
arget_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	
	2	
arget 12c Send 12cRegPtr Cnt   str.CLR		
arget_l2c_Send_l2cRegPtr_Cnt_T_str.CLR arget_l2c_Send_l2cRegPtr_Cnt_T_str.ODR	0	

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	(
Name	Input Value
target_l2c_Send_l2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
target I2c SetRecv I2cRegPtr Cnt T str.CNT	129
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44
	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target I2c SetRecv I2cRegPtr Cnt T str.CLR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129
	6
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target I2c SetStatus I2cRegPtr Cnt T str.PSC	44
target I2c SetStatus I2cRegPtr Cnt T str.PID11	4466
	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target I2c SetStatus I2cRegPtr Cnt T str.SET	1
target I2c SetStatus I2cRegPtr Cnt T str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKL	566
target I2c SetupMasterReceive I2cRegPtr Cnt T str.CLKH	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
target_l2c_SetupMasterReceive_l2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2

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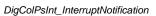
Name	Input Value		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3 567		
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.IMR	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	129 6		
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DRR target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.SAR	567		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3		
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
target_i2cREG1_temp.OAR	567		
target_i2cREG1_temp.IMR	44		
target_i2cREG1_temp.STR target_i2cREG1_temp.CLKL	4444 566		
target i2cREG1 temp.CLKH	4466		
target_i2cREG1_temp.CNT	129		
target_i2cREG1_temp.DRR	6		
target_i2cREG1_temp.SAR	567		
target_i2cREG1_temp.DXR	44		
target_i2cREG1_temp.MDR target_i2cREG1_temp.IVR	566 554		
target_i2cREG1_temp.EMDR	1		
target_i2cREG1_temp.PSC	44		
target_i2cREG1_temp.PID11	4466		
target_i2cREG1_temp.PID12	44		
target_i2cREG1_temp.DMAC	1		
target_i2cREG1_temp.FUN target_i2cREG1_temp.DIR	2		
target_i2cREG1_temp.DIN	0		
target_i2cREG1_temp.DOUT	1		
target_i2cREG1_temp.SET	1		
target_i2cREG1_temp.CLR	2		
target_i2cREG1_temp.ODR	0		
target_i2cREG1_temp.PD target_i2cREG1_temp.PSL	3		
Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8	8	- Toodit
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	<b>✓</b>
DigColPsInt_Buffer_Cnt_M_u08[1]	15	15	~
DigColPsInt_Buffer_Cnt_M_u08[2]	16	16	~
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	<b>V</b>
DigColPsInt_CmdFailOccurred_Cnt_M_lgc DigColPsInt ColCustDatFound Cnt M lgc	1	1	Ž
DigColPsInt ColSnsrData Ont M u16	566	566	_
DigColPsInt_CurrentSlave_Cnt_M_u08	50	50	~
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE	INIT_COMPLETE	~
DigColPsInt_I2CHwCustData_Uls_M_u16	0	0	~
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	0	0	<b>V</b>
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	<b>✓</b>
DigColPsInt_NackOccured_Cnt_M_lgc DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	~
DigColPsInt_RecvdDataType_Cnt_M_u08	2	2	_
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	
DigColPsInt_SpurSnsrData_Cnt_M_u16			
bigoon oint_oparonorbatta_ont_in_a to	129	129	•
DigColPsInt_TransactionCnt_Cnt_M_u08	129 7	129 7	•

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Name	Actual Value	Expected Value	Resul
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	567	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	44	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	4444	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKL	566	566	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CLKH	4466	4466	•
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.CNT	129	129	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6 567	6 567	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	44	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.MDR	566	566	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.IVR	554	554	
target I2c GenStopCond I2cRegPtr Cnt T str.EMDR	1	1	
target_l2c_GenStopCond_l2cRegPtr_Cnt_T_str.PSC	44	44	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	4466	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	44	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_l2c_Send_l2cRegPtr_Cnt_T_str.OAR	567	567	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566 4466	
target_l2c_Send_l2cRegPtr_Cnt_T_str.CLKH	4466 129	129	
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	
target_i2c_Send_i2cRegPtr_Cnt_T_str.SAR	567	567	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.OAR	567	567	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.IMR	44	44	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444 566	4444 566	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.CLKL	4466	4466	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	
target_12c_SetRecv_12cRegPtr_Cnt_1_str.Cn1 target_12c_SetRecv_12cRegPtr_Cnt_T_str.DRR	6	6	
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.SAR	567	567	
target_i2c_SetRecv_i2cRegPtr_Cnt_T_str.DXR	44	44	
target_i2c_SetRecv_i2cRegPtr_Cnt_T_str.MDR	566	566	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.PID11	4466	4466	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	•
target_l2c_SetRecv_l2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	•
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	~
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	<b>✓</b>
target_l2c_SetStatus_l2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	<b>✓</b>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	<u> </u>
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	<u> </u>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	<u> </u>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	·
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	<b>✓</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	<u> </u>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	<u> </u>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	<b>*</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>*</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>~</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	<b>*</b>
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	•
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	_
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID11	4466	4466	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.PID12	44	44	•
target_l2c_SetupMasterTransmit_l2cRegPtr_Cnt_T_str.DMAC	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	•
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	<b>✓</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	<b>Y</b>
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	~
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	~
target I2c SetupMasterTransmit I2cRegPtr Cnt T str.PSL	3	3	<b>~</b>

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
*none*	0	*** No Call Expected ***	0	~

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SetupWriteData	2014 10 14, 20.40.11 10000	Razoncat
Project		
Module		
Test Object		
Instrumentation: Test Object Only		
Ctatament (CO) Cavarage		

#### **Statistics**

Total Testcases	
Successful	✓
Failed	
Not Executed	

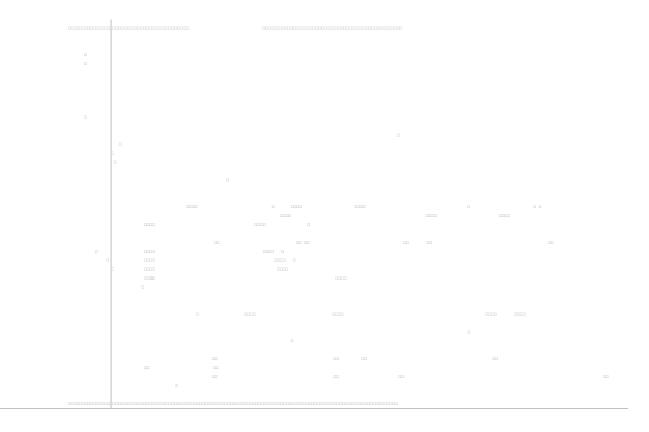
#### **Module Properties**

Branch (C1) Coverage

Project Root Directory		
Configuration File		
Target Environment		
Kind of Test		
Linker Options		
Source File(s)		
File		
Compiler Options		
О		

Comments/Desc	ription/Specification	
Name	Text	





Attributes	
Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	\$(Compiler Install Path)\include
Time Unit	Cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\Clxx_DigColPs\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP



# Test Case 1: Boundary Test Description

Test Step 1.1 (Repeat Count = 1)			✓
Name	Input Value		
	0		
	0.0		
	0		
	а		
	0		
	а		
Name	Actual Value	Expected Value	Result
			-
			~
			•
		<u> </u>	
			•
			•
	0.0	0.0	•
	9		Ĭ
		<u> </u>	
			-
			•
		<u> </u>	<b>*</b>
	<u> </u>	<u> </u>	
		-	•

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**Actual Value** 



**Expected Value** 

SetupWriteData

Name

			~
			<b>✓</b>
			<b>✓</b>
			~
			<b>✓</b>
			~
			<b>✓</b>
			~
			~
			~
		22	•
			-
			-
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			<b>✓</b>
			~
			<b>~</b>
			~
			<b>~</b>
T			
	T		

T .				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
				~
				-

Test Step 1.2 (Repeat Count = 1)	✓
Name	Input Value

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	2/1	76		1	7
	Va	ZO	717	'at	,

SetupWriteData	
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Name	Input Value		
Name	Actual Value	Expected Value	Result
Humo	Actual Value	Expected value	rtosuit ✓
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			~
			<b>*</b>
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		u u	<b>~</b>
	а		<b>*</b>
			~
			<b>*</b>
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			<b>*</b>
			~
			•
			<b>*</b>
			<b>✓</b>
			<b>*</b>
			<b>*</b>
			~
			-
			•
			<b>✓</b>
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	0		~
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	0		~
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			~
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			<b>*</b>
	0		~
			_
			~
			<b>✓</b>
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			<b>*</b>
			<b>*</b>
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			•
			<b>*</b>
	0	0	
Т			<b>V</b>
	Expected Function	Count	

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Test Step 1.3 (Repeat Count = 1)			~
Name	Input Value		
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	u u		
	0		
Manage 1	Actual Value	I =	
Name	Actual value	Expected Value	Result
Name	Actual value	Expected Value	<b>✓</b>
Name	Actual value	Expected Value	<b>✓</b>
Name	Actual Value	Expected Value	<b>*</b>
			\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Name	a	a	*
			*
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		D	***************************************
		D	· · · · · · · · · · · · · · · · · · ·
			· · · · · · · · · · · · · · · · · · ·
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Test Step 1.4 (Repeat Count = 1)			✓
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Test Step 1.5 (Repeat Count = 1)	🗸
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Test Step 1.6 (Repeat Count = 1)			V
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Test Step 1.7 (Repeat Count = 1)	🗸
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Test Step 1.8 (Repeat Count = 1)			V
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Test Step 1.9 (Repeat Count = 1)			<b>✓</b>
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Test Step 1.10 (Repeat Count = 1)	<b>✓</b>
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Actual Function	Count	Expected Function	Count	Result
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Test Step 1.11 (Repeat Count = 1)			<b>✓</b>
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Actual Value Expected Value R

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Test Step 1.13 (Repeat Count = 1)			✓
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Name	Actual Value	Expected Value	~
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Test Step 1.14 (Repeat Count = 1)			✓
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Project		
Module		
Test Object		
Instrumentation: Test Object Onl	у	
Statement (CO) Coverage		
Statement (C0) Coverage  Branch (C1) Coverage		
Dianon (01) corolage		
Statistics		

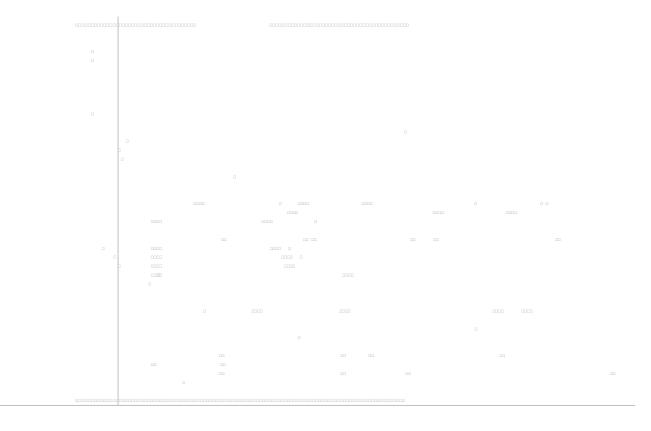
#### **Module Properties**

**Total Testcases** Successful Failed Not Executed

Project Root Directory		
Configuration File		
Target Environment		
Kind of Test		
Linker Options		
Source File(s)		
File		
Compiler Options		

Comments/Description/Spe	ecification
Name	Text





Attributes	
Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	<pre>\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd</pre>
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	\$(Compiler Install Path)\include
Time Unit	Cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\Clxx_DigColPs\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

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Test Case 1: Boundary	Test
Description	

Test Step 1.1 (Repeat Count = 1)		•
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Count Result

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**Actual Function** 

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Count Expected Function

Test Step 1.2 (Repeat Count = 1)	✓
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Input Value



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Name

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Test Step 1.3 (Repeat Count = 1)	<b>√</b>
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Test Step 1.4 (Repeat Count = 1)			
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Name Actual Value Expected Value Resul

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Test Step 1.6 (Repeat Count = 1)			✓
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Name	Actual Value	Expected Value	Result
Name	Actual Value	Expected Value	<b>✓</b>
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Count Result

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**Actual Function** 

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Count Expected Function

Test Step 1.7 (Repeat Count = 1)			~
Name	Input Value		
Name	Actual Value	Expected Value	Result
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Name	Actual Value	Expected Value	Result
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Actual Function	Count	Expected Function	Count	Result
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Test Step 1.8 (Repeat Count = 1) Name		V
Name	Input Value	

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Actual Function	Count	Expected Function	Count	Result
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Test Step 1.9 (Repeat Count = 1)			✓
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Name	Actual Value	Expected Value	Result
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Test Step 1.10 (Repeat Count = 1)	🗸
Name	Input Value

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Actual Function	Count	Expected Function		Count	Result
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Test Step 1.11 (Repeat Count = 1) Name	Input Value		✓
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