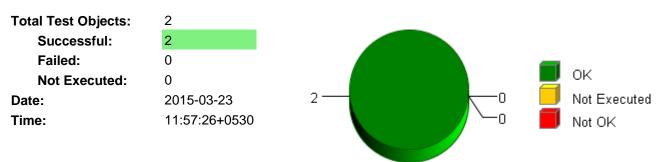


#### **Summary**

#### **Overall Test Object Results (including Coverage)**



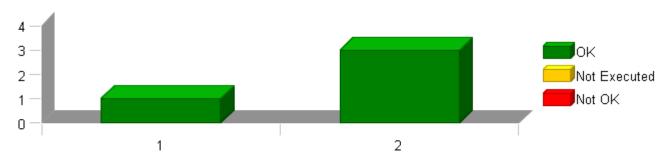
#### **Selected Project Items**

Test Object "CBD\_UnitTest/AssistFireWall/AssistFirewall\_Init1" Test Object "CBD\_UnitTest/AssistFireWall/AssistFirewall\_Per1"

#### **Used Test Environments**

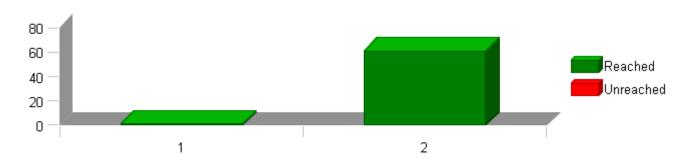
TI TMS 570 PLS UDE (Default)

#### **Test Case Results for Each Test Object (without Coverage)**



The table above shows each test object on the x axis and the number of test cases of the respective test object on the y axis. Each bar is divided into passed, not executed and failed test cases. The test case results do not take into account any coverage result (i.e. if all test cases of a test object are passed in this table but the coverage is failed, the overall test object result will be failed).

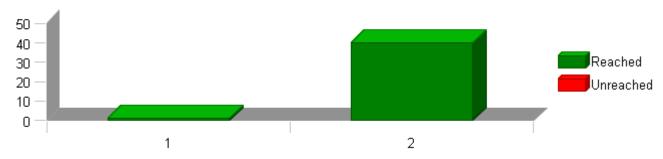
#### Statement (C0) Coverage: Total Statements for Each Test Object





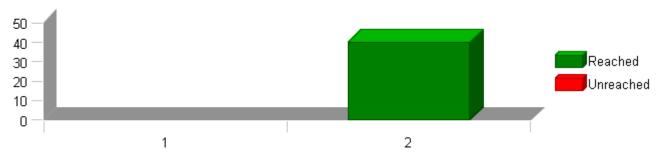
The table above shows each test object on the x axis and the number of statements of the respective test object on the y axis. Each bar is divided into reached statements (i.e. statements that have been executed during the test) and unreached statements.

#### Branch (C1) Coverage: Total Branches for Each Test Object



The table above shows each test object on the x axis and the number of branches of the respective test object on the y axis. Each bar is divided into reached branches (i.e. branches that have been executed during the test) and unreached branches.

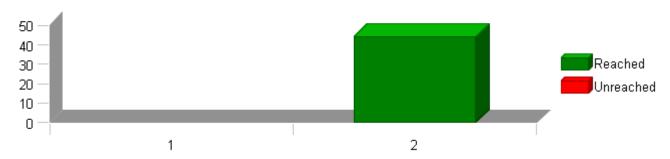
#### **Decision Coverage: Total Decision Outcomes for Each Test Object**



The table above shows test objects on the x axis and the number of possible outcomes of all decisions of the respective test object on the y axis. To achieve full DC coverage, each decision must evaluate to both true and false.

Each bar is divided into reached and unreached decision outcomes.

#### MC/DC Coverage: Total Condition Combinations for Each Test Object

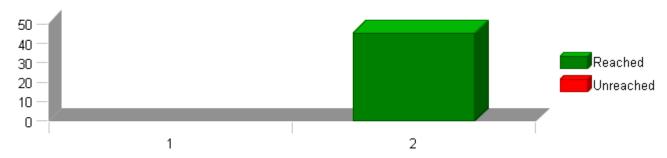


The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MC/DC coverage, each decision requires all contained atomic conditions to evaluate to both true and false independently of all other conditions. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.



#### MCC Coverage: Total Condition Combinations for Each Test Object



The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MCC coverage, each decision requires all contained atomic conditions to evaluate to all possible combinations of true and false values. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.



## **Test Object List**

The following table lists all test objects with their test case and coverage results. The cumulated results for modules, folders and test collections are also displayed, the indentation within the name column indicates the parent relationship of the elements.

Please note that only test objects are numbered within the first column. This number is referenced on the x axis within the overview charts for test case and coverage results available on previous pages (if included into the report).

No.	Name	C0	C1	DC	MC/DC	MCC	Test Cases	Result
	AssistFirewall	100 %	100 %	100 %	100 %	100 %	4 of 4 passed	~
	CBD_UnitTest	100 %	100 %	100 %	100 %	100 %	4 of 4 passed	•
	AssistFireWall	100 %	100 %	100 %	100 %	100 %	4 of 4 passed	•
1	AssistFirewall_Init1	100 %	100 %	-	-	-	1 of 1 passed	•
2	AssistFirewall Per1	100 %	100 %	100 %	100 %	100 %	3 of 3 passed	~

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AssistFirewall\_Init1

 Project
 AssistFirewall

 Module
 AssistFireWall

 Test Object
 AssistFirewall\_Init1

#### Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

#### **Statistics**

Total Testcases	1	
Successful	1	✓
Failed	0	
Not Executed	0	

#### **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\AssistFirewall
Configuration File	D:\Synergy_Work_Area\AssistFirewall\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\src\Ap_AssistFirewall.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -DBC_ASSISTFIREWALL_FAULTINJECTIONPOINT=STD_OFF -I\$(PROJECTROOT)\utp\contract \Ap_AssistFirewall -I\$(PROJECTROOT)\utp\contract -I\$(PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include -I\$ (Compiler Install Path)\include
File	\$(PROJECTROOT)\NxtrLib\src\interpolation.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -DBC_ASSISTFIREWALL_FAULTINJECTIONPOINT=STD_OFF -I\$(PROJECTROOT)\utp\contract \Ap_AssistFirewall -I\$(PROJECTROOT)\utp\contract -I\$(PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include -I\$ (Compiler Install Path)\include

Comments/Description/Spe	ecification
Name	Text
Module 'AssistFireWall'	Name of Tester:Ankita Bhardwaj Code File(s) Under Test:Ap_AssistFirewall.c Code File(s) Version:14 Module Design Document:Assist_Firewall_MDD.docx Module Design Document Version:14 Data Dictionary Version:16 Unit Test Plan Version:11 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.31 Total FLASH Used (Bytes):1568 Total RAM Used (Bytes):1568 Total RAM Used (Bytes):480 Special Test Requirements: Test Date:03-23-2015 Comments:"NOTE:1) Inline functions defined in GlobalMacro.h are not Unit Tested. 2)""CBD_Sandbox_dbg.map""map file is embedded for reference. 3) In ""AssistFirewall_Per1" function, ""Defeat_AsstTbl_Service_Cnt_Igc" always kept FALSE to make ""if((DefeatAsstTblSvc_Cnt_T_Igc <> D_FALSE_CNT_LGC) And (MECCounter_Cnt_T_enum <> ProductionMode))"" condition FALSE except Boundray Test for variables used in Condition and Path coverage. "
Test Object 'AssistFirewall_Init1'	

Attributes				
Name	Value			
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5			
Float Precision	9			
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj			
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src			
Linker File	\$(PROJECTROOT)\UnitTestEnv\static build files\sys link.cmd			

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AssistFirewall\_Init1

Attributes			
Name	Value		
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570.tpl		
Target Install Path	\$(ProgramFiles)\pls\UDE 3.2		
Time Unit	Cycles		
Timer Enabled	false		
Timer Prescale	0		
Timer Resolution	1		
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg		
Workspace File	D:\Synergy_Work_Area\AssistFirewall\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP		



#### Test Case 1: Boundary Test

Performance Metrics (With "None" Instrumentation and WithPS Environment)
CPU Cycles: Specification

TC1.1 1813.00 Cycles TC1.2 1820.00 Cycles TC1.3 1820.00 Cycles TC1.4 1820.00 Cycles TC1.5 1820.00 Cycles TC1.6 1820.00 Cycles TC1.7 1820.00 Cycles TC1.8 1820.00 Cycles

Description Vector Description

TS1.1k\_AsstFWFiltKn\_Hz\_f32 = min TS1.2k\_AsstFWFiltKn\_Hz\_f32 = max TS1.3k\_AsstFWFiltKn\_Hz\_f32 = mid TS1.4k\_AsstFWFWActiveLPF\_Hz\_f32 = min TS1.5k\_AsstFWFWActiveLPF\_Hz\_f32 = max TS1.6k\_AsstFWFWActiveLPF\_Hz\_f32 = mid TS1.7AII min TS1.8All max

Test Step 1.1 (Repeat Count = 1)			✓
Name	Input Value		
k_AsstFWFWActiveLPF_Hz_f32	40.0999985		
k_AsstFWFiltKn_Hz_f32	0.10000001		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.395837128	0.395837128 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00062871	1.00062859 ± 6.10E-05	•
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	<b>✓</b>
AssistFirewall UprBoundKSV M str.K Uls f32	0.00125586987	0.00125584798 ± 1.53E-05	<b>✓</b>

Test Step 1.2 (Repeat Count = 1)			
Name	Input Value		
k_AsstFWFWActiveLPF_Hz_f32	50.2999992		
k_AsstFWFiltKn_Hz_f32	100		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.46851933	0.46851933 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	✓
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	2.09537983	2.09537959 ± 6.10E-05	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	✓
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	<b>✓</b>

Test Step 1.3 (Repeat Count = 1)			✓
Name	Input Value		
k_AsstFWFWActiveLPF_Hz_f32	60.4000015		
k_AsstFWFiltKn_Hz_f32	50.2999992		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.531869829	0.531869769 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.46851933	0.46851933 ± 1.53E-05	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.41246235	1.41246235 ± 6.10E-05	•
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.46851933	0.46851933 ± 1.53E-05	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.46851933	0.46851933 ± 1.53E-05	<b>✓</b>

Test Step 1.4 (Repeat Count = 1)			✓
Name	Input Value		
k_AsstFWFWActiveLPF_Hz_f32	0.10000001		
k_AsstFWFiltKn_Hz_f32	10.1999998		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.12030232	0.120302327 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.06748891	1.06748891 ± 6.10E-05	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.12030232	0.120302327 ± 1.53E-05	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.12030232	0.120302327 ± 1.53E-05	<b>~</b>





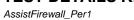
Test Step 1.5 (Repeat Count = 1)				
Name	Input Value			
k_AsstFWFWActiveLPF_Hz_f32	100			
k_AsstFWFiltKn_Hz_f32	20.2999992			
Name	Actual Value	Expected Value	Result	
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	~	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.22515893	0.225158915 ± 1.53E-05	<b>✓</b>	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.14153636	1.14153647 ± 6.10E-05	<b>✓</b>	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.22515893	0.225158915 ± 1.53E-05	✓	
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.22515893	0.225158915 ± 1.53E-05	✓	

Test Step 1.6 (Repeat Count = 1)			✓
Name	Input Value		
k_AsstFWFWActiveLPF_Hz_f32	50.2999992		
k_AsstFWFiltKn_Hz_f32	30.1000004		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.46851933	0.46851933 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.31493926	0.31493926 ± 1.53E-05	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.22104383	1.22104394 ± 6.10E-05	✓
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.31493926	0.31493926 ± 1.53E-05	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.31493926	0.31493926 ± 1.53E-05	<b>✓</b>

Test Step 1.7 (Repeat Count = 1)			✓
Name	Input Value		
k_AsstFWFWActiveLPF_Hz_f32	0.10000001		
k_AsstFWFiltKn_Hz_f32	0.10000001		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00062871	1.00062859 ± 6.10E-05	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	<b>✓</b>

Test Step 1.8 (Repeat Count = 1)			✓
Name	Input Value		
k_AsstFWFWActiveLPF_Hz_f32	100		
k_AsstFWFiltKn_Hz_f32	100		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	✓
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	2.09537983	2.09537959 ± 6.10E-05	✓
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	✓
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	✓

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 Project
 AssistFirewall

 Module
 AssistFireWall

 Test Object
 AssistFirewall\_Per1

#### Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
<b>Decision Coverage</b>	100 %
Branch (C1) Coverage	100 %
MCC Coverage	100 %
MC/DC Coverage	100 %

#### **Statistics**

Total Testcases	3
Successful	3
Failed	0
Not Executed	0

#### **Module Properties**

Project Root Directory	D:\Synergy_Work_Area\AssistFirewall
Configuration File	D:\Synergy_Work_Area\AssistFirewall\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	\$(PROJECTROOT)\src\Ap_AssistFirewall.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -DBC_ASSISTFIREWALL_FAULTINJECTIONPOINT=STD_OFF -I\$(PROJECTROOT)\utp\contract \Ap_AssistFirewall -I\$(PROJECTROOT)\utp\contract -I\$(PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include -I\$ (Compiler Install Path)\underlinclude
File	\$(PROJECTROOT)\NxtrLib\src\interpolation.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -DBC_ASSISTFIREWALL_FAULTINJECTIONPOINT=STD_OFF -I\$(PROJECTROOT)\utp\contract \Ap_AssistFirewall -I\$(PROJECTROOT)\utp\contract -I\$(PROJECTROOT)\NxtrLib\include -I\$(PROJECTROOT)\StdDef\include -I\$ (Compiler Install Path)\underlighted

Name	Text
Module 'AssistFireWall'	Name of Tester:Ankita Bhardwaj Code File(s) Under Test:Ap_AssistFirewall.c Code File(s) Version:14 Module Design Document:Assist_Firewall_MDD.docx Module Design Document:Version:14 Data Dictionary Version:16 Unit Test Plan Version:11 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.31 Total FLASH Used (Bytes):1568 Total RAM Used (Bytes):79 Total CALS Used (Bytes):79 Total CALS Used (Bytes):480 Special Test Requirements: Test Date:03-23-2015 Comments:"NOTE:1) Inline functions defined in GlobalMacro.h are not Unit Tested. 2)""CBD_Sandbox_dbg.map" map file is embedded for reference. 3) In ""AssistFirewall_Per1"" function, ""Defeat_AsstTbl_Service_Cnt_Jgc" always kept FALSE to make ""if((DefeatAsstTblSvc_Cnt_T_lgc <> D_FALSE_CNT_LGC) And (MECCounter_Cnt_T_enum <> ProductionMode))"" condition FALSE except Boundray Test for variables used in Condition and Path coverage.  "
	***************************************

Attributes	
Name	Value
Compiler Install Path	\$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9

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Attributes		
Name	Value	
InitObjDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\obj	
InitSrcDir	\$(PROJECTROOT)\UnitTestEnv\static_build_files\src	
Linker File	\$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd	
Makefile Template	\$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570.tpl	
Target Install Path	\$(ProgramFiles)\pls\UDE 3.2	
Time Unit	Cycles	
Timer Enabled	false	
Timer Prescale	0	
Timer Resolution	1	
UDE Config File	\$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg	
Workspace File	D:\Synergy_Work_Area\AssistFirewall\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP	



#### **Test Case 1: Metrics Test**

Specification

Performance Metrics (With "None" Instrumentation and WithPS Environment)
CPU Cycles:

TC1.1 6628.00 Cycles TC1.2 6630.00 Cycles

#### Description Vector description

TS1.1Shortest Execution Path:((HysteresisComp\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitHysComp\_MtrNm\_f32))=True && ((HighFreqAssist\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitHFA\_MtrNm\_f32))=True && ((BaseAssistCmd\_MtrNm\_T\_f32)<=(-k\_AsstFWInpLimitBaseAsst\_MtrNm\_f32))=True && ((DefeatAsstTblSvc\_Cnt\_T\_lgc != D\_FALSE\_CNT\_LGC) && (MECCounter\_Cnt\_T\_enum != ProductionMode))=True TS1.2"Longest Execution Path:""((HysteresisComp\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitHysComp\_MtrNm\_f32))=False && 1S1.2\*Longest Execution Path: "(inysteresisComp\_withini\_i\_i3z)>=(k\_AsstrWinpLimithysComp\_MtrNm\_T\_f32)>=raise && ((HysteresisComp\_MtrNm\_T\_f32)<=(-k\_AsstrWinpLimitHysComp\_MtrNm\_f32))=False && ((HighFreqAssist\_MtrNm\_T\_f32)>=(-k\_AsstrWinpLimitHFA\_MtrNm\_f32))=False && ((HighFreqAssist\_MtrNm\_f32))=False && ((BaseAssistCmd\_MtrNm\_T\_f32)>=(k\_AsstrWinpLimitBaseAsst\_MtrNm\_f32))=False && ((BaseAssistCmd\_MtrNm\_T\_f32)>=(-k\_AsstrWinpLimitBaseAsst\_MtrNm\_f32))=True && ((DefeatAsstTblSvc\_Cnt\_T\_lgc!=

D\_FALSE\_CNT\_LGC) && (MECCounter\_Cnt\_T\_enum != ProductionMode)) =False && ((LowFreqInput\_MtrNm\_T\_f32)>=( UprBoundFilt\_MtrNm\_T\_f32))=False && ((LowFreqInput\_MtrNm\_T\_f32))=False && DefItAsst\_MtrNm\_T\_f32 = DefItAsstLookup\_MtrNm\_T\_f32 \*

(AsstFWActive\_Uls\_T\_f32>1)=False && (AsstFWActive\_Uls\_T\_f32<=0)=True

((float32)Sign\_f32\_m(HwTorque\_HwNm\_T\_f32))=True && ( (LowFreqInput\_MtrNm\_T\_f32 < LwrBoundFilt\_MtrNm\_T\_f32) || (LowFreqInput\_MtrNm\_T\_f32 > UprBoundFilt\_MtrNm\_T\_f32) )=False && ((AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16)<((AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16)>((AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16)>((AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16)</a> (AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16 >= t\_AssitFWPstepNStepThresh\_Cnt\_u16[1])=False && (AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16 >= t\_AssitFWPstepNStepThresh\_Cnt\_u16[1])=False && (AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16 >= t\_AssitFWPstepNStepThresh\_Cnt\_u16[0])=True && (((Abs\_132\_m(SumInput\_MtrNm\_T\_132 - AssistFirewall\_CombAsstSV\_MtrNm\_M\_132) > k\_RestoreThresh\_MtrNm\_132) && (AssistFirewall\_AsstReducedPerfSV\_Cnt\_M\_lgc == TRUE)) || (TRUE == AssistFirewall\_PNCountStatus\_Cnt\_M\_lgc))=False && (AssistFirewall\_CombAsstSV\_MtrNm\_M\_132>8.8)=False && (AssistFirewall\_Comb

Name         Input Value           AssistFirewall_ActiveKSV_M_str.SV_Uls_f32         -5.30000019           AssistFirewall_ActiveKSV_M_str.K_Uls_f32         0.40000006           AssistFirewall_ActiveRawAcc_Cnt_M_u16         8487           AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc         1           AssistFirewall_CombAsstSV_MtrNm_M_f32         8.80000019           AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32         -5.19999981           AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32         0.0799999982           AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32         1.11199999           AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32         -5.30000019           AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32         0.119999997           AssistFirewall_PNCountStatus_Cnt_M_lgc         1           AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32         5.0999999	
AssistFirewall_ActiveKSV_M_str.K_Uls_f32       0.400000006         AssistFirewall_ActiveRawAcc_Cnt_M_u16       8487         AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc       1         AssistFirewall_CombAsstSV_MtrNm_M_f32       8.80000019         AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32       -5.19999981         AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32       0.0799999982         AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32       1.11199999         AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32       -5.30000019         AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32       0.119999997         AssistFirewall_PNCountStatus_Cnt_M_lgc       1         AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32       5.0999999	
AssistFirewall_ActiveRawAcc_Cnt_M_u16       8487         AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc       1         AssistFirewall_CombAsstSV_MtrNm_M_f32       8.80000019         AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32       -5.19999981         AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32       0.0799999982         AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32       1.11199999         AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32       -5.3000019         AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32       0.119999997         AssistFirewall_PNCountStatus_Cnt_M_lgc       1         AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32       5.0999999	
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc       1         AssistFirewall_CombAsstSV_MtrNm_M_f32       8.80000019         AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32       -5.19999981         AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32       0.0799999982         AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32       1.11199999         AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32       -5.3000019         AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32       0.119999997         AssistFirewall_PNCountStatus_Cnt_M_lgc       1         AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32       5.0999999	
AssistFirewall_CombAsstSV_MtrNm_M_f32       8.8000019         AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32       -5.19999981         AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32       0.0799999982         AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32       1.11199999         AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32       -5.3000019         AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32       0.119999997         AssistFirewall_PNCountStatus_Cnt_M_lgc       1         AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32       5.0999999	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32       -5.1999981         AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32       0.0799999982         AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32       1.11199999         AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32       -5.3000019         AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32       0.119999997         AssistFirewall_PNCountStatus_Cnt_M_lgc       1         AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32       5.0999999	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32       0.0799999982         AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32       1.11199999         AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32       -5.3000019         AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32       0.119999997         AssistFirewall_PNCountStatus_Cnt_M_lgc       1         AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32       5.0999999	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32       1.11199999         AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32       -5.3000019         AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32       0.119999997         AssistFirewall_PNCountStatus_Cnt_M_lgc       1         AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32       5.0999999	
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32       -5.30000019         AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32       0.119999997         AssistFirewall_PNCountStatus_Cnt_M_lgc       1         AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32       5.0999999	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32 0.119999997  AssistFirewall_PNCountStatus_Cnt_M_lgc 1  AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 5.0999999	
AssistFirewall_PNCountStatus_Cnt_M_lgc 1 AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 5.0999999	
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32 5.0999999	
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32 0.219999999	
Rte_Inst_Ap_AssistFirewall tgt_Rte_Inst_Ap_AssistFirewall	
k_AsstFWInpLimitBaseAsst_MtrNm_f32 4.80000019	
k_AsstFWInpLimitHFA_MtrNm_f32 6.40999985	
k_AsstFWInpLimitHysComp_MtrNm_f32 6.71000004	
k_AsstFWNstep_Cnt_u16 4052	
k_AsstFWPstep_Cnt_u16 2460	
k_RestoreThresh_MtrNm_f32 4.42999983	
t2_AsstFWUprBoundX_HwNm_s4p11[0][0] -14336	
t2_AsstFWUprBoundX_HwNm_s4p11[0][1] -12288	
12_AsstFWUprBoundX_HwNm_s4p11[0][2] -10240	
t2_AsstFWUprBoundX_HwNm_s4p11[0][3] -8192	
12_AsstFWUprBoundX_HwNm_s4p11[0][4] -6144	
12_AsstFWUprBoundX_HwNm_s4p11[0][5] -4096	
12_AsstFWUprBoundX_HwNm_s4p11[0][6] -2048	
12_AsstFWUprBoundX_HwNm_s4p11[0][7] 0	
t2_AsstFWUprBoundX_HwNm_s4p11[0][8] 2048	
12_AsstFWUprBoundX_HwNm_s4p11[0][9] 4096	
12_AsstFWUprBoundX_HwNm_s4p11[0][10] 6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][0] -10240	
12_AsstFWUprBoundX_HwNm_s4p11[1][1] -8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][2] -6144	
12_AsstFWUprBoundX_HwNm_s4p11[1][3] -4096	
12_AsstFWUprBoundX_HwNm_s4p11[1][4] -2048	
12_AsstFWUprBoundX_HwNm_s4p11[1][5] 0	
t2_AsstFWUprBoundX_HwNm_s4p11[1][6] 2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7] 4096	
12_AsstFWUprBoundX_HwNm_s4p11[1][8] 6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][9] 8192	
12_AsstFWUprBoundX_HwNm_s4p11[1][10] 10240	
t2_AsstFWUprBoundX_HwNm_s4p11[2][0] -2048	

0

 $t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][1]$ 

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
12_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
:2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
:2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
t2_Asst WopiBoundY_MtrNm_s4p11[4][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192

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AssistFirewall Per1 Input Value t2 AsstFWUprBoundY MtrNm s4p11[7][5] -6144 -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][6] t2 AsstFWUprBoundY MtrNm s4p11[7][7] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][8] t2 AsstFWUprBoundY MtrNm s4p11[7][9] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][10] 4096 t AsstFWDefltAssistX HwNm u8p8[0] 947 t\_AsstFWDefltAssistX\_HwNm\_u8p8[1] 973 t\_AsstFWDefltAssistX\_HwNm\_u8p8[2] 998 t\_AsstFWDefltAssistX\_HwNm\_u8p8[3] 1024 t\_AsstFWDefltAssistX\_HwNm\_u8p8[4] 1050 t\_AsstFWDefltAssistX\_HwNm\_u8p8[5] 1075 t\_AsstFWDefltAssistX\_HwNm\_u8p8[6] 1101 t AsstFWDefltAssistX\_HwNm\_u8p8[7] 1126 t\_AsstFWDefltAssistX\_HwNm\_u8p8[8] 1152 1178 t\_AsstFWDefltAssistX\_HwNm\_u8p8[9] t\_AsstFWDefltAssistX\_HwNm\_u8p8[10] 1203 t AsstFWDefltAssistX HwNm u8p8[11] 1229 t\_AsstFWDefltAssistX\_HwNm\_u8p8[12] 1254 1280 t AsstFWDefltAssistX HwNm u8p8[13] t\_AsstFWDefltAssistX\_HwNm\_u8p8[14] 1306 t\_AsstFWDefltAssistX\_HwNm\_u8p8[15] 1331 t\_AsstFWDefltAssistX\_HwNm\_u8p8[16] 1357 t\_AsstFWDefltAssistX\_HwNm\_u8p8[17] 1382 t AsstFWDefltAssistX HwNm u8p8[18] 1408 t\_AsstFWDefltAssistX\_HwNm\_u8p8[19] 1434 -205 t AsstFWDefltAssistY MtrNm s4p11[0] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[1] 0 2048 t AsstFWDefltAssistY MtrNm s4p11[2] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[3] 4096 4096 t AsstFWDefltAssistY MtrNm s4p11[4] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[5] 6144 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[6] 6144 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[7] 8192 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[8] 8192 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[9] 10240  $t\_AsstFWDefltAssistY\_MtrNm\_s4p11[10]$ 12288 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[11] 14336 t AsstFWDefltAssistY MtrNm s4p11[12] 16384 t AsstFWDefltAssistY\_MtrNm\_s4p11[13] 18432 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[14] 20480 t AsstFWDefltAssistY MtrNm s4p11[15] 22528 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[16] 24576 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[17] 26624 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[18] 28672 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[19] 30720 t AsstFWPstepNstepThresh Cnt u16[0] 234 t\_AsstFWPstepNstepThresh\_Cnt\_u16[1] 655 t\_AsstFWVehSpd\_Kph\_u9p7[0] 19072 19200 t\_AsstFWVehSpd\_Kph\_u9p7[1] t AsstFWVehSpd\_Kph\_u9p7[2] 19328 t\_AsstFWVehSpd\_Kph\_u9p7[3] 19456 19584 t AsstFWVehSpd Kph u9p7[4] t\_AsstFWVehSpd\_Kph\_u9p7[5] 19712 t AsstFWVehSpd Kph u9p7[6] 19840 t\_AsstFWVehSpd\_Kph\_u9p7[7] 19968 tgt\_AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32.value 7.30000019  $tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lgc.value$ 1 tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32.value 7.19999981 tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32.value -5.4000001 7.0999999 tgt\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32.value tot AssistFirewall Per1 MEC Counter Cnt enum.value tgt\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32.value tgt AssistFirewall Per1 AsstFirewallActive Uls f32 tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32 tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32 tgt\_AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 CombinedAssist MtrNm f32 tot AssistFirewall Per1 CombinedAssist MtrNm f32 tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_It\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Igc

tgt AssistFirewall Per1 HighFregAssist MtrNm f32

tgt\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32

tgt AssistFirewall Per1 MEC Counter Cnt enum

tgt\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32

tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32

tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 HighFregAssist MtrNm f32

 $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$ 

tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum

 $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32$ 

tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HwTorque\_HwNm\_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.30000019	-5.30000019 ± 4.88E-04	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487	8487 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	17.9200001	17.9200001 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-3.35039997	-3.35039997 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019	-5.30000019 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999	5.0999999 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	17.9200001	17.9200001 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x00	0x00	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

- 10/ 10/5 10 10	
Test Step 1.2 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-3.4000001
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4797
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0199999996
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.5
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.60000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00899999961
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.79999995
k_AsstFWInpLimitHFA_MtrNm_f32	3.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	3.29999995
k_AsstFWNstep_Cnt_u16	4551
k_AsstFWPstep_Cnt_u16	2337
k_RestoreThresh_MtrNm_f32	6.9000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3] t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_Asst WopiboundX_1WNm_s4p11[3][7]	14336
t2_Asst WopiounuX_nwin_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_Asst WopioundX_1WMn_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_nwini_s4p11[4][1] t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2] t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2 AsstFWUprBoundX HwNm s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7] t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192 10240

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7] t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8] t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_Asst WopiBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefitAssistX_HwNm_u8p8[0]	282
t_AsstFWDefitAssistX_HwNm_u8p8[1]	307
t_AsstFWDefltAssistX_HwNm_u8p8[2]	333
t_AsstFWDefltAssistX_HwNm_u8p8[3]	358
t_AsstFWDefltAssistX_HwNm_u8p8[4]	384
t_AsstFWDefltAssistX_HwNm_u8p8[5]	410
t_AsstFWDefltAssistX_HwNm_u8p8[6]	435
t_AsstFWDefltAssistX_HwNm_u8p8[7]	461
t_AsstFWDefltAssistX_HwNm_u8p8[8]	486
t_AsstFWDefltAssistX_HwNm_u8p8[9]	512
t_AsstFWDefltAssistX_HwNm_u8p8[10]	538
t_AsstFWDefltAssistX_HwNm_u8p8[11]	563
t_AsstFWDefltAssistX_HwNm_u8p8[12]	589
t_AsstFWDefltAssistX_HwNm_u8p8[13]	614
t_AsstFWDefltAssistX_HwNm_u8p8[14]	640
t_AsstFWDefltAssistX_HwNm_u8p8[15]	666
t_AsstFWDefltAssistX_HwNm_u8p8[16]	691
:_AsstFWDefltAssistX_HwNm_u8p8[17]	717
:_AsstFWDefltAssistX_HwNm_u8p8[18]	742
:_AsstFWDefltAssistX_HwNm_u8p8[19]	768
t_AsstFWDefltAssistY_MtrNm_s4p11[0] t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4096 6144
t_AsstFWDefitAssistY_mtrNm_s4p11[1] t_AsstFWDefitAssistY_MtrNm_s4p11[2]	8192
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	8192
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	8192
:_AsstFWDefitAssistY_MtrNm_s4p11[5]	8192
_AsstFWDefltAssistY_MtrNm_s4p11[6]	8192
_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192
:_AsstFWDefltAssistY_MtrNm_s4p11[8]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	26624
:_AsstFWDefltAssistY_MtrNm_s4p11[17]	28672
:_AsstFWDefltAssistY_MtrNm_s4p11[18]	30720
:_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720
:_AsstFWPstepNstepThresh_Cnt_u16[0]	170
_AsstFWPstepNstepThresh_Cnt_u16[1]	399
:_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
:_AsstFWVehSpd_Kph_u9p7[3]	19456
:_AsstFWVehSpd_Kph_u9p7[4]	19584
_AsstFWVehSpd_Kph_u9p7[5] _AsstFWVehSpd_Kph_u9p7[6]	19712 19840
_AsstFWVehSpd_Kph_u9p7[b] _AsstFWVehSpd_Kph_u9p7[7]	19968
_Assir-vvvenspd_kpr_usp7[/] gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-8.5
gt_AssistFirewall_Per1_baseAssistCmd_withtin_i3z.value gt_AssistFirewall_Per1_befeat_AsstTbl_Service_Cnt_lgc.value	0
gt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002
gt_AssistTirewall_Per1_HwTorque_HwNm_f32.value	-9
gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002
gt_Assisti rewail_rer1_rysteresisComp_withvin_i3z.value gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	77
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt	
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32
Name	Actual Value Expected Value Res

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveRawAcc_Cnt_M_u16	246	246 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	0.400000095	0.400000095 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.08599997	1.08600008 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-6.19999981	-6.19999981 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.90100002	7.90100002 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	0.400000095	0.400000095 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	<b>✓</b>

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

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Test Case 2: Boundary Test

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#### Specification

AssistFirewall Per1

Performance Metrics (With "None" Instrumentation and WithPS Environment) CPU Cycles: CPU Cycles:

TC2.1 6628.00 Cycles
TC2.2 6628.00 Cycles
TC2.3 6629.00 Cycles
TC2.3 6629.00 Cycles
TC2.4 6629.00 Cycles
TC2.5 6629.00 Cycles
TC2.6 6629.00 Cycles
TC2.7 6629.00 Cycles
TC2.8 6629.00 Cycles
TC2.10 6629.00 Cycles
TC2.11 6629.00 Cycles
TC2.11 6629.00 Cycles
TC2.12 6629.00 Cycles
TC2.13 6629.00 Cycles
TC2.14 6629.00 Cycles
TC2.15 6629.00 Cycles
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TC2.106 6629.00 Cycles
TC2.107 6629.00 Cycles
TC2.108 6629.00 Cycles
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TC2.106 6629.00 Cycles
TC2.107 6629.00 Cycles
TC2.108 6629.00 Cycles

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TC2.108 6629.00 Cycles TC2.109 6629.00 Cycles TC2.110 6629.00 Cycles

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TC2.111 6629.00 Cycles
TC2.112 6629.00 Cycles
TC2.113 6629.00 Cycles
TC2.114 6629.00 Cycles
TC2.115 6629.00 Cycles
TC2.116 6629.00 Cycles
TC2.117 6629.00 Cycles
TC2.118 6629.00 Cycles
TC2.118 6629.00 Cycles
TC2.119 6629.00 Cycles





**Description** Vector Description

TS2.1BaseAssistCmd MtrNm f32 = min TS2.2BaseAssistCmd\_MtrNm\_f32 = max TS2.3BaseAssistCmd\_MtrNm\_f32 = zero TS2.4BaseAssistCmd\_MtrNm\_f32 = pos TS2.5BaseAssistCmd\_MtrNm\_f32= neg TS2.6HighFreqAssist\_MtrNm\_f32 = min TS2.7HighFreqAssist\_MtrNm\_f32 = max TS2.8HighFreqAssist\_MtrNm\_f32 = zero TS2.9HighFreqAssist\_MtrNm\_f32 = pos TS2.10HighFreqAssist\_MtrNm\_f32 = neg TS2.11HwTorque\_HwNm\_f32 = min TS2.12HwTorque\_HwNm\_f32 = max TS2.13HwTorque\_HwNm\_f32 = zero TS2.14HwTorque\_HwNm\_f32 = pos TS2.15HwTorque\_HwNm\_f32 = neg TS2.16HysteresisComp\_MtrNm\_f32 = min TS2.17HysteresisComp\_MtrNm\_f32 = max TS2.18HysteresisComp\_MtrNm\_f32 = zero TS2.19HysteresisComp\_MtrNm\_f32 = pos TS2.20HysteresisComp\_MtrNm\_f32 = neg TS2.21VehicleSpeed\_Kph\_f32 = min TS2.22VehicleSpeed\_Kph\_f32 = max TS2.23VehicleSpeed\_Kph\_f32 = mid TS2.24t\_AsstFWVehSpd\_Kph\_u9p7[8] = min TS2.25t\_AsstFWVehSpd\_Kph\_u9p7[8] = max TS2.26t\_AsstFWVehSpd\_Kph\_u9p7[8] = mid TS2.27t2\_AsstFWUprBoundX\_HwNm\_s4p11[11] = min TS2.28t2\_AsstFWUprBoundX\_HwNm\_s4p11[11] = max TS2.28t2\_AsstFWUprBoundX\_HwNm\_s4p11[11] = max
TS2.29t2\_AsstFWUprBoundX\_HwNm\_s4p11[11] = zero
TS2.30t2\_AsstFWUprBoundX\_HwNm\_s4p11[11] = pos
TS2.30t2\_AsstFWUprBoundX\_HwNm\_s4p11[11] = neg
TS2.32t2\_AsstFWUprBoundY\_MtrNm\_s4p11[11] = min
TS2.33t2\_AsstFWUprBoundY\_MtrNm\_s4p11[11] = max
TS2.34t2\_AsstFWUprBoundY\_MtrNm\_s4p11[11] = zero TS2.35t2\_AsstFWUprBoundY\_MtrNm\_s4p11[11] = pos TS2.36t2\_AsstFWUprBoundY\_MtrNm\_s4p11[11] = neg TS2.37AssistFirewall\_UprBoundKSV\_M\_str.SV = min TS2.38AssistFirewall\_UprBoundKSV\_M\_str.SV = max TS2.39AssistFirewall\_UprBoundKSV\_M\_str.SV= zero TS2.40AssistFirewall\_UprBoundKSV\_M\_str.SV.SV = pos TS2.41AssistFirewall\_UprBoundKSV\_M\_str.SV.SV = neg TS2.42AssistFirewall\_UprBoundKSV\_M\_str.K= min TS2.43AssistFirewall\_UprBoundKSV\_M\_str.K= max TS2.44AssistFirewall\_UprBoundKSV\_M\_str.K.K = mid TS2.45AssistFirewall\_LwrBoundKSV\_M\_str.SV= min TS2.46AssistFirewall\_LwrBoundKSV\_M\_str.SV= max TS2.47AssistFirewall\_LwrBoundKSV\_M\_str.SV= zero TS2.48AssistFirewall\_LwrBoundKSV\_M\_str.SV= pos TS2.49AssistFirewall\_LwrBoundKSV\_M\_str.SV = neg TS2.50AssistFirewall\_LwrBoundKSV\_M\_str.K= min TS2.51AssistFirewall\_LwrBoundKSV\_M\_str.K= max TS2.52AssistFirewall\_LwrBoundKSV\_M\_str.K= mid TS2.53AssistFirewall\_ActiveKSV\_M\_str.SV = min TS2.54AssistFirewall\_ActiveKSV\_M\_str.SV = max TS2.55AssistFirewall\_ActiveKSV\_M\_str.SV = zero TS2.56AssistFirewall\_ActiveKSV\_M\_str.SV= pos TS2.57AssistFirewall\_ActiveKSV\_M\_str.SV= neg TS2.58AssistFirewall\_ActiveKSV\_M\_str.K= min TS2.59AssistFirewall\_ActiveKSV\_M\_str.K= max TS2.60AssistFirewall\_ActiveKSV\_M\_str.K= mid
TS2.61AssistFirewall\_HiFreqKSV\_M\_str.LPF.SV = min
TS2.62AssistFirewall\_HiFreqKSV\_M\_str.LPF.SV = max TS2.63AssistFirewall\_HiFreqKSV\_M\_str.LPF.SV= zero TS2.64AssistFirewall\_HiFreqKSV\_M\_str.LPF.SV= pos TS2.65AssistFirewall\_HiFreqKSV\_M\_str.LPF.SV= neg TS2.66AssistFirewall\_HiFreqKSV\_M\_str.LPF.K= min TS2.67AssistFirewall\_HiFreqKSV\_M\_str.LPF.K= max TS2.68AssistFirewall\_HiFreqKSV\_M\_str.LPF.K= mid TS2.69AssistFirewall\_HiFreqKSV\_M\_str.CF = min TS2.70AssistFirewall\_HiFreqKSV\_M\_str.CF = max TS2.71AssistFirewall\_HiFreqKSV\_M\_str.CF=mid TS2.72k\_AsstFWInpLimitHysComp\_MtrNm\_f32 = min TS2.73k\_AsstFWInpLimitHysComp\_MtrNm\_f32 = max TS2.74k\_AsstFWInpLimitHysComp\_MtrNm\_f32 = mid TS2.75k\_AsstFWInpLimitHFA\_MtrNm\_f32 = mid TS2.75k\_AsstFWInpLimitHFA\_MtrNm\_f32 = max TS2.77k\_AsstFWInpLimitHFA\_MtrNm\_f32 = mid TS2.78k\_AsstFWInpLimitBaseAsst\_MtrNm\_f32 = min TS2.79k\_AsstFWInpLimitBaseAsst\_MtrNm\_f32 = max TS2.80k\_AsstFWInpLimitBaseAsst\_MtrNm\_f32 = mid TS2.81AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16 = min TS2.82AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16= max TS2.83AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16 = mid TS2.84t\_AsstFWPstepNstepThresh\_Cnt\_u16[2] = min TS2.85t\_AsstFWPstepNstepThresh\_Cnt\_u16[2] = max TS2.86t\_AsstFWPstepNstepThresh\_Cnt\_u16[2] =mid TS2.87k\_AsstFWPstep\_Cnt\_u16 = min TS2.88k\_AsstFWPstep\_Cnt\_u16 = max TS2.88K\_AsstFWPstep\_Cnt\_u16 = max
TS2.89k\_AsstFWPstep\_Cnt\_u16 = mid
TS2.90k\_AsstFWNstep\_Cnt\_u16 = min
TS2.91k\_AsstFWNstep\_Cnt\_u16 = max
TS2.92k\_AsstFWNstep\_Cnt\_u16 = mid
TS2.93AssistFirewall\_PNCountStatus\_Cnt\_M\_lgc = FASLE
TS2.94AssistFirewall\_PNCountStatus\_Cnt\_M\_lgc = TRUE



TS2.95AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32 = min
TS2.96AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32 = max
TS2.97AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32 = pos
TS2.98AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32 = pos
TS2.99AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32 = neg
TS2.100AssistFirewall\_AsstReducedPerfSV\_Cnt\_M\_lgc = FALSE
TS2.101AssistFirewall\_AsstReducedPerfSV\_Cnt\_M\_lgc = FALSE
TS2.101AssistFirewall\_AsstReducedPerfSV\_Cnt\_M\_lgc = TRUE
TS2.1031\_AsstFWDefitAssistX\_HwNm\_u8p8[20] = min
TS2.1031\_AsstFWDefitAssistX\_HwNm\_u8p8[20] = mid
TS2.1051\_AsstFWDefitAssistY\_MtrNm\_s4p11[20] = min
TS2.1051\_AsstFWDefitAssistY\_MtrNm\_s4p11[20] = max
TS2.1071\_AsstFWDefitAssistY\_MtrNm\_s4p11[20] = pos
TS2.1081\_AsstFWDefitAssistY\_MtrNm\_s4p11[20] = pos
TS2.1091\_AsstFWDefitAssistY\_MtrNm\_s4p11[20] = neg
TS2.110k\_RestoreThresh\_MtrNm\_f32 = min
TS2.111k\_RestoreThresh\_MtrNm\_f32 = min
TS2.111k\_RestoreThresh\_MtrNm\_f32 = mid
TS2.111bMEC\_Counter\_Cnt\_enum==>Max
TS2.115MEC\_Counter\_Cnt\_enum==>Min
TS2.115MIC\_Counter\_Cnt\_enum==>Max
TS2.117MEC\_Counter\_Cnt\_enum==>Pos
TS2.119All min
TS2.119All Max

Test Step 2.1 (Repeat Count = 1)	Innut Maline
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.099999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.090000036
AssistFirewall_ActiveRawAcc_Cnt_M_u16	109
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.89999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0700000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0099999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
c_AsstFWInpLimitBaseAsst_MtrNm_f32	4
c_AsstFWInpLimitHFA_MtrNm_f32	2.5
k_AsstFWInpLimitHysComp_MtrNm_f32	3.78999996
k_AsstFWNstep_Cnt_u16	3928
<_AsstFWPstep_Cnt_u16	1107
k_RestoreThresh_MtrNm_f32	1.89999998
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
2 AsstFWUprBoundX HwNm s4p11[1][9]	10240
:2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
z_AsstFWUprBoundX_HwNm_s4p11[2][1] 2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
:z_AsstFWUprBoundX_HwNm_s4p11[z][z] :2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[2][3] 2_AsstFWUprBoundX_HwNm_s4p11[2][4]	
	-8192 
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048

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Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[5][0] 2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14330
	-12288
2_AsstFWUprBoundX_HwNm_s4p11[5][2] 2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288
2 AsstFWUprBoundX HwNm s4p11[7][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
z_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-30720
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
	1 to the contract of the contr
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240

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AssistFirewall Per1 Input Value t2 AsstFWUprBoundY MtrNm s4p11[1][6] 14336 16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][7] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][8] 18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][9] 20480 t2 AsstFWUprBoundY MtrNm s4p11[1][10] 22528 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][0] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][1] 2048  $t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][2]$ 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][3] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][4] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][5] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][6] 12288 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][7] t2 AsstFWUprBoundY MtrNm\_s4p11[2][8] 16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][9] 18432 20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][10] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][0] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][1] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][2] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][3] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][4] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][5] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][6] 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][7] 16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][8] 18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][9] 20480 22528 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][10] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][0] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][1] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][2] 2048 4096 t2 AsstFWUprBoundY MtrNm s4p11[4][3] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][4] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][5] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][6] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][7] 12288 t2 AsstFWUprBoundY MtrNm s4p11[4][8] 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][9] 16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][10] 18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][0] -30720 t2 AsstFWUprBoundY MtrNm s4p11[5][1] -28672 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][2] -26624 t2 AsstFWUprBoundY MtrNm s4p11[5][3] -24576 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][4] -22528 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][5] -20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][6] -18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][7] -16384 -14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][8] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][9] -12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][10] -10240 -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][0] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][1] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][2] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][3] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][4] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][5] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][6] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][7] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][8] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][9] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][10] 14336 -14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][0] t2 AsstFWUprBoundY\_MtrNm\_s4p11[7][1] -12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][2] -10240 t2 AsstFWUprBoundY MtrNm s4p11[7][3] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][4] -6144 -4096 t2 AsstFWUprBoundY MtrNm s4p11[7][5] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][6] -2048

2048

4096

6144

26

51

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][7] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][8]

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][9]

t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][10]

t\_AsstFWDefltAssistX\_HwNm\_u8p8[0]

t\_AsstFWDefltAssistX\_HwNm\_u8p8[1]

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710010ti 110Wali_1 011			1 - 1 - 1 - 1 - 1 - 1
Name	Input Value		
t_AsstFWDefltAssistX_HwNm_u8p8[2]	77		
t_AsstFWDefltAssistX_HwNm_u8p8[3]	102		
t_AsstFWDefltAssistX_HwNm_u8p8[4]	128		
t_AsstFWDefltAssistX_HwNm_u8p8[5]	154		
t_AsstFWDefltAssistX_HwNm_u8p8[6]	179		
t_AsstFWDefltAssistX_HwNm_u8p8[7]	205		
t_AsstFWDefltAssistX_HwNm_u8p8[8]	230		
t_AsstFWDefltAssistX_HwNm_u8p8[9]	256		
t_AsstFWDefltAssistX_HwNm_u8p8[10]	282		
t_AsstFWDefltAssistX_HwNm_u8p8[11] t AsstFWDefltAssistX HwNm u8p8[12]	307 333		
t AsstFWDefitAssistX HwNm u8p8[13]	358		
t_AsstFWDefitAssistX_HwNm_u8p8[14]	384		
t_AsstFWDefitAssistX_HwNm_u8p8[15]	410		
t_AsstFWDefltAssistX_HwNm_u8p8[16]	435		
t_AsstFWDefltAssistX_HwNm_u8p8[17]	461		
t_AsstFWDefltAssistX_HwNm_u8p8[18]	486		
t_AsstFWDefltAssistX_HwNm_u8p8[19]	512		
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-205		
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	-184		
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	-164		
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	-143		
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	-123		
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	-102		
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	-82		
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	-61		
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	-41		
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	-20		
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	0		
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	20		
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	41		
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	61		
t_AsstFWDefitAssistY_MtrNm_s4p11[14]	82		
t_AsstFWDefltAssistY_MtrNm_s4p11[15] t_AsstFWDefltAssistY_MtrNm_s4p11[16]	102 123		
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	143		
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	164		
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	184		
t_AsstFWPstepNstepThresh_Cnt_u16[0]	0		
t_AsstFWPstepNstepThresh_Cnt_u16[1]	0		
t_AsstFWVehSpd_Kph_u9p7[0]	1408		
t_AsstFWVehSpd_Kph_u9p7[1]	1536		
t_AsstFWVehSpd_Kph_u9p7[2]	1664		
t_AsstFWVehSpd_Kph_u9p7[3]	1792		
t_AsstFWVehSpd_Kph_u9p7[4]	1920		
t_AsstFWVehSpd_Kph_u9p7[5]	2048		
t_AsstFWVehSpd_Kph_u9p7[6]	2176		
t_AsstFWVehSpd_Kph_u9p7[7]	2304		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-8.80000019		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	9		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90.1999969	100	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_Mi		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_M		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_			
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mti		
tgt_kte_inst_Ap_AssistFirewall.AssistFirewall_Per1_Hw1orque_Hwnm_ts2 tgt_kte_inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_ tgt_AssistFirewall_Per1_HysteresisComp_M		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph		
Name	Actual Value	Expected Value	Resu
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	2.82099986	2.8210001 ± 4.88E-04	Rest
	0	0 ± 1	
AssistFirewall ActiveRawAcc Cnt M u16		1	
AssistFirewall_ActiveRawAcc_Cnt_M_u16 AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1		
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1 0.08984375		
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall_CombAsstSV_MtrNm_M_f32	0.08984375	0.08984375 ± 4.88E-04	
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc			
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall_CombAsstSV_MtrNm_M_f32 AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	0.08984375 1.9920001	0.08984375 ± 4.88E-04 1.99199998 ± 4.88E-04	

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Name	Actual Value	Expected Value	Result
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	0.08984375	0.08984375 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	✓
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Name	Input Value
AssistFirewall ActiveKSV M str.SV UIs f32	4
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0199999996
AssistFirewall_ActiveRawAcc_Cnt_M_u16	200
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.13
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0099999978
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.20000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
ssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00899999961
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
ssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2
ssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00300000003
tte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
_AsstFWInpLimitBaseAsst_MtrNm_f32	2.20000005
_AsstFWInpLimitHFA_MtrNm_f32	1.20000005
_AsstFWInpLimitHysComp_MtrNm_f32	3
_AsstFWNstep_Cnt_u16	4796
_AsstFWPstep_Cnt_u16	246
_RestoreThresh_MtrNm_f32	1.20000005
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
P_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
2 AsstFWUprBoundX HwNm s4p11[1][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288
z_AsstFWUprBoundX_HwNm_s4p11[z][1] 2 AsstFWUprBoundX HwNm s4p11[2][2]	
	-10240
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192 C444
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][7] 2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0 2048

AssistFirewall\_Per1

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DASSENDATIONS AND MART SEPTING   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   1938   19	Name	Input Value
Paper   Pape		•
D. AND AMERICAN STATE   1917   1918   2040   2. AND AMERICAN STATE   1918   2. AND AMERICAN		
2. AutoProfit (Bottom 2) (Minhor, 1961)   1939   2253     2. AutoProfit (Bottom 2) (Minhor, 1961)   1179   2253     2. AutoProfit (Bottom 2) (Minhor, 1961)   1179   2043     2. AutoProfit (Bottom 2) (Minhor, 1961)   1171   2044     2. AutoProfit (Bottom 2) (Minhor, 1961)   1171   1084     2. AutoProfit (Bottom 2) (Minhor, 1961)   1084     2. AutoProfit (Bottom 2) (Minhor, 1961)   1171   1084     2. AutoProfit (Bottom		
2. Auto-Physician Ministry 1911 1910   2678   2. Auto-Physician Ministry 1911 1910   2649   2. Auto-Physician Ministry 1911 1911   2049   3. Auto-Physician Ministry 1911 191   2049   4. Auto-Physician Ministry 1911 191   2049   5. Auto-Physician Ministry 1911 191   2049   5. Auto-Physician Ministry 1911 191   2049   6. Auto-Physician Ministry 1911 191   2049   6. Auto-Physician Ministry 1911 191   2049   7. Auto-Physician Ministry 1911 191   2049   7. Auto-Physician Ministry 1911 191   2049   7. Auto-Physician Ministry 1911 191   2049   8. Auto-Physician Ministry 1911 191   2049   8. Auto-Physician Ministry 1911 191   2049   8. Auto-Physician Ministry 1911 191   2049   9. Auto-P		
2. ASPAPUR BOACH   MARIN SPITTED   208		
2_AssPrivgbooms   Menn_sep11291   008   2_AssPrivgbooms   Menn_sep11291   014   2_AssPrivgbooms   Menn_sep11291   014   2_AssPrivgbooms   Menn_sep11291   0124   2_AssPrivgbooms   Menn_sep11291   0124   2_AssPrivgbooms   Menn_sep11291   0128   2_AssPrivgbooms   Menn_sep11291   0124   2_AssPrivgbooms   Menn_sep11291   0124   2_AssPrivgbooms   Menn_sep11291   0144   2_AssPrivgbooms   Menn_sep11291   0144		
2_Amer   Martin   M		
2_AssFVUPSOUND Mehrs -951123   9192   2_AssFVUPSOUND Mehrs -951123   9192   2_AssFVUPSOUND Mehrs -951125   9192   2_AssFVUPSOUND Mehrs -951125   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   91226   912		
2.AssPitylipsiand* Mehrs 49110[9]   0140   2.AssPitylipsiand* Mehrs 49110[9]   10240   2.AssPitylipsiand* Mehrs 49110[9]   1238   2.AssPitylipsiand* Mehrs 49110[9]   10344   2.AssPitylipsiand* Mehrs 49110[9]   10344   2.AssPitylipsiand* Mehrs 49110[9]   10344   2.AssPitylipsiand* Mehrs 49110[9]   10342   2.AssPitylipsiand* Mehrs 49110[9]   10422   2.AssPitylipsiand* Mehrs 49110[9]   10422   2.AssPitylipsiand* Mehrs 49110[9]   10424   2.AssPitylipsiand* Mehrs 49110[9]   10444   2.AssPitylipsiand* Meh		
2_AssiPutUpBooms   Mehns   _sel 170191   10208   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   12308   123		
2. ASSFWUKBORDMR   Marks   spir12 35   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   122888   122888   122888   122888   122888   122888		
2. AssiSVUJpSound* Minhs* sigh10[15]   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388		
2. Ansel*Wijsbeauty   Mehm   apit 100   10   20489   10   10   20489   10   20489   10   20489   10   20489   10   20489   10   20489   10   20489   10   20489   10   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489   20489		
L. ANSEWUNDSCHOOLY JAMEN AS 1911 [10]   22525		
P. ASSEPT/USPGOUNTY   Mehm   a 5411   10   10   10   10   10   10   10		
Z.ASEPWIDFSOURD', Minth', app11(3)		
Z.ASEPWUPDEOUY_JMNTn.sp115 3    10240		
2_AssFWUpFibury   Minth   Sel 11314   1288   2288   2. AssFWUpFibury   Minth   Sel 11314   1288   2. AssFWUpFibury   Minth   Sel 11315   1436   2. AssFWUpFibury   Minth   Sel 11315   1436   2. AssFWUpFibury   Minth   Sel 11315   1436   2. AssFWUpFibury   Minth   Sel 11315   2050   2. AssFWUpFibury   Minth   Sel 11315   2. AssFWUpFibury   Minth   Se		
2. AssEWUpfbount/ Minns 49113[6]   14336   12. AssEWupfbount/ Minns 49113[6]   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384   19384		
2. AssEWVLyDebound*, Minks, sept 15(8)   1942   2. AssEWVLyDebound*, Minks, sept 15(8)   0   24576   2. AssEWVLyDebound*, Minks, sept 15(8)   0   10240   2. AssEWVLyDebound*, Minks, sept 15(8)   0   12286   2. AssEWVLyDebound*, Minks, sept 15(8)   0   12286   2. AssEWVLyDebound*, Minks, sept 15(8)   0   16384   2. AssEWVLyDebound*, Minks, sept 15(8)   0   20400   2. AssEWVLyDebound*, Minks, sept 15(8)   0		
2. AssEW/Upfordow/Y_Minns_sep1130   2. AssEW/Upfordow/Y_Minns_sep1130   2. AssEW/Upfordow/Y_Minns_sep1130   2. AssEW/Upfordow/Y_Minns_sep1130   2. AssEW/Upfordow/Y_Minns_sep1140   2. AssEW/Upfordow/Y_Minns_sep1140   2. AssEW/Upfordow/Y_Minns_sep1140   2. AssEW/Upfordow/Y_Minns_sep1140   3. AssEW/Upfordow/Y_Minns_sep1140   4. AssEW/Upfordow/Y_Minns_se		
2. AssEVVLybbound* Minhs. spot 15  9    2268    2. AssEVNLybbound* Minhs. spot 15  16     2476    2. AssEVNLybbound* Minhs. spot 15  16     2476    2. AssEVNLybbound* Minhs. spot 15  16     2088    2. AssEVNLybbound* Minhs. spot 16  17     4096    2. AssEVNLybbound* Minhs. spot 16  17     4096    2. AssEVNLybbound* Minhs. spot 16  18     4112    2. AssEVNLybbound* Minhs. spot 16  18     4112    2. AssEVNLybbound* Minhs. spot 16  18     4128    2. AssEVNLybbound* Minhs. spot 16  18     4136    2. AssEVNLybbound* Minhs. spot 16  19     2048    2. AssEVNLybbound* Minhs. spot 16  19     4136    2. AssEVNLybbound* Minhs. spot 16  19     4142    2. AssEVNLybbound* Minhs. spot 16  19     4192    2. AssEVNLybbound* Minhs. spot 16  19     4193    2. AssEVNLybbound* Minhs. spot 16  19     4193	t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
2. AssiPVUprideandY_Mehm_sept113(10)	t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
2. AssFWUpGeound*, Mehm., sejot14[0]   0   0   0   0   0   0   0   0   0	t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
Z.ASSF/VIJpRBoundY_Mirkm_sep114  0     2048     Z.ASSF/VIJpRBoundY_Mirkm_sep114  0     2048     Z.ASSF/VIJpRBoundY_Mirkm_sep114  0     4098     Z.ASSF/VIJpRBoundY_Mirkm_sep114  0     4192     Z.ASSF/VIJpRBoundY_Mirkm_sep114  0     4192     Z.ASSF/VIJpRBoundY_Mirkm_sep114  0     4192     Z.ASSF/VIJpRBoundY_Mirkm_sep114  0     4288     Z.ASSF/VIJPRBoundY_Mirkm_sep115  0     4286     Z.ASSF/VIJPRBoundY_Mirkm_sep115  0     4288     Z.ASSF/VIJPRBoundY_Mirkm_sep115  0     4288     Z.ASSF/VIJPRBoundY_Mirkm_sep115  0     4288     Z.ASSF/VIJPRBoundY_Mirkm_sep115  0     44336     Z.ASSF/VIJPRBoundY_Mirkm_sep115  0     44336     Z.ASSF/VIJPRBoundY_Mirkm_sep115  0     4288     Z.ASSF/VIJPRBoundY_Mirkm_sep115  0     4288     Z.ASSF/VIJPRBoundY_Mirkm_sep115  0     4288     Z.ASSF/VIJPRBoundY_Mirkm_sep115  0     4288     Z.ASSF/VIJPRBoundY_Mirkm_sep116  0     4288     Z.ASSF/VIJPRBoundY_Mirkm_s	t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
2. AssFWUpGoundY_Minm_sep11[4]]   298   2. AssFWUpGoundY_Minm_sep11[4]]   406   2. AssFWUpGoundY_Minm_sep11[4]]   5104   2. AssFWUpGoundY_Minm_sep11[4]]   5102   2. AssFWUpGoundY_Minm_sep11[4]]   5102   2. AssFWUpGoundY_Minm_sep11[4]]   10240   2. AssFWUpGoundY_Minm_sep11[4]]   1436   2. AssFWUpGoundY_Minm_sep11[4]]   1436   2. AssFWUpGoundY_Minm_sep11[4]]   1436   2. AssFWUpGoundY_Minm_sep11[4]]   1436   2. AssFWUpGoundY_Minm_sep11[4]]   16384   2. AssFWUpGoundY_Minm_sep11[6]]   2286   2. AssFWUpGoundY_Minm_sep11[6]]   2286   2. AssFWUpGoundY_Minm_sep11[6]]   2286   2. AssFWUpGoundY_Minm_sep11[6]]   2286   2. AssFWUpGoundY_Minm_sep11[6]]   2487   2. AssFWUpGoundY_Minm_sep11[6]]   2488   2. AssFWUpGoundY_Minm_sep11[6]]   3484   3. AssFWUpGoundY_Minm_sep11[6]]   3484   3. AssFWUpGoundY_Minm_sep11[6]]   3	t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576
L. ASSIP/Up/BoundY, Minhm.sep114[4]3         6144           12. ASSIP/Up/BoundY, Minhm.sep114[4]3         6144           12. ASSIP/Up/BoundY, Minhm.sep114[4]3         6144           12. ASSIP/Up/BoundY, Minhm.sep114[4]5         10240           12. ASSIP/Up/BoundY, Minhm.sep114[4]7         4336           12. ASSIP/Up/BoundY, Minhm.sep114[4]8         16384           12. ASSIP/Up/BoundY, Minhm.sep114[4]9         18382           12. ASSIP/Up/BoundY, Minhm.sep116[9]         28672           12. ASSIP/Up/BoundY, Minhm.sep116[9]         28672           12. ASSIP/Up/BoundY, Minhm.sep116[9]         24676           12. ASSIP/Up/BoundY, Minhm.sep116[9]         16334           12. ASSIP/Up/BoundY, Minhm.sep116[9]         16334           12. ASSIP/Up/BoundY, Minhm.sep116[9]         16334           12. ASSIP/Up/BoundY, Minhm.sep116[9]         16334           12. ASSIP/Up/BoundY, Minhm.sep116[9]         10240           12. ASSIP/Up/BoundY, Minhm.sep116[9]         10240           12. ASSIP/Up/BoundY, Minhm.sep116[9]         10240           12.	t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
2_AssFVUpRoundY_Mirkm_sep11[4][4]   8182	t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048
2. AssFYUp/Boundy Minthm_sep11(4) 3	t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
2. AssFVUpRoundY_Mirkm_s4p116  6  6  6  6  6  6  6  6  6  6  6  6		
2. AssFPVUpRBoundY_Minhm_s4p114[6]   2. AssFPVUpRBoundY_Minhm_s4p114[6]   2. AssFPVUpRBoundY_Minhm_s4p114[7]   2. AssFPVUpRBoundY_Minhm_s4p114[7]   2. AssFPVUpRBoundY_Minhm_s4p114[7]   2. AssFPVUpRBoundY_Minhm_s4p114[8]   3. AssFPVUpRBoundY_Minhm_s4p114[7]   2. AssFPVUpRBoundY_Minhm_s4p116[7]   2. AssFPVUpRBoundY_Minhm_s4p116[7]   2. AssFPVUpRBoundY_Minhm_s4p116[7]   2. AssFPVUpRBoundY_Minhm_s4p116[7]   2. AssFPVUpRBoundY_Minhm_s4p116[8]   2. AssFPVUpRBoundY_Minhm_s4p117[8]   2. AssFPVUpRBoundY_Minhm_s4p117[8]   2. AssFPVUpRBoundY_Minhm_s4p117[8]   2. AssFPVUpRBoundY_Minhm_s4p117[8]   2. AssFPVUpRBoundY_Minhm_s4p117[8]   2. AssFP		
2. AssEPVUPBoundY_Minkm_s4p114[8]       12288         2. AssEPVUPBoundY_Minkm_s4p114[8]       16384         12. AssEPVUPBoundY_Minkm_s4p114[8]       16384         2. AssEPVUPBoundY_Minkm_s4p114[8]       18432         2. AssEPVUPBoundY_Minkm_s4p115[9]       20480         2. AssEPVUPBoundY_Minkm_s4p115[9]       -28672         2. AssEPVUPBoundY_Minkm_s4p115[8]       -28664         2. AssEPVUPBoundY_Minkm_s4p115[8]       -28678         2. AssEPVUPBoundY_Minkm_s4p115[8]       -20480         2. AssEPVUPBoundY_Minkm_s4p115[8]       -20480         2. AssEPVUPBoundY_Minkm_s4p115[8]       -18432         2. AssEPVUPBoundY_Minkm_s4p115[8]       -18432         2. AssEPVUPBoundY_Minkm_s4p115[8]       -18436         2. AssEPVUPBoundY_Minkm_s4p115[8]       -12288         2. AssEPVUPBoundY_Minkm_s4p115[9]       -10240         2. AssEPVUPBoundY_Minkm_s4p115[9]       -10240         2. AssEPVUPBoundY_Minkm_s4p115[9]       -10240         2. AssEPVUPBoundY_Minkm_s4p116[9]       -2048         2. AssEPVUPBoundY_Minkm_s4p116[9]       -2048         2. AssEPVUPBoundY_Minkm_s4p116[9]       -004         2. AssEPVUPBoundY_Minkm_s4p116[9]       -004         2. AssEPVUPBoundY_Minkm_s4p116[9]       -004         2. AssEPVUPBoundY_Minkm_s4p116[9]       <		
2. AssFWUprBoundY_MtrNm_s4p114  8    16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384   16384		
2_AssFWUpRoundY_MtrNm_s4p11{  S }   16384    2_AssFWUpRoundY_MtrNm_s4p11{  S }   16432    2_AssFWUpRoundY_MtrNm_s4p11{  S }   20480    2_AssFWUpRoundY_MtrNm_s4p11{  S }   20480    2_AssFWUpRoundY_MtrNm_s4p11{  S }   26624    2_AssFWUpRoundY_MtrNm_s4p11{  S }   26624    2_AssFWUpRoundY_MtrNm_s4p11{  S }   24576    2_AssFWUpRoundY_MtrNm_s4p11{  S }   20480    2_AssFWUpRoundY_MtrNm_s4p11{  S }   20480    2_AssFWUpRoundY_MtrNm_s4p11{  S }   20480    2_AssFWUpRoundY_MtrNm_s4p11{  S }   20480    2_AssFWUpRoundY_MtrNm_s4p11{  S }   14332    2_AssFWUpRoundY_MtrNm_s4p11{  S }   14336    2_AssFWUpRoundY_MtrNm_s4p11{  S }   12888    2_AssFWUpRoundY_MtrNm_s4p11{  S }   1288    2_AssFWUpRoundY_MtrNm_s4p11{  S }   1436    2_AssFWUpRoundY_MtrNm_s4p11{  S }   1438    2_AssFWUpRoundY_MtrNm_s4p11{  S }   1448    2_AssFWUpRoundY_MtrNm_s4p11{  S }   1438    2_AssF		
2. AssFWUpfboundY_MirNm_s4p11[4] 9  18432   2. AssFWUpfboundY_MirNm_s4p11[6] 1   20480   2. AssFWUpfboundY_MirNm_s4p11[6] 1   26664   2. AssFWUpfboundY_MirNm_s4p11[6] 1   26664   2. AssFWUpfboundY_MirNm_s4p11[6] 2   24576   2. AssFWUpfboundY_MirNm_s4p11[6] 3   22528   2. AssFWUpfboundY_MirNm_s4p11[6] 4   20480   2. AssFWUpfboundY_MirNm_s4p11[6] 6   18432   2. AssFWUpfboundY_MirNm_s4p11[6] 6   18432   2. AssFWUpfboundY_MirNm_s4p11[6] 6   16384   2. AssFWUpfboundY_MirNm_s4p11[6] 7   144336   2. AssFWUpfboundY_MirNm_s4p11[6] 9   10240   2. AssFWUpfboundY_MirNm_s4p11[6] 9   10240   2. AssFWUpfboundY_MirNm_s4p11[6] 9   10240   2. AssFWUpfboundY_MirNm_s4p11[6] 9   2048   2. AssFWUpfboundY_MirNm_s4p11[6] 9   3192   2. AssFWUpfboundY_MirNm_s4p11[7] 9   3192   2. AssFWUpfboundY_MirNm_s4p11[7] 9   3192   3. Ass		
2. AssFWUprBoundY_MrNm_s4p11[5][0]   28872     2. AssFWUprBoundY_MrNm_s4p11[5][0]   28672     2. AssFWUprBoundY_MrNm_s4p11[5][1]   26624     2. AssFWUprBoundY_MrNm_s4p11[5][2]   24576     2. AssFWUprBoundY_MrNm_s4p11[5][3]   22528     2. AssFWUprBoundY_MrNm_s4p11[5][3]   20880     2. AssFWUprBoundY_MrNm_s4p11[5][6]   18432     2. AssFWUprBoundY_MrNm_s4p11[5][7]   14336     2. AssFWUprBoundY_MrNm_s4p11[5][7]   14336     2. AssFWUprBoundY_MrNm_s4p11[5][7]   14336     2. AssFWUprBoundY_MrNm_s4p11[5][8]   10240     2. AssFWUprBoundY_MrNm_s4p11[5][9]   10240     2. AssFWUprBoundY_MrNm_s4p11[5][0]   2048     2. AssFWUprBoundY_MrNm_s4p11[6][0]   4336     2. AssFWUprBoundY_MrNm_s4p11[6][0]   4228     2. AssFWUprBoundY_MrNm_s4p11[6][0]   4228     2. AssFWUprBoundY_MrNm_s4p11[6][0]   4228     2. AssFWUprBoundY_MrNm_s4p11[7][0]   4066     2. AssFW		
22 AssIFWUpfboundY_MirNm_s4p11[5][0]   -28672		
2. AsstFWUpfBoundY_MtrNm_s4p116  1    -26624     -24676       -24676		
2. AssIFWUpfBoundY_Mirkm_s4p11[5] 2   -24576     2. AssIFWUpfBoundY_Mirkm_s4p11[5] 3   -22528     2. AssIFWUpfBoundY_Mirkm_s4p11[5] 5   -18432     2. AssIFWUpfBoundY_Mirkm_s4p11[5] 5   -18432     2. AssIFWUpfBoundY_Mirkm_s4p11[5] 6   -16384     2. AssIFWUpfBoundY_Mirkm_s4p11[5] 6   -16384     2. AssIFWUpfBoundY_Mirkm_s4p11[5] 8   -12288     2. AssIFWUpfBoundY_Mirkm_s4p11[5] 9   -10240     2. AssIFWUpfBoundY_Mirkm_s4p11[6] 0   -2048     2. AssIFWUpfBoundY_Mirkm_s4p11[6] 0   -2048     2. AssIFWUpfBoundY_Mirkm_s4p11[6] 1   0     2. AssIFWUpfBoundY_Mirkm_s4p11[6] 1   0     2. AssIFWUpfBoundY_Mirkm_s4p11[6] 2   2048     2. AssIFWUpfBoundY_Mirkm_s4p11[6] 3   4096     2. AssIFWUpfBoundY_Mirkm_s4p11[6] 6   6144     2. AssIFWUpfBoundY_Mirkm_s4p11[6] 6   10240     2. AssIFWUpfBoundY_Mirkm_s4p11[6] 7   12288     2. AssIFWUpfBoundY_Mirkm_s4p11[6] 9   16384     2. AssIFWUpfBoundY_Mirkm_s4p11[6] 9   16384     2. AssIFWUpfBoundY_Mirkm_s4p11[6] 9   16384     2. AssIFWUpfBoundY_Mirkm_s4p11[6] 9   16384     2. AssIFWUpfBoundY_Mirkm_s4p11[7] 1   -10240     2. AssIFWUpfBoundY_Mirkm_s4p11[7] 2   -10240     2. AssIFWUpfBoundY_Mirkm_s4p11[7] 2   -10240     2. AssIFWUpfBoundY_Mirkm_s4p11[7] 2   -10240     2. AssIFWUpfBoundY_Mirkm_s4p11[7] 3   -10240     2. AssIFWUpfBoundY_Mirkm_s4p11[7] 3   -10240     2. AssIFWUpfBoundY_Mirkm_s4p11[7] 5   -2048     2. AssIFWUpfBoundY_Mirkm_s4p11[7] 6   0     2. AssIFWUpfBoundY_Mirkm_s4p11[7] 6   0     2. AssIFWUpfBoundY_Mirkm_s4p11[7] 9   -10240     2. AssIFWUpfBoundY_Mirkm_s4p11[7] 9   -10240     2. AssIFWUpfBoundY_Mirkm_s		
P. AssFWUpfBoundY_MtrNm_s4p11[6][3]   -2268     P. AssFWUpfBoundY_MtrNm_s4p11[6][4]   -20480     P. AssFWUpfBoundY_MtrNm_s4p11[6][5]   -18432     P. AssFWUpfBoundY_MtrNm_s4p11[6][6]   -18432     P. AssFWUpfBoundY_MtrNm_s4p11[6][7]   -14336     P. AssFWUpfBoundY_MtrNm_s4p11[6][7]   -14336     P. AssFWUpfBoundY_MtrNm_s4p11[6][8]   -12288     P. AssFWUpfBoundY_MtrNm_s4p11[6][9]   -10240     P. AssFWUpfBoundY_MtrNm_s4p11[6][1]   -2048     P. AssFWUpfBoundY_MtrNm_s4p11[6][1]   -2048     P. AssFWUpfBoundY_MtrNm_s4p11[6][1]   -2048     P. AssFWUpfBoundY_MtrNm_s4p11[6][2]   -2048     P. AssFWUpfBoundY_MtrNm_s4p11[6][3]   -4096     P. AssFWUpfBoundY_MtrNm_s4p11[6][4]   -4144     P. AssFWUpfBoundY_MtrNm_s4p11[6][5]   -4049     P. AssFWUpfBoundY_MtrNm_s4p11[6][6]   -40240     P. AssFWUpfBoundY_MtrNm_s4p11[6][6]   -40240     P. AssFWUpfBoundY_MtrNm_s4p11[6][6]   -40240     P. AssFWUpfBoundY_MtrNm_s4p11[6][6]   -40240     P. AssFWUpfBoundY_MtrNm_s4p11[7][6]   -40240     P.		
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t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]		
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 10640		
12		
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]       -8192         t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]       0         t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]       2048         t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]       4096         t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]       6144         t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]       8192         t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]       10240         t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]       12288         t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]       14336         t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]       16384         t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]       18432         t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]       -12288         t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]       -10240         t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]       -10240         t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]       -8192         t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]       -4096         t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]       0         t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]       0         t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]       0         t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]       0         t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]       0         t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]       0         t2_AsstFWUprBoundY_	t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-12288
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t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
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t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 10240 t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 12288 t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 14336 t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 16384 t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 18432 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] -12288 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] -10240 t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] -8192 t2_AsstFWUprBoundY_MtrNm_s4p11[7][3] -6144 t2_AsstFWUprBoundY_MtrNm_s4p11[7][4] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][5] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] 6144	t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
12_AsstFWUprBoundY_MtrNm_s4p11[6][7]       12288         12_AsstFWUprBoundY_MtrNm_s4p11[6][8]       14336         12_AsstFWUprBoundY_MtrNm_s4p11[6][9]       16384         12_AsstFWUprBoundY_MtrNm_s4p11[6][10]       18432         12_AsstFWUprBoundY_MtrNm_s4p11[7][0]       -12288         12_AsstFWUprBoundY_MtrNm_s4p11[7][1]       -10240         12_AsstFWUprBoundY_MtrNm_s4p11[7][2]       -8192         12_AsstFWUprBoundY_MtrNm_s4p11[7][3]       -6144         12_AsstFWUprBoundY_MtrNm_s4p11[7][4]       -4096         12_AsstFWUprBoundY_MtrNm_s4p11[7][6]       0         12_AsstFWUprBoundY_MtrNm_s4p11[7][6]       0         12_AsstFWUprBoundY_MtrNm_s4p11[7][8]       4096         12_AsstFWUprBoundY_MtrNm_s4p11[7][8]       4096         12_AsstFWUprBoundY_MtrNm_s4p11[7][9]       6144         12_AsstFWUprBoundY_MtrNm_s4p11[7][9]       6144         12_AsstFWUprBoundY_MtrNm_s4p11[7][9]       6144         12_AsstFWUprBoundY_MtrNm_s4p11[7][0]       8192		10240
12_AsstFWUprBoundY_MtrNm_s4p11[6][8]       14336         12_AsstFWUprBoundY_MtrNm_s4p11[6][9]       16384         12_AsstFWUprBoundY_MtrNm_s4p11[6][10]       18432         12_AsstFWUprBoundY_MtrNm_s4p11[7][0]       -12288         12_AsstFWUprBoundY_MtrNm_s4p11[7][1]       -10240         12_AsstFWUprBoundY_MtrNm_s4p11[7][2]       -8192         12_AsstFWUprBoundY_MtrNm_s4p11[7][3]       -6144         12_AsstFWUprBoundY_MtrNm_s4p11[7][4]       -4096         12_AsstFWUprBoundY_MtrNm_s4p11[7][5]       -2048         12_AsstFWUprBoundY_MtrNm_s4p11[7][6]       0         12_AsstFWUprBoundY_MtrNm_s4p11[7][7]       2048         12_AsstFWUprBoundY_MtrNm_s4p11[7][8]       4096         12_AsstFWUprBoundY_MtrNm_s4p11[7][8]       4096         12_AsstFWUprBoundY_MtrNm_s4p11[7][9]       6144         12_AsstFWUprBoundY_MtrNm_s4p11[7][9]       6144         12_AsstFWUprBoundY_MtrNm_s4p11[7][0]       8192		
12_AsstFWUprBoundY_MtrNm_s4p11[6][9] 16384 12_AsstFWUprBoundY_MtrNm_s4p11[6][10] 18432 12_AsstFWUprBoundY_MtrNm_s4p11[7][0] -12288 12_AsstFWUprBoundY_MtrNm_s4p11[7][1] -10240 12_AsstFWUprBoundY_MtrNm_s4p11[7][2] -8192 12_AsstFWUprBoundY_MtrNm_s4p11[7][3] -6144 12_AsstFWUprBoundY_MtrNm_s4p11[7][4] -4096 12_AsstFWUprBoundY_MtrNm_s4p11[7][5] -2048 12_AsstFWUprBoundY_MtrNm_s4p11[7][6] 0 12_AsstFWUprBoundY_MtrNm_s4p11[7][7] 2048 12_AsstFWUprBoundY_MtrNm_s4p11[7][8] 4096 12_AsstFWUprBoundY_MtrNm_s4p11[7][8] 4096 12_AsstFWUprBoundY_MtrNm_s4p11[7][8] 4096 12_AsstFWUprBoundY_MtrNm_s4p11[7][9] 6144 12_AsstFWUprBoundY_MtrNm_s4p11[7][9] 6144 12_AsstFWUprBoundY_MtrNm_s4p11[7][0] 8192		
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]       18432         t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]       -12288         t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]       -10240         t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]       -8192         t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]       -6144         t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]       -4096         t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]       -2048         t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]       0         t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]       2048         t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]       4096         t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]       6144         t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]       6144         t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]       8192		
12_AsstFWUprBoundY_MtrNm_s4p11[7][0]       -12288         12_AsstFWUprBoundY_MtrNm_s4p11[7][1]       -10240         12_AsstFWUprBoundY_MtrNm_s4p11[7][2]       -8192         12_AsstFWUprBoundY_MtrNm_s4p11[7][3]       -6144         12_AsstFWUprBoundY_MtrNm_s4p11[7][4]       -4096         12_AsstFWUprBoundY_MtrNm_s4p11[7][5]       -2048         12_AsstFWUprBoundY_MtrNm_s4p11[7][6]       0         12_AsstFWUprBoundY_MtrNm_s4p11[7][7]       2048         12_AsstFWUprBoundY_MtrNm_s4p11[7][8]       4096         12_AsstFWUprBoundY_MtrNm_s4p11[7][9]       6144         12_AsstFWUprBoundY_MtrNm_s4p11[7][0]       8192		
12_AsstFWUprBoundY_MtrNm_s4p11[7][1] -10240 12_AsstFWUprBoundY_MtrNm_s4p11[7][2] -8192 12_AsstFWUprBoundY_MtrNm_s4p11[7][3] -6144 12_AsstFWUprBoundY_MtrNm_s4p11[7][4] -4096 12_AsstFWUprBoundY_MtrNm_s4p11[7][5] -2048 12_AsstFWUprBoundY_MtrNm_s4p11[7][6] 0 12_AsstFWUprBoundY_MtrNm_s4p11[7][7] 2048 12_AsstFWUprBoundY_MtrNm_s4p11[7][8] 4096 12_AsstFWUprBoundY_MtrNm_s4p11[7][9] 6144 12_AsstFWUprBoundY_MtrNm_s4p11[7][0] 8192		
12_AsstFWUprBoundY_MtrNm_s4p11[7][2]       -8192         12_AsstFWUprBoundY_MtrNm_s4p11[7][3]       -6144         12_AsstFWUprBoundY_MtrNm_s4p11[7][4]       -4096         12_AsstFWUprBoundY_MtrNm_s4p11[7][5]       -2048         12_AsstFWUprBoundY_MtrNm_s4p11[7][6]       0         12_AsstFWUprBoundY_MtrNm_s4p11[7][7]       2048         12_AsstFWUprBoundY_MtrNm_s4p11[7][8]       4096         12_AsstFWUprBoundY_MtrNm_s4p11[7][9]       6144         12_AsstFWUprBoundY_MtrNm_s4p11[7][10]       8192		
12_AsstFWUprBoundY_MtrNm_s4p11[7][3]       -6144         12_AsstFWUprBoundY_MtrNm_s4p11[7][4]       -4096         12_AsstFWUprBoundY_MtrNm_s4p11[7][5]       -2048         12_AsstFWUprBoundY_MtrNm_s4p11[7][6]       0         12_AsstFWUprBoundY_MtrNm_s4p11[7][7]       2048         12_AsstFWUprBoundY_MtrNm_s4p11[7][8]       4096         12_AsstFWUprBoundY_MtrNm_s4p11[7][9]       6144         12_AsstFWUprBoundY_MtrNm_s4p11[7][10]       8192		
12_AsstFWUprBoundY_MtrNm_s4p11[7][4]       -4096         12_AsstFWUprBoundY_MtrNm_s4p11[7][5]       -2048         12_AsstFWUprBoundY_MtrNm_s4p11[7][6]       0         12_AsstFWUprBoundY_MtrNm_s4p11[7][7]       2048         12_AsstFWUprBoundY_MtrNm_s4p11[7][8]       4096         12_AsstFWUprBoundY_MtrNm_s4p11[7][9]       6144         12_AsstFWUprBoundY_MtrNm_s4p11[7][10]       8192		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] 8192		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]     0       t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]     2048       t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]     4096       t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]     6144       t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]     8192		
12_AsstFWUprBoundY_MtrNm_s4p11[7][7]       2048         12_AsstFWUprBoundY_MtrNm_s4p11[7][8]       4096         12_AsstFWUprBoundY_MtrNm_s4p11[7][9]       6144         12_AsstFWUprBoundY_MtrNm_s4p11[7][10]       8192		
12_AsstFWUprBoundY_MtrNm_s4p11[7][8]       4096         t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]       6144         t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]       8192		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] 8192		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] 8192		
t_AsstrWDetitAssistX_HwNm_u8p8[0] 51		
	t_AsstFWDefltAssistX_HwNm_u8p8[0]	51

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Name	Input Value		
t_AsstFWDefltAssistX_HwNm_u8p8[1]	77		
t_AsstFWDefltAssistX_HwNm_u8p8[2]	102		
t_AsstFWDefltAssistX_HwNm_u8p8[3]	128 154		
t_AsstFWDefltAssistX_HwNm_u8p8[4] t_AsstFWDefltAssistX_HwNm_u8p8[5]	179		
t_AsstFWDefitAssistX_HwNm_u8p8[6]	205		
t_AsstFWDefitAssistX_HwNm_u8p8[7]	230		
t_AsstFWDefltAssistX_HwNm_u8p8[8]	256		
t_AsstFWDefltAssistX_HwNm_u8p8[9]	282		
t_AsstFWDefltAssistX_HwNm_u8p8[10]	307		
t_AsstFWDefltAssistX_HwNm_u8p8[11]	333		
t_AsstFWDefltAssistX_HwNm_u8p8[12]	358		
t_AsstFWDefltAssistX_HwNm_u8p8[13]	384		
t_AsstFWDefltAssistX_HwNm_u8p8[14]	410		
t_AsstFWDefltAssistX_HwNm_u8p8[15]	435		
t_AsstFWDefltAssistX_HwNm_u8p8[16]	461		
t_AsstFWDefltAssistX_HwNm_u8p8[17]	486		
t_AsstFWDefltAssistX_HwNm_u8p8[18]	512		
t_AsstFWDefltAssistX_HwNm_u8p8[19]	538		
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-205		
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	-143		
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	-82		
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	-20		
t_AsstFWDeftAssistY_MtrNm_s4p11[4]	41		
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	102		
t_AsstFWDeftAssistY_MtrNm_s4p11[6]	164		
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	225 287		
t_AsstFWDefitAssistY_MtrNm_s4p11[8] t_AsstFWDefitAssistY_MtrNm_s4p11[9]	348		
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	410		
t_AsstFWDefitAssistY_MtrNm_s4p11[11]	471		
t_AsstFWDefitAssistY_MtrNm_s4p11[12]	532		
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	594		
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	655		
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	717		
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	778		
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	840		
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	901		
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	963		
t_AsstFWPstepNstepThresh_Cnt_u16[0]	123		
t_AsstFWPstepNstepThresh_Cnt_u16[1]	211		
t_AsstFWVehSpd_Kph_u9p7[0]	4352		
t_AsstFWVehSpd_Kph_u9p7[1]	4480		
t_AsstFWVehSpd_Kph_u9p7[2]	4608		
t_AsstFWVehSpd_Kph_u9p7[3]	4736		
t_AsstFWVehSpd_Kph_u9p7[4]	4864		
t_AsstFWVehSpd_Kph_u9p7[5]	4992		
t_AsstFWVehSpd_Kph_u9p7[6]	5120		
t_AsstFWVehSpd_Kph_u9p7[7]	5248		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	8.80000019		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	2 2000005		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2.20000005		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2 2		
	1		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	20.1000004		
tgt_AssistFirewall_Per1_venicleSpeed_kpn_is2.value tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	Ills f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_Mt		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_Mi		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	*		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mtr		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_M		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_		
Name	Actual Value	Expected Value	Resu
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.92000008	3.92000008 ± 4.88E-04	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	211	211 ± 1	
	1	1	
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	l'		
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc AssistFirewall_CombAsstSV_MtrNm_M_f32	0.439941406	0.439941406 ± 4.88E-04	
		0.439941406 ± 4.88E-04 3.02399993 ± 4.88E-04	

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4.5.5	stFi	rewa	Ш	Per1	

Name	Actual Value	Expected Value	Result
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.98199999	1.98199999 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	0.439941406	0.439941406 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	•
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Т				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.3 (Repeat Count = 1)	<u> </u>
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.029999993
AssistFirewall_ActiveRawAcc_Cnt_M_u16	400
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.13999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0199999996
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.29999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0099999978
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00400000019
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.20000005
k_AsstFWInpLimitHFA_MtrNm_f32	1.3999998
k_AsstFWInpLimitHysComp_MtrNm_f32	4
k_AsstFWNstep_Cnt_u16	4672
k_AsstFWPstep_Cnt_u16	369
k_RestoreThresh_MtrNm_f32	1.29999995
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
	1-7.0

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Name  2_AsstFWUprBoundX_HwNm_s4p11[2][8]  2_AsstFWUprBoundX_HwNm_s4p11[2][9]  2_AsstFWUprBoundX_HwNm_s4p11[2][10]  2_AsstFWUprBoundX_HwNm_s4p11[3][0]	Input Value 4096 6144 8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][9] 2_AsstFWUprBoundX_HwNm_s4p11[2][10] 2_AsstFWUprBoundX_HwNm_s4p11[3][0]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][10] 2_AsstFWUprBoundX_HwNm_s4p11[3][0]		
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	8192	
	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144	
	8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]		
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240	
2 AsstFWUprBoundX HwNm s4p11[7][3]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2048	
, , , , , , , , , , , , , , , , , , , ,	-2046 0	
2_AsstFWUprBoundX_HwNm_s4p11[7][7]		
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-26624	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-24576	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-8192	
	-6144	
2 AsstEWI InrRoundY MtrNm s4n11[0][10]	-0144	
	-8102	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]  2_AsstFWUprBoundY_MtrNm_s4p11[1][0]  2_AsstFWUprBoundY_MtrNm_s4p11[1][1]  2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-8192 -6144 -4096	

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- Toolst liewall_1 of 1	
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2 AsstFWUprBoundY MtrNm s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240

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Name	Input Value		
t_AsstFWDefltAssistX_HwNm_u8p8[0]	77		
t_AsstFWDefltAssistX_HwNm_u8p8[1]	102		
t_AsstFWDefltAssistX_HwNm_u8p8[2]	128		
t_AsstFWDefltAssistX_HwNm_u8p8[3]	154		
t_AsstFWDefltAssistX_HwNm_u8p8[4]	179		
t_AsstFWDefltAssistX_HwNm_u8p8[5]	205		
t_AsstFWDefltAssistX_HwNm_u8p8[6]	230		
t_AsstFWDefltAssistX_HwNm_u8p8[7]	256		
t_AsstFWDefltAssistX_HwNm_u8p8[8]	282		
t_AsstFWDefltAssistX_HwNm_u8p8[9]	307		
	333		
t_AsstFWDefitAssistX_HwNm_u8p8[10]			
t_AsstFWDefltAssistX_HwNm_u8p8[11]	358		
t_AsstFWDefltAssistX_HwNm_u8p8[12]	384		
t_AsstFWDefltAssistX_HwNm_u8p8[13]	410		
t_AsstFWDefltAssistX_HwNm_u8p8[14]	435		
t_AsstFWDefltAssistX_HwNm_u8p8[15]	461		
t_AsstFWDefltAssistX_HwNm_u8p8[16]	486		
t_AsstFWDefltAssistX_HwNm_u8p8[17]	512		
t_AsstFWDefltAssistX_HwNm_u8p8[18]	538		
t_AsstFWDefltAssistX_HwNm_u8p8[19]	563		
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2458		
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2662		
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2867		
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3072		
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3277		
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3482		
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	3686		
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	3891		
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4096		
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4301		
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	4506		
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	4710		
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	4915		
t_AsstFWDefitAssistY_MtrNm_s4p11[13]	5120		
t_AsstFWDefitAssistY_MtrNm_s4p11[14]	5325		
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	5530		
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	5734		
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	5939		
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6144		
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6349		
t_AsstFWPstepNstepThresh_Cnt_u16[0]	124		
t_AsstFWPstepNstepThresh_Cnt_u16[1]	215		
t_AsstFWVehSpd_Kph_u9p7[0]	7296		
t_AsstFWVehSpd_Kph_u9p7[1]	7424		
t_AsstFWVehSpd_Kph_u9p7[2]	7552		
t_AsstFWVehSpd_Kph_u9p7[3]	7680		
t_AsstFWVehSpd_Kph_u9p7[4]	7808		
t_AsstFWVehSpd_Kph_u9p7[5]	7936		
t_AsstFWVehSpd_Kph_u9p7[6]	8064		
t_AsstFWVehSpd_Kph_u9p7[7]	8192		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	0		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3.099999		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	30.2000008		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_U	Uls f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_Mtr		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_Mt		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt	*		
	-		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mtrl		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_Mt		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_		
Name	Actual Value	Expected Value	Result
	L. C.	4.8499999 ± 4.88E-04	<b>✓</b>
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	4.8499999		
	4.8499999 215	215 ± 1	-
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32		215 ± 1	
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32 AssistFirewall_ActiveRawAcc_Cnt_M_u16	215		~
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32 AssistFirewall_ActiveRawAcc_Cnt_M_u16 AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	215 1	1	~

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Name	Actual Value	Expected Value	Result
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.97600007	2.97600007 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.10009766	3.10009766 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.4 (Repeat Count = 1)		· ·
Name	Input Value	
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6	
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0399999991	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	6500	
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.14999998	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0299999993	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.39999998	





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_Asst WopiboundX_1WNin_s4p11[5][4] t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2 AsstFWUprBoundX HwNm s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_Asst WopiboundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-22326
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1] t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5] t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480 22528
tz_AsstFWUprBoundY_MtrNm_s4p11[o][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
LE MOSE WODEDOURGE WILLIAM SADELLE	-6192 -6144
	VITT
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3] t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3] t2_AsstFWUprBoundY_MtrNm_s4p11[7][4] t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048 0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3] t2_AsstFWUprBoundY_MtrNm_s4p11[7][4] t2_AsstFWUprBoundY_MtrNm_s4p11[7][5] t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048 0 2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3] t2_AsstFWUprBoundY_MtrNm_s4p11[7][4] t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048 0 2048

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Name	Input Value			
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288			
t_AsstFWDefltAssistX_HwNm_u8p8[0]	102			
t_AsstFWDefltAssistX_HwNm_u8p8[1]	128			
t_AsstFWDefltAssistX_HwNm_u8p8[2]	154			
t_AsstFWDefltAssistX_HwNm_u8p8[3]	179			
t_AsstFWDefltAssistX_HwNm_u8p8[4]	205			
t_AsstFWDefltAssistX_HwNm_u8p8[5]	230			
t_AsstFWDefltAssistX_HwNm_u8p8[6]	256			
t_AsstFWDefltAssistX_HwNm_u8p8[7]	282			
t_AsstFWDefltAssistX_HwNm_u8p8[8]	307			
t_AsstFWDefltAssistX_HwNm_u8p8[9]	333			
t_AsstFWDefltAssistX_HwNm_u8p8[10]	358			
t_AsstFWDefltAssistX_HwNm_u8p8[11]	384			
t_AsstFWDefltAssistX_HwNm_u8p8[12]	410			
t_AsstFWDefltAssistX_HwNm_u8p8[13]	435			
t_AsstFWDefltAssistX_HwNm_u8p8[14]	461			
t_AsstFWDefltAssistX_HwNm_u8p8[15]	486			
t_AsstFWDefltAssistX_HwNm_u8p8[16]	512			
t_AsstFWDefltAssistX_HwNm_u8p8[17]	538			
t_AsstFWDefltAssistX_HwNm_u8p8[18]	563			
t AsstFWDefltAssistX HwNm u8p8[19]	589			
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2662			
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2867			
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3072			
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3277			
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	3482			
t AsstFWDefltAssistY MtrNm s4p11[5]	3686			
t AsstFWDefltAssistY MtrNm s4p11[6]	3891			
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	4096			
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4301			
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4506			
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4710			
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	4915			
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5120			
t_AsstFWDefitAssistY_MtrNm_s4p11[13]	5325			
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5530			
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5734			
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	5939			
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	6144			
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	6349			
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	6554			
t_AsstFWPstepNstepThresh_Cnt_u16[0]	125			
	219			
t_AsstFWPstepNstepThresh_Cnt_u16[1] t AsstFWVehSpd Kph u9p7[0]	10240			
	10368			
t_AsstFWVehSpd_Kph_u9p7[1]				
t_AsstFWVehSpd_Kph_u9p7[2]	10496			
t_AsstFWVehSpd_Kph_u9p7[3]	10624			
t_AsstFWVehSpd_Kph_u9p7[4]	10752			
t_AsstFWVehSpd_Kph_u9p7[5]	10880			
t_AsstFWVehSpd_Kph_u9p7[6]	11008			
t_AsstFWVehSpd_Kph_u9p7[7]	11136			
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.5			
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0			
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4.0999999			
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4			
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4			
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0			
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	40.2999992			
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_I			
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_Mtr			
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_Mt			
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_				
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mtr			
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_t			
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_Mi			
	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_			
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum				
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_	I and the second		
The state of the s	Actual Value	Expected Value		Result
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32		I and the second		Result
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32  Name  AssistFirewall_ActiveKSV_M_str.SV_Uls_f32  AssistFirewall_ActiveRawAcc_Cnt_M_u16	Actual Value	<b>Expected Value</b> 5.76000023 ± 4.88E-04 219 ± 1		Result
tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_VehicleSpeed_Kph_f32  Name  AssistFirewall_ActiveKSV_M_str.SV_Uls_f32  AssistFirewall_ActiveRawAcc_Cnt_M_u16  AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	Actual Value 5.76000023 219	Expected Value 5.76000023 ± 4.88E-04 219 ± 1 1		Result
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32  Name  AssistFirewall_ActiveKSV_M_str.SV_Uls_f32  AssistFirewall_ActiveRawAcc_Cnt_M_u16	<b>Actual Value</b> 5.76000023 219	<b>Expected Value</b> 5.76000023 ± 4.88E-04 219 ± 1		Result

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Name	Actual Value	Expected Value	Result
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8.0399996	8.03999996 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.97000003	3.97000003 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.20019531	3.20019531 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Т	ullet			
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Name -	Immut Value
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0500000007
AssistFirewall_ActiveRawAcc_Cnt_M_u16	800
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.15999997
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.039999991
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.5
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.029999993
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00600000005
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
_AsstFWInpLimitBaseAsst_MtrNm_f32	2
c_AsstFWInpLimitHFA_MtrNm_f32	1.70000005
_AsstFWInpLimitHysComp_MtrNm_f32	2.0999999
c_AsstFWNstep_Cnt_u16	4424
c_AsstFWPstep_Cnt_u16	615
_RestoreThresh_MtrNm_f32	1.5
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
2_AsstFWUprBoundX_HWNm_s4p11[1][2] 2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
z_AsstFWUprBoundX_HwNm_s4p11[1][3] 2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048

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	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][4] 2 AsstFWUprBoundX HwNm s4p11[4][5]	
	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192 -6144
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-8192
	-6144
2 AsstFWUprBoundY MtrNm s4n11[0][8]	
2_AsstFWUprBoundY_MtrNm_s4p11[0][8] 2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-4096

AssistFirewall\_Per1





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-10240 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2046 0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4] t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
t2_Asst WoprBoundY_MtrNm_s4p11[2][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
t2_Asst WoprBoundY_MtrNm_s4p11[2][10]	14336
	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0] t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	
	-14336 -12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2] t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-12288 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3] t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
t2_Asst WopiBoundY_MtrNm_s4p11[3][6]	-4096
t2_Asst WoprBoundY_MtrNm_s4p11[3][7]	-2048
t2_Asst WopiBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-8192
	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
t2_Asst WoprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
t2_Asst WoprBoundY_MtrNm_s4p11[4][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-10240
t2 AsstFWUprBoundY MtrNm s4p11[5][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144
t2 AsstFWUprBoundY MtrNm s4p11[6][2]	8192
t2_Asst WoprBoundY_MtrNm_s4p11[6][3]	10240
t2_Asst WoprBoundY_MtrNm_s4p11[6][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
t2_Asst WoprBoundY_MtrNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
	10240

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AssistFirewall Per1 Input Value t2 AsstFWUprBoundY MtrNm s4p11[7][9] 12288 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][10] t AsstFWDefltAssistX HwNm u8p8[0] 128 t\_AsstFWDefltAssistX\_HwNm\_u8p8[1] 154 t AsstFWDefltAssistX HwNm u8p8[2] 179 t\_AsstFWDefltAssistX\_HwNm\_u8p8[3] 205 t AsstFWDefltAssistX HwNm u8p8[4] 230 t\_AsstFWDefltAssistX\_HwNm\_u8p8[5] 256 t\_AsstFWDefltAssistX\_HwNm\_u8p8[6] 282 t\_AsstFWDefltAssistX\_HwNm\_u8p8[7] 307 t\_AsstFWDefltAssistX\_HwNm\_u8p8[8] 333 t\_AsstFWDefltAssistX\_HwNm\_u8p8[9] 358 t\_AsstFWDefltAssistX\_HwNm\_u8p8[10] 384 t\_AsstFWDefltAssistX\_HwNm\_u8p8[11] 410 t\_AsstFWDefltAssistX\_HwNm\_u8p8[12] 435 461 t\_AsstFWDefltAssistX\_HwNm\_u8p8[13] t\_AsstFWDefltAssistX\_HwNm\_u8p8[14] 486 t AsstFWDefltAssistX HwNm u8p8[15] 512 t\_AsstFWDefltAssistX\_HwNm\_u8p8[16] 538 563 t AsstFWDefltAssistX HwNm u8p8[17] t\_AsstFWDefltAssistX\_HwNm\_u8p8[18] 589 t\_AsstFWDefltAssistX\_HwNm\_u8p8[19] 614 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[0] 2867 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[1] 3072 t AsstFWDefltAssistY MtrNm s4p11[2] 3277 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[3] 3482 3686 t AsstFWDefltAssistY MtrNm s4p11[4] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[5] 3891 t AsstFWDefltAssistY MtrNm s4p11[6] 4096 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[7] 4301 4506 t AsstFWDefltAssistY MtrNm s4p11[8] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[9] 4710 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[10] 4915 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[11] 5120 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[12] 5325 5530 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[13]  $t\_AsstFWDefltAssistY\_MtrNm\_s4p11[14]$ 5734 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[15] 5939 t AsstFWDefltAssistY MtrNm s4p11[16] 6144 t AsstFWDefltAssistY\_MtrNm\_s4p11[17] 6349 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[18] 6554 6758 t AsstFWDefltAssistY MtrNm s4p11[19] t\_AsstFWPstepNstepThresh\_Cnt\_u16[0] 126 t\_AsstFWPstepNstepThresh\_Cnt\_u16[1] 223 t\_AsstFWVehSpd\_Kph\_u9p7[0] 13184 t\_AsstFWVehSpd\_Kph\_u9p7[1] 13312 t AsstFWVehSpd Kph\_u9p7[2] 13440 t\_AsstFWVehSpd\_Kph\_u9p7[3] 13568 t\_AsstFWVehSpd\_Kph\_u9p7[4] 13696 13824 t\_AsstFWVehSpd\_Kph\_u9p7[5] 13952 t\_AsstFWVehSpd\_Kph\_u9p7[6] t\_AsstFWVehSpd\_Kph\_u9p7[7] 14080 tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value -5.5 tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lgc.value 0 tgt AssistFirewall Per1 HighFregAssist MtrNm f32.value 5.0999999 tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32.value 5 tgt AssistFirewall Per1 HysteresisComp MtrNm f32.value  $tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum.value$ 1 tgt\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32.value 50.0999985  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32$ tgt\_AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32 tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32 tgt\_AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32 tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_CombinedAssist MtrNm f32 tgt AssistFirewall Per1 CombinedAssist MtrNm f32 tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_It\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Igc tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32 tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32 tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HwTorque\_HwNm\_f32 tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32 tot Rte Inst Ap AssistFirewall.AssistFirewall Per1 HysteresisComp MtrNm f32 tgt AssistFirewall Per1 HysteresisComp MtrNm f32 tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32 tgt AssistFirewall Per1 VehicleSpeed Kph f32 Expected Value Result AssistFirewall\_ActiveKSV\_M\_str.SV\_Uls\_f32 6 6500001 6.6500001 ± 4.88E-04 AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16 223 223 ± 1 AssistFirewall AsstReducedPerfSV Cnt M Igc

3.29980469

AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32

3.29980469 ± 4.88E-04

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Name	Actual Value	Expected Value	Result
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.83199978	5.83199978 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.39700007	1.39699996 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.96400023	4.96400023 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.29980469	3.29980469 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

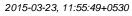
Т				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	-

Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	8
AssistFirewall_ActiveKSV_M_str.K_UIs_f32	0.0599999987
AssistFirewall_ActiveR3v_ivi_str.K_Ots_132 AssistFirewall ActiveRawAcc Cnt M u16	1000
	1
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.16999996
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.60000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0399999991
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00700000022
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1
<_AsstFWInpLimitHFA_MtrNm_f32	1.8999998
k_AsstFWInpLimitHysComp_MtrNm_f32	2.5
k_AsstFWNstep_Cnt_u16	4300
k_AsstFWPstep_Cnt_u16	738
x_RestoreThresh_MtrNm_f32	1.60000002
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432
12_Asst WorldoundX_TWNIII_s4p11[1][0] 12 AsstFWUprBoundX HwNm s4p11[1][1]	-16384
:2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336
:2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240 -8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048

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Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144	
:2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048	
	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]		
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144	
2 AsstFWUprBoundX HwNm s4p11[6][6]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	0	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10] t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	6144
t2 AsstFWUprBoundY MtrNm s4p11[6][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288





Name	Input Value		
	·		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	14336 16384		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432		
t_AsstFWDefltAssistX_HwNm_u8p8[0]	154		
t_AsstFWDefltAssistX_HwNm_u8p8[1]	179		
t AsstFWDefltAssistX HwNm u8p8[2]	205		
t_AsstFWDefltAssistX_HwNm_u8p8[3]	230		
t_AsstFWDefltAssistX_HwNm_u8p8[4]	256		
t_AsstFWDefltAssistX_HwNm_u8p8[5]	282		
t_AsstFWDefltAssistX_HwNm_u8p8[6]	307		
t_AsstFWDefltAssistX_HwNm_u8p8[7]	333		
t_AsstFWDefltAssistX_HwNm_u8p8[8]	358		
t_AsstFWDefltAssistX_HwNm_u8p8[9]	384		
t_AsstFWDefltAssistX_HwNm_u8p8[10]	410		
t_AsstFWDefltAssistX_HwNm_u8p8[11]	435		
t_AsstFWDefltAssistX_HwNm_u8p8[12]	461		
t_AsstFWDefltAssistX_HwNm_u8p8[13]	486		
t_AsstFWDefltAssistX_HwNm_u8p8[14]	512		
t_AsstFWDefltAssistX_HwNm_u8p8[15]	538		
t_AsstFWDefltAssistX_HwNm_u8p8[16]	563		
t_AsstFWDefltAssistX_HwNm_u8p8[17]	589		
t_AsstFWDefltAssistX_HwNm_u8p8[18] t_AsstFWDefltAssistX_HwNm_u8p8[19]	614 640		
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	3072		
t_AsstFWDefitAssistY_MtrNm_s4p11[1]	3277		
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	3482		
t AsstFWDefltAssistY MtrNm s4p11[3]	3686		
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3891		
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4096		
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4301		
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4506		
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4710		
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4915		
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5120		
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5325		
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5530		
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5734		
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5939		
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6144		
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6349		
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6554		
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6758		
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6963		
t_AsstFWPstepNstepThresh_Cnt_u16[0]	127 227		
t_AsstFWPstepNstepThresh_Cnt_u16[1]			
t_AsstFWVehSpd_Kph_u9p7[0] t_AsstFWVehSpd_Kph_u9p7[1]	16128 16256		
t_AsstFWVehSpd_Kph_u9p7[2]	16384		
t_AsstFWVehSpd_Kph_u9p7[3]	16512		
t_AsstFWVehSpd_Kph_u9p7[4]	16640		
t_AsstFWVehSpd_Kph_u9p7[5]	16768		
t_AsstFWVehSpd_Kph_u9p7[6]	16896		
t_AsstFWVehSpd_Kph_u9p7[7]	17024		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-8.80000019		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	6		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	60.2999992		
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32$	tgt_AssistFirewall_Per1_AsstFirewallActive_U	Jls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_Mti		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_Mt		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I			
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mtrl		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_Mt		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_	I and the second se	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	7.51999998	7.51999998 ± 4.88E-04	<b>V</b>
AssistFirewall_ActiveRawAcc_Cnt_M_u16	227	227 ± 1	
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	

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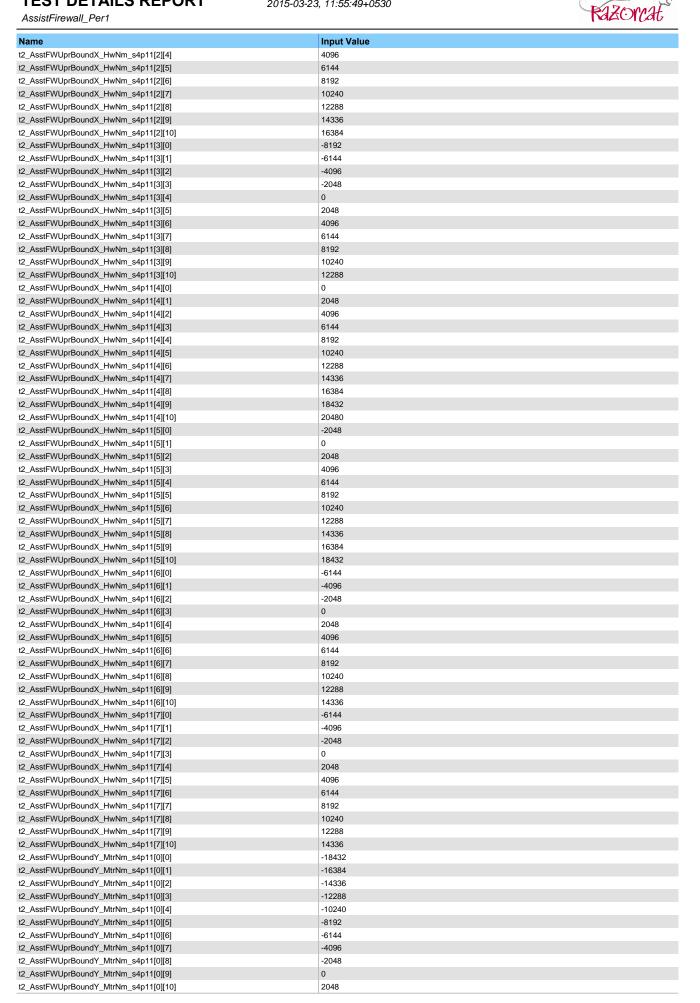
Name	Actual Value	Expected Value	Result
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.39990234	3.39990234 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.73000002	6.73000002 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.51200008	2.51200008 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.95800018	5.95800018 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.39990234	3.39990234 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

Т				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	<b>~</b>

Mana	Innuit Value
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1000
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.17999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.60000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.039999991
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00700000022
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
c_AsstFWInpLimitBaseAsst_MtrNm_f32	1
C_AsstFWInpLimitHFA_MtrNm_f32	1.89999998
c_AsstFWInpLimitHysComp_MtrNm_f32	2.5
c_AsstFWNstep_Cnt_u16	4300
c_AsstFWPstep_Cnt_u16	738
c_RestoreThresh_MtrNm_f32	1.70000005
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048

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Name	Input Value
	· ·
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192
	-8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-12288
t2 AsstFWUprBoundY MtrNm s4p11[4][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4] t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-10240 -9102
	-8192 -6444
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2 AcetEM/IntRoundy MtrNm c/n11[7][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5] t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240 12288





Name	Innut Value		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	Input Value 14336		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480		
t_AsstFWDefltAssistX_HwNm_u8p8[0]	179		
t_AsstFWDefltAssistX_HwNm_u8p8[1]	205		
t_AsstFWDefltAssistX_HwNm_u8p8[2]	230		
t_AsstFWDefltAssistX_HwNm_u8p8[3]	256		
t_AsstFWDefltAssistX_HwNm_u8p8[4]	282		
t_AsstFWDefltAssistX_HwNm_u8p8[5]	307		
t_AsstFWDefltAssistX_HwNm_u8p8[6]	333		
t_AsstFWDefltAssistX_HwNm_u8p8[7]	358		
t_AsstFWDefltAssistX_HwNm_u8p8[8]	384		
t_AsstFWDefltAssistX_HwNm_u8p8[9]	410		
t_AsstFWDefltAssistX_HwNm_u8p8[10]	435		
t_AsstFWDefltAssistX_HwNm_u8p8[11] t_AsstFWDefltAssistX_HwNm_u8p8[12]	461 486		
t_AsstFWDefltAssistX_HwNm_u8p8[13]	512		
t_AsstFWDefltAssistX_HwNm_u8p8[14]	538		
t_AsstFWDefltAssistX_HwNm_u8p8[15]	563		
t_AsstFWDefltAssistX_HwNm_u8p8[16]	589		
t_AsstFWDefltAssistX_HwNm_u8p8[17]	614		
t_AsstFWDefltAssistX_HwNm_u8p8[18]	640		
t_AsstFWDefltAssistX_HwNm_u8p8[19]	666		
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3277		
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3482		
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3686		
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3891		
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096		
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4301		
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4506		
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4710		
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4915		
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5120		
t_AsstFWDefltAssistY_MtrNm_s4p11[10] t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5325 5530		
t_AsstFWDefitAssistY_MtrNm_s4p11[12]	5734		
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5939		
t_AsstFWDefitAssistY_MtrNm_s4p11[14]	6144		
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6349		
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6554		
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6758		
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6963		
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7168		
t_AsstFWPstepNstepThresh_Cnt_u16[0]	128		
t_AsstFWPstepNstepThresh_Cnt_u16[1]	231		
t_AsstFWVehSpd_Kph_u9p7[0]	19072		
t_AsstFWVehSpd_Kph_u9p7[1]	19200		
t_AsstFWVehSpd_Kph_u9p7[2]	19328		
t_AsstFWVehSpd_Kph_u9p7[3]	19456		
t_AsstFWVehSpd_Kph_u9p7[4]	19584		
t_AsstFWVehSpd_Kph_u9p7[5]	19712		
t_AsstFWVehSpd_Kph_u9p7[6]	19840 19968		
t_AsstFWVehSpd_Kph_u9p7[7] tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1		
tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	8.80000019		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	6		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	60.2000008		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_Mt	rNm_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32$	tgt_AssistFirewall_Per1_CombinedAssist_Mt	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lg	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Ser	rvice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mtr		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_	f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_M		
tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_	I and the second	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	7.51999998	7.51999998 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	231	231 ± 1	•

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Name	Actual Value	Expected Value	Result
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.5	3.5 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.92000008	6.92000008 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.47200012	2.47199988 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.95800018	5.95800018 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.5	3.5 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	•
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	<b>~</b>
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.8 (Repeat Count = 1)	v v
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall ActiveKSV M str.K Uls f32	0.0799999982
AssistFirewall ActiveRawAcc Cnt M u16	106
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	1.19000006
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0700000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00899999961
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k AsstFWInpLimitBaseAsst MtrNm f32	3
k_AsstFWInpLimitHFA_MtrNm_f32	1.29999995
k AsstFWInpLimitHysComp MtrNm f32	3.29999995
k_AsstFWNstep_Cnt_u16	4052
k_AsstFWPstep_Cnt_u16	984
k RestoreThresh MtrNm f32	1.79999995
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2 AsstFWUprBoundX HwNm s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3] t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	16384 -16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336 -12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048

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Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-4096
	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240
2 AsstFWUprBoundY MtrNm s4p11[5][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
1 1 16.1	





	Input Value
, , , , , , ,	20480
	22528
, , , , , , ,	24576
_ , ,	26624 28672
	205
	230
	256
,	282
	307
,	333
t_AsstFWDefltAssistX_HwNm_u8p8[6]	358
t_AsstFWDefltAssistX_HwNm_u8p8[7]	384
t_AsstFWDefltAssistX_HwNm_u8p8[8]	410
t_AsstFWDefltAssistX_HwNm_u8p8[9]	435
t_AsstFWDefltAssistX_HwNm_u8p8[10]	461
t_AsstFWDefltAssistX_HwNm_u8p8[11]	486
t_AsstFWDefltAssistX_HwNm_u8p8[12]	512
	538
	563
	589
	614
	640
	666
, , ,	691
	3482 3686
,	3891
	4096
,	4301
	4506
, . ;	4710
	4915
, .,	5120
, , ,	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6554
,	6758
	6963
	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7373
t_AsstFWPstepNstepThresh_Cnt_u16[0]	129
	235
	22016
, , , , , , ,	22144 22272
	22400
, , , , , , ,	22528
	22656
	22784
	22912
	3
	0
	0
	8
,	8
	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	80.1999969
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_! \\$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
A COLUMN A COLUMN A COLUMN A COLUMN ACCOUNT A COLUMN A COLUMN ACCOUNT A COLUMN A COLUMN A COLUMN A COLUMN A	tgt_Assisti ilewaii_F et i_i iigiii reqAssist_ivitiiviii_i32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistTirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32  Name	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveRawAcc_Cnt_M_u16	235	235 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.60009766	3.60009766 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.46399999	1.46399999 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.33400011	4.33400011 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>~</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.9460001	7.9460001 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.60009766	3.60009766 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Т				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	<b>~</b>
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	-

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.099999
Assist irewall_ActiveKSV_M_str.K_UIs_f32	0.090000036
Assisti rewall_ActiveRoV_M_str.N_ois_i32	109
	1
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.079999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.8999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0700000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0099999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
:_AsstFWInpLimitBaseAsst_MtrNm_f32	4
:_AsstFWInpLimitHFA_MtrNm_f32	2.5
:_AsstFWInpLimitHysComp_MtrNm_f32	3.78999996
z_AsstFWNstep_Cnt_u16	3928
z_AsstFWPstep_Cnt_u16	1107
_RestoreThresh_MtrNm_f32	1.8999998
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
2 AsstFWUprBoundX HwNm s4p11[0][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-8192
2_AsstFWUprBoundX_HWNm_s4p11[1][2] 2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-6144
z_AsstFWUprBoundX_HwNm_s4p11[1][3] 2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][0] 2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0 2048

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Name	Input Value	
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384	
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432	
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480	
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-12288	
ادر المراجعة المراجع	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-6144	
	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-2046 0	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]		
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	4096	
12_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432	
12_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384	
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192	
10240		





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-12288
1 1 1 1	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	
1 1 1 1 1	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-16384 -14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-16384 -14336

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	230
t_AsstFWDefltAssistX_HwNm_u8p8[1]	256
t_AsstFWDefltAssistX_HwNm_u8p8[2]	282
t_AsstFWDefltAssistX_HwNm_u8p8[3]	307
t_AsstFWDefltAssistX_HwNm_u8p8[4]	333
t_AsstFWDefltAssistX_HwNm_u8p8[5]	358
t_AsstFWDefltAssistX_HwNm_u8p8[6]	384
t_AsstFWDefltAssistX_HwNm_u8p8[7]	410
t_AsstFWDefltAssistX_HwNm_u8p8[8]	435 461
t_AsstFWDefltAssistX_HwNm_u8p8[9] t_AsstFWDefltAssistX_HwNm_u8p8[10]	486
t_AsstFWDefitAssistX_HwNm_u8p8[11]	512
t_AsstFWDefitAssistX_HwNm_u8p8[12]	538
t_AsstFWDefltAssistX_HwNm_u8p8[13]	563
t_AsstFWDefltAssistX_HwNm_u8p8[14]	589
t_AsstFWDefitAssistX_HwNm_u8p8[15]	614
t_AsstFWDefltAssistX_HwNm_u8p8[16]	640
t_AsstFWDefltAssistX_HwNm_u8p8[17]	666
t_AsstFWDefltAssistX_HwNm_u8p8[18]	691
t_AsstFWDefltAssistX_HwNm_u8p8[19]	717
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7578
t_AsstFWPstepNstepThresh_Cnt_u16[0]	130
t_AsstFWPstepNstepThresh_Cnt_u16[1]	239
t_AsstFWVehSpd_Kph_u9p7[0]	24960
t_AsstFWVehSpd_Kph_u9p7[1]	25088
t_AsstFWVehSpd_Kph_u9p7[2]	25216
t_AsstFWVehSpd_Kph_u9p7[3]	25344
t_AsstFWVehSpd_Kph_u9p7[4]	25472
t_AsstFWVehSpd_Kph_u9p7[5]	25600
t_AsstFWVehSpd_Kph_u9p7[6]	25728
t_AsstFWVehSpd_Kph_u9p7[7]	25856 4
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.5
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	9
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002
tgt_Assisti ilewaii_Fe11_HStelesisComp_MitMit_i3z.value tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90.0100021
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt kte inst ap assistritewali.Assistritewali peri hysteresiscomo wimmi 132	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.82099986	2.8210001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	239	239 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.70019531	3.70019531 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.63199997	2.63199997 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.2329998	5.2329998 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.11900008	1.11899996 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.70019531	3.70019531 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.10 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3
AssistFirewall ActiveKSV M str.K Uls f32	0.0099999978
AssistFirewall_ActiveRawAcc_Cnt_M_u16	112
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00899999961
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00800000038
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0020000009
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	2.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	4.28000021
k_AsstFWNstep_Cnt_u16	3804
k_AsstFWPstep_Cnt_u16	1230
k_RestoreThresh_MtrNm_f32	2
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-18432

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384
	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10] t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-14336
tz_AsstFWUprBoundX_HwNm_s4p11[4][0] t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-14336 -12288
tz_AsstFWUprBoundX_HwNm_s4p11[4][1] t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2] t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-10240 -8192
tz_AsstFWUprBoundX_HwNm_s4p11[4][3] t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-6192 -6144
tz_AsstFWUprBoundX_HwNm_s4p11[4][4] t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144
t2_Asst WopiboundX_1WNm_s4p11[4][6]	-2048
t2_Asst WopiBoundX_HwNm_s4p11[4][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_Asst WopiboundX_HwNm_s4p11[4][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	6144
	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0] t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_Asst WopiboundX_HwNm_s4p11[5][2] t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_Asst WopiboundX_HwNm_s4p11[5][4]	-8192
t2_Asst WopiboundX_1WNm_s4p11[5][4] t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_Asst WopiboundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstrWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_Asst WopiboundX_HwNm_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_Asst WopiboundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_Asst WopiboundX_HwNm_s4p11[7][4]	20480
	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240 -8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-10240 -8192 -6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240 -8192 -6144

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336
	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288 -10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	
	-4096 -12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
	-8192



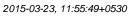


Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	256
t_AsstFWDefltAssistX_HwNm_u8p8[1]	282 307
t_AsstFWDefltAssistX_HwNm_u8p8[2]	
t_AsstFWDefltAssistX_HwNm_u8p8[3]	333 358
t_AsstFWDefltAssistX_HwNm_u8p8[4]	384
t_AsstFWDefltAssistX_HwNm_u8p8[5]	410
t_AsstFWDefltAssistX_HwNm_u8p8[6]	435
t_AsstFWDefltAssistX_HwNm_u8p8[7] t_AsstFWDefltAssistX_HwNm_u8p8[8]	461
t_AsstFWDefitAssistX_HwNm_u8p8[9]	486
t_AsstFWDefltAssistX_HwNm_u8p8[10]	512
t_AsstFWDefitAssistX_HwNm_u8p8[11]	538
	563
t_AsstFWDefltAssistX_HwNm_u8p8[12] t_AsstFWDefltAssistX_HwNm_u8p8[13]	589
	614
t_AsstFWDefltAssistX_HwNm_u8p8[14]	640
t_AsstFWDefltAssistX_HwNm_u8p8[15]	666
t_AsstFWDefltAssistX_HwNm_u8p8[16]	691
t_AsstFWDefltAssistX_HwNm_u8p8[17] t_AsstFWDefltAssistX_HwNm_u8p8[18]	717
t_AsstFWDefitAssistX_HwNm_u8p8[18]  t_AsstFWDefitAssistX_HwNm_u8p8[19]	742
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4096
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4506
· · · · ·	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[4] t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5120
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	5325
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5734
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	5939
t AsstFWDefitAssistY MtrNm s4p11[11]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6349
t AsstFWDefltAssistY MtrNm s4p11[13]	6554
t AsstFWDefltAssistY MtrNm s4p11[14]	6758
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7168
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	7373
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	7578
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	7782
t AsstFWPstepNstepThresh Cnt u16[0]	131
t_AsstFWPstepNstepThresh_Cnt_u16[1]	243
t_AsstFWVehSpd_Kph_u9p7[0]	27904
t_AsstFWVehSpd_Kph_u9p7[1]	28032
t_AsstFWVehSpd_Kph_u9p7[2]	28160
t_AsstFWVehSpd_Kph_u9p7[3]	28288
t_AsstFWVehSpd_Kph_u9p7[4]	28416
t_AsstFWVehSpd_Kph_u9p7[5]	28544
t_AsstFWVehSpd_Kph_u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7]	28800
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.5
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	10.1999998
tgt_Rts_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	
•	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall\_Per1



AssistFirewall\_Per1





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240 12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384 18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288 -10340
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2] t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-8192 -6144
	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4] t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-4096 -2048
	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288 -10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6] t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9] t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_Asst WoprboundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2 AsstFWUprBoundX HwNm s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2 AsstFWUprBoundX HwNm s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2 AsstFWUprBoundX HwNm s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_Asst WoprBoundX_HwNm_s4p11[7][2]	-8192
t2_Asst WoprboundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_Asst WoprboundX_HwNm_s4p11[7][4]	-2048
t2_Asst WoprboundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_Asst WoprboundX_nwnn_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	4096

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2015-03-23, 11:55:49+0530



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-16384
	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-14330
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	
	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-4096 2049
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192 -6144





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	282
t_AsstFWDefltAssistX_HwNm_u8p8[1]	307
t_AsstFWDefltAssistX_HwNm_u8p8[2]	333
t_AsstFWDefltAssistX_HwNm_u8p8[3]	358
t_AsstFWDefltAssistX_HwNm_u8p8[4]	384
t_AsstFWDefltAssistX_HwNm_u8p8[5]	410
t_AsstFWDefltAssistX_HwNm_u8p8[6]	435
t_AsstFWDefltAssistX_HwNm_u8p8[7]	461
t_AsstFWDefltAssistX_HwNm_u8p8[8]	486
t_AsstFWDefltAssistX_HwNm_u8p8[9]	512
t_AsstFWDefltAssistX_HwNm_u8p8[10]	538
t_AsstFWDefltAssistX_HwNm_u8p8[11] t_AsstFWDefltAssistX_HwNm_u8p8[12]	563 589
t_AsstFWDefitAssistX_HwNm_u8p8[13]	614
t_AsstFWDefitAssistX_HwNm_u8p8[14]	640
t_AsstFWDefltAssistX_HwNm_u8p8[15]	666
t_AsstFWDefltAssistX_HwNm_u8p8[16]	691
t_AsstFWDefltAssistX_HwNm_u8p8[17]	717
t_AsstFWDefltAssistX_HwNm_u8p8[18]	742
t_AsstFWDefltAssistX_HwNm_u8p8[19]	768
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5325 5530
t_AsstFWDefltAssistY_MtrNm_s4p11[7] t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7782
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	7987
t_AsstFWPstepNstepThresh_Cnt_u16[0]	132
t_AsstFWPstepNstepThresh_Cnt_u16[1] t_AsstFWVehSpd_Kph_u9p7[0]	247 30848
t_AsstFWVehSpd_Kph_u9p7[1]	30976
t_AsstFWVehSpd_Kph_u9p7[2]	31104
t_AsstFWVehSpd_Kph_u9p7[3]	31232
t_AsstFWVehSpd_Kph_u9p7[4]	31360
t_AsstFWVehSpd_Kph_u9p7[5]	31488
t_AsstFWVehSpd_Kph_u9p7[6]	31616
t_AsstFWVehSpd_Kph_u9p7[7]	31744
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-10
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	22 2000002
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	22.2999992 tot AccicEirouall Port AcctEirouallActivo Lille f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_UIs_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_kte_Inst_Ap_AssistFireWall.AssistFireWall_Per1_CombinedAssist_MtrNm_r32 tgt_kte_Inst_Ap_AssistFireWall.AssistFireWall_Per1_Defeat_AsstTbl_Service_Cnt_li	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
	-9 //
	tqt AssistFirewall Per1 HwTorque HwNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.06939983	5.06939983 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	247	247 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.89990234	-3.89990234 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.25	4.25 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.459999979	0.460000008 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.85699987	2.85700011 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-3.89990234	-3.89990234 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.12 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	6.0999999
AssistFirewall ActiveKSV M str.K UIs f32	0.00700000022
AssistFirewall_ActiveRawAcc_Cnt_M_u16	118
AssistFirewall AsstReducedPerfSV Cnt M Igc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.3999998
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00800000038
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.02999997
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00499999989
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0399999991
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.70000005
k_AsstFWInpLimitHFA_MtrNm_f32	2.5
k_AsstFWInpLimitHysComp_MtrNm_f32	5.26000023
k_AsstFWNstep_Cnt_u16	3556
k_AsstFWPstep_Cnt_u16	1476
k RestoreThresh MtrNm f32	2.2000005
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336

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Name	Input Value
name t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	6144
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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-2048
	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-6144
	-4096





Name	Inner Weller
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefltAssistX_HwNm_u8p8[0]	307
t_AsstFWDefltAssistX_HwNm_u8p8[1]	333
t_AsstFWDefltAssistX_HwNm_u8p8[2]	358
t_AsstFWDefltAssistX_HwNm_u8p8[3]	384
t_AsstFWDefltAssistX_HwNm_u8p8[4]	410
t_AsstFWDefltAssistX_HwNm_u8p8[5]	435
t_AsstFWDefltAssistX_HwNm_u8p8[6]	461
t_AsstFWDefltAssistX_HwNm_u8p8[7]	486
t_AsstFWDefltAssistX_HwNm_u8p8[8]	512
t_AsstFWDefltAssistX_HwNm_u8p8[9]	538
t_AsstFWDefltAssistX_HwNm_u8p8[10]	563
t_AsstFWDefltAssistX_HwNm_u8p8[11]	589
t_AsstFWDefltAssistX_HwNm_u8p8[12]	614
t_AsstFWDefltAssistX_HwNm_u8p8[13]	640
t_AsstFWDefltAssistX_HwNm_u8p8[14]	666
t_AsstFWDefltAssistX_HwNm_u8p8[15]	691
t_AsstFWDefltAssistX_HwNm_u8p8[16]	717
t AsstFWDefitAssistX HwNm u8p8[17]	742
t_AsstFWDefltAssistX_HwNm_u8p8[18]	768
t_AsstFWDefltAssistX_HwNm_u8p8[19]	794
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	8192
t_AsstFWPstepNstepThresh_Cnt_u16[0]	133
t_AsstFWPstepNstepThresh_Cnt_u16[1]	251
t_AsstFWVehSpd_Kph_u9p7[0]	33792
t_AsstFWVehSpd_Kph_u9p7[1]	33920
t_AsstFWVehSpd_Kph_u9p7[2]	34048
t_AsstFWVehSpd_Kph_u9p7[3]	34176
t_AsstFWVehSpd_Kph_u9p7[4]	34304
t_AsstFWVehSpd_Kph_u9p7[5]	34432
t_AsstFWVehSpd_Kph_u9p7[6]	34560
t_AsstFWVehSpd_Kph_u9p7[7]	34688
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2.20000005
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	10
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	33.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_tte_mst_Ap_Assist newall.Assist newall_ren_combinedAssist_ivititvin_isz	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lq	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_letgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
2 AsstFWUprBoundX HwNm s4p11[7][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
	4000
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6] t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
	-4096
t2 Acet N/I In Roundy MtrNm can 117121	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstrWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	333
t_AsstFWDefltAssistX_HwNm_u8p8[1]	358
t_AsstFWDefltAssistX_HwNm_u8p8[2]	384
t_AsstFWDefltAssistX_HwNm_u8p8[3]	410
t_AsstFWDefltAssistX_HwNm_u8p8[4]	435
t_AsstFWDefltAssistX_HwNm_u8p8[5]	461
t_AsstFWDefltAssistX_HwNm_u8p8[6]	486
t_AsstFWDefltAssistX_HwNm_u8p8[7]	512
t_AsstFWDefltAssistX_HwNm_u8p8[8]	538
t_AsstFWDefltAssistX_HwNm_u8p8[9]	563
t_AsstFWDefltAssistX_HwNm_u8p8[10]	589
t_AsstFWDefltAssistX_HwNm_u8p8[11]	614
t_AsstFWDefltAssistX_HwNm_u8p8[12]	640
t_AsstFWDefltAssistX_HwNm_u8p8[13]	666
t_AsstFWDefltAssistX_HwNm_u8p8[14]	691
t_AsstFWDefltAssistX_HwNm_u8p8[15]	717
t_AsstFWDefltAssistX_HwNm_u8p8[16]	742
t_AsstFWDefltAssistX_HwNm_u8p8[17] t_AsstFWDefltAssistX_HwNm_u8p8[18]	768 794
t_AsstFWDefitAssistX_HwNm_u8p8[19]	819
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	7373
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7987 8192
t_AsstFWDefltAssistY_MtrNm_s4p11[18] t_AsstFWDefltAssistY_MtrNm_s4p11[19]	8397
t AsstFWPstepNstepThresh Cnt u16[0]	134
t_AsstFWPstepNstepThresh_Cnt_u16[1]	255
t_AsstFWVehSpd_Kph_u9p7[0]	36736
t_AsstFWVehSpd_Kph_u9p7[1]	36864
t_AsstFWVehSpd_Kph_u9p7[2]	36992
t_AsstFWVehSpd_Kph_u9p7[3]	37120
t_AsstFWVehSpd_Kph_u9p7[4]	37248
t_AsstFWVehSpd_Kph_u9p7[5]	37376
t_AsstFWVehSpd_Kph_u9p7[6]	37504
t_AsstFWVehSpd_Kph_u9p7[7]	37632
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	0
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	44.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_It	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Itgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Itgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.991999984	0.991999984 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	255	255 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	2.20019531	2.20019531 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.14589977	6.14589977 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.95799994	2.95799994 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>~</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.04500008	5.04500008 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.991999984	0.991999984 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	2.20019531	2.20019531 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Τ			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.14 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2
AssistFirewall ActiveKSV M str.K Uls f32	0.00899999961
AssistFirewall_ActiveRawAcc_Cnt_M_u16	124
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.6000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0099999978
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.04999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00700000022
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0599999987
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.29999995
k_AsstFWInpLimitHFA_MtrNm_f32	1.29999995
k_AsstFWInpLimitHysComp_MtrNm_f32	6.23999977
k_AsstFWNstep_Cnt_u16	3308
k_AsstFWPstep_Cnt_u16	1722
k_RestoreThresh_MtrNm_f32	2.4000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240

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Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0	
2 AsstFWUprBoundX HwNm s4p11[3][8]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144	
, , , , , , , , , , , , , , , , , , , ,		
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240	
P_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096	
2 AsstFWUprBoundX HwNm s4p11[7][2]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144	
P_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	12288	

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-12288
	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-4096
t2_Asst Wopibound1_ivitNin_s4p11[4][0] t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-2048
	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048 0





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	358
t_AsstFWDefltAssistX_HwNm_u8p8[1]	384
t_AsstFWDefltAssistX_HwNm_u8p8[2]	410
t_AsstFWDefltAssistX_HwNm_u8p8[3]	435
t_AsstFWDefltAssistX_HwNm_u8p8[4]	461
t_AsstFWDefltAssistX_HwNm_u8p8[5]	486
t_AsstFWDefltAssistX_HwNm_u8p8[6]	512
t_AsstFWDefltAssistX_HwNm_u8p8[7]	538
t_AsstFWDefltAssistX_HwNm_u8p8[8]	563
t_AsstFWDefltAssistX_HwNm_u8p8[9]	589
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	614 640
t_AsstFWDefitAssistX_HwNm_u8p8[12]	666
t_AsstFWDefitAssistX_HwNm_u8p8[13]	691
t_AsstFWDefitAssistX_HwNm_u8p8[14]	717
t_AsstFWDefltAssistX_HwNm_u8p8[15]	742
t_AsstFWDefltAssistX_HwNm_u8p8[16]	768
t_AsstFWDefltAssistX_HwNm_u8p8[17]	794
t_AsstFWDefltAssistX_HwNm_u8p8[18]	819
t_AsstFWDefltAssistX_HwNm_u8p8[19]	845
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5530
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[6] t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5939 6144
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	8602
t_AsstFWPstepNstepThresh_Cnt_u16[0] t_AsstFWPstepNstepThresh_Cnt_u16[1]	135 259
t_AsstFWVehSpd_Kph_u9p7[0]	39680
t_AsstFWVehSpd_kph_u9p7[1]	39808
t_AsstFWVehSpd_Kph_u9p7[2]	39936
t_AsstFWVehSpd_Kph_u9p7[3]	40064
t_AsstFWVehSpd_Kph_u9p7[4]	40192
t_AsstFWVehSpd_Kph_u9p7[5]	40320
t_AsstFWVehSpd_Kph_u9p7[6]	40448
t_AsstFWVehSpd_Kph_u9p7[7]	40576
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4.099999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5.5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.099999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1 55.2999992
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AssirfirewallActive_Ois_i32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall\_Per1

Status\_Cnt\_T\_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.98199999	1.98199999 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	259	259 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.20019531	4.20019531 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.07500005	1.07500005 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.97550011	3.97550011 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.27399969	6.27400017 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4.20019531	4.20019531 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	<b>~</b>

τ -				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	_

0x01

0x01

Test Step 2.15 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0099999978
AssistFirewall_ActiveRawAcc_Cnt_M_u16	127
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.70000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0199999996
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.05999994
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00800000038
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.070000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.5999999
k_AsstFWInpLimitHFA_MtrNm_f32	1.60000002
k_AsstFWInpLimitHysComp_MtrNm_f32	6.73000002
k_AsstFWNstep_Cnt_u16	3184
k_AsstFWPstep_Cnt_u16	1845
k_RestoreThresh_MtrNm_f32	2.5
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192

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ASSIST ITEWAII_PETT		
Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0	
2 AsstFWUprBoundX HwNm s4p11[2][5]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288	
	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]		
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0	
2 AsstFWUprBoundX HwNm s4p11[6][2]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096	
z_AsstFWUprBoundX_HwNm_s4p11[6][3] 2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240	
:_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240	
, = 1 t-n-1		
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288	

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Name Input Value





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	384
t_AsstFWDefltAssistX_HwNm_u8p8[1]	410
t_AsstFWDefltAssistX_HwNm_u8p8[2]	435
t_AsstFWDefltAssistX_HwNm_u8p8[3]	461
t_AsstFWDefltAssistX_HwNm_u8p8[4]	486
t_AsstFWDefltAssistX_HwNm_u8p8[5]	512
t_AsstFWDefltAssistX_HwNm_u8p8[6]	538
t_AsstFWDefltAssistX_HwNm_u8p8[7] t_AsstFWDefltAssistX_HwNm_u8p8[8]	563 589
t_AsstFWDefitAssistX_HwNm_u8p8[9]	614
t_AsstFWDefltAssistX_HwNm_u8p8[10]	640
t_AsstFWDefltAssistX_HwNm_u8p8[11]	666
t_AsstFWDefltAssistX_HwNm_u8p8[12]	691
t AsstFWDefltAssistX HwNm u8p8[13]	717
t_AsstFWDefltAssistX_HwNm_u8p8[14]	742
t_AsstFWDefltAssistX_HwNm_u8p8[15]	768
t_AsstFWDefltAssistX_HwNm_u8p8[16]	794
t_AsstFWDefltAssistX_HwNm_u8p8[17]	819
t_AsstFWDefltAssistX_HwNm_u8p8[18]	845
t_AsstFWDefltAssistX_HwNm_u8p8[19]	870
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	7373 7578
t_AsstFWDefltAssistY_MtrNm_s4p11[13] t_AsstFWDefltAssistY_MtrNm_s4p11[14]	7782
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	7987
t AsstFWDefitAssistY_MtrNm_s4p11[16]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	8806
t_AsstFWPstepNstepThresh_Cnt_u16[0]	136
t_AsstFWPstepNstepThresh_Cnt_u16[1]	263
t_AsstFWVehSpd_Kph_u9p7[0]	42624
t_AsstFWVehSpd_Kph_u9p7[1]	42752
t_AsstFWVehSpd_Kph_u9p7[2]	42880
t_AsstFWVehSpd_Kph_u9p7[3]	43008
t_AsstFWVehSpd_Kph_u9p7[4]	43136
t_AsstFWVehSpd_Kph_u9p7[5]	43264
t_AsstFWVehSpd_Kph_u9p7[6]	43392
t_AsstFWVehSpd_Kph_u9p7[7]	43520
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2.20000005
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.69999981
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	66.4000015
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lg	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32
0 _ 1 _ 1 _ 1 _ 1 _ 1 _ 1 _ 1 _ 1 _ 1 _	U =

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.97000003	2.97000003 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	263	263 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.29980469	-4.29980469 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.17000008	2.17000008 ± 4.88E-04	<b>~</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.88000011	4.88000011 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>~</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	0.93000007	0.930000007 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-4.29980469	-4.29980469 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>~</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.16 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4
AssistFirewall ActiveKSV M str.K Uls f32	0.019999996
AssistFirewall_ActiveRawAcc_Cnt_M_u16	130
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.79999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.029999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.07000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00899999961
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0799999982
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.9000001
k_AsstFWInpLimitHFA_MtrNm_f32	1.8999998
k_AsstFWInpLimitHysComp_MtrNm_f32	1.3999998
k_AsstFWNstep_Cnt_u16	3060
k_AsstFWPstep_Cnt_u16	1968
k_RestoreThresh_MtrNm_f32	2.5999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2 AsstFWUprBoundX HwNm s4p11[2][2]	
	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
1 1 1 1 1	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
, , , , , ,	
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	8192 10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192 10240

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-16384
2 AsstFWUprBoundY MtrNm s4p11[2][7]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-12288
z_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-10240
z_AsstFWUprBoundY_MtrNm_s4p11[2][9] 2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-8192
z_AsstFWUprBoundY_MtrNm_s4p11[2][10] 2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	4096
2 AsstFWUprBoundY MtrNm s4p11[5][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336
z_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	410
t_AsstFWDefltAssistX_HwNm_u8p8[1]	435
t_AsstFWDefltAssistX_HwNm_u8p8[2]	461 486
t_AsstFWDefltAssistX_HwNm_u8p8[3]	512
t_AsstFWDefltAssistX_HwNm_u8p8[4]	538
t_AsstFWDefltAssistX_HwNm_u8p8[5] t_AsstFWDefltAssistX_HwNm_u8p8[6]	563
t_AsstFWDefltAssistX_HwNm_u8p8[7]	589
t_AsstFWDefltAssistX_HwNm_u8p8[8]	614
t_AsstFWDefitAssistX_HwNm_u8p8[9]	640
t_AsstFWDefltAssistX_HwNm_u8p8[10]	666
t_AsstFWDefitAssistX_HwNm_u8p8[11]	691
t_AsstFWDefltAssistX_HwNm_u8p8[12]	717
t_AsstFWDefitAssistX_HwNm_u8p8[13]	742
t_AsstFWDefitAssistX_HwNm_u8p8[14]	768
t_AsstFWDefitAssistX_HwNm_u8p8[15]	794
t_AsstFWDefitAssistX_HwNm_u8p8[15]  t_AsstFWDefitAssistX_HwNm_u8p8[16]	819
t_AsstFWDefitAssistX_HwNm_u8p8[16]  t_AsstFWDefitAssistX_HwNm_u8p8[17]	845
t_AsstFWDefitAssistX_HwNm_u8p8[17]  t_AsstFWDefitAssistX_HwNm_u8p8[18]	870
t AsstFWDefitAssistX HwNm u8p8[19]	896
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	5734
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6349
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	7168
t AsstFWDefltAssistY MtrNm s4p11[11]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	7578
t AsstFWDefltAssistY MtrNm s4p11[13]	7782
t AsstFWDefltAssistY MtrNm s4p11[14]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	8397
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	8602
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	9011
t AsstFWPstepNstepThresh Cnt u16[0]	137
t_AsstFWPstepNstepThresh_Cnt_u16[1]	267
t_AsstFWVehSpd_Kph_u9p7[0]	45568
t_AsstFWVehSpd_Kph_u9p7[1]	45696
t_AsstFWVehSpd_Kph_u9p7[2]	45824
t_AsstFWVehSpd_Kph_u9p7[3]	45952
t_AsstFWVehSpd_Kph_u9p7[4]	46080
t_AsstFWVehSpd_Kph_u9p7[5]	46208
t_AsstFWVehSpd_Kph_u9p7[6]	46336
t_AsstFWVehSpd_Kph_u9p7[7]	46464
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-8.80000019
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	77.1999969
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	1
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall Per1 HwTorque HwNm f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	
	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.92000008	3.92000008 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	267	267 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-2.89990234	-2.89990234 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.01799989	3.01799989 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.8829999	5.8829999 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.07999992	2.07999992 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-2.89990234	-2.89990234 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>~</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T T			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	-

Test Step 2.17 (Repeat Count = 1)	• • • • • • • • • • • • • • • • • • •
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5
AssistFirewall ActiveKSV M str.K Uls f32	0.029999993
AssistFirewall_ActiveRawAcc_Cnt_M_u16	133
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.8999998
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.039999991
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.08000004
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0099999978
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.090000036
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.19999981
k_AsstFWInpLimitHFA_MtrNm_f32	2
k_AsstFWInpLimitHysComp_MtrNm_f32	1.70000005
k_AsstFWNstep_Cnt_u16	2936
k_AsstFWPstep_Cnt_u16	2091
k_RestoreThresh_MtrNm_f32	2.70000005
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096

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Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096	
2 AsstFWUprBoundX HwNm s4p11[2][5]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336	
:2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0	
	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]		
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336	
:2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384	
2 AsstFWUprBoundX HwNm s4p11[6][2]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-6144 -4096	
	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]		
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	16384	

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ASSISTITEWAII_Per I		MACIMI
Name	Input Value	
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-26624	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-24576	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	6144	
P_AsstFWUprBoundY_MtrNm_s4p11[3][1]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	26624	
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	12288	
P_AsstFWUprBoundY_MtrNm_s4p11[5][5]	14336	
P_AsstFWUprBoundY_MtrNm_s4p11[5][6]	16384	
P_AsstFWUprBoundY_MtrNm_s4p11[5][7]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	22528	
P_AsstFWUprBoundY_MtrNm_s4p11[5][10]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-14336	
P_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288	
P_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240	
P_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192	
P_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096	
P_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0	
P_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	4096	
	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]		

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News	Invest Value
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4] t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	22528
t_AsstFWDefltAssistX_HwNm_u8p8[0]	435
t_AsstFWDefltAssistX_HwNm_u8p8[1]	461
t_AsstFWDefltAssistX_HwNm_u8p8[2]	486
t_AsstFWDefltAssistX_HwNm_u8p8[3]	512
t_AsstFWDefltAssistX_HwNm_u8p8[4]	538
t_AsstFWDefltAssistX_HwNm_u8p8[5]	563
t_AsstFWDefltAssistX_HwNm_u8p8[6]	589
t_AsstFWDefltAssistX_HwNm_u8p8[7]	614
t_AsstFWDefltAssistX_HwNm_u8p8[8]	640
t_AsstFWDefltAssistX_HwNm_u8p8[9]	666
t_AsstFWDefltAssistX_HwNm_u8p8[10]	691
t_AsstFWDefltAssistX_HwNm_u8p8[11]	717
t_AsstFWDefltAssistX_HwNm_u8p8[12]	742
t_AsstFWDefltAssistX_HwNm_u8p8[13]	768
t_AsstFWDefltAssistX_HwNm_u8p8[14]	794
t_AsstFWDefltAssistX_HwNm_u8p8[15]	819
t_AsstFWDefltAssistX_HwNm_u8p8[16]	845
t_AsstFWDefltAssistX_HwNm_u8p8[17]	870
t_AsstFWDefltAssistX_HwNm_u8p8[18]	896
t_AsstFWDefltAssistX_HwNm_u8p8[19]	922
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	5325
t_AsstFWDefitAssistY_MtrNm_s4p11[1]	5530 5734
t_AsstFWDefltAssistY_MtrNm_s4p11[2] t_AsstFWDefltAssistY_MtrNm_s4p11[3]	5939
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	6144
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	9216
t_AsstFWPstepNstepThresh_Cnt_u16[0]	138
t_AsstFWPstepNstepThresh_Cnt_u16[1]	271
t_AsstFWVehSpd_Kph_u9p7[0]	27904
t_AsstFWVehSpd_Kph_u9p7[1]	28032
t_AsstFWVehSpd_Kph_u9p7[2]	28160
t_AsstFWVehSpd_Kph_u9p7[3]	28288
t_AsstFWVehSpd_Kph_u9p7[4]	28416
t_AsstFWVehSpd_Kph_u9p7[5]	28544
t_AsstFWVehSpd_Kph_u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7]  tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	28800 4.0999999
tgt_AssistFirewall_Per1_Defeat_AssistCmd_intinfm_i32.value	4.0399999
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.80000019
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	88.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_le	
	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_i32  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4.8499999	4.8499999 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	271	271 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.89990234	-3.89990234 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.11199999	4.11199999 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.8499999	6.8499999 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.91000009	2.91000009 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-3.89990234	-3.89990234 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	•

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.18 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6
AssistFirewall ActiveKSV M str.K Uls f32	0.039999991
AssistFirewall_ActiveRawAcc_Cnt_M_u16	136
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.09000003
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0199999996
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.100000001
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.5
k_AsstFWInpLimitHFA_MtrNm_f32	2.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	2.0999999
k_AsstFWNstep_Cnt_u16	2812
k_AsstFWPstep_Cnt_u16	2214
k RestoreThresh MtrNm f32	2.79999995
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
	0
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
2 AsstFWUprBoundX HwNm s4p11[5][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
2 AsstFWUprBoundX HwNm s4p11[5][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	6144
z_AsstFWUprBoundY_MtrNm_s4p11[0][0] 2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	18432 20480

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Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	26624
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-14336
z_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-12288
z_asstrwuprBoundY_MtrNm_s4p11[2][6]  2	-12288 -10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	26624
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	28672
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	6144
	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	26624
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	
	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144 4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	

AssistFirewall Per1

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Input Value t2 AsstFWUprBoundY MtrNm s4p11[7][4] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][5] 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][6] 16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][7] 18432 t2 AsstFWUprBoundY MtrNm s4p11[7][8] 20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][9] 22528 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][10] 24576  $t\_AsstFWDefltAssistX\_HwNm\_u8p8[0]$ 461 t\_AsstFWDefltAssistX\_HwNm\_u8p8[1] 486 t AsstFWDefltAssistX HwNm u8p8[2] 512 t\_AsstFWDefltAssistX\_HwNm\_u8p8[3] 538 t AsstFWDefltAssistX HwNm u8p8[4] 563 589 t\_AsstFWDefltAssistX\_HwNm\_u8p8[5] t AsstEWDefltAssistX HwNm u8n8[6] 614 t\_AsstFWDefltAssistX\_HwNm\_u8p8[7] 640 t AsstFWDefltAssistX HwNm u8p8[8] 666 t\_AsstFWDefltAssistX\_HwNm\_u8p8[9] 691 t AsstFWDefltAssistX HwNm u8p8[10] 717 t\_AsstFWDefltAssistX\_HwNm\_u8p8[11] 742 t AsstFWDefltAssistX HwNm u8p8[12] 768 t\_AsstFWDefltAssistX\_HwNm\_u8p8[13] 794 t\_AsstFWDefltAssistX\_HwNm\_u8p8[14] 819 t\_AsstFWDefltAssistX\_HwNm\_u8p8[15] 845 t\_AsstFWDefltAssistX\_HwNm\_u8p8[16] 870 t\_AsstFWDefltAssistX\_HwNm\_u8p8[17] 896 t\_AsstFWDefltAssistX\_HwNm\_u8p8[18] 922 947 t\_AsstFWDefltAssistX\_HwNm\_u8p8[19] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[0] 5530 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[1] 5734 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[2] 5939 t AsstFWDefltAssistY MtrNm s4p11[3] 6144 t AsstFWDefltAssistY\_MtrNm\_s4p11[4] 6349 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[5] 6554 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[6] 6758 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[7] 6963 t AsstFWDefltAssistY MtrNm s4p11[8] 7168 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[9] 7373 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[10] 7578 t AsstFWDefltAssistY MtrNm s4p11[11] 7782 t AsstFWDefltAssistY MtrNm s4p11[12] 7987 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[13] 8192 t AsstFWDefltAssistY MtrNm s4p11[14] 8397 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[15] 8602 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[16] 8806 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[17] 9011 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[18] 9216 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[19] 9421 t\_AsstFWPstepNstepThresh\_Cnt\_u16[0] 139 t\_AsstFWPstepNstepThresh\_Cnt\_u16[1] 275 t\_AsstFWVehSpd\_Kph\_u9p7[0] 30848 t\_AsstFWVehSpd\_Kph\_u9p7[1] 30976 t\_AsstFWVehSpd\_Kph\_u9p7[2] 31104 31232 t\_AsstFWVehSpd\_Kph\_u9p7[3] t\_AsstFWVehSpd\_Kph\_u9p7[4] 31360 t\_AsstFWVehSpd\_Kph\_u9p7[5] 31488 t\_AsstFWVehSpd\_Kph\_u9p7[6] 31616 31744 t AsstFWVehSpd Kph u9p7[7] tgt\_AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32.value 5.0999999 tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lgc.value 0 tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32.value 2 -4  $tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32.value$ tot AssistFirewall Per1 HysteresisComp MtrNm f32.value 0 tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum.value 2 tot AssistFirewall Per1 VehicleSpeed Kph f32.value 99 3000031  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32$ tgt\_AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 BaseAssistCmd MtrNm f32 tot AssistFirewall Per1 BaseAssistCmd MtrNm f32 tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32 tgt\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32 tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Pe  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32 tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HwTorque\_HwNm\_f32 tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$  $tgt\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum$ tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32$ tgt\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.76000023	5.76000023 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	275	275 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.60009766	-4.60009766 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.07499981	5.07499981 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.65999985	7.65999985 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>~</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.9000001	3.9000001 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-4.60009766	-4.60009766 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Τ				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	•

Test Step 2.19 (Repeat Count = 1)	▼ ·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7
AssistFirewall ActiveKSV M str.K Uls f32	0.0500000007
AssistFirewall_ActiveRawAcc_Cnt_M_u16	139
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.059999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.029999993
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.200000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.80000019
k_AsstFWInpLimitHFA_MtrNm_f32	2.4000001
k_AsstFWInpLimitHysComp_MtrNm_f32	2.43000007
k_AsstFWNstep_Cnt_u16	2688
k_AsstFWPstep_Cnt_u16	2337
k_RestoreThresh_MtrNm_f32	2.9000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0

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ASSISTFITEWAII_PETT		(MAC)
Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384	
:2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048	
2 AsstFWUprBoundX HwNm s4p11[6][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]		
	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096	
	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][7]		
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	20480	

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Name	Input Value	
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	26624	
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	28672	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336	
	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]		
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	16384	
P_AsstFWUprBoundY_MtrNm_s4p11[5][5]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	24576	
P_AsstFWUprBoundY_MtrNm_s4p11[5][9]	26624	
P_AsstFWUprBoundY_MtrNm_s4p11[5][10]	28672	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240	
P_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192	
P_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144	
P_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096	
P_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0	
P_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096	
P_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	10240	
2_ASSIF W OPI BOUND 1 _ WILLINITI_S4P 1 1[7][2]		





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	26624
t_AsstFWDefltAssistX_HwNm_u8p8[0]	486
t_AsstFWDefltAssistX_HwNm_u8p8[1]	512
t_AsstFWDefltAssistX_HwNm_u8p8[2]	538
t_AsstFWDefltAssistX_HwNm_u8p8[3]	563
t_AsstFWDefltAssistX_HwNm_u8p8[4]	589
t_AsstFWDefltAssistX_HwNm_u8p8[5]	614
t_AsstFWDefltAssistX_HwNm_u8p8[6] t_AsstFWDefltAssistX_HwNm_u8p8[7]	640 666
t_AsstFWDefitAssistX_HwNm_u8p8[8]	691
t_AsstFWDefltAssistX_HwNm_u8p8[9]	717
t_AsstFWDefltAssistX_HwNm_u8p8[10]	742
t_AsstFWDefltAssistX_HwNm_u8p8[11]	768
t_AsstFWDefltAssistX_HwNm_u8p8[12]	794
t_AsstFWDefltAssistX_HwNm_u8p8[13]	819
t_AsstFWDefltAssistX_HwNm_u8p8[14]	845
t_AsstFWDefltAssistX_HwNm_u8p8[15]	870
t_AsstFWDefltAssistX_HwNm_u8p8[16]	896
t_AsstFWDefltAssistX_HwNm_u8p8[17]	922
t_AsstFWDefltAssistX_HwNm_u8p8[18]	947
t_AsstFWDefltAssistX_HwNm_u8p8[19]	973
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	7987
t_AsstFWDefitAssistY_MtrNm_s4p11[12]	8192 8397
t_AsstFWDefltAssistY_MtrNm_s4p11[13] t_AsstFWDefltAssistY_MtrNm_s4p11[14]	8602
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	9011
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	9626
t_AsstFWPstepNstepThresh_Cnt_u16[0]	140
t_AsstFWPstepNstepThresh_Cnt_u16[1]	279
t_AsstFWVehSpd_Kph_u9p7[0]	33792
t_AsstFWVehSpd_Kph_u9p7[1]	33920
t_AsstFWVehSpd_Kph_u9p7[2]	34048
t_AsstFWVehSpd_Kph_u9p7[3]	34176
t_AsstFWVehSpd_Kph_u9p7[4]	34304
t_AsstFWVehSpd_Kph_u9p7[5]	34432
t_AsstFWVehSpd_Kph_u9p7[6]	34560
t_AsstFWVehSpd_Kph_u9p7[7]	34688
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	123.099998
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_le	· ·
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.6500001	6.6500001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	279	279 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.70019531	-4.70019531 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.21780014	6.21780014 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.76700002	0.76700002 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.80000019	4.80000019 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-4.70019531	-4.70019531 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.20 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8
AssistFirewall ActiveKSV M str.K Uls f32	0.059999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	142
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.29999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.070000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.20000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.039999991
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.30000012
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	2.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	2.77999997
k_AsstFWNstep_Cnt_u16	2564
k_AsstFWPstep_Cnt_u16	2460
k_RestoreThresh_MtrNm_f32	3
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384

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ASSISTRIEWAII_Per I		
Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144	
P_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384	
:_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432	
	-14336	
!_AsstFWUprBoundX_HwNm_s4p11[7][0]		
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240	
?_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192	
P_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144	
P_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096	
_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2048	
P_AsstFWUprBoundX_HwNm_s4p11[7][7]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048	
_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384	
P_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240 8102	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-2048	

AssistFirewall\_Per1





Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-8192
2 AsstFWUprBoundY MtrNm s4p11[2][7]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-2048
z_AsstFWUprBoundY_MtrNm_s4p11[2][9] 2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
2 AsstFWUprBoundY MtrNm s4p11[5][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144
z_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192
2 AsstFWUprBoundY MtrNm s4p11[7][1]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	10240 12288





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	512
t_AsstFWDefltAssistX_HwNm_u8p8[1]	538
t_AsstFWDefltAssistX_HwNm_u8p8[2]	563
t_AsstFWDefltAssistX_HwNm_u8p8[3]	589
t_AsstFWDefltAssistX_HwNm_u8p8[4]	614
t_AsstFWDefltAssistX_HwNm_u8p8[5]	640
t_AsstFWDefltAssistX_HwNm_u8p8[6]	666
t_AsstFWDefltAssistX_HwNm_u8p8[7]	691
t_AsstFWDefltAssistX_HwNm_u8p8[8]	717
t_AsstFWDefltAssistX_HwNm_u8p8[9]	742
t_AsstFWDefltAssistX_HwNm_u8p8[10]	768
t_AsstFWDefltAssistX_HwNm_u8p8[11]	794
t_AsstFWDefltAssistX_HwNm_u8p8[12]	819
t_AsstFWDefltAssistX_HwNm_u8p8[13]	845 870
t_AsstFWDefltAssistX_HwNm_u8p8[14] t_AsstFWDefltAssistX_HwNm_u8p8[15]	870 896
t_AsstFWDefltAssistX_HwNm_u8p8[16]	922
t AsstFWDefitAssistX HwNm u8p8[17]	947
t_AsstFWDefltAssistX_HwNm_u8p8[18]	973
t_AsstFWDefltAssistX_HwNm_u8p8[19]	998
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	9626 9830
t_AsstFWDefitAssistY_MtrNm_s4p11[19] t AsstFWPstepNstepThresh Cnt u16[0]	141
t_AsstFWPstepNstepThresh_Cnt_u16[1]	283
t_AsstFWVehSpd_Kph_u9p7[0]	36736
t_AsstFWVehSpd_Kph_u9p7[1]	36864
t_AsstFWVehSpd_Kph_u9p7[2]	36992
t_AsstFWVehSpd_Kph_u9p7[3]	37120
t_AsstFWVehSpd_Kph_u9p7[4]	37248
t_AsstFWVehSpd_Kph_u9p7[5]	37376
t_AsstFWVehSpd_Kph_u9p7[6]	37504
t_AsstFWVehSpd_Kph_u9p7[7]	37632
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-6
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	234.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_longletering	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7.51999998	7.51999998 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	283	283 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.79980469	-4.79980469 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.56739998	6.56739998 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.19200015	2.19199991 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.79999971	1.79999995 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-4.79980469	-4.79980469 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.21 (Repeat Count = 1)	✓
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall ActiveKSV M str.K Uls f32	0.0700000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	123
AssistFirewall AsstReducedPerfSV Cnt M Iqc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.3999998
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	8
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.079999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.29999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.050000007
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.40000006
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.4000001
k_AsstFWInpLimitHFA_MtrNm_f32	2.7999995
k_AsstFWInpLimitHysComp_MtrNm_f32	3.13000011
k_AsstFWNstep_Cnt_u16	2440
k_AsstFWPstep_Cnt_u16	2583
k_RestoreThresh_MtrNm_f32	3.099999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336
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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2040
	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7] t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	0

AssistFirewall\_Per1





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-2048
	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288
t2 AsstFWUprBoundY MtrNm s4p11[5][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144
	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	
	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	12288 -16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288 -16384 -14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	12288 -16384





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144 4006
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-4096 -2048
t2_Asst WopiBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	538
t_AsstFWDefltAssistX_HwNm_u8p8[1]	563
t_AsstFWDefltAssistX_HwNm_u8p8[2]	589
t_AsstFWDefltAssistX_HwNm_u8p8[3]	614
t_AsstFWDefltAssistX_HwNm_u8p8[4]	640
t_AsstFWDefltAssistX_HwNm_u8p8[5]	666
t_AsstFWDefltAssistX_HwNm_u8p8[6]	691
t_AsstFWDefltAssistX_HwNm_u8p8[7]	717
t_AsstFWDefltAssistX_HwNm_u8p8[8]	742
t_AsstFWDefltAssistX_HwNm_u8p8[9]	768 794
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	819
t_AsstFWDefltAssistX_HwNm_u8p8[12]	845
t_AsstFWDefltAssistX_HwNm_u8p8[13]	870
t_AsstFWDefltAssistX_HwNm_u8p8[14]	896
t_AsstFWDefltAssistX_HwNm_u8p8[15]	922
t_AsstFWDefltAssistX_HwNm_u8p8[16]	947
t_AsstFWDefltAssistX_HwNm_u8p8[17]	973
t_AsstFWDefltAssistX_HwNm_u8p8[18]	998
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1024
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[6] t_AsstFWDefltAssistY_MtrNm_s4p11[7]	7373 7578
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[19] t AsstFWPstepNstepThresh Cnt u16[0]	10035 142
t_AsstFWPstepNstepThresh_Cnt_u16[1]	287
t_AsstFWVehSpd_Kph_u9p7[0]	39680
t_AsstFWVehSpd_Kph_u9p7[1]	39808
t_AsstFWVehSpd_Kph_u9p7[2]	39936
t_AsstFWVehSpd_Kph_u9p7[3]	40064
t_AsstFWVehSpd_Kph_u9p7[4]	40192
t_AsstFWVehSpd_Kph_u9p7[5]	40320
t_AsstFWVehSpd_Kph_u9p7[6]	40448
t_AsstFWVehSpd_Kph_u9p7[7]	40576
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-7
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	0
tgt_AssistFirewall_Per1_verlicleSpeed_kpri_is2.value  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_UIs_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.023	1.023 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	287	287 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.89990234	-4.89990234 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.90399981	7.90399981 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.79499984	2.79500008 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.19999981	2.20000005 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-4.89990234	-4.89990234 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

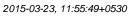
T .			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	•

Test Step 2.22 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	2.20000005
AssistFirewall ActiveKSV M str.K UIs f32	0.079999982
AssistFirewall_ActiveRawAcc_Cnt_M_u16	246
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall CombAsstSV MtrNm M f32	1.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.1000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.090000036
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.3999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.099999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.059999987
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.5
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.69999981
k AsstFWInpLimitHFA MtrNm f32	3
k_AsstFWInpLimitHysComp_MtrNm_f32	3.48000002
k_AsstFWNstep_Cnt_u16	2316
k_AsstFWPstep_Cnt_u16	2706
k RestoreThresh MtrNm f32	3.20000005
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2 AsstFWUprBoundX HwNm s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2 AsstFWUprBoundX HwNm s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2 AsstFWUprBoundX HwNm s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192
	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0177
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096





Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	26624
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288
	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
2 AsstFWUprBoundY MtrNm s4p11[4][6]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-30720
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
, , , , , , , , , , , , , , , , , , , ,	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	563
t_AsstFWDefltAssistX_HwNm_u8p8[1]	589
t_AsstFWDefltAssistX_HwNm_u8p8[2]	614
t_AsstFWDefltAssistX_HwNm_u8p8[3]	640
t_AsstFWDefltAssistX_HwNm_u8p8[4]	666
t_AsstFWDefltAssistX_HwNm_u8p8[5]	691
t_AsstFWDefltAssistX_HwNm_u8p8[6]	717
t_AsstFWDefltAssistX_HwNm_u8p8[7]	742
t_AsstFWDefltAssistX_HwNm_u8p8[8]	768
t_AsstFWDefltAssistX_HwNm_u8p8[9]	794 819
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	845
t_AsstFWDefltAssistX_HwNm_u8p8[12]	870
t_AsstFWDefltAssistX_HwNm_u8p8[13]	896
t_AsstFWDefltAssistX_HwNm_u8p8[14]	922
t_AsstFWDefltAssistX_HwNm_u8p8[15]	947
t_AsstFWDefltAssistX_HwNm_u8p8[16]	973
t_AsstFWDefltAssistX_HwNm_u8p8[17]	998
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1050
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	7168 7373
t_AsstFWDefltAssistY_MtrNm_s4p11[5] t_AsstFWDefltAssistY_MtrNm_s4p11[6]	7578
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[18] t_AsstFWDefltAssistY_MtrNm_s4p11[19]	10035 10240
t AsstFWPstepNstepThresh Cnt u16[0]	143
t_AsstFWPstepNstepThresh_Cnt_u16[1]	291
t_AsstFWVehSpd_Kph_u9p7[0]	42624
t_AsstFWVehSpd_Kph_u9p7[1]	42752
t_AsstFWVehSpd_Kph_u9p7[2]	42880
t_AsstFWVehSpd_Kph_u9p7[3]	43008
t_AsstFWVehSpd_Kph_u9p7[4]	43136
t_AsstFWVehSpd_Kph_u9p7[5]	43264
t_AsstFWVehSpd_Kph_u9p7[6]	43392
t_AsstFWVehSpd_Kph_u9p7[7]	43520
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	255
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.02400017	2.02399993 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	291	291 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5	-5 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.81100011	1.81099999 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.61399984	3.61400008 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1	1 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-5	-5 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

	Test Step 2.23 (Repeat Count = 1)  ✓	
Name	Input Value	
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.0999999	
AssistFirewall ActiveKSV M str.K Uls f32	0.00600000005	
AssistFirewall ActiveRawAcc Cnt M u16	369	
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.60000002	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0599999987	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998	
AssistFirewall LwrBoundKSV M str.SV Uls f32	1	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.090000036	
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.0999999	
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.029999993	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6	
k_AsstFWInpLimitHFA_MtrNm_f32	3.20000005	
k_AsstFWInpLimitHysComp_MtrNm_f32	3.82999992	
k_AsstFWNstep_Cnt_u16	2192	
k_AsstFWPstep_Cnt_u16	2829	
k_RestoreThresh_MtrNm_f32	3.29999995	
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336	
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288	
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-12288	
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240	





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192 10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10] t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-8192
t2_Asst WuprBoundX_HwNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7] t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2 AsstFWUprBoundX HwNm s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2 AsstFWUprBoundX HwNm s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	4096

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	26624
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	28672
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336
:2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-12288
	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
2 AsstFWUprBoundY MtrNm s4p11[4][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
2 AsstFWUprBoundY MtrNm s4p11[4][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-26624
	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192
:2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144
12_73311 VVOPIDOUNU I_WILINIII_54P I I[1][5]	-01 <del>111</del>





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_Asst WopiboundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	589
t_AsstFWDefltAssistX_HwNm_u8p8[1]	614
t_AsstFWDefltAssistX_HwNm_u8p8[2]	640
t_AsstFWDefltAssistX_HwNm_u8p8[3]	666
t_AsstFWDefltAssistX_HwNm_u8p8[4]	691
t_AsstFWDefltAssistX_HwNm_u8p8[5]	717
t_AsstFWDefltAssistX_HwNm_u8p8[6]	742
t_AsstFWDefltAssistX_HwNm_u8p8[7]	768
t_AsstFWDefltAssistX_HwNm_u8p8[8]	794
t_AsstFWDefltAssistX_HwNm_u8p8[9]	819
t_AsstFWDefltAssistX_HwNm_u8p8[10]	845 870
t_AsstFWDefltAssistX_HwNm_u8p8[11] t_AsstFWDefltAssistX_HwNm_u8p8[12]	896
t_AsstFWDefitAssistX_HwNm_u8p8[13]	922
t_AsstFWDefitAssistX_HwNm_u8p8[14]	947
t_AsstFWDefitAssistX_HwNm_u8p8[15]	973
t_AsstFWDefltAssistX_HwNm_u8p8[16]	998
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1075
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	7782 7987
t_AsstFWDefltAssistY_MtrNm_s4p11[7] t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	8602
t AsstFWDefltAssistY MtrNm s4p11[11]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	10445
t_AsstFWPstepNstepThresh_Cnt_u16[0]	144
t_AsstFWPstepNstepThresh_Cnt_u16[1]	295
t_AsstFWVehSpd_Kph_u9p7[0]	45568
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	45696 45824
t_AsstFWVehSpd_Kph_u9p7[3]	45952
t_AsstFWVehSpd_Kph_u9p7[4]	46080
t_AsstFWVehSpd_Kph_u9p7[5]	46208
t_AsstFWVehSpd_Kph_u9p7[6]	46336
t_AsstFWVehSpd_Kph_u9p7[7]	46464
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-10
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	22.200008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lt_Rt_Att_Att_Att_Att_Att_Att_Att_Att_Att	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
THE THE THE PROJECT INCHAIR ASSIST HE WAIT FOR DETECT ASSIST SELVICE CITE IN	The state of the s
	tot Assisteirewall Peri Higheregassist Mitrim 132
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tdt AssistFirewall Per1_HwTorque HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.06939983	5.06939983 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	295	295 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.10009766	-5.10009766 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.46600008	4.46600008 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.459999979	0.460000008 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.85699987	2.85700011 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-5.10009766	-5.10009766 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

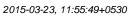
T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.24 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall ActiveKSV M str.K Uls f32	0.059999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	492
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	1.7000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0089999961
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.60000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.0999999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.079999982
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.059999987
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6.30000019
k AsstFWInpLimitHFA MtrNm f32	3.4000001
k_AsstFWInpLimitHysComp_MtrNm_f32	4.17999983
k_AsstFWNstep_Cnt_u16	2068
k_AsstFWPstep_Cnt_u16	2952
k RestoreThresh MtrNm f32	3.4000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2 AsstFWUprBoundX HwNm s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192
	1 0.00

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710010tt 110Wall_1 011	
Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5] t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_Asst WopiBoundX_HwNm_s4p11[5][8]	8192
t2_Asst WoprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2 AsstFWUprBoundX HwNm s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
tz_Assti WopibodildX_HWNII_s+p+1[/][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096 -2048 0





Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-10240 -8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]		
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	6144	
t2_AsstrWUprBoundY_MtrNm_s4p11[4][0]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	12288	
12_AsstFWUprBoundY_MtrNm_s4p11[4][4]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	26624	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-26624	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-24576	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-4096	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] t_AsstFWDefltAssistX_HwNm_u8p8[0]	614
t_AsstFWDefltAssistX_HwNm_u8p8[1]	640
t_AsstFWDefltAssistX_HwNm_u8p8[2]	666
t_AsstFWDefltAssistX_HwNm_u8p8[3]	691
t_AsstFWDefltAssistX_HwNm_u8p8[4]	717
t_AsstFWDefltAssistX_HwNm_u8p8[5]	742
t_AsstFWDefltAssistX_HwNm_u8p8[6]	768
t_AsstFWDefltAssistX_HwNm_u8p8[7]	794
t_AsstFWDefltAssistX_HwNm_u8p8[8]	819
t_AsstFWDefltAssistX_HwNm_u8p8[9]	845
t_AsstFWDefltAssistX_HwNm_u8p8[10]	870
t_AsstFWDefltAssistX_HwNm_u8p8[11]	896
t_AsstFWDefltAssistX_HwNm_u8p8[12]	922
t_AsstFWDefltAssistX_HwNm_u8p8[13]	947
t_AsstFWDefltAssistX_HwNm_u8p8[14]	973
t_AsstFWDefltAssistX_HwNm_u8p8[15]	998
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1101
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	7168 7373
t_AsstFWDefltAssistY_MtrNm_s4p11[3] t_AsstFWDefltAssistY_MtrNm_s4p11[4]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	7987
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	10650
t_AsstFWPstepNstepThresh_Cnt_u16[0]	145
t_AsstFWPstepNstepThresh_Cnt_u16[1]	299
t_AsstFWVehSpd_Kph_u9p7[0]	0
t_AsstFWVehSpd_Kph_u9p7[1]	0
t_AsstFWVehSpd_Kph_u9p7[2]	0
t_AsstFWVehSpd_Kph_u9p7[3]	0
t_AsstFWVehSpd_Kph_u9p7[4]	0
t_AsstFWVehSpd_Kph_u9p7[5] t_AsstFWVehSpd_Kph_u9p7[6]	0
t_AsstFWVehSpd_Kph_u9p7[7]	0
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3.099999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	10.1999998
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
<u> </u>	

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.85399985	3.85400009 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	299	299 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.29980469	3.29980469 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.17559981	3.17560005 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.61199999	5.61199999 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.18799996	2.18799996 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.29980469	3.29980469 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~

T ✓				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.25 (Repeat Count = 1)	· ·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	5.0999999
AssistFirewall ActiveKSV M str.K Uls f32	0.00800000038
AssistFirewall_ActiveRawAcc_Cnt_M_u16	615
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall CombAsstSV MtrNm M f32	1.79999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0099999978
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.70000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.090000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.099999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.070000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6.5999999
k_AsstFWInpLimitHFA_MtrNm_f32	3.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	4.53000021
k_AsstFWNstep_Cnt_u16	1944
k_AsstFWPstep_Cnt_u16	3075
k_RestoreThresh_MtrNm_f32	3.5
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144

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Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240	
2 AsstFWUprBoundX HwNm s4p11[6][2]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144	
, , , , , , , , , , , , , , , , , , , ,		
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096 -2049	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096	
P_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096	
P_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0	
P_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192	
	10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288	
:_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144	
2_A33ti WOpiBodild1_Wti14iii_34p11[0][0]		

AssistFirewall\_Per1



Name	Innut Value
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10] t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144 -4096
t2 AcctEM/InrRoundV MtrNm c4c44[7][2]	74417711
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	640
t_AsstFWDefltAssistX_HwNm_u8p8[1]	666
t_AsstFWDefltAssistX_HwNm_u8p8[2]	691
t_AsstFWDefltAssistX_HwNm_u8p8[3]	717
t_AsstFWDefltAssistX_HwNm_u8p8[4]	742
t_AsstFWDefltAssistX_HwNm_u8p8[5]	768
t_AsstFWDefltAssistX_HwNm_u8p8[6]	794
t_AsstFWDefltAssistX_HwNm_u8p8[7]	819
t_AsstFWDefltAssistX_HwNm_u8p8[8]	845
t_AsstFWDefltAssistX_HwNm_u8p8[9]	870
t_AsstFWDefltAssistX_HwNm_u8p8[10]	896
t_AsstFWDefltAssistX_HwNm_u8p8[11]	922
t_AsstFWDefltAssistX_HwNm_u8p8[12]	947
t_AsstFWDefltAssistX_HwNm_u8p8[13]	973
t_AsstFWDefltAssistX_HwNm_u8p8[14]	998
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[17] t_AsstFWDefltAssistX_HwNm_u8p8[18]	1075 1101
t_AsstFWDefitAssistX_HwNm_u8p8[19]	1126
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	7373
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	10240
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[19] t AsstFWPstepNstepThresh Cnt u16[0]	10854 146
t_AsstFWPstepNstepThresh_Cnt_u16[1]	303
t_AsstFWVehSpd_Kph_u9p7[0]	65408
t_AsstFWVehSpd_Kph_u9p7[1]	65408
t_AsstFWVehSpd_Kph_u9p7[2]	65408
t_AsstFWVehSpd_Kph_u9p7[3]	65408
t_AsstFWVehSpd_Kph_u9p7[4]	65408
t_AsstFWVehSpd_Kph_u9p7[5]	65408
t_AsstFWVehSpd_Kph_u9p7[6]	65408
t_AsstFWVehSpd_Kph_u9p7[7]	65408
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	20.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.05919981	5.05919981 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	303	303 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.39990234	3.39990234 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.17000008	4.17000008 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.63999987	4.63999987 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.09299994	3.09299994 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.39990234	3.39990234 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	✓

T			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.26 (Repeat Count = 1)	value of the second of the sec
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.099999
AssistFirewall ActiveKSV M str.K Uls f32	0.00899999961
AssistFirewall_ActiveRawAcc_Cnt_M_u16	738
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.8999998
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.019999996
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.079999982
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6.9000001
k_AsstFWInpLimitHFA_MtrNm_f32	3.79999995
k_AsstFWInpLimitHysComp_MtrNm_f32	4.88000011
k_AsstFWNstep_Cnt_u16	1820
k_AsstFWPstep_Cnt_u16	3198
k_RestoreThresh_MtrNm_f32	3.5999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4	204 K





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-4096
t2_Asst WopiBoundY_MtrNm_s4p11[4][7]	-2048
	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	24576
	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048
	0

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Input Value t2 AsstFWUprBoundY MtrNm s4p11[7][4] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][5] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][6] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][7] 8192 t2 AsstFWUprBoundY MtrNm s4p11[7][8] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][9] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][10] 14336  $t\_AsstFWDefltAssistX\_HwNm\_u8p8[0]$ 666 t\_AsstFWDefltAssistX\_HwNm\_u8p8[1] 691 t AsstFWDefltAssistX HwNm u8p8[2] 717 t\_AsstFWDefltAssistX\_HwNm\_u8p8[3] 742 t AsstFWDefltAssistX HwNm u8p8[4] 768 794 t\_AsstFWDefltAssistX\_HwNm\_u8p8[5] t AsstEWDefltAssistX HwNm u8n8[6] 819 t\_AsstFWDefltAssistX\_HwNm\_u8p8[7] 845 t AsstFWDefltAssistX HwNm u8p8[8] 870 t\_AsstFWDefltAssistX\_HwNm\_u8p8[9] 896 t AsstFWDefltAssistX HwNm u8p8[10] 922 t\_AsstFWDefltAssistX\_HwNm\_u8p8[11] 947 t AsstFWDefltAssistX HwNm u8p8[12] 973 t\_AsstFWDefltAssistX\_HwNm\_u8p8[13] 998 t\_AsstFWDefltAssistX\_HwNm\_u8p8[14] 1024 t\_AsstFWDefltAssistX\_HwNm\_u8p8[15] 1050 t\_AsstFWDefltAssistX\_HwNm\_u8p8[16] 1075 t\_AsstFWDefltAssistX\_HwNm\_u8p8[17] 1101 t\_AsstFWDefltAssistX\_HwNm\_u8p8[18] 1126 1152 t\_AsstFWDefltAssistX\_HwNm\_u8p8[19] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[0] 7168 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[1] 7373 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[2] 7578 7782 t AsstFWDefltAssistY MtrNm s4p11[3] t AsstFWDefltAssistY\_MtrNm\_s4p11[4] 7987 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[5] 8192 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[6] 8397 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[7] 8602 t AsstFWDefltAssistY MtrNm s4p11[8] 8806 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[9] 9011 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[10] 9216 t AsstFWDefltAssistY MtrNm s4p11[11] 9421 t AsstFWDefltAssistY MtrNm s4p11[12] 9626 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[13] 9830 10035 t AsstFWDefltAssistY MtrNm s4p11[14] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[15] 10240 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[16] 10445 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[17] 10650 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[18] 10854 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[19] 11059 t\_AsstFWPstepNstepThresh\_Cnt\_u16[0] 147 t\_AsstFWPstepNstepThresh\_Cnt\_u16[1] 307 12800 t\_AsstFWVehSpd\_Kph\_u9p7[0] t\_AsstFWVehSpd\_Kph\_u9p7[1] 12800 t\_AsstFWVehSpd\_Kph\_u9p7[2] 12800 12800 t\_AsstFWVehSpd\_Kph\_u9p7[3] t\_AsstFWVehSpd\_Kph\_u9p7[4] 12800 t\_AsstFWVehSpd\_Kph\_u9p7[5] 12800 t\_AsstFWVehSpd\_Kph\_u9p7[6] 12800 12800 t AsstFWVehSpd Kph u9p7[7] tgt\_AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32.value 7 tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lgc.value 0 tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32.value 2 3  $tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32.value$ 5.0999999 tot AssistFirewall Per1 HysteresisComp MtrNm f32.value tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum.value tot AssistFirewall Per1 VehicleSpeed Kph f32.value  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32$ tgt\_AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 BaseAssistCmd MtrNm f32 tot AssistFirewall Per1 BaseAssistCmd MtrNm f32 tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32 tgt\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32 tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Pe  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HwTorque\_HwNm\_f32$ tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$  $tgt\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum$ tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32$ tgt\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32

AssistFirewall\_Per1







Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][8] t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	-20480 -20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	-20480 -20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0] t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][4] t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-20480 -20480
t2_AsstFWUprBoundX_HWNm_s4p11[7][6] t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-20480 -20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240

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7.0010ti II OVAII_I OTT	
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
12_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-18432
12_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-8192
12_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048
	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	691
t_AsstFWDefltAssistX_HwNm_u8p8[1]	717
t_AsstFWDefltAssistX_HwNm_u8p8[2]	742
t_AsstFWDefltAssistX_HwNm_u8p8[3]	768
t_AsstFWDefltAssistX_HwNm_u8p8[4]	794
t_AsstFWDefltAssistX_HwNm_u8p8[5]	819
t_AsstFWDefltAssistX_HwNm_u8p8[6]	845
t_AsstFWDefltAssistX_HwNm_u8p8[7]	870
t_AsstFWDefltAssistX_HwNm_u8p8[8]	896
t_AsstFWDefltAssistX_HwNm_u8p8[9]	922
t_AsstFWDefltAssistX_HwNm_u8p8[10]	947
t_AsstFWDefltAssistX_HwNm_u8p8[11]	973
t_AsstFWDefltAssistX_HwNm_u8p8[12]	998
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[17] t_AsstFWDefltAssistX_HwNm_u8p8[18]	1126 1152
t_AsstFWDefitAssistX_mwNrii_uopo[16]  t AsstFWDefitAssistX HwNm_u8p8[19]	1178
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[19] t_AsstFWPstepNstepThresh_Cnt_u16[0]	11264 148
t_AsstFWPstepNstepThresh_Cnt_u16[1]	311
t_AsstFWVehSpd_Kph_u9p7[0]	1408
t_AsstFWVehSpd_Kph_u9p7[1]	1536
t_AsstFWVehSpd_Kph_u9p7[2]	1664
t_AsstFWVehSpd_Kph_u9p7[3]	1792
t_AsstFWVehSpd_Kph_u9p7[4]	1920
t_AsstFWVehSpd_Kph_u9p7[5]	2048
t_AsstFWVehSpd_Kph_u9p7[6]	2176
t_AsstFWVehSpd_Kph_u9p7[7]	2304
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	40.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	1 -
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

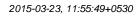
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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.96000004	3.96000004 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	311	311 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.89990234	4.89990234 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.37989998	6.37989998 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.96799994	6.96799994 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.37099981	4.37099981 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4.89990234	4.89990234 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

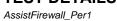
T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.28 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5
AssistFirewall ActiveKSV M str.K Uls f32	0.019999996
AssistFirewall_ActiveRawAcc_Cnt_M_u16	984
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.039999991
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00899999961
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.099999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.10000001
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	7.5
k_AsstFWInpLimitHFA_MtrNm_f32	4.19999981
k_AsstFWInpLimitHysComp_MtrNm_f32	5.57999992
k_AsstFWNstep_Cnt_u16	1572
k_AsstFWPstep_Cnt_u16	3444
k_RestoreThresh_MtrNm_f32	3.79999995
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	20480





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2 AsstFWUprBoundX HwNm s4p11[4][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	20480
t2_Asst WoprboundX_nwnn_s4p11[4][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][4] t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	20480
	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	





18432
20480
22528
-8192
-6144
-4096
-2048
0
2048
4096
6144
8192 10240
12288
-2048
0
2048
4096
6144
8192
10240
12288
14336
16384
18432
-24576
-22528
-20480
-18432
-16384
-14336
-12288
-10240
-8192
-6144
-4096 -4000
-12288 -10240
-8192
-6144
-4096
-2048
0
2048
4096
6144
8192
-18432
-16384
-14336
-12288
-10240
-8192
-6144
-4096
-2048
0
2048
-2048
0
2048
4096
6144
8192 10240
10240 12288
14336
14336
18432
10706
0

AssistFirewall\_Per1

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Name	Input Value
Name t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	717
t_AsstFWDefltAssistX_HwNm_u8p8[1]	742
t_AsstFWDefltAssistX_HwNm_u8p8[2]	768
t_AsstFWDefltAssistX_HwNm_u8p8[3]	794
t_AsstFWDefltAssistX_HwNm_u8p8[4]	819
t_AsstFWDefltAssistX_HwNm_u8p8[5]	845
t_AsstFWDefltAssistX_HwNm_u8p8[6]	870
t_AsstFWDefltAssistX_HwNm_u8p8[7]	896
t_AsstFWDefltAssistX_HwNm_u8p8[8]	922
t_AsstFWDefltAssistX_HwNm_u8p8[9]	947
t_AsstFWDefltAssistX_HwNm_u8p8[10]	973
t_AsstFWDefltAssistX_HwNm_u8p8[11]	998
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[16] t_AsstFWDefltAssistX_HwNm_u8p8[17]	1126 1152
, , ,	
t_AsstFWDefltAssistX_HwNm_u8p8[18] t_AsstFWDefltAssistX_HwNm_u8p8[19]	1178 1203
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	11469
t_AsstFWPstepNstepThresh_Cnt_u16[0]	149
t_AsstFWPstepNstepThresh_Cnt_u16[1]	315
t_AsstFWVehSpd_Kph_u9p7[0]	4352
t_AsstFWVehSpd_Kph_u9p7[1]	4480
t_AsstFWVehSpd_Kph_u9p7[2]	4608 4736
t_AsstFWVehSpd_Kph_u9p7[3]	4/36
t_AsstFWVehSpd_Kph_u9p7[4] t_AsstFWVehSpd_Kph_u9p7[5]	4864
t_AsstFWVehSpd_Kph_u9p7[6]	5120
t_AsstFWVehSpd_Kph_u9p7[7]	5248
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	50.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tot Dto Inst An AssistEirough AssistEirough Dord CombinedAssist MtrNm f22	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Iq	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

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AssistFirewall Per1

Status\_Cnt\_T\_enum

NTC\_Cnt\_T\_enum

Param\_Cnt\_T\_u08

Status\_Cnt\_T\_enum

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**Actual Value Expected Value** AssistFirewall\_ActiveKSV\_M\_str.SV\_Uls\_f32 4.9000001 ± 4.88E-04 4.9000001 AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16 315 315 ± 1 AssistFirewall\_AsstReducedPerfSV\_Cnt\_M\_lgc AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32 5.60009766 5.60009766 ± 4.88E-04 AssistFirewall\_HiFreqKSV\_M\_str.LPF\_Str.SV\_Uls\_f32 4.08400011 4.08400011 ± 4.88E-04 AssistFirewall\_LwrBoundKSV\_M\_str.SV\_Uls\_f32 7.9369998 7.9369998 ± 4.88E-04 AssistFirewall\_PNCountStatus\_Cnt\_M\_lgc 5.38999987 5.38999987 ± 4.88E-04  $AssistFirewall\_UprBoundKSV\_M\_str.SV\_Uls\_f32$ tgt\_AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32.value 1 ± 3.05E-05 5.60009766 5.60009766 ± 9.77E-04  $tgt\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32.value$ NTC\_Cnt\_T\_enum 0xC6 0xC6 Param\_Cnt\_T\_u08 0x01 0x01

0x01

0xC9

0x01

0x01

Τ				<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result	
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~	
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>	
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~	
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>	
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	•	

0x01

0xC9

0x01

0x01

Name	Input Value	
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6	
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.029999993	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1107	
Assistinewall_Activertawacc_ont_w_uro	1	
Assist Tewali_AssixeducedreTGV_CTI_M_igc	-2.29999995	
Assist Firewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007	
Assist liewall_HiFreqKSV_M_str.CF_Uls_f32	1.0199998	
.ssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.10000002	
Assisti ilewaii_EwiBoundKSV_M_str.K_Uls_f32	0.0099999978	
ssisti ilewaii_Ewibound3v_iii_sti.k_ois_i32	0	
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4	
·	0.20000003	
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32  Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
кте_msr_Ap_Assistrirewaii k_AsstFWInpLimitBaseAsst_MtrNm_f32	тус_кте_пізс_Ар_Assistrilewali 7.80000019	
: AsstFWInpLimithFA MtrNm f32	4.40000019	
	5.92999983	
_AsstFWInpLimitHysComp_MtrNm_f32	5.92999963	
_AsstFWNstep_Cnt_u16	3567	
_AsstFWPstep_Cnt_u16	111	
RestoreThresh_MtrNm_f32	3.9000001	
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0	
2_AsstFWUprBoundX_HwNm_s4p11[0][1]		
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0	
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0	
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0	
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0	
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0	
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0	
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0	
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	0	
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0	
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0	
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0	
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0	
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0	
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0	
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0	
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0	
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0	
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0	

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AssistFirewall_Per1	TO TO TO THE TOTAL PARTY OF THE
lame	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
P_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
P_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
P_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
P_AsstFWUprBoundX_HwNm_s4p11[2][9]	0
P_AsstFWUprBoundX_HwNm_s4p11[2][10]	0
P_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
P_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
	0
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
P_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
P_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
P_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
P_AsstFWUprBoundX_HwNm_s4p11[5][3]	0
P_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
P_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
P_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	0
P_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
	0
P_AsstFWUprBoundX_HwNm_s4p11[6][4]  AsstFWUprBoundX_HwNm_s4p11[6][5]	0
_	0
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0 0
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
P_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
P_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
P_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	0
P_AsstFWUprBoundY_MtrNm_s4p11[0][0]	4096
P_AsstFWUprBoundY_MtrNm_s4p11[0][1]	6144
	8192
P_AsstFWUprBoundY_MtrNm_s4p11[0][2]	
	10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240 12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][3] 2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	

AssistFirewall\_Per1





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-16384 -14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-10240
t2_Asst WoprBoundY_MtrNm_s4p11[1][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7] t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096 0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_Asst WoprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	12288





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	742
t_AsstFWDefltAssistX_HwNm_u8p8[1]	768
t_AsstFWDefltAssistX_HwNm_u8p8[2]	794
t_AsstFWDefltAssistX_HwNm_u8p8[3]	819
t_AsstFWDefltAssistX_HwNm_u8p8[4]	845
t_AsstFWDefltAssistX_HwNm_u8p8[5]	870
t_AsstFWDefltAssistX_HwNm_u8p8[6]	896
t_AsstFWDefltAssistX_HwNm_u8p8[7]	922
t_AsstFWDefltAssistX_HwNm_u8p8[8]	947
t_AsstFWDefltAssistX_HwNm_u8p8[9]	973
t_AsstFWDefltAssistX_HwNm_u8p8[10]	998
t_AsstFWDefitAssistX_HwNm_u8p8[11]	1024
t AsstFWDefitAssistX HwNm u8p8[12]	
	1050
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1229
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	11059
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	11264
	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	11674
t_AsstFWPstepNstepThresh_Cnt_u16[0]	150
t_AsstFWPstepNstepThresh_Cnt_u16[1]	319
t_AsstFWVehSpd_Kph_u9p7[0]	7296
t_AsstFWVehSpd_Kph_u9p7[1]	7424
t_AsstFWVehSpd_Kph_u9p7[2]	7552
t_AsstFWVehSpd_Kph_u9p7[3]	7680
t_AsstFWVehSpd_Kph_u9p7[4]	7808
t_AsstFWVehSpd_Kph_u9p7[5]	7936
t_AsstFWVehSpd_Kph_u9p7[6]	8064
t_AsstFWVehSpd_Kph_u9p7[7]	8192
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2.20000005
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-6
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	60.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_intf\(\text{int}\) tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall\_Per1

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N	A - 4 I V-I	From a set of Malica	D14
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.82000017	5.82000017 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	319	319 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.70019531	-5.70019531 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.17999983	5.17999983 ± 4.88E-04	-
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.199	1.199 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	-
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1	1 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-5.70019531	-5.70019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	-
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>*</b>

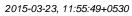
Т				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	•
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.30 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	7
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.039999991
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1230
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-2.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0599999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.02999997
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.019999996
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.300000012
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	8.10000038
k_AsstFWInpLimitHFA_MtrNm_f32	4.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	6.28000021
k_AsstFWNstep_Cnt_u16	1324
k_AsstFWPstep_Cnt_u16	3690
k RestoreThresh MtrNm f32	4
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0
_ ,	





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2 AsstFWUprBoundX HwNm s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
	-8192
tz_asstfvuprboungy_intrinm_s4p11[U][U]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	I -614 <del>4</del>
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096 -2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096 -2048 0





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240
	12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
:2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144 4006
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-4096 -2048
t2_Asst WopiBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	768
t_AsstFWDefltAssistX_HwNm_u8p8[1]	794
t_AsstFWDefltAssistX_HwNm_u8p8[2]	819
t_AsstFWDefltAssistX_HwNm_u8p8[3]	845
t_AsstFWDefltAssistX_HwNm_u8p8[4]	870
t_AsstFWDefltAssistX_HwNm_u8p8[5]	896
t_AsstFWDefltAssistX_HwNm_u8p8[6]	922
t_AsstFWDefltAssistX_HwNm_u8p8[7]	947
t_AsstFWDefltAssistX_HwNm_u8p8[8]	973
t_AsstFWDefltAssistX_HwNm_u8p8[9]	998
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[11] t_AsstFWDefltAssistX_HwNm_u8p8[12]	1050 1075
t_AsstFWDefitAssistX_HwNm_u8p8[13]	1101
t AsstFWDefitAssistX HwNm u8p8[14]	1126
t_AsstFWDefitAssistX_HwNm_u8p8[15]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1254
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	9626 9830
t_AsstFWDefltAssistY_MtrNm_s4p11[9] t_AsstFWDefltAssistY_MtrNm_s4p11[10]	10035
t AsstFWDefitAssistY MtrNm s4p11[11]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	10445
t AsstFWDefltAssistY MtrNm s4p11[13]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	11878
t_AsstFWPstepNstepThresh_Cnt_u16[0]	151
t_AsstFWPstepNstepThresh_Cnt_u16[1]	323
t_AsstFWVehSpd_Kph_u9p7[0]	10240
t_AsstFWVehSpd_Kph_u9p7[1]	10368
t_AsstFWVehSpd_Kph_u9p7[2]	10496
t_AsstFWVehSpd_Kph_u9p7[3] t_AsstFWVehSpd_Kph_u9p7[4]	10624 10752
t_AsstFWVehSpd_Kph_u9p7[5]	10880
t_AsstFWVehSpd_Kph_u9p7[6]	11008
t_AsstFWVehSpd_Kph_u9p7[7]	11136
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3.099999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-7
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	70.1999969
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
WE THE HIS ALL ASSISTED WAI ASSISTED WAIL PART VANICIAS DAPA KAN 137	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.71999979	6.71999979 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	323	323 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.79980469	-5.79980469 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.28200006	6.28200006 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.09599996	2.09599996 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.2999995	2.29999995 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-5.79980469	-5.79980469 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Τ				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.31 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	8
AssistFirewall ActiveKSV M str.K UIs f32	0.050000007
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1353
AssistFirewall AsstReducedPerfSV Cnt M Iqc	0
AssistFirewall CombAsstSV MtrNm M f32	-2.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0700000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.03999996
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.029999993
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.40000006
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	8.39999962
k_AsstFWInpLimitHFA_MtrNm_f32	4.80000019
k_AsstFWInpLimitHysComp_MtrNm_f32	6.63000011
k_AsstFWNstep_Cnt_u16	1200
k_AsstFWPstep_Cnt_u16	3813
k_RestoreThresh_MtrNm_f32	4.0999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-20480





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-14336 -12288
tz_AsstFWUprBoundX_HwNm_s4p11[2][4] t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-10240
t2_Asst WopfboundX_1WNIII_s4p11[2][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][4] t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-12288 -10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-8192
t2_Asst WopiBoundX_HwNm_s4p11[4][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][5] t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-10240 -8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	-2048
t2 AsstFWUprBoundX HwNm s4p11[7][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-4096
	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-16384
	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-8192
	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432
	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528
	22528 24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	24576 -14336 -12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	24576 -14336

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	794
t_AsstFWDefltAssistX_HwNm_u8p8[1]	819
t_AsstFWDefltAssistX_HwNm_u8p8[2]	845
t_AsstFWDefltAssistX_HwNm_u8p8[3]	870
t_AsstFWDefltAssistX_HwNm_u8p8[4] t_AsstFWDefltAssistX_HwNm_u8p8[5]	896 922
t_AsstFWDefltAssistX_HwNm_u8p8[6]	947
t_AsstFWDefltAssistX_HwNm_u8p8[7]	973
t_AsstFWDefltAssistX_HwNm_u8p8[8]	998
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1280
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	10240 10445
t_AsstFWDefltAssistY_MtrNm_s4p11[11] t_AsstFWDefltAssistY_MtrNm_s4p11[12]	10650
t_AsstFWDefitAssistY_MtrNm_s4p11[13]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	12083
t_AsstFWPstepNstepThresh_Cnt_u16[0]	152
t_AsstFWPstepNstepThresh_Cnt_u16[1]	327
t_AsstFWVehSpd_Kph_u9p7[0]	13184
t_AsstFWVehSpd_Kph_u9p7[1]	13312
t_AsstFWVehSpd_Kph_u9p7[2]	13440
t_AsstFWVehSpd_Kph_u9p7[3]	13568
t_AsstFWVehSpd_Kph_u9p7[4]	13696
t_AsstFWVehSpd_Kph_u9p7[5]	13824
t_AsstFWVehSpd_Kph_u9p7[6]	13952
t_AsstFWVehSpd_Kph_u9p7[7]	14080
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.099999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	80.099985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_kte_inst_Ap_assistFirewali.AssistFirewali_Per1_Combinedassist_witrNm_i32 tgt_kte_inst_Ap_assistFirewali.AssistFirewali_Per1_Defeat_assitTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 HvsteresisComp MtrNm f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

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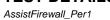
AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7.5999999	7.5999999 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	327	327 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.89990234	-5.89990234 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.41300011	7.41300011 ± 4.88E-04	<b>~</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.8269999	2.8269999 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>~</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.20000005	3.20000005 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-5.89990234	-5.89990234 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>~</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	·

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.32 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1476
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-2.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	8
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.04999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.099999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.039999991
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.5
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2
k_AsstFWInpLimitHFA_MtrNm_f32	5
k_AsstFWInpLimitHysComp_MtrNm_f32	0.20000003
k_AsstFWNstep_Cnt_u16	1076
k_AsstFWPstep_Cnt_u16	3936
k_RestoreThresh_MtrNm_f32	4.19999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2 AsstFWUprBoundX HwNm s4p11[2][2]	
	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
, , , , , , , , , , , , , , , , , , , ,	
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-32768
	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-32768
	-32768 -32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-32768 -32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-32768 -32768 -32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-32768 -32768





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5] t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-32768 -32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-32768 -32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-32768
	-32768 -32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-32768 -32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-32768

AssistFirewall Per1

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Input Value t2 AsstFWUprBoundY MtrNm s4p11[7][4] -32768 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][5] -32768 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][6] -32768 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][7] -32768 t2 AsstFWUprBoundY MtrNm s4p11[7][8] -32768 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][9] -32768 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][10] -32768  $t\_AsstFWDefltAssistX\_HwNm\_u8p8[0]$ 819 t\_AsstFWDefltAssistX\_HwNm\_u8p8[1] 845 t AsstFWDefltAssistX HwNm u8p8[2] 870 t\_AsstFWDefltAssistX\_HwNm\_u8p8[3] 896 t AsstFWDefltAssistX HwNm u8p8[4] 922 947 t\_AsstFWDefltAssistX\_HwNm\_u8p8[5] t AsstEWDefltAssistX HwNm u8n8[6] 973 t\_AsstFWDefltAssistX\_HwNm\_u8p8[7] 998 t AsstFWDefltAssistX HwNm u8p8[8] 1024 t\_AsstFWDefltAssistX\_HwNm\_u8p8[9] 1050 t AsstFWDefltAssistX HwNm u8p8[10] 1075 t\_AsstFWDefltAssistX\_HwNm\_u8p8[11] 1101 t AsstFWDefltAssistX HwNm u8p8[12] 1126 t\_AsstFWDefltAssistX\_HwNm\_u8p8[13] 1152 t\_AsstFWDefltAssistX\_HwNm\_u8p8[14] 1178 t\_AsstFWDefltAssistX\_HwNm\_u8p8[15] 1203 t\_AsstFWDefltAssistX\_HwNm\_u8p8[16] 1229 t\_AsstFWDefltAssistX\_HwNm\_u8p8[17] 1254 t\_AsstFWDefltAssistX\_HwNm\_u8p8[18] 1280 1306 t\_AsstFWDefltAssistX\_HwNm\_u8p8[19] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[0] 8397 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[1] 8602 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[2] 8806 t AsstFWDefltAssistY MtrNm s4p11[3] 9011 t AsstFWDefltAssistY\_MtrNm\_s4p11[4] 9216 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[5] 9421 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[6] 9626 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[7] 9830 t AsstFWDefltAssistY MtrNm s4p11[8] 10035 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[9] 10240 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[10] 10445 t AsstFWDefltAssistY MtrNm s4p11[11] 10650 t AsstFWDefltAssistY MtrNm s4p11[12] 10854 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[13] 11059 t AsstFWDefltAssistY MtrNm s4p11[14] 11264 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[15] 11469 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[16] 11674 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[17] 11878 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[18] 12083 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[19] 12288 t\_AsstFWPstepNstepThresh\_Cnt\_u16[0] 153 t\_AsstFWPstepNstepThresh\_Cnt\_u16[1] 331 t\_AsstFWVehSpd\_Kph\_u9p7[0] 16128 t\_AsstFWVehSpd\_Kph\_u9p7[1] 16256 t\_AsstFWVehSpd\_Kph\_u9p7[2] 16384 16512 t\_AsstFWVehSpd\_Kph\_u9p7[3] t\_AsstFWVehSpd\_Kph\_u9p7[4] 16640 t\_AsstFWVehSpd\_Kph\_u9p7[5] 16768 t\_AsstFWVehSpd\_Kph\_u9p7[6] 16896 17024 t AsstFWVehSpd Kph u9p7[7] tgt\_AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32.value 5.0999999 tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lgc.value 0 tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32.value 8 -9  $tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32.value$ tot AssistFirewall Per1 HysteresisComp MtrNm f32.value 5 tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum.value tot AssistFirewall Per1 VehicleSpeed Kph f32.value 90 1999969  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32$ tgt\_AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32 tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 BaseAssistCmd MtrNm f32 tot AssistFirewall Per1 BaseAssistCmd MtrNm f32 tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32 tgt\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32 tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lt\_tgt\_AssistFirewall\_Pe  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32$ tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32 tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HwTorque\_HwNm\_f32 tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$  $tgt\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum$ tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum  $tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32$ tgt\_AssistFirewall\_Per1\_VehicleSpeed\_Kph\_f32



AssistFirewall	_Per1

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.03400004	1.03400004 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	331	331 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	•
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6	-6 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.93599987	7.93599987 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.57599974	4.57600021 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-4.5	-4.5 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-6	-6 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	•
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.33 (Repeat Count = 1)	🗸
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0700000003
AssistFirewall ActiveRawAcc Cnt M u16	1599
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-2.70000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.090000036
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.05999994
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0500000007
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.60000024
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1
k_AsstFWInpLimitHFA_MtrNm_f32	5.19999981
k_AsstFWInpLimitHysComp_MtrNm_f32	0.230000004
k_AsstFWNstep_Cnt_u16	952
k_AsstFWPstep_Cnt_u16	4059
k_RestoreThresh_MtrNm_f32	4.30000019
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2 AsstFWUprBoundX HwNm s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2 AsstFWUprBoundX HwNm s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	32767
	32767
t2_Asst-Wuprboundy_MtrNm s4p11 0  2	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	32767 32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	32767 32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	32767





Namo	Innut Value
Name t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	Input Value 32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6] t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	32767 32767
tz_AsstFWUprBoundY_MtrNm_s4p11[2][7] t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	32767 32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6] t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	32767 32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9] t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	32767

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	32767 32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	32767
t_AsstFWDefltAssistX_HwNm_u8p8[0]	845
t_AsstFWDefltAssistX_HwNm_u8p8[1]	870
t_AsstFWDefltAssistX_HwNm_u8p8[2]	896
t_AsstFWDefltAssistX_HwNm_u8p8[3]	922
t_AsstFWDefltAssistX_HwNm_u8p8[4]	947
t_AsstFWDefltAssistX_HwNm_u8p8[5]	973
t_AsstFWDefltAssistX_HwNm_u8p8[6]	998
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1075 1101
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	1126
t_AsstFWDefitAssistX_HwNm_u8p8[12]	1152
t_AsstFWDefitAssistX_HwNm_u8p8[13]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1331
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	9626 9830
t_AsstFWDefltAssistY_MtrNm_s4p11[6] t_AsstFWDefltAssistY_MtrNm_s4p11[7]	10035
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[19] t AsstFWPstepNstepThresh Cnt u16[0]	12493 154
t_AsstFWPstepNstepThresh_Cnt_u16[1]	335
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
t_AsstFWVehSpd_Kph_u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6 2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	11.3000002
tgt_AssistFirewall_Per1_verlicleSpeed_kpri_is2.value  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.046	2.046 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	335	335 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.20019531	4.20019531 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.21070004	1.21070004 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.04502439	4.04502439 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	12.7997074	12.7997074 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4.20019531	4.20019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Τ				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.34 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4
AssistFirewall ActiveKSV M str.K Uls f32	0.079999982
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1722
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-2.79999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00800000038
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.07000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0599999987
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.10000002
k_AsstFWInpLimitHFA_MtrNm_f32	5.4000001
k_AsstFWInpLimitHysComp_MtrNm_f32	0.430000007
k_AsstFWNstep_Cnt_u16	828
k_AsstFWPstep_Cnt_u16	4182
k_RestoreThresh_MtrNm_f32	4.4000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2 AsstFWUprBoundX HwNm s4p11[2][2]	
	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
10101014 Anna Carlotte Anna Anna Anna Anna Anna Anna Anna Ann	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0 0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0 0 0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0 0

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	0
	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0
	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	0 0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	0
t_AsstFWDefltAssistX_HwNm_u8p8[0]	870
t_AsstFWDefltAssistX_HwNm_u8p8[1]	896
t_AsstFWDefltAssistX_HwNm_u8p8[2]	922
t_AsstFWDefltAssistX_HwNm_u8p8[3]	947
t_AsstFWDefltAssistX_HwNm_u8p8[4]	973
t_AsstFWDefltAssistX_HwNm_u8p8[5]	998
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1280 1306
t_AsstFWDefltAssistX_HwNm_u8p8[17] t_AsstFWDefltAssistX_HwNm_u8p8[18]	1331
t_AsstFWDefitAssistX_HwNm_u8p8[19]	1357
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[19] t AsstFWPstepNstepThresh Cnt u16[0]	12698 155
t_AsstFWPstepNstepThresh_Cnt_u16[1]	339
t_AsstFWVehSpd_Kph_u9p7[0]	22016
t_AsstFWVehSpd_Kph_u9p7[1]	22144
t_AsstFWVehSpd_Kph_u9p7[2]	22272
t_AsstFWVehSpd_Kph_u9p7[3]	22400
t_AsstFWVehSpd_Kph_u9p7[4]	22528
t_AsstFWVehSpd_Kph_u9p7[5]	22656
t_AsstFWVehSpd_Kph_u9p7[6]	22784
t_AsstFWVehSpd_Kph_u9p7[7]	22912
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	22.1000004
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	1 -
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32



AssistFirewall_Per1	
Name	

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.68000007	3.68000007 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	339	339 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.29980469	-4.29980469 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.21864009	2.21864009 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.73399973	5.73400021 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.03400004	1.03400004 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-4.29980469	-4.29980469 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.35 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5
AssistFirewall ActiveKSV M str.K Uls f32	0.090000036
AssistFirewall ActiveRawAcc Cnt M u16	1845
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-2.9000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00899999961
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.08000004
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.070000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.070000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	5.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	3.48000002
k_AsstFWNstep_Cnt_u16	704
k_AsstFWPstep_Cnt_u16	4305
k_RestoreThresh_MtrNm_f32	4.5
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144
12_M551FWOPIDOUNUA_MWNNI_S4P11[2][U]	-0144

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Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240	
2 AsstFWUprBoundX HwNm s4p11[6][2]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048	
_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096	
P_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144	
P_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192	
P_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336	
P_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288	
AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240	
:_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048	
P_AsstFWUprBoundX_HwNm_s4p11[7][9]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0	
P_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048	
P_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192	
? AsstFWUprBoundY MtrNm s4p11[0][5]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5] 2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	10240 12288	

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0] t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3] t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5] t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
m= neem or element a sum male de off life.	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
	2048 4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	896
t_AsstFWDefltAssistX_HwNm_u8p8[1]	922
t_AsstFWDefltAssistX_HwNm_u8p8[2]	947 973
t_AsstFWDefltAssistX_HwNm_u8p8[3] t_AsstFWDefltAssistX_HwNm_u8p8[4]	998
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1254
t_AsstFWDefitAssistX_HwNm_u8p8[15]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1382
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	12902
t_AsstFWPstepNstepThresh_Cnt_u16[0]	156
t_AsstFWPstepNstepThresh_Cnt_u16[1]	343
t_AsstFWVehSpd_Kph_u9p7[0]	24960
t_AsstFWVehSpd_Kph_u9p7[1]	25088
t_AsstFWVehSpd_Kph_u9p7[2]	25216
t_AsstFWVehSpd_Kph_u9p7[3]	25344
t_AsstFWVehSpd_Kph_u9p7[4]	25472
t_AsstFWVehSpd_Kph_u9p7[5]	25600
t_AsstFWVehSpd_Kph_u9p7[6]	25728
t_AsstFWVehSpd_Kph_u9p7[7]	25856
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0 4.099999
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	33.2000008
tgt_Rts_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	*
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32
.gonot_rp_/tooloti irovialii/tooloti irovvali_i oi i_voilioloopeeu_rpii_loz	19. 10.00 1. 10.10 1. 10.10 10.00 0000 1. 10.10 10.20 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10 10.10

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4.55000019	4.55000019 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	343	343 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.39990234	-4.39990234 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.05022001	4.05022001 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.370000005	0.370000005 ± 4.88E-04	<b>~</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>~</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.18600011	2.18600011 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-4.39990234	-4.39990234 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	<b>~</b>
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.36 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00499999989
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1968
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	2.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00999999978
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.09000003
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.079999982
ssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4
ssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.079999982
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
_AsstFWInpLimitBaseAsst_MtrNm_f32	2.0999999
_AsstFWInpLimitHFA_MtrNm_f32	5.80000019
_AsstFWInpLimitHysComp_MtrNm_f32	3.82999992
_AsstFWNstep_Cnt_u16	580
_AsstFWPstep_Cnt_u16	4428
_RestoreThresh_MtrNm_f32	4.5999999
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-12288
LE_7 toot 17 Opt Boding 1 _With Will_0+p 1 1[0][+]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-10240
	-10240 -8192





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-10240
	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-2048
	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-20480
:2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-14336





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	-2048
t_AsstFWDefltAssistX_HwNm_u8p8[0]	922
t_AsstFWDefltAssistX_HwNm_u8p8[1]	947
t_AsstFWDefltAssistX_HwNm_u8p8[2]	973
t_AsstFWDefltAssistX_HwNm_u8p8[3]	998
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1101
	1126
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[9]	
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1382
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1408
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	11469
1 1 1	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	13107
t_AsstFWPstepNstepThresh_Cnt_u16[0]	157
t_AsstFWPstepNstepThresh_Cnt_u16[1]	347
t_AsstFWVehSpd_Kph_u9p7[0]	27904
t_AsstFWVehSpd_Kph_u9p7[1]	28032
t_AsstFWVehSpd_Kph_u9p7[2]	28160
t_AsstFWVehSpd_Kph_u9p7[3]	28288
t_AsstFWVehSpd_Kph_u9p7[4]	28416
t_AsstFWVehSpd_Kph_u9p7[5]	28544
t_AsstFWVehSpd_Kph_u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7]	28800
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	44.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	
·	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lq	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_letgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32  tgt_AssistFirewall_Per1_HwTorque_HwNm_f32  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.96999979	5.96999979 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	347	347 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.89990234	4.89990234 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.03299999	5.03299999 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.63999987	2.6400001 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.51999998	3.51999998 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4.89990234	4.89990234 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.37 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6
AssistFirewall ActiveKSV M str.K Uls f32	0.0700000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	3321
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	-3.2999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.900001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0099999978
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0500000007
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-16
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00800000038
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.70000005
k_AsstFWInpLimitHFA_MtrNm_f32	8
k_AsstFWInpLimitHysComp_MtrNm_f32	0.430000007
k_AsstFWNstep_Cnt_u16	4305
k_AsstFWPstep_Cnt_u16	861
k_RestoreThresh_MtrNm_f32	5.69999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
2 AsstFWUprBoundX HwNm s4p11[5][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-30720
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-24576
t2_Asst WopiBoundY_MtrNm_s4p11[0][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-20480
	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-1843 <i>Z</i> -16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][6] 2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	2048
	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240
:2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	
	4096

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefitAssistX_HwNm_u8p8[0]	947
t_AsstFWDefltAssistX_HwNm_u8p8[1]	973
t_AsstFWDefltAssistX_HwNm_u8p8[2]	998
t_AsstFWDefltAssistX_HwNm_u8p8[3]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1336 1331
t_AsstFWDefltAssistX_HwNm_u8p8[15] t_AsstFWDefltAssistX_HwNm_u8p8[16]	1357
t_AsstFWDefitAssistX_HwNm_u8p8[17]	1382
t_AsstFWDefitAssistX_HwNm_u8p8[18]	1408
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1434
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	11059
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[11] t_AsstFWDefltAssistY_MtrNm_s4p11[12]	11674
t AsstFWDefltAssistY MtrNm s4p11[13]	12083
t AsstFWDefltAssistY MtrNm s4p11[14]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	13312
t_AsstFWPstepNstepThresh_Cnt_u16[0]	158
t_AsstFWPstepNstepThresh_Cnt_u16[1]	351
t_AsstFWVehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1]	30976
t_AsstFWVehSpd_Kph_u9p7[2]	31104
t_AsstFWVehSpd_Kph_u9p7[3]	31232
t_AsstFWVehSpd_Kph_u9p7[4]	31360
t_AsstFWVehSpd_Kph_u9p7[5]	31488
t_AsstFWVehSpd_Kph_u9p7[6]	31616 31744
t_AsstFWVehSpd_Kph_u9p7[7] tqt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_BaseAssistCmd_mtmm_r32.value tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	40.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFi$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall\_Per1

Status\_Cnt\_T\_enum

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Actual Value	Expected Value	Result
5.57999992	5.57999992 ± 4.88E-04	~
351	351 ± 1	~
1	1	~
-6.5	-6.5 ± 4.88E-04	<b>✓</b>
6.89330006	6.89330006 ± 4.88E-04	•
5.09499979	5.09499979 ± 4.88E-04	•
1	1	•
-15.9919996	-15.9919996 ± 4.88E-04	~
1	1 ± 3.05E-05	•
-6.5	-6.5 ± 9.77E-04	•
0xC6	0xC6	•
0x01	0x01	<b>✓</b>
0x01	0x01	~
0xC9	0xC9	~
0x01	0x01	-
	5.57999992 351 1 -6.5 6.89330006 5.09499979 1 -15.9919996 1 -6.5 0xC6 0x01 0x01 0xC9	5.57999992     5.57999992 ± 4.88E-04       351     351 ± 1       1     1       -6.5     -6.5 ± 4.88E-04       6.89330006     6.89330006 ± 4.88E-04       5.09499979     5.09499979 ± 4.88E-04       1     1       -15.9919996     -15.9919996 ± 4.88E-04       1     1 ± 3.05E-05       -6.5     -6.5 ± 9.77E-04       0xC6     0xC6       0x01     0x01       0xC9     0xC9

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

0x01

0x01

Test Step 2.38 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5
AssistFirewall ActiveKSV M str.K Uls f32	0.079999982
AssistFirewall_ActiveRawAcc_Cnt_M_u16	3444
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	-3.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0199999996
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.02999997
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	15.9995003
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00899999961
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6
k_AsstFWInpLimitHFA_MtrNm_f32	1.29999995
k_AsstFWInpLimitHysComp_MtrNm_f32	3.48000002
k_AsstFWNstep_Cnt_u16	4428
k_AsstFWPstep_Cnt_u16	984
k_RestoreThresh_MtrNm_f32	5.80000019
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][9] 2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
2 AsstFWUprBoundX HwNm s4p11[5][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
2 AsstFWUprBoundX HwNm s4p11[5][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-24576
	-24576 -22528
12_AsstFWUprBoundY_MtrNm_s4p11[0][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-14336

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240
:2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	8192





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	22528
t_AsstFWDefltAssistX_HwNm_u8p8[0]	77
t_AsstFWDefltAssistX_HwNm_u8p8[1]	102 128
t_AsstFWDefltAssistX_HwNm_u8p8[2]	154
t_AsstFWDefltAssistX_HwNm_u8p8[3] t_AsstFWDefltAssistX_HwNm_u8p8[4]	179
t_AsstFWDefltAssistX_HwNm_u8p8[5]	205
t_AsstFWDefltAssistX_HwNm_u8p8[6]	230
t_AsstFWDefltAssistX_HwNm_u8p8[7]	256
t_AsstFWDefltAssistX_HwNm_u8p8[8]	282
t_AsstFWDefitAssistX_HwNm_u8p8[9]	307
t_AsstFWDefltAssistX_HwNm_u8p8[10]	333
t_AsstFWDefltAssistX_HwNm_u8p8[11]	358
t_AsstFWDefltAssistX_HwNm_u8p8[12]	384
t_AsstFWDefltAssistX_HwNm_u8p8[13]	410
t AsstFWDefitAssistX HwNm u8p8[14]	435
t_AsstFWDefitAssistX_HwNm_u8p8[15]	461
t_AsstFWDefltAssistX_HwNm_u8p8[16]	486
t_AsstFWDefltAssistX_HwNm_u8p8[17]	512
t_AsstFWDefltAssistX_HwNm_u8p8[18]	538
t_AsstFWDefltAssistX_HwNm_u8p8[19]	563
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	10650
t_AsstFWDefitAssistY_MtrNm_s4p11[6]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	13517
t_AsstFWPstepNstepThresh_Cnt_u16[0]	159
t_AsstFWPstepNstepThresh_Cnt_u16[1]	355
t_AsstFWVehSpd_Kph_u9p7[0]	33792
t_AsstFWVehSpd_Kph_u9p7[1]	33920
t_AsstFWVehSpd_Kph_u9p7[2]	34048
t_AsstFWVehSpd_Kph_u9p7[3]	34176
t_AsstFWVehSpd_Kph_u9p7[4]	34304
t_AsstFWVehSpd_Kph_u9p7[5]	34432
t_AsstFWVehSpd_Kph_u9p7[6]	34560
t_AsstFWVehSpd_Kph_u9p7[7]	34688
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-9
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	50.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32$	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Results = 0.0000000000000000000000000000000000$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tot Dte Inst An AssistFirewell AssistFirewell Dark MEC Country Cot source	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	4

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4.5999999	4.5999999 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	355	355 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6.60009766	-6.60009766 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.58560002	1.58560002 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.97399998	5.97399998 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	15.7295046	15.7295046 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-6.60009766	-6.60009766 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.39 (Repeat Count = 1)	value of the second of the sec
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5
AssistFirewall ActiveKSV M str.K Uls f32	0.090000036
AssistFirewall_ActiveRawAcc_Cnt_M_u16	3567
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.029999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.03999996
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.070000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	0
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0099999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	8
k_AsstFWInpLimitHFA_MtrNm_f32	2.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	0.100000001
k_AsstFWNstep_Cnt_u16	4551
k_AsstFWPstep_Cnt_u16	1107
k_RestoreThresh_MtrNm_f32	5.9000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	10240 12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][0] t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1] t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7] t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048 4096
t2_AsstFWUprBoundX_riwNrii_s4p11[6][6] t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-12288





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5] t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2_Asst WopiBoundY_MtrNm_s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	24576 26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_Asst Woprbound1_initinin_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_Asst WopiBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	8192





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576
t_AsstFWDefltAssistX_HwNm_u8p8[0]	26
t_AsstFWDefltAssistX_HwNm_u8p8[1]	51
t_AsstFWDefltAssistX_HwNm_u8p8[2]	77
t_AsstFWDefltAssistX_HwNm_u8p8[3]	102 128
t_AsstFWDefltAssistX_HwNm_u8p8[4]	154
t_AsstFWDefltAssistX_HwNm_u8p8[5]	179
t_AsstFWDefltAssistX_HwNm_u8p8[6]	205
t_AsstFWDefltAssistX_HwNm_u8p8[7] t_AsstFWDefltAssistX_HwNm_u8p8[8]	230
t_AsstFWDefitAssistX_HwNm_u8p8[9]	256
t_AsstFWDefltAssistX_HwNm_u8p8[10]	282
t_AsstFWDefitAssistX_HwNm_u8p8[11]	307
	333
t_AsstFWDefltAssistX_HwNm_u8p8[12] t_AsstFWDefltAssistX_HwNm_u8p8[13]	358
t_AsstFWDefitAssistX_HwNm_u8p8[13] t AsstFWDefitAssistX_HwNm_u8p8[14]	384
, , ,	410
t_AsstFWDefltAssistX_HwNm_u8p8[15]	435
t_AsstFWDefltAssistX_HwNm_u8p8[16] t_AsstFWDefltAssistX_HwNm_u8p8[17]	461
	486
t_AsstFWDefltAssistX_HwNm_u8p8[18] t_AsstFWDefltAssistX_HwNm_u8p8[19]	512
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	10035
	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[2] t_AsstFWDefltAssistY_MtrNm_s4p11[3]	10445
• • • • • • • • • • • • • • • • • • • •	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[4] t_AsstFWDefltAssistY_MtrNm_s4p11[5]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	11059
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	11264
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	11469
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	11674
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	11878
t AsstFWDefitAssistY MtrNm s4p11[11]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12288
t AsstFWDefltAssistY MtrNm s4p11[13]	12493
t AsstFWDefltAssistY MtrNm s4p11[14]	12698
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	12902
t AsstFWDefltAssistY MtrNm s4p11[16]	13107
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	13312
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	13517
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	13722
t AsstFWPstepNstepThresh Cnt u16[0]	160
t_AsstFWPstepNstepThresh_Cnt_u16[1]	359
t_AsstFWVehSpd_Kph_u9p7[0]	36736
t_AsstFWVehSpd_Kph_u9p7[1]	36864
t_AsstFWVehSpd_Kph_u9p7[2]	36992
t_AsstFWVehSpd_Kph_u9p7[3]	37120
t_AsstFWVehSpd_Kph_u9p7[4]	37248
t_AsstFWVehSpd_Kph_u9p7[5]	37376
t_AsstFWVehSpd_Kph_u9p7[6]	37504
t_AsstFWVehSpd_Kph_u9p7[7]	37632
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	60.2000008
tgt_Rts_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	*
•	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-4.55000019	-4.55000019 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	359	359 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.70019531	5.70019531 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.97900009	4.97900009 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.72300005	4.72300005 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-0.109999999	-0.109999999 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	•
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	5.70019531	5.70019531 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	•
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

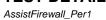
T			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	-

Test Step 2.40 (Repeat Count = 1)	• • • • • • • • • • • • • • • • • • •
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1
AssistFirewall ActiveKSV M str.K Uls f32	0.059999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	3690
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.039999991
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.04999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0799999982
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.019999996
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	7
k_AsstFWInpLimitHFA_MtrNm_f32	1.3999998
k_AsstFWInpLimitHysComp_MtrNm_f32	1.10000002
k_AsstFWNstep_Cnt_u16	4674
k_AsstFWPstep_Cnt_u16	1230
k_RestoreThresh_MtrNm_f32	6
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336

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Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192	
2 AsstFWUprBoundX HwNm s4p11[6][2]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096	
P_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048	
P_AsstFWUprBoundX_HwNm_s4p11[7][4]	0	
:_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048	
	4096	
P_AsstFWUprBoundX_HwNm_s4p11[7][6]		
	6144	
	8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]		
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][8] 2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240 12288	
2_AsstFWUprBoundX_HwNm_s4p11[7][8] 2_AsstFWUprBoundX_HwNm_s4p11[7][9] 2_AsstFWUprBoundX_HwNm_s4p11[7][10]		
2_AsstFWUprBoundX_HwNm_s4p11[7][8] 2_AsstFWUprBoundX_HwNm_s4p11[7][9] 2_AsstFWUprBoundX_HwNm_s4p11[7][10] 2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[7][8] 2_AsstFWUprBoundX_HwNm_s4p11[7][9] 2_AsstFWUprBoundX_HwNm_s4p11[7][10] 2_AsstFWUprBoundY_MtrNm_s4p11[0][0] 2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	12288 -24576	
2_AsstFWUprBoundX_HwNm_s4p11[7][8] 2_AsstFWUprBoundX_HwNm_s4p11[7][9] 2_AsstFWUprBoundX_HwNm_s4p11[7][10] 2_AsstFWUprBoundY_MtrNm_s4p11[0][0] 2_AsstFWUprBoundY_MtrNm_s4p11[0][1] 2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	12288 -24576 -22528 -20480	
2_AsstFWUprBoundX_HwNm_s4p11[7][8] 2_AsstFWUprBoundX_HwNm_s4p11[7][9] 2_AsstFWUprBoundX_HwNm_s4p11[7][10] 2_AsstFWUprBoundY_MtrNm_s4p11[0][0] 2_AsstFWUprBoundY_MtrNm_s4p11[0][1] 2_AsstFWUprBoundY_MtrNm_s4p11[0][1] 2_AsstFWUprBoundY_MtrNm_s4p11[0][2] 2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	12288 -24576 -22528 -20480 -18432	
2_AsstFWUprBoundX_HwNm_s4p11[7][8] 2_AsstFWUprBoundX_HwNm_s4p11[7][9] 2_AsstFWUprBoundX_HwNm_s4p11[7][10] 2_AsstFWUprBoundY_MtrNm_s4p11[0][0] 2_AsstFWUprBoundY_MtrNm_s4p11[0][1] 2_AsstFWUprBoundY_MtrNm_s4p11[0][2] 2_AsstFWUprBoundY_MtrNm_s4p11[0][3] 2_AsstFWUprBoundY_MtrNm_s4p11[0][3] 2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	12288 -24576 -22528 -20480 -18432 -16384	
2_AsstFWUprBoundX_HwNm_s4p11[7][7] 2_AsstFWUprBoundX_HwNm_s4p11[7][8] 2_AsstFWUprBoundX_HwNm_s4p11[7][9] 2_AsstFWUprBoundX_HwNm_s4p11[7][10] 2_AsstFWUprBoundY_MtrNm_s4p11[0][0] 2_AsstFWUprBoundY_MtrNm_s4p11[0][1] 2_AsstFWUprBoundY_MtrNm_s4p11[0][2] 2_AsstFWUprBoundY_MtrNm_s4p11[0][3] 2_AsstFWUprBoundY_MtrNm_s4p11[0][4] 2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288 -24576 -22528 -20480 -18432	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384
	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	16384
	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
	43300
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336 16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	14336 16384 18432 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	14336 16384 18432 -6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	14336 16384 18432 -6144





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	51
t_AsstFWDefltAssistX_HwNm_u8p8[1]	77 102
t_AsstFWDefltAssistX_HwNm_u8p8[2]	128
t_AsstFWDefltAssistX_HwNm_u8p8[3] t_AsstFWDefltAssistX_HwNm_u8p8[4]	154
t_AsstFWDefltAssistX_HwNm_u8p8[5]	179
t_AsstFWDefltAssistX_HwNm_u8p8[6]	205
t_AsstFWDefitAssistX_HwNm_u8p8[7]	230
t_AsstFWDefltAssistX_HwNm_u8p8[8]	256
t_AsstFWDefitAssistX_HwNm_u8p8[9]	282
t_AsstFWDefltAssistX_HwNm_u8p8[10]	307
t_AsstFWDefltAssistX_HwNm_u8p8[11]	333
t_AsstFWDefltAssistX_HwNm_u8p8[12]	358
t_AsstFWDefitAssistX_HwNm_u8p8[13]	384
t AsstFWDefltAssistX HwNm u8p8[14]	410
t_AsstFWDefitAssistX_HwNm_u8p8[15]	435
t_AsstFWDefitAssistX_HwNm_u8p8[16]	461
t_AsstFWDefitAssistX_HwNm_u8p8[17]	486
t_AsstFWDefitAssistX_HwNm_u8p8[18]	512
t_AsstFWDefltAssistX_HwNm_u8p8[19]	538
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	13926
t_AsstFWPstepNstepThresh_Cnt_u16[0]	161
t_AsstFWPstepNstepThresh_Cnt_u16[1]	363
t_AsstFWVehSpd_Kph_u9p7[0]	39680
t_AsstFWVehSpd_Kph_u9p7[1]	39808
t_AsstFWVehSpd_Kph_u9p7[2]	39936
t_AsstFWVehSpd_Kph_u9p7[3]	40064
t_AsstFWVehSpd_Kph_u9p7[4]	40192
t_AsstFWVehSpd_Kph_u9p7[5]	40320
t_AsstFWVehSpd_Kph_u9p7[6]	40448
t_AsstFWVehSpd_Kph_u9p7[7]	40576
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	70.4000015
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_left and the property of the p$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

2015-03-23, 11:55:49+0530



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.93999998	0.93999998 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	363	363 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6.70019531	-6.70019531 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-4.57999992	-4.57999992 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.4920001	5.4920001 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.1500001	5.1500001 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.93999998	0.939999998 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-6.70019531	-6.70019531 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.41 (Repeat Count = 1) ✓	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2
AssistFirewall ActiveKSV M str.K Uls f32	0.090000036
AssistFirewall ActiveRawAcc Cnt M u16	3813
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.70000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.05999994
AssistFirewall LwrBoundKSV M str.SV Uls f32	6.099999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.090000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.200000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2
k_AsstFWInpLimitHFA_MtrNm_f32	1.60000002
k_AsstFWInpLimitHysComp_MtrNm_f32	1.3999998
k_AsstFWNstep_Cnt_u16	3567
k_AsstFWPstep_Cnt_u16	1353
k_RestoreThresh_MtrNm_f32	6.099999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288





Input Value
-10240
-8192
-6144
-4096
-2048
0
2048
4096
6144
8192
-4096
-2048
0
2048
4096
6144 8192
10240
12288 14336
16384
0
2048
4096
6144 8192
10240 12288
14336
16384
18432
20480
-2048 0
2048
4096
6144
8192 10240
12288
14336
16384
18432
-8192
-6144
-4096
-2048
0
2048
4096
6144
8192
10240
12288
-6144
-4096
-4096 -2048
-2048 0
2048
4096
6144
8192
10240
12288
14336
-22528
-22526 -20480
-18432
10-10-2
-16384
-16384 -14336
-14336

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192 -6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144 4006
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	77
t_AsstFWDefltAssistX_HwNm_u8p8[1]	102
t_AsstFWDefltAssistX_HwNm_u8p8[2]	128
t_AsstFWDefltAssistX_HwNm_u8p8[3]	154
t_AsstFWDefltAssistX_HwNm_u8p8[4]	179
t_AsstFWDefltAssistX_HwNm_u8p8[5]	205
t_AsstFWDefltAssistX_HwNm_u8p8[6]	230
t_AsstFWDefltAssistX_HwNm_u8p8[7]	256
t_AsstFWDefltAssistX_HwNm_u8p8[8]	282
t_AsstFWDefltAssistX_HwNm_u8p8[9]	307
t_AsstFWDefltAssistX_HwNm_u8p8[10]	333
t_AsstFWDefltAssistX_HwNm_u8p8[11]	358
t_AsstFWDefltAssistX_HwNm_u8p8[12]	384
t_AsstFWDefltAssistX_HwNm_u8p8[13]	410
t_AsstFWDefltAssistX_HwNm_u8p8[14]	435
t_AsstFWDefltAssistX_HwNm_u8p8[15]	461
t_AsstFWDefltAssistX_HwNm_u8p8[16]	486
t_AsstFWDefltAssistX_HwNm_u8p8[17]	512
t_AsstFWDefltAssistX_HwNm_u8p8[18]  t_AsstFWDefltAssistX_HwNm_u8p8[19]	538 563
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	10240
t_AsstFWDefitAssistY_MtrNm_s4p11[1]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	10650
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	14131
t_AsstFWPstepNstepThresh_Cnt_u16[0]	162
t_AsstFWPstepNstepThresh_Cnt_u16[1]	367
t_AsstFWVehSpd_Kph_u9p7[0] t_AsstFWVehSpd_Kph_u9p7[1]	42624 42752
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	42880
t_AsstFWVehSpd_Kph_u9p7[3]	43008
t_AsstFWVehSpd_Kph_u9p7[4]	43136
t_AsstFWVehSpd_Kph_u9p7[5]	43264
t_AsstFWVehSpd_Kph_u9p7[6]	43392
t_AsstFWVehSpd_Kph_u9p7[7]	43520
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	80.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.81999993	1.82000005 ± 4.88E-04	•
AssistFirewall_ActiveRawAcc_Cnt_M_u16	367	367 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6.89990234	-6.89990234 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.14999998	1.14999998 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.64099979	5.64099979 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.4000001	-5.4000001 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-6.89990234	-6.89990234 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.42 (Repeat Count = 1)	Test Step 2.42 (Repeat Count = 1)	
Name	Input Value	
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3	
AssistFirewall ActiveKSV M str.K Uls f32	0.10000001	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	3936	
AssistFirewall AsstReducedPerfSV Cnt M lqc	0	
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.79999995	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0599999987	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.07000005	
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.059999987	
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1	
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00125584798	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1	
k_AsstFWInpLimitHFA_MtrNm_f32	2	
k_AsstFWInpLimitHysComp_MtrNm_f32	1.29999995	
k_AsstFWNstep_Cnt_u16	3690	
k_AsstFWPstep_Cnt_u16	1476	
k_RestoreThresh_MtrNm_f32	6.19999981	
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384	
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336	
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288	
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384	
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432	
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240	

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8] t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1] t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2040
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4] t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_Asst WoprBoundX_HwNm_s4p11[7][8]	12288
t2_Asst WoprBoundX_1WNIII_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-14336
	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-10240
	-10240 -8192

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5] t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	20480
t2_AsstFWOpiBoundY_MtrNm_s4p11[3][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	102
t_AsstFWDefltAssistX_HwNm_u8p8[1]	128 154
t_AsstFWDefltAssistX_HwNm_u8p8[2]	
t_AsstFWDefltAssistX_HwNm_u8p8[3]	179 205
t_AsstFWDefltAssistX_HwNm_u8p8[4]	230
t_AsstFWDefltAssistX_HwNm_u8p8[5]	256
t_AsstFWDefltAssistX_HwNm_u8p8[6]	282
t_AsstFWDefltAssistX_HwNm_u8p8[7] t_AsstFWDefltAssistX_HwNm_u8p8[8]	307
t_AsstFWDefitAssistX_HwNm_u8p8[9]	333
t_AsstFWDefltAssistX_HwNm_u8p8[10]	358
	384
t_AsstFWDefltAssistX_HwNm_u8p8[11] t_AsstFWDefltAssistX_HwNm_u8p8[12]	410
	435
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	461
, , ,	
t_AsstFWDefltAssistX_HwNm_u8p8[15]	486
t_AsstFWDefltAssistX_HwNm_u8p8[16]	512 538
t_AsstFWDefltAssistX_HwNm_u8p8[17] t_AsstFWDefltAssistX_HwNm_u8p8[18]	563
t_AsstFWDefitAssistX_HwNm_u8p8[18]  t_AsstFWDefitAssistX_HwNm_u8p8[19]	589
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	10650
	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[2] t_AsstFWDefltAssistY_MtrNm_s4p11[3]	11059
• • • • • • • • • • • • • • • • • • • •	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[4] t_AsstFWDefltAssistY_MtrNm_s4p11[5]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	11674
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	11878
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12288
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	12493
t AsstFWDefitAssistY MtrNm s4p11[11]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12902
t AsstFWDefltAssistY MtrNm s4p11[13]	13107
t AsstFWDefltAssistY MtrNm s4p11[14]	13312
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	13517
t AsstFWDefltAssistY MtrNm s4p11[16]	13722
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	13926
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	14131
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	14336
t AsstFWPstepNstepThresh Cnt u16[0]	163
t_AsstFWPstepNstepThresh_Cnt_u16[1]	371
t_AsstFWVehSpd_Kph_u9p7[0]	45568
t_AsstFWVehSpd_Kph_u9p7[1]	45696
t_AsstFWVehSpd_Kph_u9p7[2]	45824
t_AsstFWVehSpd_Kph_u9p7[3]	45952
t_AsstFWVehSpd_Kph_u9p7[4]	46080
t_AsstFWVehSpd_Kph_u9p7[4]	46208
t_AsstFWVehSpd_Kph_u9p7[6]	46336
t_AsstFWVehSpd_Kph_u9p7[7]	46464
t_Assir-wvenspd_kpn_usp7[7] tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_BaseAssistCmd_intrium_t32.value tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFireWall_Per1_Dereat_Assist_MtrNm_f32.value  tgt_AssistFireWall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_132.value tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90.1999969
tgt_AssistFirewall_Fer1_verlicleSpeed_Rpri_is2.value  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
•	*
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.70000005	2.70000005 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	371	371 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	7	7 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.13800001	2.13800001 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.05999994	5.05999994 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	0.99874413	0.99874413 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	7	7 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

T			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.43 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4
AssistFirewall ActiveKSV M str.K Uls f32	0.200000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4059
AssistFirewall AsstReducedPerfSV Cnt M Igc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.9000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.070000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.08000004
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.090000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.715390444
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.10000002
k_AsstFWInpLimitHFA_MtrNm_f32	4
k_AsstFWInpLimitHysComp_MtrNm_f32	2.0999999
k_AsstFWNstep_Cnt_u16	3813
k_AsstFWPstep_Cnt_u16	1599
k_RestoreThresh_MtrNm_f32	6.30000019
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192

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ASSISTRIEWAII_PELL		
Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0	
2 AsstFWUprBoundX HwNm s4p11[2][5]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0	
	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]		
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	2048	
	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]		
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048	
2 AsstFWUprBoundX HwNm s4p11[6][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096	
	6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]		
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384	
	18432	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]		
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-6144	
2_A33ti WOpi Bodila i _iviti viii _34p i i [0][0]	* : : :	

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5] t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7] t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	8192 -16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-16384 -14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240
t2_Asst WopfboundY_MtrNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	





t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	Input Value 10240
	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
	16384
	18432
	20480
	22528
t_AsstFWDefltAssistX_HwNm_u8p8[0]	128
t_AsstFWDefltAssistX_HwNm_u8p8[1]	154
t_AsstFWDefltAssistX_HwNm_u8p8[2]	179
t_AsstFWDefltAssistX_HwNm_u8p8[3]	205
t_AsstFWDefltAssistX_HwNm_u8p8[4]	230
t_AsstFWDefltAssistX_HwNm_u8p8[5]	256
	282
	307
	333
	358
	384
	410
	435
	461
	486
, , ,	512
	538 563
	589
	614
1	10650
, , ,	10854
, . ;	11059
	11264
	11469
	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	13312
	13517
, , ,	13722
	13926
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	14131
	14336
	14541
	164 375
	1408
	1536
	1664
	1792
	1920
	2048
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	2176
	2304
	6
	0
•	3
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	11.1000004
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
,	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32  tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum  tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.20000005	3.20000005 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	375	375 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.10009766	7.10009766 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.22399998	3.22399998 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.82562494	5.82562494 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.95528805	1.95528805 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	7.10009766	7.10009766 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	✓

T			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.44 (Repeat Count = 1)	· ·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5
AssistFirewall ActiveKSV M str.K Uls f32	0.300000012
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4182
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.09000003
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.5
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.20000005
k_AsstFWInpLimitHFA_MtrNm_f32	5
k_AsstFWInpLimitHysComp_MtrNm_f32	2.29999995
k_AsstFWNstep_Cnt_u16	3936
k_AsstFWPstep_Cnt_u16	1722
k_RestoreThresh_MtrNm_f32	6.4000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192 10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8] t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0] t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3] t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5] t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240 12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_Asst WoprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-4096
tz_/tost Webizodila1_wartii_o-p11[o][o]	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

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1 (1)
Input Value
0
2048
4096
-16384
-14336
-12288
-10240
-8192
-6144
-4096
-2048
0
2048
4096
-8192
-6144
-4096
-2048
0
2048
4096
6144
8192
10240
12288
-14336
-12288
-10240
-8192
-6144
-4096
-2048
0
2048
4096
6144
-8192
-6144
-4096
-2048
0
2048
4096
6144
8192
10240
12288
-10240
-8192
-6144
-4096
-2048
0
2048
4096
6144
8192
10240
-14336
-12288
-10240
-8192
-6144
-4096
-2048
0
2048
4096
6144
4096
1000
6144
6144 8192





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576
t_AsstFWDefltAssistX_HwNm_u8p8[0]	154
t_AsstFWDefltAssistX_HwNm_u8p8[1]	179
t_AsstFWDefltAssistX_HwNm_u8p8[2]	205
t_AsstFWDefltAssistX_HwNm_u8p8[3]	230
t_AsstFWDefltAssistX_HwNm_u8p8[4]	256 282
t_AsstFWDefltAssistX_HwNm_u8p8[5]	307
t_AsstFWDefltAssistX_HwNm_u8p8[6]	333
t_AsstFWDefitAssistX_HwNm_u8p8[7] t_AsstFWDefitAssistX_HwNm_u8p8[8]	358
t_AsstFWDefitAssistX_HwNm_u8p8[9]	384
t_AsstFWDefitAssistX_HwNm_u8p8[10]	410
	435
t_AsstFWDefitAssistX_HwNm_u8p8[11] t_AsstFWDefitAssistX_HwNm_u8p8[12]	461
	486
t_AsstFWDefltAssistX_HwNm_u8p8[13] t AsstFWDefltAssistX HwNm u8p8[14]	512
, ; ;	538
t_AsstFWDefItAssistX_HwNm_u8p8[15]	563
t_AsstFWDefItAssistX_HwNm_u8p8[16]	589
t_AsstFWDefltAssistX_HwNm_u8p8[17] t_AsstFWDefltAssistX_HwNm_u8p8[18]	614
t_AsstFWDefitAssistX_HwNm_u8p8[19]	640
t_AsstFWDefitAssistX_nwinn_uopo[19]  t_AsstFWDefitAssistY_MtrNm_s4p11[0]	10854
t_AsstFWDefitAssistY_MtrNm_s4p11[1]	11059
·	11264
t_AsstFWDefitAssistY_MtrNm_s4p11[2] t_AsstFWDefitAssistY_MtrNm_s4p11[3]	11469
· · · · · · · · · · · · · · · · · · ·	11674
t_AsstFWDefitAssistY_MtrNm_s4p11[4] t_AsstFWDefitAssistY_MtrNm_s4p11[5]	11878
t_AsstFWDefitAssistY_MtrNm_s4p11[6]	12083
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	12288
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	12493
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	12698
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	12902
t AsstFWDefitAssistY MtrNm s4p11[11]	13107
t_AsstFWDefitAssistY_MtrNm_s4p11[12]	13312
t AsstFWDefltAssistY MtrNm s4p11[13]	13517
t AsstFWDefltAssistY MtrNm s4p11[14]	13722
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	13926
t AsstFWDefltAssistY MtrNm s4p11[16]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	14336
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	14541
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	14746
t AsstFWPstepNstepThresh Cnt u16[0]	165
t_AsstrWPstepNstepThresh_Cnt_u16[1]	379
t_AsstrWVehSpd_Kph_u9p7[0]	4352
t_AsstFWVehSpd_Kph_u9p7[1]	4480
t_AsstFWVehSpd_Kph_u9p7[2]	4608
t_AsstFWVehSpd_Kph_u9p7[3]	4736
t_AsstrWVehSpd_Kph_u9p7[4]	4864
t_AsstFWVehSpd_Kph_u9p7[5]	4992
t_AsstFWVehSpd_Kph_u9p7[6]	5120
t_AsstFWVehSpd_Kph_u9p7[7]	5248
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	22.3999996
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
.goor_rp_rodion nowan.nosion nowan_r or r_Dasenssistoniu_ivitiVIII_loz	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tot Rte Inst An AssistFirewall AssistFirewall Per1 CombinedAssist MtrNm f22	19. John Homan of Toombinous Gold Civiliani Loc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tnt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_li	tot AssistFirewall Per1 Defeat AsstThl Service Cnt loc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_letgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_letgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_letgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.5	3.5 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	379	379 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.20019531	7.20019531 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.28000021	4.28000021 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.900001	6.9000001 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.5	2.5 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	7.20019531	7.20019531 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.45 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.400000006
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4305
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.090000036
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-8.80000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.200000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00499999989
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
_AsstFWInpLimitBaseAsst_MtrNm_f32	1.20000005
_AsstFWInpLimitHFA_MtrNm_f32	2
_AsstFWInpLimitHysComp_MtrNm_f32	2.5
_AsstFWNstep_Cnt_u16	4059
_AsstFWPstep_Cnt_u16	1845
_RestoreThresh_MtrNm_f32	6.5
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096

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Assistriiewaii_Pei i		
Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096	
2 AsstFWUprBoundX HwNm s4p11[2][5]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048	
2 AsstFWUprBoundX HwNm s4p11[6][2]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144	
, , , , , , , , , , , , , , , , , , , ,		
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[7][0] 2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	0	





Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][0] 2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
	10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
2 AsstFWUprBoundY MtrNm s4p11[4][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][1] 2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-0144 -4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144
	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	0192
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	26624
t_AsstFWDefltAssistX_HwNm_u8p8[0]	179
t_AsstFWDefltAssistX_HwNm_u8p8[1]	205 230
t_AsstFWDefltAssistX_HwNm_u8p8[2]	
t_AsstFWDefltAssistX_HwNm_u8p8[3] t_AsstFWDefltAssistX_HwNm_u8p8[4]	256 282
t_AsstFWDefltAssistX_HwNm_u8p8[5]	307
t_AsstFWDefltAssistX_HwNm_u8p8[6]	333
t_AsstFWDefltAssistX_HwNm_u8p8[7]	358
t_AsstFWDefltAssistX_HwNm_u8p8[8]	384
t_AsstFWDefltAssistX_HwNm_u8p8[9]	410
t_AsstFWDefltAssistX_HwNm_u8p8[10]	435
t_AsstFWDefltAssistX_HwNm_u8p8[11]	461
t_AsstFWDefltAssistX_HwNm_u8p8[12]	486
t_AsstFWDefitAssistX_HwNm_u8p8[13]	512
t AsstFWDefltAssistX HwNm u8p8[14]	538
t_AsstFWDefltAssistX_HwNm_u8p8[15]	563
t_AsstFWDefltAssistX_HwNm_u8p8[16]	589
t_AsstFWDefltAssistX_HwNm_u8p8[17]	614
t_AsstFWDefltAssistX_HwNm_u8p8[18]	640
t_AsstFWDefltAssistX_HwNm_u8p8[19]	666
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	14950
t_AsstFWPstepNstepThresh_Cnt_u16[0]	166
t_AsstFWPstepNstepThresh_Cnt_u16[1]	383
t_AsstFWVehSpd_Kph_u9p7[0]	7296
t_AsstFWVehSpd_Kph_u9p7[1]	7424
t_AsstFWVehSpd_Kph_u9p7[2]	7552
t_AsstFWVehSpd_Kph_u9p7[3]	7680
t_AsstFWVehSpd_Kph_u9p7[4]	7808
t_AsstFWVehSpd_Kph_u9p7[5]	7936
t_AsstFWVehSpd_Kph_u9p7[6]	8064
t_AsstFWVehSpd_Kph_u9p7[7]	8192
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5 2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	33.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tut ind indi AD Assistrirewali. Assistrirewali Peri Veniclespeed Kpn 132	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.5999999	3.5999999 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	383	383 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.29980469	7.29980469 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.0630002	5.0630002 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.64000034	-5.63999987 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.99499989	3.99499989 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	7.29980469	7.29980469 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.46 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7
AssistFirewall ActiveKSV M str.K Uls f32	0.5
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4428
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00800000038
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.20000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8.80000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.300000012
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00600000005
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.5
k_AsstFWInpLimitHFA_MtrNm_f32	1
k_AsstFWInpLimitHysComp_MtrNm_f32	2.70000005
k_AsstFWNstep_Cnt_u16	4182
k_AsstFWPstep_Cnt_u16	1968
k_RestoreThresh_MtrNm_f32	6.599999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048

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ASSIST II EWAII_PETT	
Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
P_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
P_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
P_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
P_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
stranger	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
:_AsstFWOpiBoundX_HwNm_s4p11[7][3] ?_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
	-2046
P_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
_AsstFWUprBoundX_HwNm_s4p11[7][6]	
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
P_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192
	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	
	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096 -2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][3] 2_AsstFWUprBoundY_MtrNm_s4p11[0][4] 2_AsstFWUprBoundY_MtrNm_s4p11[0][5] 2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	

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Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0.
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-30720
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-16384
	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-14336 -12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-30720
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
2_Asst Worldond	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240
	8192
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192 10240
	8192 10240 12288





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	205
t_AsstFWDefltAssistX_HwNm_u8p8[1]	230
t_AsstFWDefltAssistX_HwNm_u8p8[2]	256
t_AsstFWDefltAssistX_HwNm_u8p8[3]	282 307
t_AsstFWDefltAssistX_HwNm_u8p8[4]	333
t_AsstFWDefltAssistX_HwNm_u8p8[5]	358
t_AsstFWDefltAssistX_HwNm_u8p8[6]	384
t_AsstFWDefltAssistX_HwNm_u8p8[7] t_AsstFWDefltAssistX_HwNm_u8p8[8]	410
t_AsstFWDefitAssistX_HwNm_u8p8[9]	435
t_AsstFWDefltAssistX_HwNm_u8p8[10]	461
	486
t_AsstFWDefltAssistX_HwNm_u8p8[11] t_AsstFWDefltAssistX_HwNm_u8p8[12]	512
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	538 563
	589
t_AsstFWDefltAssistX_HwNm_u8p8[15]	614
t_AsstFWDefltAssistX_HwNm_u8p8[16]	614
t_AsstFWDefltAssistX_HwNm_u8p8[17] t_AsstFWDefltAssistX_HwNm_u8p8[18]	666
t_AsstFWDefitAssistX_HwNm_u8p8[19]	691
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	11264
t_AsstFWDefitAssistY_MtrNm_s4p11[1]	11469
·	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[2] t_AsstFWDefltAssistY_MtrNm_s4p11[3]	11878
· · · · · · · · · · · · · · · · · · ·	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[4] t_AsstFWDefltAssistY_MtrNm_s4p11[5]	12288
t_AsstFWDefitAssistY_MtrNm_s4p11[6]	12493
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	12698
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	12902
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	13107
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	13312
t AsstFWDefitAssistY MtrNm s4p11[11]	13517
t_AsstFWDefitAssistY_MtrNm_s4p11[12]	13722
t AsstFWDefitAssistY MtrNm s4p11[13]	13926
t AsstFWDefitAssistY MtrNm s4p11[14]	14131
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	14541
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	14746
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	14950
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	15155
t AsstFWPstepNstepThresh Cnt u16[0]	167
t_AsstFWPstepNstepThresh_Cnt_u16[1]	387
t_AsstFWVehSpd_Kph_u9p7[0]	10240
t_AsstFWVehSpd_kph_u9p7[1]	10368
t_AsstFWVehSpd_kph_u9p7[2]	10496
t_AsstFWVehSpd_Kph_u9p7[3]	10624
t_AsstFWVehSpd_Kph_u9p7[4]	10752
t_AsstFWVehSpd_Kph_u9p7[4]	10880
t_AsstFWVehSpd_Kph_u9p7[6]	11008
t_AsstFWVenSpd_kph_u9p7[7]	11136
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	0  -6
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	44.0999985
tgt_AssistFirewall_Fer1_verificeSpeed_Apri_isz.value  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AssirtIrewallActive_Ois_132 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	•
	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
	1 -
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.5	3.5 ± 4.88E-04	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	387	387 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.39990234	-7.39990234 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.99039984	5.99039984 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.96000004	4.96000004 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.93400002	4.93400002 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.39990234	-7.39990234 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8
AssistFirewall_ActiveKSV_M_str.K_UIs_f32	0.600000024
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4551
AssistFirewall_ActiveRawAcc_Cit_ivi_u16 AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall_AssiReducedPenSv_Cnt_m_gc AssistFirewall CombAsstSV MtrNm M f32	4.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.400001
AssistFirewall_HiFreqKSV_M_str.LFF_Str.K_Uls_f32	0.00899999961
•	1.2999995
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	0
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	· ·
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00700000022
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
<_AsstFWInpLimitBaseAsst_MtrNm_f32	1.60000002
<_AsstFWInpLimitHFA_MtrNm_f32	4
<_AsstFWInpLimitHysComp_MtrNm_f32	2.9000001
<_AsstFWNstep_Cnt_u16	4305
<_AsstFWPstep_Cnt_u16	2091
x_RestoreThresh_MtrNm_f32	6.6999981
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4] t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-0144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7] t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9] t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2 AsstFWUprBoundX HwNm s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWOpiBoundX_nwini_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_Asst WopioundX_nwn_s4p11[6][5]	4096
t2_Asst WopiBoundX_HwNm_s4p11[7][0]	-8192
t2_Asst Wopiounux_nwnn_s4p11[7][0]	-6144
t2_Asst WoproduidX_nwin_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_Asst WopiboundX_1WNm_s4p11[7][2]	-2048
t2_Asst Wopiounux_nwnii_s4p11[7][6]	0
t2_Asst WopfboundX_nwnn_s4p11[7][4]	2048
t2_Asst WopioundX_nwin_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_Asst WopiodidA_riwin_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192
t2_Asst Wopiodulu1_MtrNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-2040
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	2048
	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-24576
	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048
	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-12288
	-10240





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	230
t_AsstFWDefltAssistX_HwNm_u8p8[1]	256
t_AsstFWDefltAssistX_HwNm_u8p8[2]	282
t_AsstFWDefltAssistX_HwNm_u8p8[3]	307
t_AsstFWDefitAssistX_HwNm_u8p8[4]	333
	358
t_AsstFWDefltAssistX_HwNm_u8p8[5]	
t_AsstFWDefltAssistX_HwNm_u8p8[6]	384
t_AsstFWDefltAssistX_HwNm_u8p8[7]	410
t_AsstFWDefltAssistX_HwNm_u8p8[8]	435
t_AsstFWDefltAssistX_HwNm_u8p8[9]	461
t_AsstFWDefltAssistX_HwNm_u8p8[10]	486
t_AsstFWDefltAssistX_HwNm_u8p8[11]	512
t_AsstFWDefltAssistX_HwNm_u8p8[12]	538
t_AsstFWDefltAssistX_HwNm_u8p8[13]	563
t_AsstFWDefltAssistX_HwNm_u8p8[14]	589
t_AsstFWDefltAssistX_HwNm_u8p8[15]	614
t_AsstFWDefltAssistX_HwNm_u8p8[16]	640
t_AsstFWDefltAssistX_HwNm_u8p8[17]	666
t_AsstFWDefltAssistX_HwNm_u8p8[18]	691
t_AsstFWDefltAssistX_HwNm_u8p8[19]	717
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	13517
	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	15360
t_AsstFWPstepNstepThresh_Cnt_u16[0]	168
t_AsstFWPstepNstepThresh_Cnt_u16[1]	391
t_AsstFWVehSpd_Kph_u9p7[0]	13184
t_AsstFWVehSpd_Kph_u9p7[1]	13312
t_AsstFWVehSpd_Kph_u9p7[2]	13440
t_AsstFWVehSpd_Kph_u9p7[3]	13568
t_AsstFWVehSpd_Kph_u9p7[4]	13696
t_AsstFWVehSpd_Kph_u9p7[5]	13824
t_AsstFWVehSpd_Kph_u9p7[6]	13952
t_AsstFWVehSpd_Kph_u9p7[7]	14080
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2.20000005
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-7
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
•	
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	55.099985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

AssistFirewall\_Per1

Status\_Cnt\_T\_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	3.19999981	3.20000005 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	391	391 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.5	-7.5 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.01350021	7.01350021 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-2	-2 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.92299986	5.92299986 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.5	-7.5 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param Cnt T u08	0x01	0x01	<b>✓</b>

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

0x01

0x01

Test Step 2.48 (Repeat Count = 1)		
Name	Input Value	
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	1.10000002	
AssistFirewall ActiveKSV M str.K Uls f32	0.400000006	
AssistFirewall ActiveRawAcc Cnt M u16	4674	
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.5	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	8	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0099999978	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.3999998	
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.5	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5	
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7	
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00800000038	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.70000005	
k_AsstFWInpLimitHFA_MtrNm_f32	2.20000005	
k_AsstFWInpLimitHysComp_MtrNm_f32	3.0999999	
k_AsstFWNstep_Cnt_u16	4428	
k_AsstFWPstep_Cnt_u16	2214	
k_RestoreThresh_MtrNm_f32	6.80000019	
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288	
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336	
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384	
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432	
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384	
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336	
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288	
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-18432	





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_riwNini_s4p11[3][1] t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_Asst WopiboundX_HwNm_s4p11[3][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_Asst WopiboundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	-6144
t2_AsstFWUprBoundX_riwNrii_s4p11[4][0] t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-0144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1] t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2] t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2046 0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2 AsstFWUprBoundX HwNm s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2 AsstFWUprBoundX HwNm s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2 AsstFWUprBoundX HwNm s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
12_7 toot: W Opi Bodild 1_Will Will _ 5-p 1 [[0][-1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	2048
	2048 4096

2015-03-23, 11:55:49+0530

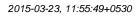


Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5] t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240
tz_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
tz_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	
, , , , ,	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240
	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096 
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	256
t_AsstFWDefltAssistX_HwNm_u8p8[1]	282
t_AsstFWDefltAssistX_HwNm_u8p8[2]	307
t_AsstFWDefltAssistX_HwNm_u8p8[3]	333
t_AsstFWDefltAssistX_HwNm_u8p8[4]	358
t_AsstFWDefltAssistX_HwNm_u8p8[5]	384
t_AsstFWDefltAssistX_HwNm_u8p8[6]	410
t_AsstFWDefltAssistX_HwNm_u8p8[7]	435
t_AsstFWDefltAssistX_HwNm_u8p8[8]	461
t_AsstFWDefltAssistX_HwNm_u8p8[9]	486 512
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	538
t_AsstFWDefitAssistX_HwNm_u8p8[12]	563
t_AsstFWDefltAssistX_HwNm_u8p8[13]	589
t_AsstFWDefltAssistX_HwNm_u8p8[14]	614
t_AsstFWDefltAssistX_HwNm_u8p8[15]	640
t_AsstFWDefltAssistX_HwNm_u8p8[16]	666
t_AsstFWDefltAssistX_HwNm_u8p8[17]	691
t_AsstFWDefltAssistX_HwNm_u8p8[18]	717
t_AsstFWDefltAssistX_HwNm_u8p8[19]	742
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	12698 12902
t_AsstFWDefltAssistY_MtrNm_s4p11[6] t_AsstFWDefltAssistY_MtrNm_s4p11[7]	13107
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	15155
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[19] t AsstFWPstepNstepThresh Cnt u16[0]	15565 169
t_AsstFWPstepNstepThresh_Cnt_u16[1]	395
t_AsstFWVehSpd_Kph_u9p7[0]	16128
t_AsstFWVehSpd_Kph_u9p7[1]	16256
t_AsstFWVehSpd_Kph_u9p7[2]	16384
t_AsstFWVehSpd_Kph_u9p7[3]	16512
t_AsstFWVehSpd_Kph_u9p7[4]	16640
t_AsstFWVehSpd_Kph_u9p7[5]	16768
t_AsstFWVehSpd_Kph_u9p7[6]	16896
t_AsstFWVehSpd_Kph_u9p7[7]	17024
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8 2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	66.5
tgt_AssistFirewall_Per1_verlicleSpeed_kpri_is2.value  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	-
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.659999967	0.660000026 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	395	395 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.60009766	-7.60009766 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.98999977	7.98999977 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-0.25	-0.25 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.91200018	6.91200018 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.659999967	0.660000026 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.60009766	-7.60009766 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>~</b>

Т				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.49 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall ActiveKSV M str.K Uls f32	0.10000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4797
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	4,5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.019999996
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.5
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.600000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00899999961
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.79999995
k_AsstFWInpLimitHFA_MtrNm_f32	3.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	3.29999995
k_AsstFWNstep_Cnt_u16	4551
k_AsstFWPstep_Cnt_u16	2337
k RestoreThresh MtrNm f32	6.9000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
	-12288
t2 AsstFWUnrBoundY MtrNm s4n11[7][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	282
t_AsstFWDefltAssistX_HwNm_u8p8[1]	307
t_AsstFWDefltAssistX_HwNm_u8p8[2]	333
t_AsstFWDefltAssistX_HwNm_u8p8[3]	358
t_AsstFWDefltAssistX_HwNm_u8p8[4]	384
t_AsstFWDefltAssistX_HwNm_u8p8[5]	410
t_AsstFWDefltAssistX_HwNm_u8p8[6]	435
t_AsstFWDefltAssistX_HwNm_u8p8[7]	461
t_AsstFWDefltAssistX_HwNm_u8p8[8]	486
t_AsstFWDefltAssistX_HwNm_u8p8[9]	512 538
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	563
t_AsstFWDefitAssistX_HwNm_u8p8[12]	589
t_AsstFWDefitAssistX_HwNm_u8p8[13]	614
t_AsstFWDefltAssistX_HwNm_u8p8[14]	640
t_AsstFWDefltAssistX_HwNm_u8p8[15]	666
t_AsstFWDefltAssistX_HwNm_u8p8[16]	691
t_AsstFWDefltAssistX_HwNm_u8p8[17]	717
t_AsstFWDefltAssistX_HwNm_u8p8[18]	742
t_AsstFWDefltAssistX_HwNm_u8p8[19]	768
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	12698 12902
t_AsstFWDefltAssistY_MtrNm_s4p11[5] t_AsstFWDefltAssistY_MtrNm_s4p11[6]	13107
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[18] t_AsstFWDefltAssistY_MtrNm_s4p11[19]	15565 15770
t AsstFWPstepNstepThresh Cnt u16[0]	170
t_AsstFWPstepNstepThresh_Cnt_u16[1]	399
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
t_AsstFWVehSpd_Kph_u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-9 1.10000002
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	77.0999985
tgt_Rts_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	1
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.98000002	1.98000002 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	246	246 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	4	4 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.15799999	1.15799999 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-6.4000001	-6.4000001 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.90100002	7.90100002 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4	4 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x00	0x00	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~

T ✓				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	-
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	_

Test Step 2.50 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	3.099999
AssistFirewall ActiveKSV M str.K UIs f32	0.5
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4920
AssistFirewall AsstReducedPerfSV Cnt M Igc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.69999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.029999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.6000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00125584798
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0099999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.8999998
k_AsstFWInpLimitHFA_MtrNm_f32	1.10000002
k_AsstFWInpLimitHysComp_MtrNm_f32	3.5
k_AsstFWNstep_Cnt_u16	4674
k_AsstFWPstep_Cnt_u16	2460
k RestoreThresh MtrNm f32	7
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	10240

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-10240
2 AsstFWUprBoundY MtrNm s4p11[2][7]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096
z_AsstFWUprBoundY_MtrNm_s4p11[2][9] 2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
	-2040
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
2 AsstFWUprBoundY MtrNm s4p11[5][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096
z_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048
	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-6144





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefltAssistX_HwNm_u8p8[0]	307
t_AsstFWDefltAssistX_HwNm_u8p8[1]	333
t_AsstFWDefltAssistX_HwNm_u8p8[2]	358
t_AsstFWDefltAssistX_HwNm_u8p8[3]	384
t_AsstFWDefltAssistX_HwNm_u8p8[4]	410
t_AsstFWDefltAssistX_HwNm_u8p8[5]	435
t_AsstFWDefltAssistX_HwNm_u8p8[6]	461
t_AsstFWDefltAssistX_HwNm_u8p8[7]	486
t_AsstFWDefltAssistX_HwNm_u8p8[8]	512
t_AsstFWDefltAssistX_HwNm_u8p8[9]	538
t_AsstFWDefltAssistX_HwNm_u8p8[10]	563
t_AsstFWDefltAssistX_HwNm_u8p8[11]	589
t_AsstFWDefltAssistX_HwNm_u8p8[12]	614
t_AsstFWDefltAssistX_HwNm_u8p8[13]	640
t_AsstFWDefltAssistX_HwNm_u8p8[14]	666
t_AsstFWDefltAssistX_HwNm_u8p8[15]	691
t_AsstFWDefltAssistX_HwNm_u8p8[16]	717
t_AsstFWDefltAssistX_HwNm_u8p8[17]	742
t_AsstFWDefltAssistX_HwNm_u8p8[18]	768
t_AsstFWDefltAssistX_HwNm_u8p8[19]	794
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	15974
t_AsstFWPstepNstepThresh_Cnt_u16[0]	171
t_AsstFWPstepNstepThresh_Cnt_u16[1]	403
t_AsstFWVehSpd_Kph_u9p7[0]	22016
t_AsstFWVehSpd_Kph_u9p7[1]	22144
t_AsstFWVehSpd_Kph_u9p7[2]	22272
t_AsstFWVehSpd_Kph_u9p7[3]	22400
t_AsstFWVehSpd_Kph_u9p7[4]	22528
t_AsstFWVehSpd_Kph_u9p7[5]	22656
t_AsstFWVehSpd_Kph_u9p7[6]	22784
t_AsstFWVehSpd_Kph_u9p7[7]	22912
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3.099999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	88.0800018
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Iq	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.54999995	1.54999995 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	403	403 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.89990234	5.89990234 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.31700015	2.31699991 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.99497652	4.99497652 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.08899999	1.08899999 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	5.89990234	5.89990234 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.51 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.79999995
AssistFirewall ActiveKSV M str.K Uls f32	0.090000036
AssistFirewall_ActiveRawAcc_Cnt_M_u16	5043
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.039999991
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.70000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.715390444
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.019999996
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2
k_AsstFWInpLimitHFA_MtrNm_f32	2.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	3.70000005
k_AsstFWNstep_Cnt_u16	3567
k_AsstFWPstep_Cnt_u16	2583
k_RestoreThresh_MtrNm_f32	7.0999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288

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Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144	
	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]		
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0	
2 AsstFWUprBoundX HwNm s4p11[7][1]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144	
	8192	
2 ASSTEWUDIBOUNGY MITINM S4D11101141	The state of the s	
	10240	
.2_AsstFWUprBoundY_MtrNm_s4p11[0][4] .2_AsstFWUprBoundY_MtrNm_s4p11[0][5] .2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	10240 12288	

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432 20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10] t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-18432
t2_Asst WoprBoundY_MtrNm_s4p11[2][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-14336
t2_Asst WoprBoundY_MtrNm_s4p11[2][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-6192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	333
t_AsstFWDefltAssistX_HwNm_u8p8[1]	358
t_AsstFWDefltAssistX_HwNm_u8p8[2]	384
t_AsstFWDefltAssistX_HwNm_u8p8[3]	410
t_AsstFWDefltAssistX_HwNm_u8p8[4]	435
t_AsstFWDefltAssistX_HwNm_u8p8[5]	461
t_AsstFWDefltAssistX_HwNm_u8p8[6]	486
t_AsstFWDefltAssistX_HwNm_u8p8[7]	512
t_AsstFWDefltAssistX_HwNm_u8p8[8]	538
t_AsstFWDefltAssistX_HwNm_u8p8[9]	563
t_AsstFWDefltAssistX_HwNm_u8p8[10]	589
t_AsstFWDefltAssistX_HwNm_u8p8[11]	614
t_AsstFWDefltAssistX_HwNm_u8p8[12]	640
t_AsstFWDefltAssistX_HwNm_u8p8[13]	666
t_AsstFWDefltAssistX_HwNm_u8p8[14]	691
t_AsstFWDefltAssistX_HwNm_u8p8[15]	717
t_AsstFWDefltAssistX_HwNm_u8p8[16]	742
t_AsstFWDefltAssistX_HwNm_u8p8[17]	768
t_AsstFWDefltAssistX_HwNm_u8p8[18]	794 819
t_AsstFWDefltAssistX_HwNm_u8p8[19]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[0] t_AsstFWDefltAssistY_MtrNm_s4p11[1]	12493
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	12698
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	13107
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	16179
t_AsstFWPstepNstepThresh_Cnt_u16[0]	172
t_AsstFWPstepNstepThresh_Cnt_u16[1]	407
t_AsstFWVehSpd_Kph_u9p7[0]	24960
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	25088 25216
t_AsstFWVenSpd_kpn_u9p7[2] t_AsstFWVenSpd_kph_u9p7[3]	25216 25344
t_AsstFWVehSpd_kph_u9p7[4]	25344 25472
t_AsstFWVehSpd_kph_u9p7[4] t_AsstFWVehSpd_kph_u9p7[5]	25600
t_AsstFWVehSpd_Kph_u9p7[6]	25728
t_AsstFWVehSpd_Kph_u9p7[7]	25856
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	99.0299988
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.54799986	2.5480001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1476	1476 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6.70019531	-6.70019531 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.29199982	3.29200006 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.4462471	-5.4462471 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.296	2.296 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-6.70019531	-6.70019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.52 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall ActiveKSV M str.K Uls f32	0.100000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	5166
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	4.900001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.7999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall LwrBoundKSV M str.K Uls f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.029999993
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.0999999
k AsstFWInpLimitHFA MtrNm f32	3.29999995
k_AsstFWInpLimitHysComp_MtrNm_f32	3.9000001
k_AsstFWNstep_Cnt_u16	3690
k_AsstFWPstep_Cnt_u16	2706
k RestoreThresh MtrNm f32	7.19999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2 AsstFWUprBoundX HwNm s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2 AsstFWUprBoundX HwNm s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240
E_, SSS. 1. Op. SSSSSSSS_TMTMT_OTP ! [[E][O]	1.02.0





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2 AsstFWUprBoundX HwNm s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2 AsstFWUprBoundX HwNm s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2 AsstFWUprBoundX HwNm s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	
12_710011 11 Opi DodilaX_111111111_0+p 1 1[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8] t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[7][8] t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	-2048 0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8] t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048 0 2048 2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8] t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-2048 0 2048 2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8] t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048 0 2048 2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8] t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-2048 0 2048 2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8] t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048 0 2048 2048 4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8] t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048 0 2048 2048 4096 6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8] t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048 0 2048 2048 4096 6144 8192 10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8] t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048 0 2048 2048 4096 6144 8192 10240 12288

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7.00.00 0.10.10.10.10.10.10.10.10.10.10.10.10.10		
Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	20480	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	2048	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	358
t_AsstFWDefltAssistX_HwNm_u8p8[1]	384
t_AsstFWDefltAssistX_HwNm_u8p8[2]	410
t_AsstFWDefltAssistX_HwNm_u8p8[3]	435
t_AsstFWDefltAssistX_HwNm_u8p8[4]	461
t_AsstFWDefltAssistX_HwNm_u8p8[5]	486
t_AsstFWDefltAssistX_HwNm_u8p8[6]	512
t_AsstFWDefltAssistX_HwNm_u8p8[7]	538 563
t_AsstFWDefltAssistX_HwNm_u8p8[8] t_AsstFWDefltAssistX_HwNm_u8p8[9]	589
t_AsstFWDefltAssistX_HwNm_u8p8[10]	614
t_AsstFWDefltAssistX_HwNm_u8p8[11]	640
t AsstFWDefltAssistX HwNm u8p8[12]	666
t AsstFWDefltAssistX HwNm u8p8[13]	691
t_AsstFWDefltAssistX_HwNm_u8p8[14]	717
t_AsstFWDefltAssistX_HwNm_u8p8[15]	742
t_AsstFWDefltAssistX_HwNm_u8p8[16]	768
t_AsstFWDefltAssistX_HwNm_u8p8[17]	794
t_AsstFWDefltAssistX_HwNm_u8p8[18]	819
t_AsstFWDefltAssistX_HwNm_u8p8[19]	845
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	14950 15155
t_AsstFWDefltAssistY_MtrNm_s4p11[13] t_AsstFWDefltAssistY_MtrNm_s4p11[14]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	16384
t_AsstFWPstepNstepThresh_Cnt_u16[0]	173
t_AsstFWPstepNstepThresh_Cnt_u16[1]	411
t_AsstFWVehSpd_Kph_u9p7[0]	27904
t_AsstFWVehSpd_Kph_u9p7[1]	28032
t_AsstFWVehSpd_Kph_u9p7[2]	28160
t_AsstFWVehSpd_Kph_u9p7[3]	28288
t_AsstFWVehSpd_Kph_u9p7[4]	28416
t_AsstFWVehSpd_Kph_u9p7[5]	28544
t_AsstFWVehSpd_Kph_u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7]	28800
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	123.010002 tot AssistEirowall Port AssistirowallActive Lile f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
THE THE THE PROJECT TOWARD ASSIST TOWARD FOR CONTINUED ASSIST WITHIN 132	13- 1000 Hewaii et i _00Hbiiled/3515[William]
	tot AssistFirewall Per1 Defeat AsstThl Service Cnt Inc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lett_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32

AssistFirewall\_Per1







Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8] t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10] t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_Asst WopiboundX_1WMin_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2 AsstFWUprBoundX HwNm s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	6144
	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	18432
LE MOST WOODDOUGGE WITHING SADERIUM	10432





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
2 AsstFWUprBoundY MtrNm s4p11[2][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048
z_AsstFWUprBoundY_MtrNm_s4p11[2][9] 2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096
	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	26624
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	2048
z_AsstFWUprBoundY_MtrNm_s4p11[5][7]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048





Name	Input Value
12_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
12_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
z_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefitAssistX_HwNm_u8p8[0]	384
: AsstFWDefitAssistX HwNm u8p8[1]	410
: AsstFWDefitAssistX HwNm u8p8[2]	435
_AsstFWDefitAssistX_HwNm_u8p8[3]	461
AsstFWDefitAssistX HwNm u8p8[4]	486
AsstFWDefitAssistX HwNm u8p8[5]	512
_AsstFWDefitAssistX_HwNm_u8p8[6]	538
_AsstFWDefitAssistX_HwNm_u8p8[7]	563
_AsstFWDefitAssistX_HwNm_u8p8[8]	589
_AsstFWDefltAssistX_HwNm_u8p8[9]	614
_AsstFWDefltAssistX_HwNm_u8p8[10]	640
AsstFWDefitAssistX HwNm u8p8[11]	666
AsstFWDefitAssistX_HwNm_u8p8[12]	691
, , ,	
_AsstFWDefitAssistX_HwNm_u8p8[13]	717 742
_AsstFWDefitAssistX_HwNm_u8p8[14]	
_AsstFWDefltAssistX_HwNm_u8p8[15]	768
_AsstFWDefltAssistX_HwNm_u8p8[16]	794
_AsstFWDefltAssistX_HwNm_u8p8[17]	819
_AsstFWDefltAssistX_HwNm_u8p8[18]	845
_AsstFWDefltAssistX_HwNm_u8p8[19]	870
_AsstFWDefltAssistY_MtrNm_s4p11[0]	12698
_AsstFWDefltAssistY_MtrNm_s4p11[1]	12902
:_AsstFWDefltAssistY_MtrNm_s4p11[2]	13107
_AsstFWDefltAssistY_MtrNm_s4p11[3]	13312
_AsstFWDefltAssistY_MtrNm_s4p11[4]	13517
_AsstFWDefltAssistY_MtrNm_s4p11[5]	13722
:_AsstFWDefltAssistY_MtrNm_s4p11[6]	13926
:_AsstFWDefltAssistY_MtrNm_s4p11[7]	14131
:_AsstFWDefltAssistY_MtrNm_s4p11[8]	14336
:_AsstFWDefltAssistY_MtrNm_s4p11[9]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	14746
_AsstFWDefltAssistY_MtrNm_s4p11[11]	14950
:_AsstFWDefltAssistY_MtrNm_s4p11[12]	15155
:_AsstFWDefltAssistY_MtrNm_s4p11[13]	15360
:_AsstFWDefltAssistY_MtrNm_s4p11[14]	15565
:_AsstFWDefltAssistY_MtrNm_s4p11[15]	15770
_AsstFWDefltAssistY_MtrNm_s4p11[16]	15974
_AsstFWDefltAssistY_MtrNm_s4p11[17]	16179
:_AsstFWDefltAssistY_MtrNm_s4p11[18]	16384
_AsstFWDefltAssistY_MtrNm_s4p11[19]	16589
_AsstFWPstepNstepThresh_Cnt_u16[0]	174
_AsstFWPstepNstepThresh_Cnt_u16[1]	415
_AsstFWVehSpd_Kph_u9p7[0]	30848
_AsstFWVehSpd_Kph_u9p7[1]	30976
_AsstFWVehSpd_Kph_u9p7[2]	31104
_AsstFWVehSpd_Kph_u9p7[3]	31232
_AsstFWVehSpd_Kph_u9p7[4]	31360
_AsstFWVehSpd_Kph_u9p7[5]	31488
_AsstFWVehSpd_Kph_u9p7[6]	31616
:_AsstFWVehSpd_Kph_u9p7[7]	31744
gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2
gt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
gt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.0999999
gt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.0999999
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	234.050003
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cn	t_l( tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
rgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

AssistFirewall\_Per1





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-7.03999996	-7.03999996 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	415	415 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.10009766	8.10009766 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.42399979	5.42399979 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.82999992	6.82999992 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.41599989	4.41599989 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.10009766	8.10009766 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.54 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8.80000019
AssistFirewall ActiveKSV M str.K UIs f32	0.30000012
AssistFirewall_ActiveRawAcc_Cnt_M_u16	5412
AssistFirewall AsstReducedPerfSV Cnt M Iqc	0
AssistFirewall CombAsstSV MtrNm M f32	-4.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.070000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall LwrBoundKSV M str.K Uls f32	0.10000001
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0500000007
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.29999995
k_AsstFWInpLimitHFA_MtrNm_f32	5.5
k_AsstFWInpLimitHysComp_MtrNm_f32	4.30000019
k_AsstFWNstep_Cnt_u16	3936
k_AsstFWPstep_Cnt_u16	2952
k RestoreThresh MtrNm f32	7.400001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288 14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2 AsstFWUprBoundX HwNm s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6] t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_Asstr-WoprBoundX_HwNm_s4p11[7][7] t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	20480

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	26624
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0
	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	2048
2 AsstFWUprBoundY MtrNm s4p11[4][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
z_AsstFWUprBoundY_MtrNm_s4p11[5][2] 2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
:2_AsstFWUprBoundY_MtrNm_s4p11[5][3] :2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-2048 0
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144
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t2_AsstFWUprBoundY_MtrNm_s4p11[7][4] t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] t_AsstFWUprBoundY_MtrNm_s4p11[7][10] t_AsstFWDefltAssistX_HwNm_u8p8[0] t_AsstFWDefltAssistX_HwNm_u8p8[1]	Input Value 8192 10240 12288 14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5] t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] t_AsstFWUprBoundY_MtrNm_u8p8[0] t_AsstFWDefltAssistX_HwNm_u8p8[1]	10240 12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] t_AsstFWDefltAssistX_HwNm_u8p8[0] t_AsstFWDefltAssistX_HwNm_u8p8[1]	12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] t_AsstFWDefltAssistX_HwNm_u8p8[0] t_AsstFWDefltAssistX_HwNm_u8p8[1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] t_AsstFWDefltAssistX_HwNm_u8p8[0] t_AsstFWDefltAssistX_HwNm_u8p8[1]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] t_AsstFWDefltAssistX_HwNm_u8p8[0] t_AsstFWDefltAssistX_HwNm_u8p8[1]	
t_AsstFWDefltAssistX_HwNm_u8p8[0] t_AsstFWDefltAssistX_HwNm_u8p8[1]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[1]	20480
	410
A A CALE VA D CALL A CA	435
t_AsstFWDefltAssistX_HwNm_u8p8[2]	461
t_AsstFWDefltAssistX_HwNm_u8p8[3]	486
	512
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	563
	589
	614
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	768
	794
	819
	845
, ,	870
t_AsstFWDefltAssistX_HwNm_u8p8[19]	896
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	13926
	14131
	14336
	14541
	14746
, ; ;	14950
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	15770
	15974
, , ,	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	16384
	16589
	16794
	175
t_AsstFWPstepNstepThresh_Cnt_u16[1]	419
	33792
t_AsstFWVehSpd_Kph_u9p7[1]	33920
t_AsstFWVehSpd_Kph_u9p7[2]	34048
t_AsstFWVehSpd_Kph_u9p7[3]	34176
t_AsstFWVehSpd_Kph_u9p7[4]	34304
t_AsstFWVehSpd_Kph_u9p7[5]	34432
t_AsstFWVehSpd_Kph_u9p7[6]	34560
	34688
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, ,	24.2999992 tot AssistEirowall Port AsstEirowallActive IIIs f22
	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

2015-03-23, 11:55:49+0530



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.15999985	6.15999985 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	419	419 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	6.29980469	6.29980469 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.97399998	5.97399998 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.189999998	0.189999998 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.34499979	5.34499979 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	•
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	6.29980469	6.29980469 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	<b>~</b>
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.55 (Repeat Count = 1)	variation of the state of the
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0
AssistFirewall ActiveKSV M str.K Uls f32	0.059999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	5535
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.200000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0599999987
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.4000001
k_AsstFWInpLimitHFA_MtrNm_f32	6.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	4.5
k_AsstFWNstep_Cnt_u16	4059
k_AsstFWPstep_Cnt_u16	3075
k_RestoreThresh_MtrNm_f32	7.5
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336 16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10] t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-8192
t2_Asst WoproundX_HwNm_s4p11[3][1]	-6144
t2_Asst WoproundX_1wNin_s4p11[3][1]	-4096
t2_Asst WoprboundX_HwNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	12288
t2 AsstFWUprBoundX HwNm s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2 AsstFWUprBoundX HwNm s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	1843.2 20480
12_70011 VVOPIDOUIIU I _IVIIIIVIII_54P I I[U][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	22528





Input Value
24576
26624
28672
-6144
-4096
-2048
0
2048
4096
6144
8192
10240
12288 14336
-12288
-10240
-8192
-6144
-4096
-2048
0
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4096
6144
8192
-16384
-14336
-12288
-10240
-8192
-6144
-4096
-2048
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-12288 -10240
-10240 -8192
-6144
-4096
-2048
0
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-6144
-4096
-2048
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6144
8192
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12288
14336
0
2048
4096
6144
8192
10240 12288
14336
16384
16384 18432
16384 18432 20480
16384 18432 20480 8192
16384 18432 20480





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	22528 24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	435
t_AsstFWDefltAssistX_HwNm_u8p8[1]	461
t_AsstFWDefltAssistX_HwNm_u8p8[2]	486
t_AsstFWDefltAssistX_HwNm_u8p8[3]	512
t_AsstFWDefltAssistX_HwNm_u8p8[4]	538
t_AsstFWDefltAssistX_HwNm_u8p8[5]	563
t_AsstFWDefltAssistX_HwNm_u8p8[6]	589
t_AsstFWDefltAssistX_HwNm_u8p8[7]	614
t_AsstFWDefltAssistX_HwNm_u8p8[8]	640
t_AsstFWDefltAssistX_HwNm_u8p8[9]	666 691
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	717
t_AsstFWDefltAssistX_HwNm_u8p8[12]	742
t_AsstFWDefitAssistX_HwNm_u8p8[13]	768
t_AsstFWDefltAssistX_HwNm_u8p8[14]	794
t_AsstFWDefltAssistX_HwNm_u8p8[15]	819
t_AsstFWDefltAssistX_HwNm_u8p8[16]	845
t_AsstFWDefltAssistX_HwNm_u8p8[17]	870
t_AsstFWDefltAssistX_HwNm_u8p8[18]	896
t_AsstFWDefltAssistX_HwNm_u8p8[19]	922
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[5] t_AsstFWDefltAssistY_MtrNm_s4p11[6]	14131 14336
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[18] t_AsstFWDefltAssistY_MtrNm_s4p11[19]	16794 16998
t AsstFWPstepNstepThresh Cnt u16[0]	176
t_AsstFWPstepNstepThresh_Cnt_u16[1]	423
t_AsstFWVehSpd_Kph_u9p7[0]	36736
t_AsstFWVehSpd_Kph_u9p7[1]	36864
t_AsstFWVehSpd_Kph_u9p7[2]	36992
t_AsstFWVehSpd_Kph_u9p7[3]	37120
t_AsstFWVehSpd_Kph_u9p7[4]	37248
t_AsstFWVehSpd_Kph_u9p7[5]	37376
t_AsstFWVehSpd_Kph_u9p7[6]	37504
t_AsstFWVehSpd_Kph_u9p7[7]	37632
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2 -2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	57.099985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0	0 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1476	1476 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6.70019531	-6.70019531 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.43200004	1.43200004 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-0.440000057	-0.43999998 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.15399981	6.15399981 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-6.70019531	-6.70019531 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x00	0x00	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

au				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	•

Test Step 2.56 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.5
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0700000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	5658
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.090000036
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.02999997
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.30000012
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0700000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.5
k_AsstFWInpLimitHFA_MtrNm_f32	7.69999981
k_AsstFWInpLimitHysComp_MtrNm_f32	4.69999981
k_AsstFWNstep_Cnt_u16	4182
k_AsstFWPstep_Cnt_u16	3198
k_RestoreThresh_MtrNm_f32	7.5999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048
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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384 18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
t2 AsstFWUprBoundX HwNm s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2 AsstFWUprBoundX HwNm s4p11[4][2]	0
t2 AsstFWUprBoundX HwNm s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-2048

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710010tt 110Wall_1 Ct 1	
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-22528
t2_AsstrWUprBoundY_MtrNm_s4p11[1][5]	-20480
	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-8192
	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
12_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-12288 -10240





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	461
t_AsstFWDefltAssistX_HwNm_u8p8[1]	486
t_AsstFWDefltAssistX_HwNm_u8p8[2]	512
t_AsstFWDefltAssistX_HwNm_u8p8[3]	538
t_AsstFWDefltAssistX_HwNm_u8p8[4]	563
t_AsstFWDefltAssistX_HwNm_u8p8[5]	589
t_AsstFWDefltAssistX_HwNm_u8p8[6]	614
t_AsstFWDefltAssistX_HwNm_u8p8[7]	640
t_AsstFWDefltAssistX_HwNm_u8p8[8]	666
t_AsstFWDefltAssistX_HwNm_u8p8[9]	691
t_AsstFWDefltAssistX_HwNm_u8p8[10]	717
t_AsstFWDefltAssistX_HwNm_u8p8[11]	742
t_AsstFWDefltAssistX_HwNm_u8p8[12]	768
t_AsstFWDefltAssistX_HwNm_u8p8[13]	794
t_AsstFWDefltAssistX_HwNm_u8p8[14]	819
t_AsstFWDefltAssistX_HwNm_u8p8[15]	845
t_AsstFWDefltAssistX_HwNm_u8p8[16]	870
t_AsstFWDefltAssistX_HwNm_u8p8[17]	896
t_AsstFWDefltAssistX_HwNm_u8p8[18]	922
t_AsstFWDefltAssistX_HwNm_u8p8[19]	947
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	15155
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	15360
	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	16589
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	17203
t_AsstFWPstepNstepThresh_Cnt_u16[0]	177
t_AsstFWPstepNstepThresh_Cnt_u16[1]	427
t_AsstFWVehSpd_Kph_u9p7[0]	39680
t_AsstFWVehSpd_Kph_u9p7[1]	39808
t_AsstFWVehSpd_Kph_u9p7[2]	39936
t_AsstFWVehSpd_Kph_u9p7[3]	40064
t_AsstFWVehSpd_Kph_u9p7[4]	40192
t_AsstFWVehSpd_Kph_u9p7[5]	40320
t_AsstFWVehSpd_Kph_u9p7[6]	40448
t_AsstFWVehSpd_Kph_u9p7[7]	40576
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	89.0699997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_rtte_inst_Ap_Assisti irewali.Assisti irewali_i eri_combinedAssist_ivitiviii isz	
	tgt_assistfirewaii_peri_deteat_asstidi Service Cht iqc
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_tqtAssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsstTbl\_Service\_Cnt\_tqtAsst$	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Itgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.11499977	5.11499977 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	427	427 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.70019531	-7.70019531 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.58500004	2.58500004 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.46999979	2.47000003 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	0.43999998	0.439999998 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.70019531	-7.70019531 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	•
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.57 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.5
AssistFirewall ActiveKSV M str.K Uls f32	0.0799999982
AssistFirewall_ActiveRawAcc_Cnt_M_u16	5781
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.200000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.03999996
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0799999982
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.5999999
k_AsstFWInpLimitHFA_MtrNm_f32	3.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	4.9000001
k_AsstFWNstep_Cnt_u16	4305
k_AsstFWPstep_Cnt_u16	3321
k_RestoreThresh_MtrNm_f32	7.69999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384 -14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6] t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9] t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_Asst WoproundX_HwNm_s4p11[6][0]	-16384
t2_Asst WoproduidX_i wwiii_s4p i [o][o] t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2 AsstFWUprBoundX HwNm s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_Asst WoproduidX_i wwiii_s4p i [o][o] t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_Asst WoproundX_1WMin_s4p11[6][9]	4096
t2_Asst WopiBoundX_HwNm_s4p11[0][10]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2046 0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_mwnm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_Asst WoproundX_1WMin_s4p11[7][7] t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_Asst WoproundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
· · · · · · · · · · · · · · · · · · ·	-12288 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240 -8192
· · · · · · · · · · · · · · · · · · ·	-8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	0

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ASSISTRIEWAII_PELL		CIU
Name	Input Value	
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-28672	
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-26624	
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-24576	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096	
	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2040	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]		
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	486
t_AsstFWDefltAssistX_HwNm_u8p8[1]	512
t_AsstFWDefltAssistX_HwNm_u8p8[2]	538
t_AsstFWDefltAssistX_HwNm_u8p8[3]	563
t_AsstFWDefltAssistX_HwNm_u8p8[4]	589
t_AsstFWDefltAssistX_HwNm_u8p8[5]	614
t_AsstFWDefltAssistX_HwNm_u8p8[6]	640
t_AsstFWDefltAssistX_HwNm_u8p8[7]	666
t_AsstFWDefltAssistX_HwNm_u8p8[8]	691
t_AsstFWDefltAssistX_HwNm_u8p8[9]	717 742
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	768
t_AsstFWDefltAssistX_HwNm_u8p8[12]	794
t_AsstFWDefitAssistX_HwNm_u8p8[13]	819
t_AsstFWDefltAssistX_HwNm_u8p8[14]	845
t_AsstFWDefltAssistX_HwNm_u8p8[15]	870
t_AsstFWDefltAssistX_HwNm_u8p8[16]	896
t_AsstFWDefltAssistX_HwNm_u8p8[17]	922
t_AsstFWDefltAssistX_HwNm_u8p8[18]	947
t_AsstFWDefltAssistX_HwNm_u8p8[19]	973
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[5] t_AsstFWDefltAssistY_MtrNm_s4p11[6]	14541 14746
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[18] t_AsstFWDefltAssistY_MtrNm_s4p11[19]	17203 17408
t AsstFWPstepNstepThresh Cnt u16[0]	178
t_AsstFWPstepNstepThresh_Cnt_u16[1]	431
t_AsstFWVehSpd_Kph_u9p7[0]	42624
t_AsstFWVehSpd_Kph_u9p7[1]	42752
t_AsstFWVehSpd_Kph_u9p7[2]	42880
t_AsstFWVehSpd_Kph_u9p7[3]	43008
t_AsstFWVehSpd_Kph_u9p7[4]	43136
t_AsstFWVehSpd_Kph_u9p7[5]	43264
t_AsstFWVehSpd_Kph_u9p7[6]	43392
t_AsstFWVehSpd_Kph_u9p7[7]	43520
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	10.1000004
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.05999994	-5.05999994 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	431	431 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.5	8.5 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.53999996	4.53999996 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.26000023	5.26000023 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.84000003	1.84000003 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.5	8.5 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Τ				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.58 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5
AssistFirewall ActiveKSV M str.K Uls f32	0.00125584798
AssistFirewall_ActiveRawAcc_Cnt_M_u16	5904
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	-4.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.300000012
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.04999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall LwrBoundKSV M str.K Uls f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.090000036
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.70000005
k AsstFWInpLimitHFA MtrNm f32	3.4000001
k_AsstFWInpLimitHysComp_MtrNm_f32	5.0999999
k_AsstFWNstep_Cnt_u16	4428
k_AsstFWPstep_Cnt_u16	3444
k RestoreThresh MtrNm f32	7.80000019
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2 AsstFWUprBoundX HwNm s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2 AsstFWUprBoundX HwNm s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384
	1000





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10] t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048
t2_Asst WopiboundX_1WMn_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
t2_Asst-WopiboundX_1WNm_s4p11[3][1] t2_Asst-FWUprBoundX_HwNm_s4p11[3][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096 -14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1] t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_Asst WopioundX_1WMn_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2 AsstFWUprBoundX HwNm s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	0 2048

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	512
t_AsstFWDefltAssistX_HwNm_u8p8[1]	538
t_AsstFWDefltAssistX_HwNm_u8p8[2]	563
t_AsstFWDefltAssistX_HwNm_u8p8[3]	589
t_AsstFWDefltAssistX_HwNm_u8p8[4]	614
t_AsstFWDefltAssistX_HwNm_u8p8[5]	640
t_AsstFWDefltAssistX_HwNm_u8p8[6]	666
t_AsstFWDefltAssistX_HwNm_u8p8[7]	691
t_AsstFWDefltAssistX_HwNm_u8p8[8]	717
t_AsstFWDefltAssistX_HwNm_u8p8[9]	742 768
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	794
t_AsstFWDefitAssistX_HwNm_u8p8[12]	819
t_AsstFWDefltAssistX_HwNm_u8p8[13]	845
t_AsstFWDefltAssistX_HwNm_u8p8[14]	870
t_AsstFWDefltAssistX_HwNm_u8p8[15]	896
t_AsstFWDefltAssistX_HwNm_u8p8[16]	922
t_AsstFWDefltAssistX_HwNm_u8p8[17]	947
t_AsstFWDefltAssistX_HwNm_u8p8[18]	973
t_AsstFWDefltAssistX_HwNm_u8p8[19]	998
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[5] t_AsstFWDefltAssistY_MtrNm_s4p11[6]	14746 14950
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[18] t_AsstFWDefltAssistY_MtrNm_s4p11[19]	17408 17613
t AsstFWPstepNstepThresh Cnt u16[0]	179
t_AsstFWPstepNstepThresh_Cnt_u16[1]	435
t_AsstFWVehSpd_Kph_u9p7[0]	45568
t_AsstFWVehSpd_Kph_u9p7[1]	45696
t_AsstFWVehSpd_Kph_u9p7[2]	45824
t_AsstFWVehSpd_Kph_u9p7[3]	45952
t_AsstFWVehSpd_Kph_u9p7[4]	46080
t_AsstFWVehSpd_Kph_u9p7[5]	46208
t_AsstFWVehSpd_Kph_u9p7[6]	46336
t_AsstFWVehSpd_Kph_u9p7[7]	46464
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-3 2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	40.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	1
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4.99372053	4.99372053 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	435	435 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.70019531	-7.70019531 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.75	4.75 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.04999995	3.04999995 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.19000006	2.19000006 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.70019531	-7.70019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

T .			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.59 (Repeat Count = 1)	✓
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6
AssistFirewall ActiveKSV M str.K Uls f32	0.715390444
AssistFirewall_ActiveRawAcc_Cnt_M_u16	6027
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.69999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.40000006
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.05999994
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.600000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00499999989
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.79999995
k_AsstFWInpLimitHFA_MtrNm_f32	3.599999
k_AsstFWInpLimitHysComp_MtrNm_f32	5.30000019
k_AsstFWNstep_Cnt_u16	4551
k_AsstFWPstep_Cnt_u16	3567
k_RestoreThresh_MtrNm_f32	7.9000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2 AsstFWUprBoundX HwNm s4p11[2][2]	
	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2 AsstFWUprBoundX HwNm s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144 -4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144 -4096 -2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144 -4096 -2048





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144
A MANUFACTURE OF THE PROPERTY	-4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefltAssistX_HwNm_u8p8[0]	538
t_AsstFWDefltAssistX_HwNm_u8p8[1]	563
t_AsstFWDefltAssistX_HwNm_u8p8[2]	589 614
t_AsstFWDefltAssistX_HwNm_u8p8[3] t_AsstFWDefltAssistX_HwNm_u8p8[4]	640
t_AsstFWDefltAssistX_HwNm_u8p8[5]	666
t_AsstFWDefltAssistX_HwNm_u8p8[6]	691
t_AsstFWDefltAssistX_HwNm_u8p8[7]	717
t_AsstFWDefltAssistX_HwNm_u8p8[8]	742
t_AsstFWDefitAssistX_HwNm_u8p8[9]	768
t_AsstFWDefltAssistX_HwNm_u8p8[10]	794
t_AsstFWDefltAssistX_HwNm_u8p8[11]	819
t_AsstFWDefltAssistX_HwNm_u8p8[12]	845
t_AsstFWDefitAssistX_HwNm_u8p8[13]	870
t_AsstFWDefltAssistX_HwNm_u8p8[14]	896
t_AsstFWDefitAssistX_HwNm_u8p8[15]	922
t_AsstFWDefltAssistX_HwNm_u8p8[16]	947
t AsstFWDefitAssistX HwNm u8p8[17]	973
t_AsstFWDefltAssistX_HwNm_u8p8[18]	998
t AsstFWDefltAssistX HwNm u8p8[19]	1024
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	17818
t_AsstFWPstepNstepThresh_Cnt_u16[0]	180
t_AsstFWPstepNstepThresh_Cnt_u16[1]	439
t_AsstFWVehSpd_Kph_u9p7[0]	1408
t_AsstFWVehSpd_Kph_u9p7[1]	1536
t_AsstFWVehSpd_Kph_u9p7[2]	1664
t_AsstFWVehSpd_Kph_u9p7[3]	1792
t_AsstFWVehSpd_Kph_u9p7[4]	1920
t_AsstFWVehSpd_Kph_u9p7[5]	2048
t_AsstFWVehSpd_Kph_u9p7[6]	2176
t_AsstFWVehSpd_Kph_u9p7[7]	2304
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2.20000005
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	50.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tot Dto Inst An AssistEirowell AssistEirowell Dord MEC Counter Cnt onum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	1.8-2





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.70765734	1.70765722 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	439	439 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.70019531	8.70019531 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.51999998	6.51999998 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.44000006	5.44000006 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.9849999	3.9849999 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.70019531	8.70019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T .			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.60 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.5
AssistFirewall_ActiveRawAcc_Cnt_M_u16	6150
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.5
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.07000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.090000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00600000005
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
<pre>c_AsstFWInpLimitBaseAsst_MtrNm_f32</pre>	2.9000001
C_AsstFWInpLimitHFA_MtrNm_f32	3.7999995
C_AsstFWInpLimitHysComp_MtrNm_f32	5.5
c_AsstFWNstep_Cnt_u16	4674
:_AsstFWPstep_Cnt_u16	3690
_RestoreThresh_MtrNm_f32	8
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
z_AsstFWUprBoundX_HWNm_s4p11[3][9] 2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
2 AsstFWUprBoundX HwNm s4p11[5][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
2 AsstFWUprBoundX HwNm s4p11[6][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
:2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	6144

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5] t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-12288 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-8192
t2_Asst WopiBoundY_MtrNm_s4p11[1][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	12288 -16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240
t2_Asst WopiBoundY_MtrNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	563
t_AsstFWDefltAssistX_HwNm_u8p8[1]	589
t_AsstFWDefltAssistX_HwNm_u8p8[2]	614
t_AsstFWDefltAssistX_HwNm_u8p8[3]	640
t_AsstFWDefltAssistX_HwNm_u8p8[4]	666
t_AsstFWDefltAssistX_HwNm_u8p8[5]	691
t_AsstFWDefltAssistX_HwNm_u8p8[6]	717
t_AsstFWDefltAssistX_HwNm_u8p8[7]	742
t_AsstFWDefltAssistX_HwNm_u8p8[8]	768
t_AsstFWDefltAssistX_HwNm_u8p8[9]	794 819
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	845
t_AsstFWDefltAssistX_HwNm_u8p8[12]	870
t_AsstFWDefitAssistX_HwNm_u8p8[13]	896
t_AsstFWDefltAssistX_HwNm_u8p8[14]	922
t_AsstFWDefltAssistX_HwNm_u8p8[15]	947
t_AsstFWDefltAssistX_HwNm_u8p8[16]	973
t_AsstFWDefltAssistX_HwNm_u8p8[17]	998
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1050
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[4] t_AsstFWDefltAssistY_MtrNm_s4p11[5]	14950 15155
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	15360
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	16998
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[16] t_AsstFWDefltAssistY_MtrNm_s4p11[17]	17408
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	17613 17818
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	18022
t AsstFWPstepNstepThresh Cnt u16[0]	181
t_AsstFWPstepNstepThresh_Cnt_u16[1]	443
t_AsstFWVehSpd_Kph_u9p7[0]	4352
t_AsstFWVehSpd_Kph_u9p7[1]	4480
t_AsstFWVehSpd_Kph_u9p7[2]	4608
t_AsstFWVehSpd_Kph_u9p7[3]	4736
t_AsstFWVehSpd_Kph_u9p7[4]	4864
t_AsstFWVehSpd_Kph_u9p7[5]	4992
t_AsstFWVehSpd_Kph_u9p7[6]	5120
t_AsstFWVehSpd_Kph_u9p7[7]	5248
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igc.value tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	0 1
tgt_AssistFireWall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	60.4000015
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_locations and the property of $	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.5	3.5 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1476	1476 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	•
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.70019531	7.70019531 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.85000014	1.85000002 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.26999998	1.26999998 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.96999979	4.96999979 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	•
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	7.70019531	7.70019531 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	•
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x00	0x00	<b>~</b>
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.61 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	6273
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.9000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-52.7999992
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.60000024
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.08000004
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00700000022
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3
k_AsstFWInpLimitHFA_MtrNm_f32	4
k_AsstFWInpLimitHysComp_MtrNm_f32	5.69999981
k_AsstFWNstep_Cnt_u16	3567
k_AsstFWPstep_Cnt_u16	3813
k_RestoreThresh_MtrNm_f32	8.10000038
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240
_ ,	





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192 10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10] t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_Asst WoprboundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][0] t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240 -8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1] t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4] t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192 10240
tz_AsstFWUprBoundX_HwNm_s4p11[7][5] t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_Asst WopibulidX_1WNin_s4p11[7][7] t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
== 1000 110p:200:10 = 110:10   p : 1[0][0]	

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Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
:2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
z_AsstFWUprBoundY_MtrNm_s4p11[6][3] 2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6192
	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefitAssistX_HwNm_u8p8[0]	589
t_AsstFWDefltAssistX_HwNm_u8p8[1]	614
t_AsstFWDefltAssistX_HwNm_u8p8[2]	640
t_AsstFWDefltAssistX_HwNm_u8p8[3]	666
t_AsstFWDefltAssistX_HwNm_u8p8[4]	691
t_AsstFWDefltAssistX_HwNm_u8p8[5]	717
t_AsstFWDefltAssistX_HwNm_u8p8[6]	742
t_AsstFWDefltAssistX_HwNm_u8p8[7]	768
t_AsstFWDefltAssistX_HwNm_u8p8[8]	794
t_AsstFWDefltAssistX_HwNm_u8p8[9]	819
t_AsstFWDefltAssistX_HwNm_u8p8[10]	845
t_AsstFWDefltAssistX_HwNm_u8p8[11]	870
t_AsstFWDefltAssistX_HwNm_u8p8[12]	896
t_AsstFWDefltAssistX_HwNm_u8p8[13]	922
t_AsstFWDefltAssistX_HwNm_u8p8[14]	947
t_AsstFWDefltAssistX_HwNm_u8p8[15]	973
t_AsstFWDefltAssistX_HwNm_u8p8[16]	998
t_AsstFWDefitAssistX_HwNm_u8p8[17]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1075
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	14746 14950
t_AsstFWDefltAssistY_MtrNm_s4p11[3] t_AsstFWDefltAssistY_MtrNm_s4p11[4]	15155
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	15360
t_AsstFWDefitAssistY_MtrNm_s4p11[6]	15565
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	18227
t_AsstFWPstepNstepThresh_Cnt_u16[0]	182
t_AsstFWPstepNstepThresh_Cnt_u16[1]	447
t_AsstFWVehSpd_Kph_u9p7[0]	7296
t_AsstFWVehSpd_Kph_u9p7[1]	7424
t_AsstFWVehSpd_Kph_u9p7[2]	7552
t_AsstFWVehSpd_Kph_u9p7[3]	7680
t_AsstFWVehSpd_Kph_u9p7[4]	7808
t_AsstFWVehSpd_Kph_u9p7[5] t AsstFWVehSpd Kph u9p7[6]	7936 8064
t_AsstFWVenSpd_kpn_u9p7[6] t_AsstFWVehSpd_kph_u9p7[7]	8192
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	70.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

AssistFirewall\_Per1







Nama	Input Value
Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	8192
ASSIEVVUDIBOURGY MITTING SANTHUIGI	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	12288





Name		
	Name	Input Value
	t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336
2. Assert Victorian Minns   1941  1010   1942    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    1944    194		16384
2.AmPW/b60mm/ Johns _sep1109		
2		
L. Asari Virti Boson's Manh   septility   14388		
2 ASSANDARDSONAN Mente sept1105         1.0280           2 ASSANDARDSONAN Mente sept1106         31020           2 ASSANDARDSONAN Mente sept1106         4144           2 ASSANDARDSONAN Mente sept1107         4068           2 ASSANDARDSONAN MENTE SEP1107         0           2 ASSANDARDSONAN MENTE SEP1107         1028           2 ASSANDARDSONAN MENTE SEP1107         1026           2 ASSANDARDSONAN MENTE SEP1107         1042           2 ASSANDARDSONAN MENTE SEP1107         1040		
2.AsaFWQ Bound's Manhs _sep11108   -0102   -0.AsaFWQ Bound's Manhs _sep11108   -0102   -0.AsaFWQ Bound's Manhs _sep11108   -0106   -0.AsaFWQ Bound's Manhs _sep11108   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06   -0.06	t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-14336
2_AmaPrilyBookand   Ambre _ sept 11 5    -6144    -2_AmaPrilyBookand   Ambre _ sept 11 7    -6164    -2_AmaPrilyBookand   Ambre _ sept 11 7    -6164    -2_AmaPrilyBookand   Ambre _ sept 11 7    -6166    -2_AmaPrilyBookand   Ambre _ sept 11 7    -6264    -2_AmaPrilyBookand   Ambre _ sept 11 7    -6064    -2_AmaPrilyBookand   Ambre _ sept 11 7    -6064    -2_AmaPrilyBookand   Ambre _ sept 12 7    -6064    -2_Am	t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-12288
P.A.BEFUNDSONONY	t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-10240
2.ABF/UGBOURD, Miching, 1651 TILING   5164   2.ABF/UGBOURD, Miching, 1651 TILING   2068   2068   2.ABF/UGBOURD, Miching, 1651 TILING   2069   2.ABF/UGBOURD, Miching, 1651 TILING   2.ABF/UGBOU	t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-8192
2. Asself-Villy-Bound Marks 16511[10]		-6144
2_ABF/UpGBoard/, Mehm. as511178		
P. ASSEPUNDBOOMY   Minth, sept 1001   1044   1026   1044   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026   1026		
2.AssFVU/p8ount/ Min*.psi112 1   914	t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	
2. AssEPUNJEBOUNY   Minh. sep112 12 10    10240     2. AssEPUNJEBOUNY   Minh. sep112 12 10    10240     2. AssEPUNJEBOUNY   Minh. sep112 12 11     3. AssEPUNJEBOUNY   Minh. sep112 13 11     3. AssEPUNJEBOUNY   Minh. sep112 13 11     4. AssEPUNJEBOUNY   Minh. sep112 13 11     4. AssEPUNJEBOUNY   Minh. sep112 13 11     5. AssEPUNJEBOUNY   Minh. sep112 13 11     5. AssEPUNJEBOUNY   Minh. sep113 13 11     6. AssEPUNJEBOUNY   Minh. sep113 13 11     6. AssEPUNJEBOUNY   Minh. sep113 13 11     7. AssEPUNJEBOUNY   Minh. sep113 13 11     8. AssEPUNJEBOUNY   Minh. sep113 13 11     9. AssEPUNJEBOUNY   Minh. sep113 13 1     9. AssEPUNJEBOUNY   Minh. sep113 13 1     9. AssE	t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	4096
2. AssFW/UpStandy   Mem., seb1028    1024    1288    2. AssFW/UpStandy   Mem., seb1028    1288    1288    1288    2. AssFW/UpStandy   Mem., seb1028    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459    1459	t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144
	t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	8192
	t2 AsstFWUprBoundY MtrNm s4p11[2][3]	10240
2.AssFWUpDebunY, MnPn, apt 1928   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14388   14		
2. AssEWUrpEdumY Minhs spin 12[6]   16384		
2.AssFWUpBoundY_Mnhm_sep110  17		
2. AssFWUpDeburyf, Minhs, s4p112  8    22828   22828   2. AssFWUpDeburyf, Minhs, s4p115  19    24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576   24576		
Z. AssEV/Upfood/ Mrkms apt 102 09   2828    Z. AssEV/Upfood/ Mrkms apt 103 01   0   0     Z. AssEV/Upfood/ Mrkms apt 103 01   0   0     Z. AssEV/Upfood/ Mrkms apt 103 01   208    Z. AssEV/Upfood/ Mrkms apt 103 01   0   0     Z. AssEV/Upfood/ Mrkms apt 103 01   0   0     Z. AssEV/Upfood/ Mrkms apt 103 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 103 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 103 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 103 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 103 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 103 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 103 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 103 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 103 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 103 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 103 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 103 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 103 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 104 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 104 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 104 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 104 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 104 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 104 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 104 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 104 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 104 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 104 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 104 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 104 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 104 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 104 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 104 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 104 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 104 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 105 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 105 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 105 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 105 01   0   0   0     Z. AssEV/Upfood/ Mrkms apt 105 01   0   0   0     Z. AssEV/Upfood/ Mrkms		
2_AssFWUpfGood* Minkm_sep11301   0   0   0   0   0   0   0   0   0		20480
2. AssEVPUprisound*, Minkm. sept 1130    2. AssEVPUprisound*, Minkm. sept 1130    2. AssEVPUprisound*, Minkm. sept 1130    3. AssEVPUprisound*, Minkm. sept 1130    3. AssEVPUprisound*, Minkm. sept 1130    4. AssEVPUprisound*, Minkm. sept 1130    5. AssEVPUprisound*, Minkm. sept 1130    5. AssEVPUprisound*, Minkm. sept 1130    6. AssEVPUprisound*, Minkm. sept 1130    7. AssEVPUprisound*, Minkm. sept 1130    7. AssEVPUprisound*, Minkm. sept 1130    8. AssEVPUprisound*, Minkm. sept 1130    8. AssEVPUprisound*, Minkm. sept 1130    9. AssEVPUprisound*, Minkm. sept 1130    9. AssEVPUprisound*, Minkm. sept 1130    9. AssEVPUprisound*, Minkm. sept 1140    9. AssEVPUprisound*, Minkm. sept 1150    9. AssEVPUprisound*, Minkm. sept 11	t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	22528
2. AssEVVprBoundY Minkm ados113(1)   2048   2048   2048   2. AssEVVprBoundY Minkm ados113(2)   4066   2. AssEVVprBoundY Minkm ados113(2)   4096   2. AssEVVprBoundY Minkm ados113(2)   4096   2. AssEVVprBoundY Minkm ados113(2)   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096   4096	t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	24576
2. AssiPVUprBoundY_Minhn.sep113[1]         2048           2. AssiPVUprBoundY_Minhn.sep113[2]         606           2. AssiPVUprBoundY_Minhn.sep113[3]         6144           2. AssiPVUprBoundY_Minhn.sep113[4]         8192           2. AssiPVUprBoundY_Minhn.sep113[6]         1228           2. AssiPVUprBoundY_Minhn.sep113[7]         14336           2. AssiPVUprBoundY_Minhn.sep113[8]         16384           2. AssiPVUprBoundY_Minhn.sep113[8]         16384           2. AssiPVUprBoundY_Minhn.sep113[8]         1642           2. AssiPVUprBoundY_Minhn.sep113[8]         1642           2. AssiPVUprBoundY_Minhn.sep113[8]         1644           2. AssiPVUprBoundY_Minhn.sep113[8]         1644           2. AssiPVUprBoundY_Minhn.sep114[8]         1644           2. AssiPVUprBoundY_Minhn.sep114[8]         1624           2. AssiPVUprBoundY_Minhn.sep114[8]         1624           2. AssiPVUprBoundY_Minhn.sep114[8]         1624           2. AssiPVUprBoundY_Minhn.sep114[8]         1636           2. AssiPVUprBoundY_Minhn.sep114[8]         1636           2. AssiPVUprBoundY_Minhn.sep114[8]         16384           2. AssiPVUprBoundY_Minhn.sep114[8]         2040           2. AssiPVUprBoundY_Minhn.sep114[8]         2040           2. AssiPVUprBoundY_Minhn.sep114[8]         2046     <	t2 AsstFWUprBoundY MtrNm s4p11[3][0]	0
12. AssEPWUprBoundY_Mirkm_s4p11[3][3]         6144           12. AssEPWUprBoundY_Mirkm_s4p11[3][4]         8192           12. AssEPWUprBoundY_Mirkm_s4p11[3][6]         10240           12. AssEPWUprBoundY_Mirkm_s4p11[3][6]         10240           12. AssEPWUprBoundY_Mirkm_s4p11[3][7]         14336           12. AssEPWUprBoundY_Mirkm_s4p11[3][9]         14336           12. AssEPWUprBoundY_Mirkm_s4p11[3][9]         14432           12. AssEPWUprBoundY_Mirkm_s4p11[3][9]         24460           12. AssEPWUprBoundY_Mirkm_s4p11[3][9]         4066           12. AssEPWUprBoundY_Mirkm_s4p11[4][9]         4096           12. AssEPWUprBoundY_Mirkm_s4p11[4][9]         8192           12. AssEPWUprBoundY_Mirkm_s4p11[4][9]         1228           12. AssEPWUprBoundY_Mirkm_s4p11[4][9]         1228           12. AssEPWUprBoundY_Mirkm_s4p11[4][9]         1228           12. AssEPWUprBoundY_Mirkm_s4p11[4][9]         1238           12. AssEPWUprBoundY_Mirkm_s4p11[4][9]         2450           12. AssEPWUprBoundY_Mirkm_s4p11[4][9]         2450           12. AssEPWUprBoundY_Mirkm_s4p11[4][9]         2450           12. AssEPWUprBoundY_Mirkm_s4p11[4][9]         2450           12. AssEPWUprBoundY_Mirkm_s4p11[6][9]         30720           12. AssEPWUprBoundY_Mirkm_s4p11[6][9]         4066		
2.AssFWUprBoundY_MrNm_sdp11[3][4]   8192     2.AssFWUprBoundY_MrNm_sdp11[3][6]   10240     2.AssFWUprBoundY_MrNm_sdp11[3][6]   10240     2.AssFWUprBoundY_MrNm_sdp11[3][6]   10286     2.AssFWUprBoundY_MrNm_sdp11[3][6]   10286     2.AssFWUprBoundY_MrNm_sdp11[3][6]   10384     2.AssFWUprBoundY_MrNm_sdp11[3][6]   10384     2.AssFWUprBoundY_MrNm_sdp11[3][6]   10482     2.AssFWUprBoundY_MrNm_sdp11[3][6]   10482     2.AssFWUprBoundY_MrNm_sdp11[4][7]   10496     2.AssFWUprBoundY_MrNm_sdp11[4][7]   10496     2.AssFWUprBoundY_MrNm_sdp11[4][7]   10496     2.AssFWUprBoundY_MrNm_sdp11[4][7]   10240     2.AssFWUprBoundY_MrNm_sdp11[4][7]   10496     2.AssFWUprBoundY_MrNm_sdp11[4][7]   10492     2.AssFWUprBoundY_MrNm_sdp11[4][7]   10496     2.AssFWUprBoundY_MrNm_sdp11[6][7]   10496     2.AssFWUprBoundY_Mrnm		
12. AssFWUpRountY_MfrNn_sep113 s    2. AssFWUpRountY_MfrNn_sep113 s    2. AssFWUpRountY_MfrNn_sep113 s    2. AssFWUpRountY_MfrNn_sep113 s    3. AssFWUpRountY_MfrNn_sep113 s    3. AssFWUpRountY_MfrNn_sep113 s    4. AssFWUpRountY_MfrNn_sep113 s    5. AssFWUpRountY_MfrNn_sep113 s    6. AssFWUpRountY_MfrNn_sep114 s    6. AssFWUpRountY_MfrNn_sep114 s    7. AssFWUpRountY_MfrNn_sep114 s    8. AssFWUpRountY_MfrNn_sep114 s    9. AssFWUpRountY_MfrNn_sep114 s    9. AssFWUpRountY_MfrNn_sep114 s    9. AssFWUpRountY_MfrNn_sep114 s    9. AssFWUpRountY_Mfrn_sep114 s    9. AssFWUpRountY_Mfrn_sep116 s    10. AssFWUpRountY_Mfrn_sep116 s		
2.AssFWUpRbundY_Minlm_s4p115  5    10240   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   122888   12288   12288   12288   122888   12288   12288   122888   12288   12288   12288   12288		
2. AssFWUpFBoundY_Minns_s4p115  6    14336   12288   2. AssFWUpFBoundY_Minns_s4p115  7    14336   14336   12. AssFWUpFBoundY_Minns_s4p115  8    16384   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   1433	t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
2. AssEPVUlpGoundY_Mirkm_s4p11(3)[8]         14336           12. AssEPVUlpGoundY_Mirkm_s4p11(3)[8]         16384           12. AssEPVUlpGoundY_Mirkm_s4p11(3)[9]         18432           12. AssEPVUlpGoundY_Mirkm_s4p11(3)[9]         20480           12. AssEPVUlpGoundY_Mirkm_s4p11(3)[9]         4066           12. AssEPVUlpGoundY_Mirkm_s4p11(4)[1]         6144           12. AssEPVUlpGoundY_Mirkm_s4p11(4)[8]         10240           12. AssEPVUlpGoundY_Mirkm_s4p11(4)[4]         12288           12. AssEPVUlpGoundY_Mirkm_s4p11(4)[6]         16384           12. AssEPVUlpGoundY_Mirkm_s4p11(4)[8]         16384           12. AssEPVUlpGoundY_Mirkm_s4p11(4)[8]         20480           12. AssEPVUlpGoundY_Mirkm_s4p11(4)[8]         20480           12. AssEPVUlpGoundY_Mirkm_s4p11(4)[8]         20528           12. AssEPVUlpGoundY_Mirkm_s4p11(4)[9]         24576           12. AssEPVUlpGoundY_Mirkm_s4p11(4)[9]         24576           12. AssEPVUlpGoundY_Mirkm_s4p11(5)[1]         26624           2. AssEPVUlpGoundY_Mirkm_s4p11(5)[1]         26624           2. AssEPVUlpGoundY_Mirkm_s4p11(5)[1]         26624           2. AssEPVUlpGoundY_Mirkm_s4p11(6)[1]         26624           2. AssEPVUlpGoundY_Mirkm_s4p11(6)[1]         26624           2. AssEPVUlpGoundY_Mirkm_s4p11(6)[1]         26664	t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
2.AssFP\UprBoundY_MrNm_s4p113  8    16384     2AssFP\UprBoundY_MrNm_s4p113  6    20480     2AssFP\UprBoundY_MrNm_s4p113  6    20480     2AssFP\UprBoundY_MrNm_s4p113  6    4096     2AssFP\UprBoundY_MrNm_s4p114  0    4096     2AssFP\UprBoundY_MrNm_s4p114  10    4196     2AssFP\UprBoundY_MrNm_s4p114  10    4198     2AssFP\UprBoundY_MrNm_s4p114  10    4258     2AssFP\UprBoundY_MrNm_s4p114  10    4258     2AssFP\UprBoundY_MrNm_s4p114  10    4257     2AssFP\UprBoundY_MrNm_s4p114  10    4257     2AssFP\UprBoundY_MrNm_s4p115  10    4267     2AssFP\UprBoundY_MrNm_s4p115  10    4268     2AssFP\UprBoundY_MrNm_s4p116  10    4268     2AssFP\UprBoundY_MrNm_s4	t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
2_AssFWUpRoundY_MrNm_s4p113  10    20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   20480   2	t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
12. AssFWUpRoundY_Mirkm_s4p11(3)[10]       20480         12. AssFWUpRoundY_Mirkm_s4p11(4)[0]       4096         12. AssFWUpRoundY_Mirkm_s4p11(4)[1]       6144         12. AssFWUpRoundY_Mirkm_s4p11(4)[1]       6144         12. AssFWUpRoundY_Mirkm_s4p11(4)[3]       10240         12. AssFWUpRoundY_Mirkm_s4p11(4)[4]       12288         12. AssFWUpRoundY_Mirkm_s4p11(4)[6]       14336         12. AssFWUpRoundY_Mirkm_s4p11(4)[6]       16384         12. AssFWUpRoundY_Mirkm_s4p11(4)[6]       16384         12. AssFWUpRoundY_Mirkm_s4p11(4)[6]       20480         12. AssFWUpRoundY_Mirkm_s4p11(4)[6]       20480         12. AssFWUpRoundY_Mirkm_s4p11(4)[6]       24576         12. AssFWUpRoundY_Mirkm_s4p11(5)[0]       20720         12. AssFWUpRoundY_Mirkm_s4p11(5)[0]       30720         12. AssFWUpRoundY_Mirkm_s4p11(5)[1]       -28624         12. AssFWUpRoundY_Mirkm_s4p11(5)[3]       -24576         12. AssFWUpRoundY_Mirkm_s4p11(5)[6]       -24276         12. AssFWUpRoundY_Mirkm_s4p11(5)[6]       -24376         12. AssFWUpRoundY_Mirkm_s4p11(5)[6]       -18432         12. AssFWUpRoundY_Mirkm_s4p11(5)[6]       -18432         12. AssFWUpRoundY_Mirkm_s4p11(5)[6]       -18432         12. AssFWUpRoundY_Mirkm_s4p11(6)[6]       -10240         12. Ass	t2 AsstFWUprBoundY MtrNm s4p11[3][8]	16384
2. AssFWUprBoundY MtrNm_s4p11[3][10]   20480   2. AssFWUprBoundY MtrNm_s4p11[4][1]   61144   2. AssFWUprBoundY MtrNm_s4p11[4][2]   8192   2. AssFWUprBoundY MtrNm_s4p11[4][3]   10240   2. AssFWUprBoundY MtrNm_s4p11[4][3]   10240   2. AssFWUprBoundY MtrNm_s4p11[4][5]   12288   1228   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   12288   122888   12288   12288   12288   12288   12288		
12, AssFWUprBoundY, MtrNm, s4p11(4) 0    4096    12, AssFWUprBoundY, MtrNm, s4p11(4) 1    6144    12, AssFWUprBoundY, MtrNm, s4p11(4) 2    8192    12, AssFWUprBoundY, MtrNm, s4p11(4) 3    10240    12, AssFWUprBoundY, MtrNm, s4p11(4) 4    12288    12, AssFWUprBoundY, MtrNm, s4p11(4) 6    14386    12, AssFWUprBoundY, MtrNm, s4p11(4) 6    14384    12, AssFWUprBoundY, MtrNm, s4p11(4) 6    14384    13, AssFWUprBoundY, MtrNm, s4p11(4) 6    14384    14, AssFWUprBoundY, MtrNm, s4p11(4) 6    14384    15, AssFWUprBoundY, MtrNm, s4p11(4) 6    24576    16, AssFWUprBoundY, MtrNm, s4p11(5) 6    30720    17, AssFWUprBoundY, MtrNm, s4p11(5) 1    28672    18, AssFWUprBoundY, MtrNm, s4p11(5) 2    26624    19, AssFWUprBoundY, MtrNm, s4p11(5) 2    26624    10, AssFWUprBoundY, MtrNm, s4p11(5) 3    24576    10, AssFWUprBoundY, MtrNm, s4p11(5) 6    22528    10, AssFWUprBoundY, MtrNm, s4p11(5) 6    22528    10, AssFWUprBoundY, MtrNm, s4p11(5) 6    14832    10, AssFWUprBoundY, MtrNm, s4p11(5) 6    14832    10, AssFWUprBoundY, MtrNm, s4p11(5) 6    14228    11, AssFWUprBoundY, MtrNm, s4p11(5) 6    14228    11, AssFWUprBoundY, MtrNm, s4p11(6) 6    14228    12, AssFWUprBoundY, MtrNm, s4p11(6) 6    14228    13, AssFWUprBoundY, MtrNm, s4p11(6) 6    14228    14, AssFWUprBoundY, MtrNm, s4p11(6) 6    14228    15, AssFWUprBoundY, MtrNm, s4p11(6) 6    14228    16, AssFWUprBoundY, MtrNm, s4p11(6) 6    14228    17, AssFWUprBoundY, MtrNm, s4p11(6) 6    14228    18, AssFWUprBoundY, MtrNm, s4p11(6) 6    14228    19, AssFWUprBoundY, MtrNm, s4p11(6) 6    14228    10, AssFWUprBoundY, MtrNm, s4p11(6) 6    14228		
2. AssFWUprBoundY_MrNm_s4p11[4][1]   6144     2. AssFWUprBoundY_MrNm_s4p11[4][2]   8192     2. AssFWUprBoundY_MrNm_s4p11[4][3]   10240     2. AssFWUprBoundY_MrNm_s4p11[4][4]   12288     2. AssFWUprBoundY_MrNm_s4p11[4][5]   14336     2. AssFWUprBoundY_MrNm_s4p11[4][6]   16384     2. AssFWUprBoundY_MrNm_s4p11[4][7]   18432     2. AssFWUprBoundY_MrNm_s4p11[4][9]   22528     2. AssFWUprBoundY_MrNm_s4p11[4][9]   22528     2. AssFWUprBoundY_MrNm_s4p11[4][9]   24576     2. AssFWUprBoundY_MrNm_s4p11[6][9]   24576     2. AssFWUprBoundY_MrNm_s4p11[5][1]   28672     2. AssFWUprBoundY_MrNm_s4p11[5][1]   28672     2. AssFWUprBoundY_MrNm_s4p11[5][1]   26624     2. AssFWUprBoundY_MrNm_s4p11[5][1]   26624     2. AssFWUprBoundY_MrNm_s4p11[5][6]   24576     2. AssFWUprBoundY_MrNm_s4p11[6][6]   24576     2. AssFWUprBoundY_MrNm_s4p11[6][6]   26624     2. AssFWUprBoundY_MrNm_s4		
2_AssiFWUpfBoundY_MirNin_s4p11[4][2]   8192     2_AssiFWUpfBoundY_MirNin_s4p11[4][3]   10240     2_AssiFWUpfBoundY_MirNin_s4p11[4][4]   12288     2_AssiFWUpfBoundY_MirNin_s4p11[4][6]   14336     2_AssiFWUpfBoundY_MirNin_s4p11[4][6]   16384     2_AssiFWUpfBoundY_MirNin_s4p11[4][8]   20480     2_AssiFWUpfBoundY_MirNin_s4p11[4][8]   20480     2_AssiFWUpfBoundY_MirNin_s4p11[4][9]   22528     2_AssiFWUpfBoundY_MirNin_s4p11[4][9]   22528     2_AssiFWUpfBoundY_MirNin_s4p11[6][0]   30720     2_AssiFWUpfBoundY_MirNin_s4p11[5][0]   30720     2_AssiFWUpfBoundY_MirNin_s4p11[5][1]   2-26624     2_AssiFWUpfBoundY_MirNin_s4p11[5][3]   2-2664     2_AssiFWUpfBoundY_MirNin_s4p11[5][3]   2-2664     2_AssiFWUpfBoundY_MirNin_s4p11[5][4]   2-2628     2_AssiFWUpfBoundY_MirNin_s4p11[5][6]   18432     2_AssiFWUpfBoundY_MirNin_s4p11[5][6]   18432     2_AssiFWUpfBoundY_MirNin_s4p11[5][6]   18432     2_AssiFWUpfBoundY_MirNin_s4p11[6][6]   18432     2_AssiFWUpfBoundY_MirNin_s4p11[6][6]   12288     2_AssiFWUpfBoundY_MirNin_s4p11[6][6]   12288     2_AssiFWUpfBoundY_MirNin_s4p11[6][6]   10240     2_AssiFWUpfBoundY_MirNin_s4p11[6][1]   10240     2_AssiFWUpfBoundY_MirNin_s4p11[		
22. AssEFWUpFBoundY_MfrNm_s4p11[4][4]   12288   12288   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   1228	t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
12.2   AssiFWUpfBoundY   MirNm   s4p11[4][4]   12288   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   12.3   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336   14336	t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
22   AsstFWUprBoundY_MtrNm_s4p11[4] 5    14336   12. AsstFWUprBoundY_MtrNm_s4p11[4] 6    16384   20480   22. AsstFWUprBoundY_MtrNm_s4p11[4] 7    18432   20480   22. AsstFWUprBoundY_MtrNm_s4p11[4] 9    22528   22. AsstFWUprBoundY_MtrNm_s4p11[4] 9    22528   22. AsstFWUprBoundY_MtrNm_s4p11[4] 9    22528   22. AsstFWUprBoundY_MtrNm_s4p11[5] 0    30720   22. AsstFWUprBoundY_MtrNm_s4p11[5] 1    228672   22. AsstFWUprBoundY_MtrNm_s4p11[5] 1    228672   22. AsstFWUprBoundY_MtrNm_s4p11[5] 2    226624   22. AsstFWUprBoundY_MtrNm_s4p11[5] 3    224576   22. AsstFWUprBoundY_MtrNm_s4p11[5] 3    22528   22. AsstFWUprBoundY_MtrNm_s4p11[5] 5    220480   22. AsstFWUprBoundY_MtrNm_s4p11[5] 5    220480   22. AsstFWUprBoundY_MtrNm_s4p11[5] 5    220480   22. AsstFWUprBoundY_MtrNm_s4p11[5] 6    18432   22. AsstFWUprBoundY_MtrNm_s4p11[5] 7    16384   22. AsstFWUprBoundY_MtrNm_s4p11[5] 9    12288   22. AsstFWUprBoundY_MtrNm_s4p11[5] 9    12288   22. AsstFWUprBoundY_MtrNm_s4p11[6] 9    12288   22. AsstFWUprBoundY_MtrNm_s4p11[6] 9    12288   22. AsstFWUprBoundY_MtrNm_s4p11[6] 1    10240   22.	t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
2. AsstFWUprBoundY_MtrNm_s4p11[4][5]   14336   12. AsstFWUprBoundY_MtrNm_s4p11[4][6]   16384   12. AsstFWUprBoundY_MtrNm_s4p11[4][7]   18432   12. AsstFWUprBoundY_MtrNm_s4p11[4][8]   20480   12. AsstFWUprBoundY_MtrNm_s4p11[4][9]   22528   12. AsstFWUprBoundY_MtrNm_s4p11[4][9]   22528   12. AsstFWUprBoundY_MtrNm_s4p11[6][0]   30720   12. AsstFWUprBoundY_MtrNm_s4p11[5][1]   28672   22. AsstFWUprBoundY_MtrNm_s4p11[5][1]   28672   22. AsstFWUprBoundY_MtrNm_s4p11[5][1]   28672   22. AsstFWUprBoundY_MtrNm_s4p11[5][2]   226624   22. AsstFWUprBoundY_MtrNm_s4p11[5][3]   24576   22. AsstFWUprBoundY_MtrNm_s4p11[5][4]   22528   22. AsstFWUprBoundY_MtrNm_s4p11[5][6]   20480   22. AsstFWUprBoundY_MtrNm_s4p11[5][6]   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   24836   2483	t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4] 6    16384   16384   12_AsstFWUprBoundY_MtrNm_s4p11[4] 7    18432   12_AsstFWUprBoundY_MtrNm_s4p11[4] 8    2480   22528   12_AsstFWUprBoundY_MtrNm_s4p11[4] 9    22528   12_AsstFWUprBoundY_MtrNm_s4p11[4] 9    24576   24576   22_AsstFWUprBoundY_MtrNm_s4p11[5] 0    30720   12_AsstFWUprBoundY_MtrNm_s4p11[5] 1    28672   2_AsstFWUprBoundY_MtrNm_s4p11[5] 1    28672   2_AsstFWUprBoundY_MtrNm_s4p11[5] 2    26624   2_AsstFWUprBoundY_MtrNm_s4p11[5] 3    24576   2_AsstFWUprBoundY_MtrNm_s4p11[5] 3    22528   2_AsstFWUprBoundY_MtrNm_s4p11[5] 4    22528   2_AsstFWUprBoundY_MtrNm_s4p11[5] 6    24832   2_AsstFWUprBoundY_MtrNm_s4p11[5] 6    4832   2_AsstFWUprBoundY_MtrNm_s4p11[5] 6    4832   2_AsstFWUprBoundY_MtrNm_s4p11[5] 8    4336   2_AsstFWUprBoundY_MtrNm_s4p11[5] 8    4336   2_AsstFWUprBoundY_MtrNm_s4p11[5] 9    42288   2_AsstFWUprBoundY_MtrNm_s4p11[6] 0    40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   40240   4		14336
12   AssIFWUprBoundY   MtrNm s4p11[4] 7    20480   24576   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   24581   2		
12_AssIFWUprBoundY_MtrNm_s4p11[4][8]   20480     12_AssIFWUprBoundY_MtrNm_s4p11[4][9]   22528     12_AssIFWUprBoundY_MtrNm_s4p11[4][9]   24576     12_AssIFWUprBoundY_MtrNm_s4p11[5][0]   30720     12_AssIFWUprBoundY_MtrNm_s4p11[5][1]   226672     12_AssIFWUprBoundY_MtrNm_s4p11[5][1]   226672     12_AssIFWUprBoundY_MtrNm_s4p11[5][3]   226664     12_AssIFWUprBoundY_MtrNm_s4p11[5][3]   22528     12_AssIFWUprBoundY_MtrNm_s4p11[5][6]   22528     12_AssIFWUprBoundY_MtrNm_s4p11[5][6]   20480     12_AssIFWUprBoundY_MtrNm_s4p11[5][6]   18432     12_AssIFWUprBoundY_MtrNm_s4p11[5][7]   16384     12_AssIFWUprBoundY_MtrNm_s4p11[5][8]   14336     12_AssIFWUprBoundY_MtrNm_s4p11[5][8]   12288     12_AssIFWUprBoundY_MtrNm_s4p11[6][0]   10240     12_AssIFWUprBoundY_MtrNm_s4p11[6		
22   AssIFWUprBoundY_MrNm_s4p11[4] 9    22528     2. AssIFWUprBoundY_MrNm_s4p11[6] 0    -30720     2. AssIFWUprBoundY_MrNm_s4p11[5] 1    -28672     2. AssIFWUprBoundY_MrNm_s4p11[5] 1    -28672     2. AssIFWUprBoundY_MrNm_s4p11[5] 2    -26624     2. AssIFWUprBoundY_MrNm_s4p11[5] 3    -24576     2. AssIFWUprBoundY_MrNm_s4p11[5] 4    -22528     2. AssIFWUprBoundY_MrNm_s4p11[5] 5    -20480     2. AssIFWUprBoundY_MrNm_s4p11[5] 5    -20480     2. AssIFWUprBoundY_MrNm_s4p11[5] 7    -16384     2. AssIFWUprBoundY_MrNm_s4p11[5] 7    -16384     2. AssIFWUprBoundY_MrNm_s4p11[5] 9    -12288     2. AssIFWUprBoundY_MrNm_s4p11[5] 9    -12288     2. AssIFWUprBoundY_MrNm_s4p11[6] 0    -10240     2. AssIFWUprBoundY_MrNm_s4p11[6] 0    -10240     2. AssIFWUprBoundY_MrNm_s4p11[6] 1    -10240     2. AssIFWUprBoundY_MrNm_s4p11[6] 1    -10240     2. AssIFWUprBoundY_MrNm_s4p11[6] 1    -10240     2. AssIFWUprBoundY_MrNm_s4p11[6] 2    -8192     2. AssIFWUprBoundY_MrNm_s4p11[6] 3    -6144     2. AssIFWUprBoundY_MrNm_s4p11[6] 4    -4096     2. AssIFWUprBoundY_MrNm_s4p11[6] 5    -2048     2. AssIFW		
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t2_AssIFWUprBoundY_MtrNm_s4p11[5][0]       -30720         t2_AssIFWUprBoundY_MtrNm_s4p11[5][1]       -28672         t2_AssIFWUprBoundY_MtrNm_s4p11[5][3]       -24576         t2_AssIFWUprBoundY_MtrNm_s4p11[5][4]       -22528         t2_AssIFWUprBoundY_MtrNm_s4p11[5][5]       -20480         t2_AssIFWUprBoundY_MtrNm_s4p11[5][7]       -16384         t2_AssIFWUprBoundY_MtrNm_s4p11[5][8]       -14336         t2_AssIFWUprBoundY_MtrNm_s4p11[5][8]       -14336         t2_AssIFWUprBoundY_MtrNm_s4p11[5][9]       -12288         t2_AssIFWUprBoundY_MtrNm_s4p11[6][0]       -10240         t2_AssIFWUprBoundY_MtrNm_s4p11[6][1]       -10240         t2_AssIFWUprBoundY_MtrNm_s4p11[6][2]       -8192         t2_AssIFWUprBoundY_MtrNm_s4p11[6][3]       -6144         t2_AssIFWUprBoundY_MtrNm_s4p11[6][3]       -6144         t2_AssIFWUprBoundY_MtrNm_s4p11[6][6]       -2048         t2_AssIFWUprBoundY_MtrNm_s4p11[6][6]       0         t2_AssIFWUprBoundY_MtrNm_s4p11[6][6]       0         t2_AssIFWUprBoundY_MtrNm_s4p11[6][6]       0         t2_AssIFWUprBoundY_MtrNm_s4p11[6][6]       0         t2_AssIFWUprBoundY_MtrNm_s4p11[6][6]       0         t2_AssIFWUprBoundY_MtrNm_s4p11[6][6]       6144         t2_AssIFWUprBoundY_MtrNm_s4p11[6][0]       8192         t2	t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
12_AsstFWUprBoundY_MtrNm_s4p11[5][1]       -28672         12_AsstFWUprBoundY_MtrNm_s4p11[5][2]       -26624         12_AsstFWUprBoundY_MtrNm_s4p11[5][3]       -24576         12_AsstFWUprBoundY_MtrNm_s4p11[5][4]       -22528         12_AsstFWUprBoundY_MtrNm_s4p11[5][5]       -20480         12_AsstFWUprBoundY_MtrNm_s4p11[5][6]       -18432         12_AsstFWUprBoundY_MtrNm_s4p11[5][8]       -14336         12_AsstFWUprBoundY_MtrNm_s4p11[5][9]       -12288         12_AsstFWUprBoundY_MtrNm_s4p11[5][10]       -10240         12_AsstFWUprBoundY_MtrNm_s4p11[6][1]       -10240         12_AsstFWUprBoundY_MtrNm_s4p11[6][1]       -10240         12_AsstFWUprBoundY_MtrNm_s4p11[6][2]       -8192         12_AsstFWUprBoundY_MtrNm_s4p11[6][3]       -6144         12_AsstFWUprBoundY_MtrNm_s4p11[6][4]       -4096         12_AsstFWUprBoundY_MtrNm_s4p11[6][5]       -2048         12_AsstFWUprBoundY_MtrNm_s4p11[6][6]       0         12_AsstFWUprBoundY_MtrNm_s4p11[6][6]       0         12_AsstFWUprBoundY_MtrNm_s4p11[6][8]       4096         12_AsstFWUprBoundY_MtrNm_s4p11[6][6]       6144         12_AsstFWUprBoundY_MtrNm_s4p11[6][6]       0         12_AsstFWUprBoundY_MtrNm_s4p11[6][6]       6144         12_AsstFWUprBoundY_MtrNm_s4p11[6][6]       6144	t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]       -26624         t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]       -24576         t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]       -22528         t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]       -20480         t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]       -18432         t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]       -16384         t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]       -14336         t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]       -12288         t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]       -10240         t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]       -10240         t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]       -10240         t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]       -8192         t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]       -6144         t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]       -4096         t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]       0         t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]       0         t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]       0         t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]       4096         t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]       4096         t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]       6144         t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]       6144         t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]       6144         <	t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]       -26624         t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]       -24576         t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]       -22528         t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]       -20480         t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]       -18432         t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]       -16384         t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]       -14336         t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]       -12288         t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]       -10240         t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]       -10240         t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]       -10240         t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]       -8192         t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]       -6144         t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]       -4096         t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]       0         t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]       0         t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]       0         t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]       4096         t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]       4096         t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]       6144         t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]       6144         t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]       6144         <	t2 AsstFWUprBoundY MtrNm s4p11[5][1]	-28672
12_AsstFWUprBoundY_MtrNm_s4p11[5][3]       -24576         12_AsstFWUprBoundY_MtrNm_s4p11[5][4]       -22528         12_AsstFWUprBoundY_MtrNm_s4p11[5][5]       -20480         12_AsstFWUprBoundY_MtrNm_s4p11[5][6]       -18432         12_AsstFWUprBoundY_MtrNm_s4p11[5][7]       -16384         12_AsstFWUprBoundY_MtrNm_s4p11[5][8]       -14336         12_AsstFWUprBoundY_MtrNm_s4p11[5][9]       -12288         12_AsstFWUprBoundY_MtrNm_s4p11[6][0]       -10240         12_AsstFWUprBoundY_MtrNm_s4p11[6][0]       -12288         12_AsstFWUprBoundY_MtrNm_s4p11[6][1]       -10240         12_AsstFWUprBoundY_MtrNm_s4p11[6][2]       -8192         12_AsstFWUprBoundY_MtrNm_s4p11[6][2]       -8192         12_AsstFWUprBoundY_MtrNm_s4p11[6][4]       -4096         12_AsstFWUprBoundY_MtrNm_s4p11[6][5]       -2048         12_AsstFWUprBoundY_MtrNm_s4p11[6][6]       0         12_AsstFWUprBoundY_MtrNm_s4p11[6][7]       2048         12_AsstFWUprBoundY_MtrNm_s4p11[6][9]       6144         12_AsstFWUprBoundY_MtrNm_s4p11[6][9]       6144         12_AsstFWUprBoundY_MtrNm_s4p11[6][9]       6144         12_AsstFWUprBoundY_MtrNm_s4p11[6][9]       6144         12_AsstFWUprBoundY_MtrNm_s4p11[6][9]       6144         12_AsstFWUprBoundY_MtrNm_s4p11[6][9]       6144		
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t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] -4096 t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] 0		
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 0		
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 0	t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 0 t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 0	t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 2048 t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 0		
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 4096 t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 0		
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 6144 t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 0		
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 8192 t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 0		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] -2048 t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 0		
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 0		
	t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
	t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] 2048	t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3] 4096		





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	614
t_AsstFWDefltAssistX_HwNm_u8p8[1]	640
t_AsstFWDefltAssistX_HwNm_u8p8[2]	666
t_AsstFWDefltAssistX_HwNm_u8p8[3]	691 717
t_AsstFWDefltAssistX_HwNm_u8p8[4]	742
t_AsstFWDefltAssistX_HwNm_u8p8[5]	768
t_AsstFWDefltAssistX_HwNm_u8p8[6]	794
t_AsstFWDefltAssistX_HwNm_u8p8[7] t_AsstFWDefltAssistX_HwNm_u8p8[8]	819
t_AsstFWDefitAssistX_HwNm_u8p8[9]	845
t_AsstFWDefltAssistX_HwNm_u8p8[10]	870
t_AsstFWDefitAssistX_HwNm_u8p8[11]	896
t_AsstFWDefitAssistX_HwNm_u8p8[12]	922
t_AsstFWDefitAssistX_HwNm_u8p8[13]	947
t_AsstFWDefitAssistX_HwNm_u8p8[14]	973
t_AsstFWDefitAssistX_HwNm_u8p8[15]	998
t_AsstFWDefitAssistX_HwNm_u8p8[15]  t_AsstFWDefitAssistX_HwNm_u8p8[16]	1024
t_AsstFWDefitAssistX_mwNrii_uopo[16]  t AsstFWDefitAssistX HwNm_u8p8[17]	1050
t_AsstFWDefitAssistX_HwNm_u8p8[17]  t_AsstFWDefitAssistX_HwNm_u8p8[18]	1075
t AsstFWDefitAssistX HwNm u8p8[19]	1101
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	15770
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	16589
t AsstFWDefltAssistY MtrNm s4p11[11]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16998
t AsstFWDefltAssistY MtrNm s4p11[13]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	17613
t_AsstFWDefitAssistY_MtrNm_s4p11[16]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	18432
t AsstFWPstepNstepThresh Cnt u16[0]	183
t_AsstFWPstepNstepThresh_Cnt_u16[1]	451
t_AsstFWVehSpd_Kph_u9p7[0]	10240
t_AsstFWVehSpd_Kph_u9p7[1]	10368
t_AsstFWVehSpd_Kph_u9p7[2]	10496
t_AsstFWVehSpd_Kph_u9p7[3]	10624
t_AsstFWVehSpd_Kph_u9p7[4]	10752
t_AsstFWVehSpd_Kph_u9p7[5]	10880
t_AsstFWVehSpd_Kph_u9p7[6]	11008
t_AsstFWVehSpd_Kph_u9p7[7]	11136
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	80.1999969
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 HwTorque HwNm f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall Per1_HysteresisComp_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.550000012	0.550000012 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	451	451 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	48.9570007	48.9570007 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.2734375	2.2734375 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.00349998	7.00349998 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.550000012	0.550000012 ± 3.05E-05	•
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	•
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	•
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	-

Test Step 2.63 (Repeat Count = 1)	· ·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall ActiveKSV M str.K Uls f32	0.090000036
AssistFirewall_ActiveRawAcc_Cnt_M_u16	6519
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall CombAsstSV MtrNm M f32	5.099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	0
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.100000001
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.70000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4
AssistFirewall LwrBoundKSV M str.K Uls f32	0.300000012
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00899999961
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.20000005
k AsstFWInpLimitHFA MtrNm f32	4.400001
k_AsstFWInpLimitHysComp_MtrNm_f32	6.0999999
k_AsstFWNstep_Cnt_u16	3813
k_AsstFWPstep_Cnt_u16	4059
k RestoreThresh MtrNm f32	8.30000019
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144

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ASSISTITEWAII_Pet I	( OLC)	0-10
Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144	
	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]		
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096	
P_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048	
P_AsstFWUprBoundX_HwNm_s4p11[7][5]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192	
P_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0	
:_AsstFWUprBoundY_MtrNm_s4p11[0][0] ?_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	14336	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-2048
	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	16384
	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-24576
	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-8192
	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096 6144





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	640
t_AsstFWDefltAssistX_HwNm_u8p8[1]	666
t_AsstFWDefltAssistX_HwNm_u8p8[2]	691 717
t_AsstFWDefltAssistX_HwNm_u8p8[3] t_AsstFWDefltAssistX_HwNm_u8p8[4]	742
t_AsstFWDefltAssistX_HwNm_u8p8[5]	768
t_AsstFWDefltAssistX_HwNm_u8p8[6]	794
t_AsstFWDefltAssistX_HwNm_u8p8[7]	819
t_AsstFWDefltAssistX_HwNm_u8p8[8]	845
t_AsstFWDefitAssistX_HwNm_u8p8[9]	870
t_AsstFWDefltAssistX_HwNm_u8p8[10]	896
t_AsstFWDefltAssistX_HwNm_u8p8[11]	922
t_AsstFWDefltAssistX_HwNm_u8p8[12]	947
t_AsstFWDefitAssistX_HwNm_u8p8[13]	973
t_AsstFWDefltAssistX_HwNm_u8p8[14]	998
t_AsstFWDefitAssistX_HwNm_u8p8[15]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1050
t AsstFWDefitAssistX HwNm u8p8[17]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1101
t AsstFWDefltAssistX HwNm u8p8[19]	1126
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	16794
t AsstFWDefltAssistY MtrNm s4p11[11]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	18637
t_AsstFWPstepNstepThresh_Cnt_u16[0]	184
t_AsstFWPstepNstepThresh_Cnt_u16[1]	455
t_AsstFWVehSpd_Kph_u9p7[0]	13184
t_AsstFWVehSpd_Kph_u9p7[1]	13312
t_AsstFWVehSpd_Kph_u9p7[2]	13440
t_AsstFWVehSpd_Kph_u9p7[3]	13568
t_AsstFWVehSpd_Kph_u9p7[4]	13696
t_AsstFWVehSpd_Kph_u9p7[5]	13824
t_AsstFWVehSpd_Kph_u9p7[6]	13952
t_AsstFWVehSpd_Kph_u9p7[7]	14080
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.099999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-6
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	*
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_/tosion newan_r or r_rrystorosiocomp_ivintrin_ioz
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.00200009	2.00200009 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	455	455 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019	-8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.03000009	1.02999997 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-0.200000286	-0.200000003 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.9369998	7.9369998 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-8.80000019	-8.80000019 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.64 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.099999
AssistFirewall ActiveKSV M str.K Uls f32	0.100000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	6642
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	5.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00499999989
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0099999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.29999995
k_AsstFWInpLimitHFA_MtrNm_f32	4.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	6.30000019
k_AsstFWNstep_Cnt_u16	3936
k_AsstFWPstep_Cnt_u16	4182
k_RestoreThresh_MtrNm_f32	8.39999962
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2 AsstFWUprBoundX HwNm s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2 AsstFWUprBoundX HwNm s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
, , , , , , , , , , , , , , , , , , , ,	
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
	14336
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t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
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t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	8192
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t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192 10240 12288





Name	
12	
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12_AsstFWUprBoundY_MtrNm_s4p11[] 10    8192     12_AsstFWUprBoundY_MtrNm_s4p11[2  0    10240     12_AsstFWUprBoundY_MtrNm_s4p11[2  1    10240     12_AsstFWUprBoundY_MtrNm_s4p11[2  2    12288     12_AsstFWUprBoundY_MtrNm_s4p11[2  3    14336     12_AsstFWUprBoundY_MtrNm_s4p11[2  3    16384     12_AsstFWUprBoundY_MtrNm_s4p11[2  3    16384     12_AsstFWUprBoundY_MtrNm_s4p11[2  3    16384     12_AsstFWUprBoundY_MtrNm_s4p11[2  3    20480     12_AsstFWUprBoundY_MtrNm_s4p11[2  3    20480     12_AsstFWUprBoundY_MtrNm_s4p11[2  3    24576     12_AsstFWUprBoundY_MtrNm_s4p11[2  3    24576     12_AsstFWUprBoundY_MtrNm_s4p11[2  3    24576     12_AsstFWUprBoundY_MtrNm_s4p11[2  3    28672     12_AsstFWUprBoundY_MtrNm_s4p11[3  3    28672     12_AsstFWUprBoundY_MtrNm_s4p11[3  3    3192     12_AsstFWUprBoundY_MtrNm_s4p11[3  3    3193     12_AsstFWUprBoundY_MtrNm_s4p11[3  4    3193     12_AsstFWUprBoundY_MtrNm_s4p11[3  4    3193     12_AsstFWUprBoundY_MtrNm_s4p11[4  4    3193     12_AsstFWUprBo	
12_AsstFWUprBoundY_MtrNm_s4p11[2][0]       8192         12_AsstFWUprBoundY_MtrNm_s4p11[2][1]       10240         12_AsstFWUprBoundY_MtrNm_s4p11[2][2]       12288         12_AsstFWUprBoundY_MtrNm_s4p11[2][3]       14336         12_AsstFWUprBoundY_MtrNm_s4p11[2][4]       16384         12_AsstFWUprBoundY_MtrNm_s4p11[2][5]       18432         12_AsstFWUprBoundY_MtrNm_s4p11[2][6]       20480         12_AsstFWUprBoundY_MtrNm_s4p11[2][7]       22528         12_AsstFWUprBoundY_MtrNm_s4p11[2][8]       24576         12_AsstFWUprBoundY_MtrNm_s4p11[2][9]       26624         12_AsstFWUprBoundY_MtrNm_s4p11[2][10]       28672         12_AsstFWUprBoundY_MtrNm_s4p11[3][0]       4096         12_AsstFWUprBoundY_MtrNm_s4p11[3][1]       6144         12_AsstFWUprBoundY_MtrNm_s4p11[3][2]       8192         12_AsstFWUprBoundY_MtrNm_s4p11[3][4]       12288         12_AsstFWUprBoundY_MtrNm_s4p11[3][5]       14336         12_AsstFWUprBoundY_MtrNm_s4p11[3][6]       16384         12_AsstFWUprBoundY_MtrNm_s4p11[3][7]       18432         12_AsstFWUprBoundY_MtrNm_s4p11[3][9]       22528         12_AsstFWUprBoundY_MtrNm_s4p11[4][0]       8192         12_AsstFWUprBoundY_MtrNm_s4p11[4][0]       8192         12_AsstFWUprBoundY_MtrNm_s4p11[4][1]       10240	
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t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] -6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] -4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] -2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] 0	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] 2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] 4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] 6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] 8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] 2048	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] 4096	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] 6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3] 8192	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	22528
t_AsstFWDefltAssistX_HwNm_u8p8[0]	666
t_AsstFWDefltAssistX_HwNm_u8p8[1]	691 717
t_AsstFWDefltAssistX_HwNm_u8p8[2]	742
t_AsstFWDefltAssistX_HwNm_u8p8[3]	768
t_AsstFWDefltAssistX_HwNm_u8p8[4]	794
t_AsstFWDefltAssistX_HwNm_u8p8[5] t_AsstFWDefltAssistX_HwNm_u8p8[6]	819
t_AsstFWDefltAssistX_HwNm_u8p8[7]	845
t_AsstFWDefltAssistX_HwNm_u8p8[8]	870
t_AsstFWDefitAssistX_HwNm_u8p8[9]	896
t_AsstFWDefltAssistX_HwNm_u8p8[10]	922
t_AsstFWDefitAssistX_HwNm_u8p8[11]	947
t_AsstFWDefltAssistX_HwNm_u8p8[12]	973
t_AsstFWDefitAssistX_HwNm_u8p8[13]	998
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1024
t_AsstFWDefitAssistX_HwNm_u8p8[15]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1075
t AsstFWDefitAssistX HwNm u8p8[17]	1101
t_AsstFWDefitAssistX_HwNm_u8p8[18]	1126
t AsstFWDefitAssistX HwNm u8p8[19]	1152
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	16998
t AsstFWDefltAssistY MtrNm s4p11[11]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	17408
t AsstFWDefltAssistY MtrNm s4p11[13]	17613
t AsstFWDefltAssistY MtrNm s4p11[14]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	18842
t_AsstFWPstepNstepThresh_Cnt_u16[0]	185
t_AsstFWPstepNstepThresh_Cnt_u16[1]	459
t_AsstFWVehSpd_Kph_u9p7[0]	16128
t_AsstFWVehSpd_Kph_u9p7[1]	16256
t_AsstFWVehSpd_Kph_u9p7[2]	16384
t_AsstFWVehSpd_Kph_u9p7[3]	16512
t_AsstFWVehSpd_Kph_u9p7[4]	16640
t_AsstFWVehSpd_Kph_u9p7[5]	16768
t_AsstFWVehSpd_Kph_u9p7[6]	16896
t_AsstFWVehSpd_Kph_u9p7[7]	17024
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-7
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	11.1999998
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

AssistFirewall\_Per1

Status\_Cnt\_T\_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.78999996	2.78999996 ± 4.88E-04	-
AssistFirewall_ActiveRawAcc_Cnt_M_u16	459	459 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	-
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019	-8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.52099991	5.52099991 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-1.4000001	-1.39999998 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>~</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.09899998	1.09899998 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-8.80000019	-8.80000019 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	-
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>

Τ				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	_

0x01

0x01

Test Step 2.65 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.79999995
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.200000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	6765
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0399999991
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.8999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.019999996
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
c_AsstFWInpLimitBaseAsst_MtrNm_f32	3.4000001
c_AsstFWInpLimitHFA_MtrNm_f32	4.80000019
c_AsstFWInpLimitHysComp_MtrNm_f32	6.5
c_AsstFWNstep_Cnt_u16	4059
:_AsstFWPstep_Cnt_u16	4305
RestoreThresh MtrNm f32	8.5
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2 AsstFWUprBoundX HwNm s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	18432
t2 AsstFWUprBoundX HwNm s4p11[6][0]	-8192
	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	16384
	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
:2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288
	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-6144
2 AsstFWUprBoundY MtrNm s4p11[4][6]	-4096
:2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	10240





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576
t_AsstFWDefltAssistX_HwNm_u8p8[0]	691
t_AsstFWDefltAssistX_HwNm_u8p8[1]	717 742
t_AsstFWDefltAssistX_HwNm_u8p8[2]	
t_AsstFWDefltAssistX_HwNm_u8p8[3]	768 794
t_AsstFWDefltAssistX_HwNm_u8p8[4] t_AsstFWDefltAssistX_HwNm_u8p8[5]	819
t_AsstFWDefitAssistX_HwNm_u8p8[6]	845
t_AsstFWDefitAssistX_HwNm_u8p8[7]	870
t_AsstFWDefitAssistX_HwNm_u8p8[8]	896
t_AsstFWDefitAssistX_HwNm_u8p8[9]	922
t_AsstFWDefitAssistX_HwNm_u8p8[10]	947
t_AsstFWDefitAssistX_HwNm_u8p8[11]	973
t_AsstFWDefitAssistX_HwNm_u8p8[12]	998
t_AsstFWDefitAssistX_HwNm_u8p8[13]	1024
t_AsstFWDefitAssistX_HwNm_u8p8[14]	1050
t_AsstFWDefitAssistX_HwNm_u8p8[15]	1075
t_AsstFWDefitAssistX_HwNm_u8p8[16]	1101
t_AsstFWDefitAssistX_mwnin_uopo[10]  t_AsstFWDefitAssistX_HwNm_u8p8[17]	1126
t_AsstFWDefitAssistX_HwNm_u8p8[18]	1152
t_AsstFWDefitAssistX_HwNm_u8p8[19]	1178
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	15155
t_AsstFWDefitAssistY_MtrNm_s4p11[1]	15360
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	15565
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	15770
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	15974
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	16179
t_AsstFWDefitAssistY_MtrNm_s4p11[6]	16384
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	16589
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	16998
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	17203
t AsstFWDefltAssistY MtrNm s4p11[11]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	17613
t AsstFWDefltAssistY MtrNm s4p11[13]	17818
t AsstFWDefltAssistY MtrNm s4p11[14]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	19046
t AsstFWPstepNstepThresh Cnt u16[0]	186
t_AsstFWPstepNstepThresh_Cnt_u16[1]	463
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t AsstFWVehSpd Kph u9p7[5]	19712
t_AsstFWVehSpd_Kph_u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	22.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
· ·	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_li	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Iq	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Itgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Itgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32

AssistFirewall\_Per1

Status\_Cnt\_T\_enum

NTC\_Cnt\_T\_enum

Param\_Cnt\_T\_u08

Status\_Cnt\_T\_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.24000001	2.24000001 ± 4.88E-04	-
AssistFirewall_ActiveRawAcc_Cnt_M_u16	463	463 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	-
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019	-8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-4.8039999	-4.8039999 ± 4.88E-04	-
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-3	-3 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	-
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.1960001	2.1960001 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	-
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-8.80000019	-8.80000019 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	•
Param_Cnt_T_u08	0x01	0x01	<u> </u>

Τ				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	_

0x01

0xC9

0x01

0x01

0x01

0xC9

0x01

0x01

Test Step 2.66 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.300000012
AssistFirewall_ActiveRawAcc_Cnt_M_u16	6888
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00125584798
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.60000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.029999993
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.5
k_AsstFWInpLimitHFA_MtrNm_f32	5
k_AsstFWInpLimitHysComp_MtrNm_f32	6.69999981
k_AsstFWNstep_Cnt_u16	4182
k_AsstFWPstep_Cnt_u16	4428
k_RestoreThresh_MtrNm_f32	8.60000038
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0
and the second control of the second control	·





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2 AsstFWUprBoundX HwNm s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
LE_7 tooti vvopi Bodila i _iviti viii_0+p i i [o][ i]	
	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-2048 0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048 0

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048
2 AsstFWUprBoundY MtrNm s4p11[2][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048
z_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096
	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][10] 2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	4096
2 AsstFWUprBoundY MtrNm s4p11[5][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336
z_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048
	0





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	717
t_AsstFWDefltAssistX_HwNm_u8p8[1]	742
t_AsstFWDefltAssistX_HwNm_u8p8[2]	768
t_AsstFWDefltAssistX_HwNm_u8p8[3]	794 819
t_AsstFWDefltAssistX_HwNm_u8p8[4] t AsstFWDefltAssistX HwNm u8p8[5]	845
t_AsstFWDefitAssistX_HwNm_u8p8[6]	870
t_AsstFWDefltAssistX_HwNm_u8p8[7]	896
t_AsstFWDefltAssistX_HwNm_u8p8[8]	922
t_AsstFWDefltAssistX_HwNm_u8p8[9]	947
t_AsstFWDefltAssistX_HwNm_u8p8[10]	973
t_AsstFWDefltAssistX_HwNm_u8p8[11]	998
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1203
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[12] t AsstFWDefltAssistY_MtrNm_s4p11[13]	17818 18022
t_AsstFWDefitAssistY_MtrNm_s4p11[14]	18227
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	18432
t_AsstFWDefitAssistY_MtrNm_s4p11[16]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	19251
t_AsstFWPstepNstepThresh_Cnt_u16[0]	187
t_AsstFWPstepNstepThresh_Cnt_u16[1]	467
t_AsstFWVehSpd_Kph_u9p7[0]	22016
t_AsstFWVehSpd_Kph_u9p7[1]	22144
t_AsstFWVehSpd_Kph_u9p7[2]	22272
t_AsstFWVehSpd_Kph_u9p7[3]	22400
t_AsstFWVehSpd_Kph_u9p7[4]	22528
t_AsstFWVehSpd_Kph_u9p7[5]	22656
t_AsstFWVehSpd_Kph_u9p7[6]	22784
t_AsstFWVehSpd_Kph_u9p7[7]	22912
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-9
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2 22 2000005
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	33.099985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_letgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_intrium_rs2  tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_mtrnm_t32 tgt_AssistFirewall_Per1_HwTorque_HwNm_t32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32
0 = 1 = 1 = 1 = 1 = 1 = 1 = 1 = 1 = 1 =	V =

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.76999981	0.769999981 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	467	467 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019	-8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.00891638	7.00891638 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-0.800000191	-0.800000012 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.88699985	2.88700008 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.769999981	0.769999981 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-8.80000019	-8.80000019 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>~</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.67 (Repeat Count = 1)  ✓			
Name	Input Value		
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	7		
AssistFirewall ActiveKSV M str.K Uls f32	0.059999987		
AssistFirewall_ActiveRawAcc_Cnt_M_u16	7011		
AssistFirewall AsstReducedPerfSV Cnt M lqc	0		
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.5		
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	8		
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.715390444		
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998		
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8		
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.090000036		
AssistFirewall_PNCountStatus_Cnt_M_lgc	1		
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.0999999		
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.039999991		
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall		
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.5999999		
k_AsstFWInpLimitHFA_MtrNm_f32	5.19999981		
k_AsstFWInpLimitHysComp_MtrNm_f32	6.9000001		
k_AsstFWNstep_Cnt_u16	4305		
k_AsstFWPstep_Cnt_u16	4551		
k_RestoreThresh_MtrNm_f32	8.6999981		
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144		
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096		
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048		
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0		
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048		
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096		
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144		
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192		
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240		
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288		
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336		
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192		
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144		
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096		
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048		
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0		
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048		
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096		
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144		
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192		
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240		
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288		
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-18432		





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
tz_Assii Wopibodila i_Militili_s4p i i[o][s]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
	2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	0
2 AsstFWUprBoundY MtrNm s4p11[2][7]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	4096
z_AsstFWUprBoundY_MtrNm_s4p11[2][9]	6144
z_AsstFWUprBoundY_MtrNm_s4p11[2][9] 2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	8192
	-30720
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-30720 -28672
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	6144
2 AsstFWUprBoundY MtrNm s4p11[5][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048





Name  12_AsstFWUprBoundY_MtrNm_s4p11[7][4]  12_AsstFWUprBoundY_MtrNm_s4p11[7][5]  12_AsstFWUprBoundY_MtrNm_s4p11[7][6]  12_AsstFWUprBoundY_MtrNm_s4p11[7][7]  12_AsstFWUprBoundY_MtrNm_s4p11[7][8]	Input Value 6144 8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5] t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	1.02.0
	12288
10. A set FIAU is a Decembry Attack in a set 44 FRICE	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	742
t_AsstFWDefltAssistX_HwNm_u8p8[1]	768
t_AsstFWDefltAssistX_HwNm_u8p8[2]	794
t_AsstFWDefltAssistX_HwNm_u8p8[3] t_AsstFWDefltAssistX_HwNm_u8p8[4]	819 845
t_AsstFWDefltAssistX_HwNm_u8p8[5]	870
t_AsstFWDefltAssistX_HwNm_u8p8[6]	896
t_AsstFWDefltAssistX_HwNm_u8p8[7]	922
t_AsstFWDefltAssistX_HwNm_u8p8[8]	947
t_AsstFWDefltAssistX_HwNm_u8p8[9]	973
t_AsstFWDefltAssistX_HwNm_u8p8[10]	998
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[16] t_AsstFWDefltAssistX_HwNm_u8p8[17]	1152 1178
t_AsstFWDefitAssistX_HwNm_u8p8[18]	1203
t_AsstFWDefitAssistX_HwNm_u8p8[19]	1229
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[10] t_AsstFWDefltAssistY_MtrNm_s4p11[11]	17613 17818
t_AsstFWDefitAssistY_MtrNm_s4p11[12]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	19456
t_AsstFWPstepNstepThresh_Cnt_u16[0]	188
t_AsstFWPstepNstepThresh_Cnt_u16[1]	471
t_AsstFWVehSpd_Kph_u9p7[0]	24960
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	25088
t_AsstFWVehSpd_Kph_u9p7[2] t_AsstFWVehSpd_Kph_u9p7[3]	25216 25344
t_AsstFWVehSpd_Kph_u9p7[4]	25472
t_AsstFWVehSpd_Kph_u9p7[5]	25600
t_AsstFWVehSpd_Kph_u9p7[6]	25728
t_AsstFWVehSpd_Kph_u9p7[7]	25856
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	44.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lttg_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_rte_inst_ap_assistFirewali.assistFirewali_Peri_HighFreqassist_mtrnm_i32  tgt_rte_inst_ap_assistFirewall.assistFirewall_Peri_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_mtrnm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
2 2 12 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.57999992	6.57999992 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	471	471 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.60009766	7.60009766 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	9.28770256	9.28770256 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.36999989	7.36999989 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.97599983	3.97600007 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	7.60009766	7.60009766 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	✓

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.68 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.070000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	7134
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.5
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.04999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.10000001
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0500000007
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.70000005
k_AsstFWInpLimitHFA_MtrNm_f32	5.4000001
k_AsstFWInpLimitHysComp_MtrNm_f32	7.0999999
k_AsstFWNstep_Cnt_u16	4428
k_AsstFWPstep_Cnt_u16	4674
k_RestoreThresh_MtrNm_f32	1.12
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
2 AsstFWUprBoundX HwNm s4p11[5][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
2 AsstFWUprBoundX HwNm s4p11[6][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-30720
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-16384





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][6] 2 AsstFWUprBoundY MtrNm s4p11[2][7]	2048
	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
	-6192 -6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	768
t_AsstFWDefltAssistX_HwNm_u8p8[1]	794
t_AsstFWDefltAssistX_HwNm_u8p8[2]	819 845
t_AsstFWDefltAssistX_HwNm_u8p8[3] t_AsstFWDefltAssistX_HwNm_u8p8[4]	870
t_AsstFWDefltAssistX_HwNm_u8p8[5]	896
t_AsstFWDefltAssistX_HwNm_u8p8[6]	922
t_AsstFWDefltAssistX_HwNm_u8p8[7]	947
t_AsstFWDefltAssistX_HwNm_u8p8[8]	973
t_AsstFWDefltAssistX_HwNm_u8p8[9]	998
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1126
t_AsstFWDefitAssistX_HwNm_u8p8[15]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1178
t AsstFWDefltAssistX HwNm u8p8[17]	1203
t_AsstFWDefitAssistX_HwNm_u8p8[18]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1254
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	19661
t_AsstFWPstepNstepThresh_Cnt_u16[0]	189
t_AsstFWPstepNstepThresh_Cnt_u16[1]	475
t_AsstFWVehSpd_Kph_u9p7[0]	27904
t_AsstFWVehSpd_Kph_u9p7[1]	28032
t_AsstFWVehSpd_Kph_u9p7[2]	28160
t_AsstFWVehSpd_Kph_u9p7[3]	28288
t_AsstFWVehSpd_Kph_u9p7[4]	28416
t_AsstFWVehSpd_Kph_u9p7[5]	28544
t_AsstFWVehSpd_Kph_u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7]	28800
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	55.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_Ass$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7.44000006	7.44000006 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	2706	2706 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.70019531	-7.70019531 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.95000029	3.95000005 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.08999991	2.08999991 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.09499979	4.09499979 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.70019531	-7.70019531 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Name	Test Step 2.69 (Repeat Count = 1)	v
AssistFirewall ActiveKSV M, str. K, Uis, 132   0.079999982   0.079999982   0.079999982   0.079999982   0.079999982   0.079999982   0.079999982   0.079999982   0.079999982   0.079999982   0.079999983   0.079999983   0.079999983   0.079999983   0.079999983   0.0799999983   0.0799999983   0.0799999983   0.0799999983   0.0799999983   0.0799999983   0.0799999983   0.0799999983   0.0799999983   0.0799999983   0.079999999   0.079999999   0.079999999   0.079999999   0.079999999   0.0799999999   0.0799999999   0.0799999999   0.0799999999999999999999999999999999999		Input Value
AssisFirewall ActiveRSV M. str. K. Uls. 132         0.7799999982           AssisFirewall ActiveRswAcc, Cnt. M. u16         7257           AssisFirewall AssisfieducedPerSV, Cnt. Mgc         0           AssisFirewall AssisfieducedPerSV, Cnt. Mgc         2.00000005           AssisFirewall HirrogKSV, M. str. PS. vtS. Vuls. 132         2.00000005           AssisFirewall HirrogKSV, M. str. LVB. Str. Vuls. 132         1.00002001           AssisFirewall LivBoundKSV, M. str. Vuls. 132         0.00000003           AssisFirewall LivBoundKSV, M. str. Vuls. 132         0.000000003           K. JassiffVinpLimidsaeAssi, Minfun, 132         3.79999995           Rie Inst, Ap. AssisFirewall         1.5000000000           K. AssiffVinpLimithysComp, Minfun, 132         7.00000000           K. AssiffVinpLimithysComp, Minfun, 132         4.5000000000000000000000000000000000000	AssistFirewall ActiveKSV M str.SV Uls f32	
AssistFiewall, CambAsstSV, MrNm, M, 132         5,69999981           AssistFiewall, Hiffer(KSV, M, strLPF, StrK, Uls, 132         0,00000001           AssistFiewall, Hiffer(KSV, M, strLPF, StrK, Uls, 132         0,00000001           AssistFiewall, LimboundKSV, M, strLR, Str, Uls, 132         1,00000001           AssistFiewall, LimboundKSV, M, str, K, Uls, 132         0,00000003           AssistFiewall, LimboundKSV, M, str, K, Uls, 132         0,00000000000000000000000000000000000		
AssistFiewall, CambAsstSV, MrNm, M, 132         5,69999981           AssistFiewall, Hiffer(KSV, M, strLPF, StrK, Uls, 132         0,00000001           AssistFiewall, Hiffer(KSV, M, strLPF, StrK, Uls, 132         0,00000001           AssistFiewall, LimboundKSV, M, strLR, Str, Uls, 132         1,00000001           AssistFiewall, LimboundKSV, M, str, K, Uls, 132         0,00000003           AssistFiewall, LimboundKSV, M, str, K, Uls, 132         0,00000000000000000000000000000000000	AssistFirewall ActiveRawAcc Cnt M u16	7257
AssisFirewall HiFreqKSV_M_strLPF_StrSV_Uls_f32 0.10000005 AssisFirewall_HiFreqKSV_M_strLPF_StrK_Uls_f32 0.10000001 AssisFirewall_LimPodovfdKSV_M_strC_PUls_f32 1.0062899 AssisFirewall_LimPodovfdKV_M_strK_Uls_f32 0.20000005 AssisFirewall_LimPodovfdKV_M_strK_Uls_f32 0.20000003 AssisFirewall_ProdovfdKSV_M_strK_Uls_f32 0.20000003 AssisFirewall_ProdovfdKSV_M_strK_Uls_f32 0.05999999 AssisFirewall_UlpPodovfdKV_M_strK_Uls_f32 0.059999999 AssisFirewall_UlpPodovfdKV_M_strK_Uls_f32 0.059999999 AssisFirewall_UlpPodovfdKV_M_strK_Uls_f32 0.059999999 AssisFirewall_UlpPodovfdKV_M_strK_Uls_f32 0.059999999 AssisFirewall_UlpPodovfdKV_M_strK_Uls_f32 0.059999999 AssisFirewall_UlpPodovfdKV_M_strK_Uls_f32 0.0599999999 AssisFirewall_UlpPodovfdKV_M_strK_Uls_f32 0.059999996 AssisFirewall_UlpPodovfdKV_M_strK_Uls_f32 0.059999996 AssisFirewall_UlpPodovfdKV_M_strK_Uls_f32 0.059999999 AssisFirewall_UlpPodovfdKV_M_strK_Uls_f32 0.059999999999999999 AssisFirewall_UlpPodovfdK_MIN_strK_Uls_f32 0.0599999999999999999999999999999999999		0
AssistFrewall, HFreqKSV, M. str.LPF, Str.K, Uls, J32         1,00002859           AssistFrewall, LWBoundKSV, M. str.K, Uls, J32         2,20000005           AssistFrewall, LWBoundKSV, M. str.K, Uls, J32         0,200000003           AssistFrewall, LWBoundKSV, M. str.K, Uls, J32         0,000000003           AssistFrewall, LWBoundKSV, M. str.K, Uls, J32         6,0999999           AssistFrewall, LWBoundKSV, M. str.K, Uls, J32         0,0599999987           AssistFrewall, UprBoundKSV, M. str.K, Uls, J32         0,059999999           AssistFrewall, LWB, LWB, LWB, LWB, LWB, LWB, LWB, LWB	AssistFirewall_CombAsstSV_MtrNm_M_f32	5.69999981
AssistFirewall_LimPoundKSV_M_str.SV_UIs_132         1,00062859           AssistFirewall_LimPoundKSV_M_str.SV_UIs_132         0,200000003           AssistFirewall_PixPoundKSV_M_str.SV_UIs_132         0,00000003           AssistFirewall_UprBoundKSV_M_str.SV_UIS_132         6,0999999           AssistFirewall_UprBoundKSV_M_str.K_UIS_132         0,0599999987           Rie_Inst_Ap_AssistFirewall         tjt_Re_Inst_Ap_AssistFirewall           K_asstFWinpLimitBaseAsst_MirNm_132         3,7999995           K_AsstFWinpLimitHFA_MirNm_132         7,3000019           K_AsstFWinpLimitHFA_MirNm_132         7,3000019           K_AsstFWinpLimitHFA_MirNm_132         4551           K_AsstFWinpLimitHFA_MirNm_132         1,13           K_AsstFWinpLimitHFA_MirNm_132         1,13           K_AsstFWinpLimitHFA_MirNm_132         1,13           K_AsstFWinpLimitHFA_MirNm_140         2048           K_AsstFWUpBoundX_HirNm_440110[0]         2048           K_AsstFWUpBoundX_HirNm_440110[0]         2048           K_AsstFWUpBoundX_HirNm_440110[0]         6144           K_AsstFWUpBoundX_HirNm_440110[0]         8192           K_AsstFWUpBoundX_HirNm_440110[0]         1634           K_AsstFWUpBoundX_HirNm_440110[0]         16384           K_AsstFWUpBoundX_HirNm_440110[0]         1643           K_AsstFWUp	AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.20000005
AssistFirewall_LwrBoundKSV_M.str.SU_IIs_32         2.0000005           AssistFirewall_LwrBoundKSV_M.str.K_UIs_72         0.20000003           AssistFirewall_UprBoundKSV_M.str.SU_IIS_22         6.0999999           AssistFirewall_UprBoundKSV_M.str.K_UIs_72         0.0599999987           Rie_Inst.Ap_AssistFirewall         tg_Re_Inst.Ap_AssistFirewall           k_Assif-WinpLimitBaseAsst_MrNm_I32         3.79999995           k_Assif-WinpLimitBaseAsst_MrNm_I32         5.5999999           k_Assif-WinpLimitHysComp_MrNm_I32         7.3000019           k_Assif-WinpLimitHysComp_MrNm_I32         7.3000019           k_Assif-WinpLimitHysComp_MrNm_I32         4551           k_Assif-WinpLimitHysComp_MrNm_I32         1.13           k_Assif-WinpLimitHysComp_MrNm_I42         1.13           k_Assif-WinpLimitHysComp_MrNm_I42         1.13           k_Assif-WinpLimitHysComp_MrNm_I42         1.13           k_Assif-WinpLimitHysComp_MrNm_I441000         2.048           k_Assif-WinpLimitHysComp_MrNm_I4411000         2.048           k_Assif-WinpLimitHysComp_MrNm_I4411000         0           k_Assif-WinpLimitHysComp_MrNm_I44110000         2.048           k_Assif-WinpLimitHysComp_MrNm_I44110000         0           k_Assif-WinpLimitHysComp_MrNm_I44110000         0           k_Assif-WinpLimitHysComp_MrNm_I44110000         0<	AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.100000001
AssistFirewall_NrBoundKSV_M.str.K_UIs_132         0.20000003           AssistFirewall_PNCountStatus_Cnt_M.lgc         1           AssistFirewall_UpfBoundKSV_M.str.K_UIs_132         6.099999           AssistFirewall_UpfBoundKSV_M.str.K_UIs_132         0.05999999987           Rtl_Inst_Ap_AssistFirewall         tg_Re_Inst_Ap_AssistFirewall           K_AssIFWIpLimitHFA_MITM_132         3.79999999           K_AssIFWIpLimitHFA_MITM_152         5.5999999           K_AssIFWIpLimitHFA_MITM_152         7.0000019           K_AssIFWIpLimitHFA_MITM_152         4.591           K_AssIFWIpLimitHFA_MITM_152         1.3000019           K_AssIFWIPSEP_Cnt_u16         4797           K_AssIFWIPSEP_Cnt_U16         4797           K_AssIFWIPSEP_Cnt_U16         4797           K_AssIFWIPSEP_Cnt_U16         479           K_AssIFWIPSEP_Cnt_U16         2048           K_AssIFWIPSEP_Cnt_U16         2048           K_AssIFWIPSEP_Cnt_U16         0           K_AssIFWIPSEP_Cnt_U16	AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00062859
AssistFirewall_PNCountStatus_Cnt_M_lgc         1           AssistFirewall_UprBoundKSV_M_str_K_UIs_132         6.0999999           AssistFirewall_UprBoundKSV_M_str_K_UIs_132         0.0599999987           Rte_Inst_Ap_AssistFirewall         tg_Rte_Inst_Ap_AssistFirewall           k_AssifWinpLimitBaseAsst_MinVm_132         3.79999996           k_AssifWinpLimitHsA_MinVm_132         7.30000019           k_AssifWinpLimitHyA_Comp_MinVm_132         7.30000019           k_AssifWinpLimitHyB_Comp_MinVm_132         4551           k_AssifWinpLimitHyB_Comp_MinVm_132         1.13           k_AssifWinpLoundX_HwNm_4911[0]01         2048           t_AssifWinpLoundX_HwNm_4911[0]11         0           t_AssifWinpLoundX_HwNm_4911[0]12         2048           t_AssifWinpLoundX_HwNm_4911[0]13         4096           t_AssifWinpLoundX_HwNm_4911[0]15         8192           t_AssifWinpLoundX_HwNm_4911[0]16         10240           t_AssifWinpLoundX_HwNm_4911[0]16         12288           t_AssifWinpLoundX_HwNm_4911[0]19         1634           t_AssifWinpLoundX_HwNm_4911[0]19         1634           t_AssifWinpLoundX_HwNm_4911[0]19         1634           t_AssifWinpLoundX_HwNm_4911[1]10         4096           t_AssifWinpLoundX_HwNm_4911[1]11         2048           t_AssifWinpLoundX_HwNm_4911[1]10 <td>AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32</td> <td>2.20000005</td>	AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall UprBoundKSV M. str. K. Uls. 132         6.0999999           AssistFirewall UprBoundKSV M. str. K. Uls. 132         0.059999997           K. Inst. Ap. AssistFirewall         tgt. Rie. Inst. Ap. AssistFirewall           K. AssistPinpLimitBaseAsst. MtrNm_132         3.79999995           K. AssistPWInpLimitHFA MtrNm_132         5.5999999           K. AssistPWInpLimitHFA MtrNm_132         7.3000019           K. AssistPWInpLimitHFA Drump MtrNm_132         4797           K. AssistPWDep Cnt. u16         4797           K. AssistPWDep Drumt Mrnm_132         1.13           12. AssistPWUprBoundX, HwNm_s4p110[0]         -2048           12. AssistPWUprBoundX, HwNm_s4p110[0]         2048           12. AssistPWUprBoundX, HwNm_s4p110[13]         496           12. AssistPWUprBoundX, HwNm_s4p110[13]         496           12. AssistPWUprBoundX, HwNm_s4p110[16]         10240           12. AssistPWUprBoundX, HwNm_s4p110[16]         10240           12. AssistPWUprBoundX, HwNm_s4p110[17]         1228           12. AssistPWUprBoundX, HwNm_s4p110[19]         1832           12. AssistPWUprBoundX, HwNm_s4p110[19]         18334           12. AssistPWUprBoundX, HwNm_s4p110[10]         4966           12. AssistPWUprBoundX, HwNm_s4p111[11]         -2048           12. AssistPWUprBoundX, HwNm_s4p111[18]	AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.20000003
AssisFirewall_UprBoundKSV_M_str.K_Uls_132         0.0599999987           Rte_Inst.Ap_AssisFirewall         tg_Rte_Inst.Ap_AssisFirewall           k_AsstFWInpLimitHsqsAsst_MrNm_132         5.5999999           k_AsstFWInpLimitHrS_MtrNm_132         7.0000019           k_AsstFWInpLimitHrS_Ornp_MtrNm_132         4551           k_AsstFWInpLimitHrS_Orn_Lint6         4797           k_AsstFWUpte_Orn_U16         4797           k_RestorThresh_MtrNm_132         1.13           2_AsstFWUprBoundX_HwNm_s4p11[0][0]         -2048           2_AsstFWUprBoundX_HwNm_s4p11[0][1]         0           2_AsstFWUprBoundX_HwNm_s4p11[0][2]         2048           2_AsstFWUprBoundX_HwNm_s4p11[0][3]         6144           2_AsstFWUprBoundX_HwNm_s4p11[0][6]         8192           2_AsstFWUprBoundX_HwNm_s4p11[0][6]         10240           2_AsstFWUprBoundX_HwNm_s4p11[0][8]         14336           2_AsstFWUprBoundX_HwNm_s4p11[0][9]         16384           2_AsstFWUprBoundX_HwNm_s4p11[0][9]         4096           2_AsstFWUprBoundX_HwNm_s4p11[0][1]         2048           2_AsstFWUprBoundX_HwNm_s4p11[1][1]         2048           2_AsstFWUprBoundX_HwNm_s4p11[1][1]         4096           2_AsstFWUprBoundX_HwNm_s4p11[1][1]         2048           2_AsstFWUprBoundX_HwNm_s4p11[1][1]         6144	AssistFirewall_PNCountStatus_Cnt_M_lgc	1
Re Inst Ap AssistFirewall         tgt Re Inst Ap AssistFirewall           k. AssFWInpLimitBaseAsst. MirNm; 132         3.79999995           k. AssFWInpLimitHFA MirNm; 132         7.3000019           k. AssFWINpLimitHy-Comp, MirNm; 132         4551           k. AssFWINStep_Cnt_u16         4579           k. Restor Finesh. MirNm; 132         1.13           12. AssFWQDBoundX, HwNm_s4p11[0][0]         -2048           12. AssFWQDBoundX, HwNm_s4p11[0][1]         0           12. AssFWQDBoundX, HwNm_s4p11[0][2]         2048           12. AssFWQDBoundX, HwNm_s4p11[0][3]         4096           12. AssFWQDBoundX, HwNm_s4p11[0][4]         6144           12. AssFWQDBoundX, HwNm_s4p11[0][5]         8192           12. AssFWQDBoundX, HwNm_s4p11[0][7]         12288           12. AssFWQDBoundX, HwNm_s4p11[0][8]         14336           12. AssFWQDBoundX, HwNm_s4p11[0][9]         1634           12. AssFWQDBoundX, HwNm_s4p11[0][9]         1634           12. AssFWQDBoundX, HwNm_s4p11[0][1]         2048           12. AssFWQDBoundX, HwNm_s4p11[0][1]         2048           12. AssFWQDBoundX, HwNm_s4p11[0][1]         2048           12. AssFWQDBoundX, HwNm_s4p11[0][1]         2048           12. AssFWQDBoundX, HwNm_s4p11[1][4]         4096           2. AssFWQDBoundX, HwNm_s4p11[1][4]	AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.0999999
k. AsstFWInpLimitBaseAsst_MtrNm_f32         3.79999995           k. AsstFWInpLimitHysComp_MtrNm_f32         5.599999           k. AsstFWInpLimitHysComp_MtrNm_f32         7.30000019           k. AsstFWNstep_Cnt_u16         4551           k. AsstFWDestp_Cnt_u16         4797           k. RestoreThresh_MtrNm_f32         1.13           12. AsstFWUprBoundX_HwNm_s4p110[10]         -2048           12. AsstFWUprBoundX_HwNm_s4p110[1]         0           2. AsstFWUprBoundX_HwNm_s4p110[13]         4096           12. AsstFWUprBoundX_HwNm_s4p110[14]         6144           12. AsstFWUprBoundX_HwNm_s4p110[15]         8192           12. AsstFWUprBoundX_HwNm_s4p110[17]         12288           12. AsstFWUprBoundX_HwNm_s4p110[18]         14336           12. AsstFWUprBoundX_HwNm_s4p110[19]         16384           12. AsstFWUprBoundX_HwNm_s4p110[10]         18432           12. AsstFWUprBoundX_HwNm_s4p111[10]         4096           12. AsstFWUprBoundX_HwNm_s4p11[10]         10432           12. AsstFWUprBoundX_HwNm_s4p11[11]         2048           12. AsstFWUprBoundX_HwNm_s4p11[11]         2048           12. AsstFWUprBoundX_HwNm_s4p11[11]         2048           12. AsstFWUprBoundX_HwNm_s4p11[1]         2048           12. AsstFWUprBoundX_HwNm_s4p11[1]         6144	AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0599999987
k. AsstFWInpLimitHyS.comp_MtrNm_f32         5.5999999           k. AsstFWInpLimitHyS.comp_MtrNm_f32         7.3000019           k. AsstFWNstep_Cnt_u16         4551           k. AsstFWPstep_Cnt_u16         4797           k. RestoreThresh_MtrNm_f32         1.13           12. AsstFWDgboundX_HwNm_s4p11[0]1         0           12. AsstFWDgboundX_HwNm_s4p11[0]1]         0           12. AsstFWUprBoundX_HwNm_s4p11[0]2]         2048           12. AsstFWUprBoundX_HwNm_s4p11[0]3         4096           12. AsstFWUprBoundX_HwNm_s4p11[0]4         6144           12. AsstFWUprBoundX_HwNm_s4p11[0]6         10240           12. AsstFWUprBoundX_HwNm_s4p11[0]7         12288           12. AsstFWUprBoundX_HwNm_s4p11[0]8         14336           12. AsstFWUprBoundX_HwNm_s4p11[0]9         16384           12. AsstFWUprBoundX_HwNm_s4p11[0]10         4096           12. AsstFWUprBoundX_HwNm_s4p11[1]10         4096           12. AsstFWUprBoundX_HwNm_s4p11[1]11         2048           12. AsstFWUprBoundX_HwNm_s4p11[1]12         0           12. AsstFWUprBoundX_HwNm_s4p11[1]13         2048           12. AsstFWUprBoundX_HwNm_s4p11[1]14         4096           12. AsstFWUprBoundX_HwNm_s4p11[1]16         8192           12. AsstFWUprBoundX_HwNm_s4p11[1]16         8192	Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k. AsstFWinpLimitHysComp_MtrNm_[32]         7.30000019           k. AsstFWNstepCnt_u16         4551           k. AsstFWPstepCnt_u16         4797           k. RestoreThresh_MtrNm_[32]         1.13           12_AsstFWUprBoundX_HwNm_s4p11[0][0]         -2048           12_AsstFWUprBoundX_HwNm_s4p11[0][2]         0           2_AsstFWUprBoundX_HwNm_s4p11[0][3]         4096           12_AsstFWUprBoundX_HwNm_s4p11[0][4]         6144           12_AsstFWUprBoundX_HwNm_s4p11[0][5]         8192           12_AsstFWUprBoundX_HwNm_s4p11[0][6]         10240           12_AsstFWUprBoundX_HwNm_s4p11[0][7]         12288           12_AsstFWUprBoundX_HwNm_s4p11[0][8]         14336           12_AsstFWUprBoundX_HwNm_s4p11[0][9]         16344           12_AsstFWUprBoundX_HwNm_s4p11[0][9]         16344           12_AsstFWUprBoundX_HwNm_s4p11[1][9]         4096           12_AsstFWUprBoundX_HwNm_s4p11[1][9]         4096           12_AsstFWUprBoundX_HwNm_s4p11[1][9]         0           12_AsstFWUprBoundX_HwNm_s4p11[1][9]         0           12_AsstFWUprBoundX_HwNm_s4p11[1][9]         4096           12_AsstFWUprBoundX_HwNm_s4p11[1][9]         0496           12_AsstFWUprBoundX_HwNm_s4p11[1][9]         6144           12_AsstFWUprBoundX_HwNm_s4p11[1][9]         6144 <t< td=""><td>k_AsstFWInpLimitBaseAsst_MtrNm_f32</td><td>3.79999995</td></t<>	k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.79999995
k. AsstFWnstep_Cnt_u16       4551         k. AsstFWPstep_Cnt_u16       4797         k. RestoreThresh_MtrNm_g12       1.13         12_AsstFWUprBoundX_HwNm_s4p11[0][0]       -2048         12_AsstFWUprBoundX_HwNm_s4p11[0][1]       0         12_AsstFWUprBoundX_HwNm_s4p11[0][3]       4096         12_AsstFWUprBoundX_HwNm_s4p11[0][4]       6144         12_AsstFWUprBoundX_HwNm_s4p11[0][5]       8192         12_AsstFWUprBoundX_HwNm_s4p11[0][7]       12288         12_AsstFWUprBoundX_HwNm_s4p11[0][7]       12288         12_AsstFWUprBoundX_HwNm_s4p11[0][8]       14336         12_AsstFWUprBoundX_HwNm_s4p11[0][9]       16384         12_AsstFWUprBoundX_HwNm_s4p11[0][0]       4096         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       4096 <td>k_AsstFWInpLimitHFA_MtrNm_f32</td> <td>5.5999999</td>	k_AsstFWInpLimitHFA_MtrNm_f32	5.5999999
k. AsstFWPstep_Cnt_u16       4797         k. RestoreThresh_MirNm_s4p11(0)[0]       1.13         12. AsstFWUprBoundX, HwNm_s4p11(0)[1]       0         12. AsstFWUprBoundX, HwNm_s4p11(0)[2]       2048         12. AsstFWUprBoundX, HwNm_s4p11(0)[3]       4096         12. AsstFWUprBoundX, HwNm_s4p11(0)[4]       6144         12. AsstFWUprBoundX, HwNm_s4p11(0)[5]       8192         12. AsstFWUprBoundX, HwNm_s4p11(0)[6]       10240         12. AsstFWUprBoundX, HwNm_s4p11(0)[7]       12288         12. AsstFWUprBoundX, HwNm_s4p11(0)[8]       14336         12. AsstFWUprBoundX, HwNm_s4p11(0)[9]       16384         12. AsstFWUprBoundX, HwNm_s4p11(0)[10]       18432         12. AsstFWUprBoundX, HwNm_s4p11(1)[0]       4096         12. AsstFWUprBoundX, HwNm_s4p11(1)[1]       2048         12. AsstFWUprBoundX, HwNm_s4p11(1)[1]       2048         12. AsstFWUprBoundX, HwNm_s4p11(1)[2]       0         12. AsstFWUprBoundX, HwNm_s4p11(1)[3]       2048         12. AsstFWUprBoundX, HwNm_s4p11(1)[4]       4096         12. AsstFWUprBoundX, HwNm_s4p11(1)[6]       8192         12. AsstFWUprBoundX, HwNm_s4p11(1)[6]       8192         12. AsstFWUprBoundX, HwNm_s4p11(1)[6]       8192         12. AsstFWUprBoundX, HwNm_s4p11(1)[7]       10240         12. Asst	k_AsstFWInpLimitHysComp_MtrNm_f32	7.30000019
k_RestoreThresh_MtNm_f32	k_AsstFWNstep_Cnt_u16	4551
12_AsstFWUprBoundX_HwNm_s4p11[0][0]       -2048         12_AsstFWUprBoundX_HwNm_s4p11[0][1]       0         12_AsstFWUprBoundX_HwNm_s4p11[0][2]       2048         12_AsstFWUprBoundX_HwNm_s4p11[0][3]       4096         12_AsstFWUprBoundX_HwNm_s4p11[0][4]       6144         12_AsstFWUprBoundX_HwNm_s4p11[0][5]       8192         12_AsstFWUprBoundX_HwNm_s4p11[0][6]       10240         12_AsstFWUprBoundX_HwNm_s4p11[0][7]       12288         12_AsstFWUprBoundX_HwNm_s4p11[0][8]       14336         12_AsstFWUprBoundX_HwNm_s4p11[0][9]       16384         12_AsstFWUprBoundX_HwNm_s4p11[0][10]       18432         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       4096         12_AsstFWUprBoundX_HwNm_s4p11[1][1]       -2048         12_AsstFWUprBoundX_HwNm_s4p11[1][2]       0         12_AsstFWUprBoundX_HwNm_s4p11[1][3]       2048         12_AsstFWUprBoundX_HwNm_s4p11[1][3]       2048         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       6144         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       6144         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[1][7]       10240         12_AsstFWUprBoundX_HwNm_s4p11[1][8]       1228         12_AsstFWUprBoundX_HwNm_s4p11[1][8]       12288         12_AsstFWUprBoundX_HwNm_s4p11[1	k_AsstFWPstep_Cnt_u16	4797
12_AsstFWUprBoundX_HwNm_s4p11[0][2]       0         12_AsstFWUprBoundX_HwNm_s4p11[0][2]       2048         12_AsstFWUprBoundX_HwNm_s4p11[0][3]       4096         12_AsstFWUprBoundX_HwNm_s4p11[0][4]       6144         12_AsstFWUprBoundX_HwNm_s4p11[0][5]       8192         12_AsstFWUprBoundX_HwNm_s4p11[0][6]       10240         12_AsstFWUprBoundX_HwNm_s4p11[0][7]       12288         12_AsstFWUprBoundX_HwNm_s4p11[0][8]       14336         12_AsstFWUprBoundX_HwNm_s4p11[0][9]       16384         12_AsstFWUprBoundX_HwNm_s4p11[0][0]       18432         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       4096         12_AsstFWUprBoundX_HwNm_s4p11[1][1]       2048         12_AsstFWUprBoundX_HwNm_s4p11[1][2]       0         12_AsstFWUprBoundX_HwNm_s4p11[1][3]       2048         12_AsstFWUprBoundX_HwNm_s4p11[1][4]       4096         12_AsstFWUprBoundX_HwNm_s4p11[1][5]       6144         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[1][7]       10240         12_AsstFWUprBoundX_HwNm_s4p11[1][8]       12288         12_AsstFWUprBoundX_HwNm_s4p11[1][8]       12288         12_AsstFWUprBoundX_HwNm_s4p11[1][8]       12288          12_AsstFWUprBoundX_HwNm	k_RestoreThresh_MtrNm_f32	1.13
12_AsstFWUprBoundX_HwNm_s4p11[0][2]       2048         12_AsstFWUprBoundX_HwNm_s4p11[0][3]       4096         12_AsstFWUprBoundX_HwNm_s4p11[0][4]       6144         12_AsstFWUprBoundX_HwNm_s4p11[0][5]       8192         12_AsstFWUprBoundX_HwNm_s4p11[0][6]       10240         12_AsstFWUprBoundX_HwNm_s4p11[0][7]       12288         12_AsstFWUprBoundX_HwNm_s4p11[0][8]       14336         12_AsstFWUprBoundX_HwNm_s4p11[0][9]       16384         12_AsstFWUprBoundX_HwNm_s4p11[0][0]       18432         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       4096         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       2048         12_AsstFWUprBoundX_HwNm_s4p11[1][2]       0         12_AsstFWUprBoundX_HwNm_s4p11[1][3]       2048         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       4096         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[1][7]       10240         12_AsstFWUprBoundX_HwNm_s4p11[1][8]       12288         12_AsstFWUprBoundX_HwNm_s4p11[1][9]       14336	t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
12_AsstFWUprBoundX_HwNm_s4p11[0][3]       4096         12_AsstFWUprBoundX_HwNm_s4p11[0][5]       6144         12_AsstFWUprBoundX_HwNm_s4p11[0][5]       8192         12_AsstFWUprBoundX_HwNm_s4p11[0][6]       10240         12_AsstFWUprBoundX_HwNm_s4p11[0][7]       12288         12_AsstFWUprBoundX_HwNm_s4p11[0][8]       14336         12_AsstFWUprBoundX_HwNm_s4p11[0][9]       16384         12_AsstFWUprBoundX_HwNm_s4p11[0][10]       18432         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       4096         12_AsstFWUprBoundX_HwNm_s4p11[1][1]       -2048         12_AsstFWUprBoundX_HwNm_s4p11[1][2]       0         12_AsstFWUprBoundX_HwNm_s4p11[1][3]       2048         12_AsstFWUprBoundX_HwNm_s4p11[1][4]       4096         12_AsstFWUprBoundX_HwNm_s4p11[1][5]       6144         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[1][7]       10240         12_AsstFWUprBoundX_HwNm_s4p11[1][8]       12288         12_AsstFWUprBoundX_HwNm_s4p11[1][8]       12288         12_AsstFWUprBoundX_HwNm_s4p11[1][9]       14336	t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
12_AsstFWUprBoundX_HwNm_s4p11[0][4]       6144         12_AsstFWUprBoundX_HwNm_s4p11[0][5]       8192         12_AsstFWUprBoundX_HwNm_s4p11[0][6]       10240         12_AsstFWUprBoundX_HwNm_s4p11[0][7]       12288         12_AsstFWUprBoundX_HwNm_s4p11[0][8]       14336         12_AsstFWUprBoundX_HwNm_s4p11[0][9]       16384         12_AsstFWUprBoundX_HwNm_s4p11[0][0]       18432         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       -4096         12_AsstFWUprBoundX_HwNm_s4p11[1][1]       -2048         12_AsstFWUprBoundX_HwNm_s4p11[1][2]       0         12_AsstFWUprBoundX_HwNm_s4p11[1][3]       2048         12_AsstFWUprBoundX_HwNm_s4p11[1][4]       4096         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       6144         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       10240         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       12288         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       12288         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       12288         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       12288	t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
12_AsstFWUprBoundX_HwNm_s4p11[0][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[0][7]       10240         12_AsstFWUprBoundX_HwNm_s4p11[0][7]       12288         12_AsstFWUprBoundX_HwNm_s4p11[0][8]       14336         12_AsstFWUprBoundX_HwNm_s4p11[0][9]       16384         12_AsstFWUprBoundX_HwNm_s4p11[0][10]       18432         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       -4096         12_AsstFWUprBoundX_HwNm_s4p11[1][1]       -2048         12_AsstFWUprBoundX_HwNm_s4p11[1][2]       0         12_AsstFWUprBoundX_HwNm_s4p11[1][3]       2048         12_AsstFWUprBoundX_HwNm_s4p11[1][4]       4096         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       4096         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       10240         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       12288         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       12288         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       12288         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       12288	t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
12_AsstFWUprBoundX_HwNm_s4p11[0][6]       10240         12_AsstFWUprBoundX_HwNm_s4p11[0][7]       12288         12_AsstFWUprBoundX_HwNm_s4p11[0][8]       14336         12_AsstFWUprBoundX_HwNm_s4p11[0][9]       16384         12_AsstFWUprBoundX_HwNm_s4p11[0][10]       18432         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       -4096         12_AsstFWUprBoundX_HwNm_s4p11[1][1]       -2048         12_AsstFWUprBoundX_HwNm_s4p11[1][2]       0         12_AsstFWUprBoundX_HwNm_s4p11[1][3]       2048         12_AsstFWUprBoundX_HwNm_s4p11[1][4]       4096         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       6144         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[1][7]       10240         12_AsstFWUprBoundX_HwNm_s4p11[1][8]       12288         12_AsstFWUprBoundX_HwNm_s4p11[1][9]       14336	t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
12_AsstFWUprBoundX_HwNm_s4p11[0][7]       12288         12_AsstFWUprBoundX_HwNm_s4p11[0][8]       14336         12_AsstFWUprBoundX_HwNm_s4p11[0][9]       16384         12_AsstFWUprBoundX_HwNm_s4p11[0][10]       18432         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       -4096         12_AsstFWUprBoundX_HwNm_s4p11[1][1]       -2048         12_AsstFWUprBoundX_HwNm_s4p11[1][2]       0         12_AsstFWUprBoundX_HwNm_s4p11[1][3]       2048         12_AsstFWUprBoundX_HwNm_s4p11[1][4]       4096         12_AsstFWUprBoundX_HwNm_s4p11[1][5]       6144         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[1][7]       10240         12_AsstFWUprBoundX_HwNm_s4p11[1][8]       12288         12_AsstFWUprBoundX_HwNm_s4p11[1][9]       14336	t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
12_AsstFWUprBoundX_HwNm_s4p11[0][8]       14336         12_AsstFWUprBoundX_HwNm_s4p11[0][9]       16384         12_AsstFWUprBoundX_HwNm_s4p11[0][10]       18432         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       -4096         12_AsstFWUprBoundX_HwNm_s4p11[1][1]       -2048         12_AsstFWUprBoundX_HwNm_s4p11[1][2]       0         12_AsstFWUprBoundX_HwNm_s4p11[1][3]       2048         12_AsstFWUprBoundX_HwNm_s4p11[1][4]       4096         12_AsstFWUprBoundX_HwNm_s4p11[1][5]       6144         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[1][7]       10240         12_AsstFWUprBoundX_HwNm_s4p11[1][8]       12288         12_AsstFWUprBoundX_HwNm_s4p11[1][9]       14336	t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
12_AsstFWUprBoundX_HwNm_s4p11[0][9]       16384         12_AsstFWUprBoundX_HwNm_s4p11[0][10]       18432         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       -4096         12_AsstFWUprBoundX_HwNm_s4p11[1][1]       -2048         12_AsstFWUprBoundX_HwNm_s4p11[1][2]       0         12_AsstFWUprBoundX_HwNm_s4p11[1][3]       2048         12_AsstFWUprBoundX_HwNm_s4p11[1][4]       4096         12_AsstFWUprBoundX_HwNm_s4p11[1][5]       6144         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[1][7]       10240         12_AsstFWUprBoundX_HwNm_s4p11[1][8]       12288         12_AsstFWUprBoundX_HwNm_s4p11[1][9]       14336	t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
12_AsstFWUprBoundX_HwNm_s4p11[0][10]       18432         12_AsstFWUprBoundX_HwNm_s4p11[1][0]       -4096         12_AsstFWUprBoundX_HwNm_s4p11[1][1]       -2048         12_AsstFWUprBoundX_HwNm_s4p11[1][2]       0         12_AsstFWUprBoundX_HwNm_s4p11[1][3]       2048         12_AsstFWUprBoundX_HwNm_s4p11[1][4]       4096         12_AsstFWUprBoundX_HwNm_s4p11[1][5]       6144         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[1][7]       10240         12_AsstFWUprBoundX_HwNm_s4p11[1][8]       12288         12_AsstFWUprBoundX_HwNm_s4p11[1][9]       14336	t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
12_AsstFWUprBoundX_HwNm_s4p11[1][0]       -4096         12_AsstFWUprBoundX_HwNm_s4p11[1][1]       -2048         12_AsstFWUprBoundX_HwNm_s4p11[1][2]       0         12_AsstFWUprBoundX_HwNm_s4p11[1][3]       2048         12_AsstFWUprBoundX_HwNm_s4p11[1][4]       4096         12_AsstFWUprBoundX_HwNm_s4p11[1][5]       6144         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[1][7]       10240         12_AsstFWUprBoundX_HwNm_s4p11[1][8]       12288         12_AsstFWUprBoundX_HwNm_s4p11[1][9]       14336	t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
12_AsstFWUprBoundX_HwNm_s4p11[1][1]       -2048         12_AsstFWUprBoundX_HwNm_s4p11[1][2]       0         12_AsstFWUprBoundX_HwNm_s4p11[1][3]       2048         12_AsstFWUprBoundX_HwNm_s4p11[1][4]       4096         12_AsstFWUprBoundX_HwNm_s4p11[1][5]       6144         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[1][7]       10240         12_AsstFWUprBoundX_HwNm_s4p11[1][8]       12288         12_AsstFWUprBoundX_HwNm_s4p11[1][9]       14336	t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
12_AsstFWUprBoundX_HwNm_s4p11[1][2]     0       12_AsstFWUprBoundX_HwNm_s4p11[1][3]     2048       12_AsstFWUprBoundX_HwNm_s4p11[1][4]     4096       12_AsstFWUprBoundX_HwNm_s4p11[1][5]     6144       12_AsstFWUprBoundX_HwNm_s4p11[1][6]     8192       12_AsstFWUprBoundX_HwNm_s4p11[1][7]     10240       12_AsstFWUprBoundX_HwNm_s4p11[1][8]     12288       12_AsstFWUprBoundX_HwNm_s4p11[1][9]     14336	t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
12_AsstFWUprBoundX_HwNm_s4p11[1][3]       2048         12_AsstFWUprBoundX_HwNm_s4p11[1][4]       4096         12_AsstFWUprBoundX_HwNm_s4p11[1][5]       6144         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[1][7]       10240         12_AsstFWUprBoundX_HwNm_s4p11[1][8]       12288         12_AsstFWUprBoundX_HwNm_s4p11[1][9]       14336	t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
12_AsstFWUprBoundX_HwNm_s4p11[1][4]       4096         12_AsstFWUprBoundX_HwNm_s4p11[1][5]       6144         12_AsstFWUprBoundX_HwNm_s4p11[1][6]       8192         12_AsstFWUprBoundX_HwNm_s4p11[1][7]       10240         12_AsstFWUprBoundX_HwNm_s4p11[1][8]       12288         12_AsstFWUprBoundX_HwNm_s4p11[1][9]       14336	t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[1][6] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[1][7] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[1][8] 12288 t2_AsstFWUprBoundX_HwNm_s4p11[1][9] 14336	t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[1][7] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[1][8] 12288 t2_AsstFWUprBoundX_HwNm_s4p11[1][9] 14336	t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9] 14336	t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	
t2_AsstFWUprBoundX_HwNm_s4p11[1][10] 16384	t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0] -14336	t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336





Namo	Input Value
Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192 C444
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-22528
t2_Asst WoprboundY_MtrNm_s4p11[0][4]	-20480
t2_Asst WoprBoundY_MtrNm_s4p11[0][4]	-18432
	-1643 <i>z</i> -16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-14336





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5] t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8] t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	14336 -16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	6144





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	22528 794
t_AsstFWDefltAssistX_HwNm_u8p8[0] t_AsstFWDefltAssistX_HwNm_u8p8[1]	819
t_AsstFWDefltAssistX_HwNm_u8p8[2]	845
t_AsstFWDefltAssistX_HwNm_u8p8[3]	870
t_AsstFWDefltAssistX_HwNm_u8p8[4]	896
t_AsstFWDefltAssistX_HwNm_u8p8[5]	922
t_AsstFWDefltAssistX_HwNm_u8p8[6]	947
t_AsstFWDefltAssistX_HwNm_u8p8[7]	973
t_AsstFWDefltAssistX_HwNm_u8p8[8]	998
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1280
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	16794 16998
t_AsstFWDefltAssistY_MtrNm_s4p11[5] t_AsstFWDefltAssistY_MtrNm_s4p11[6]	17203
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	18022
t AsstFWDefltAssistY MtrNm s4p11[11]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	19866
t_AsstFWPstepNstepThresh_Cnt_u16[0]	190
t_AsstFWPstepNstepThresh_Cnt_u16[1]	479
t_AsstFWVehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1]	30976
t_AsstFWVehSpd_Kph_u9p7[2]	31104
t_AsstFWVehSpd_Kph_u9p7[3]	31232
t_AsstFWVehSpd_Kph_u9p7[4]	31360
t_AsstFWVehSpd_Kph_u9p7[5]	31488
t_AsstFWVehSpd_Kph_u9p7[6]	31616 31744
t_AsstFWVehSpd_Kph_u9p7[7] tqt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3.099999
tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	66.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	•
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
<u> </u>	

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.01200008	1.01199996 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	479	479 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.79980469	-7.79980469 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.9000001	2.9000001 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.76000023	3.75999999 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.89400005	4.89400005 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.79980469	-7.79980469 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.70 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	2.20000005
AssistFirewall ActiveKSV M str.K Uls f32	0.0099999978
AssistFirewall_ActiveRawAcc_Cnt_M_u16	7380
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.20000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	2.09537959
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.300000012
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.070000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.9000001
k_AsstFWInpLimitHFA_MtrNm_f32	5.80000019
k_AsstFWInpLimitHysComp_MtrNm_f32	7.5
k_AsstFWNstep_Cnt_u16	4674
k_AsstFWPstep_Cnt_u16	4920
k_RestoreThresh_MtrNm_f32	1.13999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288
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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6] t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1] t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240 -8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096 2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048   0
t2_AsstFWUprBoundX_HwNm_s4p11[7][8] t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-245/6 -22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-22528 -20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-12288
LZ ASSIEVVODIDOUIIGT IVILINIII S4DTIIOII/I	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-30720
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144
	4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	10240





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576
t_AsstFWDefltAssistX_HwNm_u8p8[0]	819
t_AsstFWDefltAssistX_HwNm_u8p8[1]	845 870
t_AsstFWDeftAssistX_HwNm_u8p8[2]	896
t_AsstFWDefltAssistX_HwNm_u8p8[3]	922
t_AsstFWDefltAssistX_HwNm_u8p8[4]	947
t_AsstFWDefltAssistX_HwNm_u8p8[5] t_AsstFWDefltAssistX_HwNm_u8p8[6]	973
t_AsstFWDefitAssistX_HwNm_u8p8[7]	998
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1024
t_AsstFWDefitAssistX_HwNm_u8p8[9]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1075
t_AsstFWDefitAssistX_HwNm_u8p8[11]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1126
t_AsstFWDefitAssistX_HwNm_u8p8[13]	1152
t_AsstFWDefitAssistX_HwNm_u8p8[14]	1178
t_AsstFWDefitAssistX_HwNm_u8p8[15]	1203
t_AsstFWDefitAssistX_HwNm_u8p8[15] t_AsstFWDefitAssistX_HwNm_u8p8[16]	1229
t_AsstFWDefitAssistX_HwNm_u8p8[16] t_AsstFWDefitAssistX_HwNm_u8p8[17]	1254
t_AsstFWDefitAssistX_HwNm_u8p8[17]  t_AsstFWDefitAssistX_HwNm_u8p8[18]	1280
t_AsstFWDefitAssistX_HwNm_u8p8[19]	1306
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	16179
t_AsstFWDefitAssistY_MtrNm_s4p11[1]	16384
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	16794
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	17408
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	17613
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	18022
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	18227
t AsstFWDefltAssistY MtrNm s4p11[11]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	18637
t AsstFWDefltAssistY MtrNm s4p11[13]	18842
t AsstFWDefltAssistY MtrNm s4p11[14]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	19251
t_AsstFWDefitAssistY_MtrNm_s4p11[16]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	19661
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	20070
t AsstFWPstepNstepThresh Cnt u16[0]	191
t_AsstFWPstepNstepThresh_Cnt_u16[1]	483
t_AsstFWVehSpd_Kph_u9p7[0]	33792
t_AsstFWVehSpd_Kph_u9p7[1]	33920
t_AsstFWVehSpd_Kph_u9p7[2]	34048
t_AsstFWVehSpd_Kph_u9p7[3]	34176
t_AsstFWVehSpd_Kph_u9p7[4]	34304
t AsstFWVehSpd Kph u9p7[5]	34432
t AsstFWVehSpd Kph u9p7[6]	34560
t_AsstFWVehSpd_Kph_u9p7[7]	34688
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	77.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
igi ilio iliot rip riodoti nomani. Addidi nowan i oli DadoAddidi Oliu WilliNIII IdZ	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
	- 19- 1000 II OWAII_I OF I_OOMOTION GOIGE_WITHIN_IOZ
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tot AssistFirewall Per1 Defeat AsstThl Service Cnt Inc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
togt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_It tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.17799997	2.17799997 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	483	483 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.70019531	8.70019531 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.46000004	4.46000004 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.06999969	6.07000017 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.80999994	6.80999994 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.70019531	8.70019531 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.71 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.099999
AssistFirewall ActiveKSV M str.K Uls f32	0.0199999996
AssistFirewall_ActiveRawAcc_Cnt_M_u16	7503
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.9000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.300000012
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.5
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0799999982
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4
k_AsstFWInpLimitHFA_MtrNm_f32	6
k_AsstFWInpLimitHysComp_MtrNm_f32	7.69999981
k_AsstFWNstep_Cnt_u16	2812
k_AsstFWPstep_Cnt_u16	1476
k_RestoreThresh_MtrNm_f32	1.14999998
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240





Name	Innut Value
Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0
t2_Asst WopiBoundX_HwNm_s4p11[7][8]	
	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-18432
	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-10240

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384 18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][10] 2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[5][1] 2	-26624
	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192 -6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144 4006
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	6144
12_AsstFWUprBoundY_MtrNm_s4p11[7][1]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	12288





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	26624
t_AsstFWDefltAssistX_HwNm_u8p8[0]	845 870
t_AsstFWDefltAssistX_HwNm_u8p8[1] t_AsstFWDefltAssistX_HwNm_u8p8[2]	896
t_AsstFWDefltAssistX_HwNm_u8p8[3]	922
t_AsstFWDefltAssistX_HwNm_u8p8[4]	947
t_AsstFWDefltAssistX_HwNm_u8p8[5]	973
t_AsstFWDefltAssistX_HwNm_u8p8[6]	998
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1331
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	17203 17408
t_AsstFWDefltAssistY_MtrNm_s4p11[5] t_AsstFWDefltAssistY_MtrNm_s4p11[6]	17613
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	18432
t AsstFWDefltAssistY MtrNm s4p11[11]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	20275
t_AsstFWPstepNstepThresh_Cnt_u16[0]	192
t_AsstFWPstepNstepThresh_Cnt_u16[1]	487
t_AsstFWVehSpd_Kph_u9p7[0]	36736
t_AsstFWVehSpd_Kph_u9p7[1]	36864
t_AsstFWVehSpd_Kph_u9p7[2]	36992
t_AsstFWVehSpd_Kph_u9p7[3]	37120
t_AsstFWVehSpd_Kph_u9p7[4]	37248
t_AsstFWVehSpd_Kph_u9p7[5]	37376
t_AsstFWVehSpd_Kph_u9p7[6]	37504 37632
t_AsstFWVehSpd_Kph_u9p7[7] tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.099999
tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	88.0699997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
	And Angiet Firewall Bord MEC Country Cot anyon
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.03799987	3.03800011 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	487	487 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8	8 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.47000027	6.46999979 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.05999994	4.05999994 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	0.852000058	0.851999998 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8	8 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

au				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	-
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	-

Test Step 2.72 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	3.099999
AssistFirewall ActiveKSV M str.K Uls f32	0.10000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	7626
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	-5,099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.7999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.090000036
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	6.19999981
k_AsstFWInpLimitHysComp_MtrNm_f32	0
k_AsstFWNstep_Cnt_u16	2688
k_AsstFWPstep_Cnt_u16	1599
k RestoreThresh MtrNm f32	1.15999997
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2 AsstFWUprBoundX HwNm s4p11[2][2]	
	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
, , , , , , , , , , , , , , , , , , , ,	
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2 AsstFWUprBoundX HwNm s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-22528
	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	
t2_Asst+WUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-18432
	-18432 -16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-16384 -14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-16384 -14336 -12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-16384 -14336

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432 20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096 -2048
	1-21/40
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0 2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0 2048 4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	0 2048 4096 6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	0 2048 4096 6144 8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0 2048 4096 6144 8192 10240 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	0 2048 4096 6144 8192 10240





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	22528 24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	870
t_AsstFWDefltAssistX_HwNm_u8p8[1]	896
t_AsstFWDefltAssistX_HwNm_u8p8[2]	922
t_AsstFWDefltAssistX_HwNm_u8p8[3]	947
t_AsstFWDefltAssistX_HwNm_u8p8[4]	973
t_AsstFWDefltAssistX_HwNm_u8p8[5]	998
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1101 1126
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1178
t_AsstFWDefitAssistX_HwNm_u8p8[13]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1357
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[5] t_AsstFWDefltAssistY_MtrNm_s4p11[6]	17613 17818
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[18] t_AsstFWDefltAssistY_MtrNm_s4p11[19]	20275 20480
t AsstFWPstepNstepThresh Cnt u16[0]	193
t_AsstFWPstepNstepThresh_Cnt_u16[1]	491
t_AsstFWVehSpd_Kph_u9p7[0]	39680
t_AsstFWVehSpd_Kph_u9p7[1]	39808
t_AsstFWVehSpd_Kph_u9p7[2]	39936
t_AsstFWVehSpd_Kph_u9p7[3]	40064
t_AsstFWVehSpd_Kph_u9p7[4]	40192
t_AsstFWVehSpd_Kph_u9p7[5]	40320
t_AsstFWVehSpd_Kph_u9p7[6]	40448
t_AsstFWVehSpd_Kph_u9p7[7]	40576
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.6500001
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1 2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	99.0500031
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.78999996	2.78999996 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	491	491 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.10009766	8.10009766 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.1500001	4.1500001 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5	5 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.82099986	1.82099998 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.10009766	8.10009766 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Τ			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.73 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.7999995
AssistFirewall ActiveKSV M str.K Uls f32	0.20000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	7749
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	-5.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.059999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.8999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall LwrBoundKSV M str.K Uls f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.10000001
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.1999981
k AsstFWInpLimitHFA MtrNm f32	6.4000001
k_AsstFWInpLimitHysComp_MtrNm_f32	8.80000019
k_AsstFWNstep_Cnt_u16	2564
k_AsstFWPstep_Cnt_u16	1722
k RestoreThresh MtrNm f32	1.16999996
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2 AsstFWUprBoundX HwNm s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2 AsstFWUprBoundX HwNm s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144
	1





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192 10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8] t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10] t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	8192
	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3] t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096 -2048
tz_AsstFWUprBoundX_HwNm_s4p11[7][4] t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
tz_AsstFWUprBoundX_HwNm_s4p11[7][5] t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-6144
	·

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5] t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-8192 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-6144 4006
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-4096 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-12288





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144 4006
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-4096 -2048
t2_Asst WopiBoundY_mitnin_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	896
t_AsstFWDefltAssistX_HwNm_u8p8[1]	922
t_AsstFWDefltAssistX_HwNm_u8p8[2]	947
t_AsstFWDefltAssistX_HwNm_u8p8[3]	973
t_AsstFWDefltAssistX_HwNm_u8p8[4]	998
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[11] t_AsstFWDefltAssistX_HwNm_u8p8[12]	1178 1203
t_AsstFWDefitAssistX_HwNm_u8p8[13]	1229
t_AsstFWDefitAssistX_HwNm_u8p8[14]	1254
t_AsstFWDefitAssistX_HwNm_u8p8[15]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1382
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[9] t_AsstFWDefltAssistY_MtrNm_s4p11[10]	18637 18842
t AsstFWDefltAssistY MtrNm s4p11[11]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	19251
t AsstFWDefltAssistY MtrNm s4p11[13]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	20685
t_AsstFWPstepNstepThresh_Cnt_u16[0]	194
t_AsstFWPstepNstepThresh_Cnt_u16[1]	495
t_AsstFWVehSpd_Kph_u9p7[0]	42624
t_AsstFWVehSpd_Kph_u9p7[1]	42752
t_AsstFWVehSpd_Kph_u9p7[2]	42880
t_AsstFWVehSpd_Kph_u9p7[3] t_AsstFWVehSpd_Kph_u9p7[4]	43008 43136
t_AsstFWVehSpd_Kph_u9p7[4] t_AsstFWVehSpd_Kph_u9p7[5]	43264
t_AsstFWVehSpd_Kph_u9p7[6]	43392
t_AsstFWVehSpd_Kph_u9p7[7]	43520
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.78000021
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-4
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	110.019997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.24000001	2.24000001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	495	495 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.20019531	8.20019531 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.87199974	4.87200022 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6	6 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.78999996	2.78999996 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.20019531	8.20019531 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Τ				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.74 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall ActiveKSV M str.K Uls f32	0.30000012
AssistFirewall_ActiveRawAcc_Cnt_M_u16	7872
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-5.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0700000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall LwrBoundKSV M str.K Uls f32	0.600000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.109999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.30000019
k AsstFWInpLimitHFA MtrNm f32	6.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	6.38000011
k_AsstFWNstep_Cnt_u16	2440
k_AsstFWPstep_Cnt_u16	1845
k RestoreThresh MtrNm f32	1.17999995
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2 AsstFWUprBoundX HwNm s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2 AsstFWUprBoundX HwNm s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192 10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336 16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1] t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0 2048
_	
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4] t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7] t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0] t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_Asst WoprboundX_1 wnn_s4p11[5][2] t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_Asst WuprBoundX_1 wwin_s4p11[5][4] t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_Asst WoprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2 AsstFWUprBoundX HwNm s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
t2 AsstFWUprBoundX HwNm s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2 AsstFWUprBoundX HwNm s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2 AsstFWUprBoundX HwNm s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-16384
12_ASSIFWOPIBOUND1_WILININ_S4p11[0][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-12288 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-12288





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	26624
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	28672
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	14336
	16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][6] 2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	
	18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
:2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	922
t_AsstFWDefltAssistX_HwNm_u8p8[1]	947
t_AsstFWDefltAssistX_HwNm_u8p8[2]	973
t_AsstFWDefltAssistX_HwNm_u8p8[3]	998
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	1178 1203
t_AsstFWDefitAssistX_HwNm_u8p8[12]	1229
t_AsstFWDefitAssistX_HwNm_u8p8[13]	1254
t_AsstFWDefitAssistX_HwNm_u8p8[14]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1382
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1408
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	18022 18227
t_AsstFWDefltAssistY_MtrNm_s4p11[6] t_AsstFWDefltAssistY_MtrNm_s4p11[7]	18432
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[19] t AsstFWPstepNstepThresh Cnt u16[0]	20890 195
t_AsstFWPstepNstepThresh_Cnt_u16[1]	499
t_AsstFWVehSpd_Kph_u9p7[0]	45568
t_AsstFWVehSpd_Kph_u9p7[1]	45696
t_AsstFWVehSpd_Kph_u9p7[2]	45824
t_AsstFWVehSpd_Kph_u9p7[3]	45952
t_AsstFWVehSpd_Kph_u9p7[4]	46080
t_AsstFWVehSpd_Kph_u9p7[5]	46208
t_AsstFWVehSpd_Kph_u9p7[6]	46336
t_AsstFWVehSpd_Kph_u9p7[7]	46464
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.90999985
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-6  1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	1 121.029999
tgt_AssistFirewall_Per1_verlicleSpeed_kpri_isz.value  tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall\_Per1



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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
z_AsstFWUprBoundX_HwNm_s4p11[3][9] 2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
2 AsstFWUprBoundX HwNm s4p11[5][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
2 AsstFWUprBoundX HwNm s4p11[5][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
z_AsstFWUprBoundY_MtrNm_s4p11[0][2] 2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-8192 C444
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-2048

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-0144
t2_Asst Wopiodulu1_MitNin_s4p11[1][0] t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9] t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144
t2_Asst WopiBoundY_MtrNm_s4p11[3][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3] t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_Asst WoprBoundY_MtrNm_s4p11[6][6]	10240
t2_Asst WopiBoundY_MtrNm_s4p11[6][7]	12288
t2_Asst WoprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432 -12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	-12288





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	947
t_AsstFWDefltAssistX_HwNm_u8p8[1]	973
t_AsstFWDefltAssistX_HwNm_u8p8[2]	998
t_AsstFWDefltAssistX_HwNm_u8p8[3]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1382
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1408
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1434
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	21094
t_AsstFWPstepNstepThresh_Cnt_u16[0]	196
t_AsstFWPstepNstepThresh_Cnt_u16[1]	503
t_AsstFWVehSpd_Kph_u9p7[0]	1408
t_AsstFWVehSpd_Kph_u9p7[1]	1536
t_AsstFWVehSpd_Kph_u9p7[2]	1664
t_AsstFWVehSpd_Kph_u9p7[3]	1792
t_AsstFWVehSpd_Kph_u9p7[4]	1920
t_AsstFWVehSpd_Kph_u9p7[5]	2048
t_AsstFWVehSpd_Kph_u9p7[6]	2176
t_AsstFWVehSpd_Kph_u9p7[7]	2304
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.03999996
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	132.039993
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_le	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
A DE LA A SAFE MA SAFE MEDIATE A SAFEN (CO.	A CATE III DA A LICHTE A CAMANI (CO
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_kte_inst_Ap_assist-irewaii.Assist-irewaii_Per1_HighFreqAssist_MitrNm_r32 tgt_kte_inst_Ap_assistFirewaii.AssistFirewaii_Per1_HwTorque_HwNm_r32	tgt_AssistFirewall_Per1_HighrreqAssist_MtrNm_132 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
,	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.91400003	2.91400003 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	503	503 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.43200004	1.43200004 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5	5 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.96799994	4.96799994 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.76 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.79999995
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8118
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.129999995
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.5
k_AsstFWInpLimitHFA_MtrNm_f32	8.80000019
k_AsstFWInpLimitHysComp_MtrNm_f32	6.38000011
k_AsstFWNstep_Cnt_u16	2192
k_AsstFWPstep_Cnt_u16	2091
k RestoreThresh MtrNm f32	2.21000004
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0
	<del>-</del>

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Assistriiewaii_Pei i		71040
Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096	
P_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0	
P_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240	
P_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336	
_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240	
	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096	
:_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048	
:_AsstFWUprBoundX_HwNm_s4p11[7][5]	0	
	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]		
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144	
P_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144	
	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5] 2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-4096 -2048	

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7.0019ti II OVAII_I OTT	
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-8192
:2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	
	-2048
I2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	2048
12_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-6144
Sk-pogua	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] t_AsstFWDefltAssistX_HwNm_u8p8[0]	128
t_AsstFWDefitAssistX_HwNm_u8p8[1]	154
t_AsstFWDefitAssistX_HwNm_u8p8[2]	179
t_AsstFWDefltAssistX_HwNm_u8p8[3]	205
t_AsstFWDefltAssistX_HwNm_u8p8[4]	230
t_AsstFWDefltAssistX_HwNm_u8p8[5]	256
t_AsstFWDefltAssistX_HwNm_u8p8[6]	282
t_AsstFWDefltAssistX_HwNm_u8p8[7]	307
t_AsstFWDefltAssistX_HwNm_u8p8[8]	333
t_AsstFWDefltAssistX_HwNm_u8p8[9]	358
t_AsstFWDefltAssistX_HwNm_u8p8[10]	384
t_AsstFWDefltAssistX_HwNm_u8p8[11]	410
t_AsstFWDefltAssistX_HwNm_u8p8[12]	435
t_AsstFWDefltAssistX_HwNm_u8p8[13]	461
t_AsstFWDefltAssistX_HwNm_u8p8[14]	486
t_AsstFWDefltAssistX_HwNm_u8p8[15]	512
t_AsstFWDefltAssistX_HwNm_u8p8[16]	538
t_AsstFWDefltAssistX_HwNm_u8p8[17]	563
t_AsstFWDefltAssistX_HwNm_u8p8[18]	589
t_AsstFWDefltAssistX_HwNm_u8p8[19]	614
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	17818 18022
t_AsstFWDefltAssistY_MtrNm_s4p11[3] t_AsstFWDefltAssistY_MtrNm_s4p11[4]	18227
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	18432
t_AsstFWDefitAssistY_MtrNm_s4p11[6]	18637
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	21299
t_AsstFWPstepNstepThresh_Cnt_u16[0]	197
t_AsstFWPstepNstepThresh_Cnt_u16[1]	507
t_AsstFWVehSpd_Kph_u9p7[0]	4352
t_AsstFWVehSpd_Kph_u9p7[1]	4480
t_AsstFWVehSpd_Kph_u9p7[2]	4608
t_AsstFWVehSpd_Kph_u9p7[3]	4736
t_AsstFWVehSpd_Kph_u9p7[4]	4864
t_AsstFWVehSpd_Kph_u9p7[5] t AsstFWVehSpd Kph_u9p7[6]	4992 5120
t_AsstFwvenSpd_kpn_u9p7[6] t_AsstFWVehSpd_kph_u9p7[7]	5120 5248
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.17000008
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	143.059998
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	-
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.51999998	2.51999998 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	507	507 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.26999998	4.26999998 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.5	5.5 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.51999998	1.51999998 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

au				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	•

Test Step 2.77 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall ActiveKSV M str.K Uls f32	0.20000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8241
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	-5.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.059999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.8999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall LwrBoundKSV M str.K Uls f32	0.60000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.140000001
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.5999999
k AsstFWInpLimitHFA MtrNm f32	3,20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	6.48999977
k_AsstFWNstep_Cnt_u16	2812
k_AsstFWPstep_Cnt_u16	2214
k RestoreThresh MtrNm f32	2.2200003
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2 AsstFWUprBoundX HwNm s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2 AsstFWUprBoundX HwNm s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384
= =	1.00

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Assistrirewaii_Peri		( MAC) (MI
Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192	
	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]		
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048	
2 AsstFWUprBoundX HwNm s4p11[6][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048	
, , , , , ,		
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048	
	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]		
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192	
. – , ,	-6144	
2 AsstFWUprBoundY MtrNm s4p11[0][3]		
	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096 -2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3] 2_AsstFWUprBoundY_MtrNm_s4p11[0][4] 2_AsstFWUprBoundY_MtrNm_s4p11[0][5] 2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-4096 -2048 0	





Name	Innut Value
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0
	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
A A FIAM D. D. ALAND A AMERICA	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
	10240
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
:_AsstFWDefitAssistX_HwNm_u8p8[0]	26
t_AsstFWDefltAssistX_HwNm_u8p8[1]	51
:_AsstFWDefltAssistX_HwNm_u8p8[2]	77
: AsstFWDefitAssistX_HwNm_u8p8[3]	102
: AsstFWDefitAssistX_HwNm_u8p8[4]	128
, , ,	
:_AsstFWDefitAssistX_HwNm_u8p8[5]	154
:_AsstFWDefitAssistX_HwNm_u8p8[6]	179
t_AsstFWDefltAssistX_HwNm_u8p8[7]	205
t_AsstFWDefltAssistX_HwNm_u8p8[8]	230
t_AsstFWDefltAssistX_HwNm_u8p8[9]	256
t_AsstFWDefltAssistX_HwNm_u8p8[10]	282
t_AsstFWDefltAssistX_HwNm_u8p8[11]	307
t_AsstFWDefltAssistX_HwNm_u8p8[12]	333
t_AsstFWDefltAssistX_HwNm_u8p8[13]	358
t_AsstFWDefltAssistX_HwNm_u8p8[14]	384
:_AsstFWDefltAssistX_HwNm_u8p8[15]	410
t_AsstFWDefltAssistX_HwNm_u8p8[16]	435
t_AsstFWDefltAssistX_HwNm_u8p8[17]	461
t_AsstFWDefltAssistX_HwNm_u8p8[18]	486
t_AsstFWDefltAssistX_HwNm_u8p8[19]	512
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	20070
t_AsstFWDefitAssistY_MtrNm_s4p11[13]	20275
· · ·	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[14] t_AsstFWDefltAssistY_MtrNm_s4p11[15]	20685
t_AsstFWDefitAssistY_MtrNm_s4p11[16]	20890
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	21504
t_AsstFWPstepNstepThresh_Cnt_u16[0]	198
t_AsstFWPstepNstepThresh_Cnt_u16[1]	511
t_AsstFWVehSpd_Kph_u9p7[0]	7296
t_AsstFWVehSpd_Kph_u9p7[1]	7424
t_AsstFWVehSpd_Kph_u9p7[2]	7552
t_AsstFWVehSpd_Kph_u9p7[3]	7680
:_AsstFWVehSpd_Kph_u9p7[4]	7808
:_AsstFWVehSpd_Kph_u9p7[5]	7936
t_AsstFWVehSpd_Kph_u9p7[6]	8064
t_AsstFWVehSpd_Kph_u9p7[7]	8192
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.30000019
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
gt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.39999998
gt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8
gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	154.300003
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_It	
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	
• • • • • • • • • • • • • • • • • • • •	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
AN AIR THE THE ACCIDING ACCIDING ACCIDING PART VARIABLE ACCIDING AND AND	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

2015-03-23, 11:55:49+0530



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.87999995	0.879999995 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	511	511 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.454	5.454 ± 4.88E-04	<b>~</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.19999981	5.19999981 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>~</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.55999994	2.55999994 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.87999995	0.879999995 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>~</b>
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	<b>~</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.78 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.099999
AssistFirewall ActiveKSV M str.K Uls f32	0.30000012
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8364
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall CombAsstSV MtrNm M f32	-5.6999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.070000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall LwrBoundKSV M str.K Uls f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.150000006
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	0
k AsstFWInpLimitHFA MtrNm f32	1
k_AsstFWInpLimitHysComp_MtrNm_f32	6.5999999
k_AsstFWNstep_Cnt_u16	2688
k_AsstFWPstep_Cnt_u16	2337
k RestoreThresh MtrNm f32	2.23000002
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336





Namo	Input Value
Name  t2 AcctEW/ In Round Y. Hwblm, c4n41[2][1]	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-14336
t2_Asst WopiboundX_1WNin_s4p11[4][0] t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192
t2_Asst Wopibound1_ivitNin_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144
	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432
	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528 24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	22528 24576 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528 24576 -6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	22528 24576 -6144





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	51
t_AsstFWDefltAssistX_HwNm_u8p8[1]	77
t_AsstFWDefltAssistX_HwNm_u8p8[2]	102
t_AsstFWDefltAssistX_HwNm_u8p8[3]	128
t_AsstFWDefltAssistX_HwNm_u8p8[4]	154
t_AsstFWDefltAssistX_HwNm_u8p8[5]	179
t_AsstFWDefltAssistX_HwNm_u8p8[6]	205
t_AsstFWDefltAssistX_HwNm_u8p8[7]	230
t_AsstFWDefltAssistX_HwNm_u8p8[8]	256
t_AsstFWDefltAssistX_HwNm_u8p8[9]	282
t_AsstFWDefltAssistX_HwNm_u8p8[10]	307
t_AsstFWDefltAssistX_HwNm_u8p8[11]	333
t_AsstFWDefltAssistX_HwNm_u8p8[12]	358
t_AsstFWDefltAssistX_HwNm_u8p8[13]	384
t_AsstFWDefltAssistX_HwNm_u8p8[14]	410
t_AsstFWDefltAssistX_HwNm_u8p8[15]	435
t_AsstFWDefltAssistX_HwNm_u8p8[16]	461
t_AsstFWDefltAssistX_HwNm_u8p8[17] t_AsstFWDefltAssistX_HwNm_u8p8[18]	486 512
t_AsstFWDefitAssistX_mwNrri_uopo[16]  t AsstFWDefitAssistX HwNm_u8p8[19]	538
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[19] t AsstFWPstepNstepThresh Cnt u16[0]	21709 199
t_AsstFWPstepNstepThresh_Cnt_u16[1]	515
t_AsstFWVehSpd_Kph_u9p7[0]	10240
t_AsstFWVehSpd_Kph_u9p7[1]	10368
t_AsstFWVehSpd_Kph_u9p7[2]	10496
t_AsstFWVehSpd_Kph_u9p7[3]	10624
t_AsstFWVehSpd_Kph_u9p7[4]	10752
t_AsstFWVehSpd_Kph_u9p7[5]	10880
t_AsstFWVehSpd_Kph_u9p7[6]	11008
t_AsstFWVehSpd_Kph_u9p7[7]	11136
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.42999983
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.70000005
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	165.100006
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	1 -
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.16999984	2.17000008 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	515	515 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.09299994	6.09299994 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.4000001	3.4000001 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.70000005	2.70000005 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

T			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.79 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.79999995
AssistFirewall ActiveKSV M str.K Uls f32	0.0599999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.159999996
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	8.80000019
k_AsstFWInpLimitHFA_MtrNm_f32	2
k_AsstFWInpLimitHysComp_MtrNm_f32	6.69999981
k_AsstFWNstep_Cnt_u16	2564
k_AsstFWPstep_Cnt_u16	1476
k_RestoreThresh_MtrNm_f32	2.24000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	18432
t2 AsstFWUprBoundX HwNm s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
and the proposition of the first of	0400
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144 -4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144 -4096 -2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-6144 -4096 -2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144 -4096 -2048 0

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-14336
2 AsstFWUprBoundY MtrNm s4p11[2][7]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-10240
z_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-8192
	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-6144 -6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144 -4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-10240
2 AsstFWUprBoundY MtrNm s4p11[5][2]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	77
t_AsstFWDefltAssistX_HwNm_u8p8[1]	102
t_AsstFWDefltAssistX_HwNm_u8p8[2]	128
t_AsstFWDefltAssistX_HwNm_u8p8[3]	154 179
t_AsstFWDefltAssistX_HwNm_u8p8[4] t_AsstFWDefltAssistX_HwNm_u8p8[5]	205
t_AsstFWDefltAssistX_HwNm_u8p8[6]	230
t_AsstFWDefltAssistX_HwNm_u8p8[7]	256
t_AsstFWDefltAssistX_HwNm_u8p8[8]	282
t_AsstFWDefltAssistX_HwNm_u8p8[9]	307
t_AsstFWDefltAssistX_HwNm_u8p8[10]	333
t_AsstFWDefltAssistX_HwNm_u8p8[11]	358
t_AsstFWDefltAssistX_HwNm_u8p8[12]	384
t_AsstFWDefltAssistX_HwNm_u8p8[13]	410
t_AsstFWDefltAssistX_HwNm_u8p8[14]	435
t_AsstFWDefltAssistX_HwNm_u8p8[15]	461
t_AsstFWDefltAssistX_HwNm_u8p8[16]	486
t_AsstFWDefltAssistX_HwNm_u8p8[17]	512
t_AsstFWDefltAssistX_HwNm_u8p8[18]	538
t_AsstFWDefltAssistX_HwNm_u8p8[19]	563
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[7] t_AsstFWDefltAssistY_MtrNm_s4p11[8]	19456 19661
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	21914
t_AsstFWPstepNstepThresh_Cnt_u16[0]	200
t_AsstFWPstepNstepThresh_Cnt_u16[1]	519
t_AsstFWVehSpd_Kph_u9p7[0]	13184
t_AsstFWVehSpd_Kph_u9p7[1]	13312
t_AsstFWVehSpd_Kph_u9p7[2]	13440
t_AsstFWVehSpd_Kph_u9p7[3]	13568
t_AsstFWVehSpd_Kph_u9p7[4]	13696
t_AsstFWVehSpd_Kph_u9p7[5]	13824
t_AsstFWVehSpd_Kph_u9p7[6]	13952
t_AsstFWVehSpd_Kph_u9p7[7] tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	14080 5.55999994
tgt_AssistFirewall_Per1_BaseAssistCmd_intrinm_132.value  tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgc.value	5.55999994
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2.5999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_le	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall\_Per1

Status\_Cnt\_T\_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.63199997	2.63199997 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	519	519 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.68479991	1.68480003 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.5	3.5 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4	4 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>

T .				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	_

0x01

0x01

Test Step 2.80 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall ActiveKSV M str.K Uls f32	0.019999996
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8610
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.9000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.029999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	2
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.60000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.170000002
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.5
k_AsstFWInpLimitHFA_MtrNm_f32	3
k_AsstFWInpLimitHysComp_MtrNm_f32	6.80000019
k_AsstFWNstep_Cnt_u16	2440
k_AsstFWPstep_Cnt_u16	1599
k_RestoreThresh_MtrNm_f32	2.25
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2 AsstFWUprBoundX HwNm s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2040
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096

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2_AsstFWUprBoundY_MtrNm_s4p11[0][8] 2_AsstFWUprBoundY_MtrNm_s4p11[0][9] 2_AsstFWUprBoundY_MtrNm_s4p11[0][10] 2_AsstFWUprBoundY_MtrNm_s4p11[1][0] 2_AsstFWUprBoundY_MtrNm_s4p11[1][1] 2_AsstFWUprBoundY_MtrNm_s4p11[1][2] 2_AsstFWUprBoundY_MtrNm_s4p11[1][3] 2_AsstFWUprBoundY_MtrNm_s4p11[1][4] 2_AsstFWUprBoundY_MtrNm_s4p11[1][6] 2_AsstFWUprBoundY_MtrNm_s4p11[1][6] 2_AsstFWUprBoundY_MtrNm_s4p11[1][6] 2_AsstFWUprBoundY_MtrNm_s4p11[1][7] 2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	10240 12288 14336 -6144 -4096 -2048 0 2048 4096 6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][10] 2_AsstFWUprBoundY_MtrNm_s4p11[1][0] 2_AsstFWUprBoundY_MtrNm_s4p11[1][1] 2_AsstFWUprBoundY_MtrNm_s4p11[1][2] 2_AsstFWUprBoundY_MtrNm_s4p11[1][3] 2_AsstFWUprBoundY_MtrNm_s4p11[1][4] 2_AsstFWUprBoundY_MtrNm_s4p11[1][5] 2_AsstFWUprBoundY_MtrNm_s4p11[1][6] 2_AsstFWUprBoundY_MtrNm_s4p11[1][6] 2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336 -6144 -4096 -2048 0 2048 4096 6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][0] 2_AsstFWUprBoundY_MtrNm_s4p11[1][1] 2_AsstFWUprBoundY_MtrNm_s4p11[1][2] 2_AsstFWUprBoundY_MtrNm_s4p11[1][3] 2_AsstFWUprBoundY_MtrNm_s4p11[1][4] 2_AsstFWUprBoundY_MtrNm_s4p11[1][5] 2_AsstFWUprBoundY_MtrNm_s4p11[1][6] 2_AsstFWUprBoundY_MtrNm_s4p11[1][6] 2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-6144 -4096 -2048 0 2048 4096 6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][1] 2_AsstFWUprBoundY_MtrNm_s4p11[1][2] 2_AsstFWUprBoundY_MtrNm_s4p11[1][3] 2_AsstFWUprBoundY_MtrNm_s4p11[1][4] 2_AsstFWUprBoundY_MtrNm_s4p11[1][5] 2_AsstFWUprBoundY_MtrNm_s4p11[1][6] 2_AsstFWUprBoundY_MtrNm_s4p11[1][6] 2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-4096 -2048 0 2048 4096 6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][2] 2_AsstFWUprBoundY_MtrNm_s4p11[1][3] 2_AsstFWUprBoundY_MtrNm_s4p11[1][4] 2_AsstFWUprBoundY_MtrNm_s4p11[1][5] 2_AsstFWUprBoundY_MtrNm_s4p11[1][6] 2_AsstFWUprBoundY_MtrNm_s4p11[1][6] 2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-2048 0 2048 4096 6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]  2_AsstFWUprBoundY_MtrNm_s4p11[1][4]  2_AsstFWUprBoundY_MtrNm_s4p11[1][5]  2_AsstFWUprBoundY_MtrNm_s4p11[1][6]  2_AsstFWUprBoundY_MtrNm_s4p11[1][6]  2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0 2048 4096 6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][4] 2_AsstFWUprBoundY_MtrNm_s4p11[1][5] 2_AsstFWUprBoundY_MtrNm_s4p11[1][6] 2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	2048 4096 6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][5] 2_AsstFWUprBoundY_MtrNm_s4p11[1][6] 2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	4096 6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][6] 2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	
2 AsstFWUprBoundY MtrNm s4p11[1][8]	8192
	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-16384
	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][6] 2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-12288 -10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
:2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	0
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
	4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][2] 2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144

AssistFirewall\_Per1





6
3
Firewall_Per1_AsstFirewallActive_Uls_f32
Firewall_Per1_BaseAssistCmd_MtrNm_f32
Firewall_Per1_CombinedAssist_MtrNm_f32
Firewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
Firewall_Per1_HighFreqAssist_MtrNm_f32
Firewall_Per1_HwTorque_HwNm_f32
Firewall_Per1_HysteresisComp_MtrNm_f32
Firewall_Per1_MEC_Counter_Cnt_enum Firewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.07800007	1.07799995 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	523	523 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.35900009	1.35899997 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.79999971	2.79999995 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5	5 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

Τ				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_ActiveKSV_M str.K Uls f32	0.10000002
AssistFirewall_ActiveRov_ivi_str.n_0is_i32 AssistFirewall_ActiveRawAcc_Cnt_M_u16	0
AssistFirewall_ActiveRawAcc_Cit_ivi_u16 AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall_AssixeducedFellSv_Cht_M_gc AssistFirewall CombAsstSV MtrNm M f32	-6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LFF_Str.K_Uls_f32	0.050000007
•	1.7999995
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.029999993
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
<_AsstFWInpLimitBaseAsst_MtrNm_f32	2.0999999
<_AsstFWInpLimitHFA_MtrNm_f32	3.29999995
<_AsstFWInpLimitHysComp_MtrNm_f32	3.9000001
k_AsstFWNstep_Cnt_u16	3690
<_AsstFWPstep_Cnt_u16	2706
x_RestoreThresh_MtrNm_f32	2.25999999
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192

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ASSISTITEWAII_Pet I	
Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
:2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
2 AsstFWUprBoundX HwNm s4p11[5][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
2 AsstFWUprBoundX HwNm s4p11[6][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
, , , , , , , , , , , , , , , , , , , ,	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
P_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
P_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
P_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
	16384
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	8192
	10240
:2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	18432
t2_Asst Wopibound1_intrini_s4p11[1][10] t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
t2_Asst Wopibound1_intrini_s4p11[4][6] t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
tz_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
	14336
t2 AsstEWUnrBoundy MtrNm s4n11161171	
	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	18432 20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432 20480 8192





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	128
t_AsstFWDefltAssistX_HwNm_u8p8[1]	154 179
t_AsstFWDefltAssistX_HwNm_u8p8[2]	
t_AsstFWDefltAssistX_HwNm_u8p8[3]	205
t_AsstFWDefltAssistX_HwNm_u8p8[4]	
t_AsstFWDefltAssistX_HwNm_u8p8[5]	256 282
t_AsstFWDefltAssistX_HwNm_u8p8[6]	307
t_AsstFWDefltAssistX_HwNm_u8p8[7] t_AsstFWDefltAssistX_HwNm_u8p8[8]	333
t_AsstFWDefitAssistX_HwNm_u8p8[9]	358
t_AsstFWDefitAssistX_HwNm_u8p8[10]	384
t_AsstFWDefitAssistX_HwNm_u8p8[11]	410
	435
t_AsstFWDefltAssistX_HwNm_u8p8[12] t_AsstFWDefltAssistX_HwNm_u8p8[13]	461
t_AsstFWDefitAssistX_HwNm_u8p8[13] t AsstFWDefitAssistX HwNm_u8p8[14]	486
, , ,	512
t_AsstFWDefltAssistX_HwNm_u8p8[15]	538
t_AsstFWDefltAssistX_HwNm_u8p8[16]	538 563
t_AsstFWDefltAssistX_HwNm_u8p8[17] t_AsstFWDefltAssistX_HwNm_u8p8[18]	589
t_AsstFWDefitAssistX_HwNm_u8p8[18]  t_AsstFWDefitAssistX_HwNm_u8p8[19]	614
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	18637
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	18842
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	19046
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	19251
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	19661
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	19866
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	20480
t AsstFWDefltAssistY MtrNm s4p11[11]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	20890
t AsstFWDefltAssistY MtrNm s4p11[13]	21094
t AsstFWDefltAssistY MtrNm s4p11[14]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	22323
t AsstFWPstepNstepThresh Cnt u16[0]	202
t_AsstFWPstepNstepThresh_Cnt_u16[1]	527
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t AsstFWVehSpd Kph u9p7[5]	19712
t AsstFWVehSpd Kph u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	123.099998
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
.goot_rp_rootet irewaii.rootet irewaii_r et r_continiiteurootet [vittlviii_132	1
tot Rte Inst An AssistFirewall AssistFirewall Per1 Defeat AsstThi Service Cot I	: ST. 1000 HOWAIL OF LEGICAL MOST DILOG VICE_OFF.
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	tot AssistFirewall Per1 HighFreqAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	,

AssistFirewall\_Per1



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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288 14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-1643Z -16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_Asst WoprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_Asst WoprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_Asst WoprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10] t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1] t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2046
t2_AsstFWUprBoundX_HwNm_s4p11[4][3] t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2 AsstFWUprBoundX HwNm s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
tz_Assti Wopibodila i _witi viii_s+p i i[o][+]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
	10240 12288





Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-6144
	-6144 -4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-4096 -2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
2_A55ti WOpibounu i_WithMin_54p i i jojj 51	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	





	lw.
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	-2040 0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	154
t_AsstFWDefltAssistX_HwNm_u8p8[1]	179
t_AsstFWDefltAssistX_HwNm_u8p8[2]	205
t_AsstFWDefltAssistX_HwNm_u8p8[3]	230
t_AsstFWDefltAssistX_HwNm_u8p8[4]	256
t_AsstFWDefltAssistX_HwNm_u8p8[5]	282
t_AsstFWDefltAssistX_HwNm_u8p8[6]	307
t_AsstFWDefltAssistX_HwNm_u8p8[7]	333
t_AsstFWDefltAssistX_HwNm_u8p8[8]	358
t_AsstFWDefltAssistX_HwNm_u8p8[9]	384
t_AsstFWDefltAssistX_HwNm_u8p8[10]	410
t_AsstFWDefltAssistX_HwNm_u8p8[11]	435
t_AsstFWDefltAssistX_HwNm_u8p8[12]	461
t_AsstFWDefltAssistX_HwNm_u8p8[13]	486
t_AsstFWDefltAssistX_HwNm_u8p8[14]	512
t_AsstFWDefltAssistX_HwNm_u8p8[15]	538
t_AsstFWDefltAssistX_HwNm_u8p8[16]	563
t_AsstFWDefltAssistX_HwNm_u8p8[17]	589
t_AsstFWDefltAssistX_HwNm_u8p8[18]	614
t_AsstFWDefltAssistX_HwNm_u8p8[19]	640
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	22528
t_AsstFWPstepNstepThresh_Cnt_u16[0]	203
t_AsstFWPstepNstepThresh_Cnt_u16[1]	531
t_AsstFWVehSpd_Kph_u9p7[0]	22016
t_AsstFWVehSpd_Kph_u9p7[1]	22144
t_AsstFWVehSpd_Kph_u9p7[2]	22272
t_AsstFWVehSpd_Kph_u9p7[3] t_AsstFWVehSpd_Kph_u9p7[4]	22400 22528
t_AsstFWVehSpd_Kph_u9p7[5]	22656
t_AsstFWVehSpd_Kph_u9p7[6]	22784 22912
t_AsstFWVehSpd_Kph_u9p7[7] tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	22912
tgt_AssistFirewall_Per1_BaseAssistCmd_intrinm_132.value  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	234.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
	tgt_AssistFirewall_Per1_Defeat_Asst1bl Service Cnt lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lq	· ·
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_letgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-7.03999996	-7.03999996 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	531	531 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.42399979	5.42399979 ± 4.88E-04	<b>~</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.55000019	7.55000019 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>~</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.01599979	4.01599979 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.83 (Repeat Count = 1)	v
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall ActiveKSV M str.K Uls f32	0.300000012
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1000
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	6.099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.070000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.600000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.109999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4
k_AsstFWInpLimitHFA_MtrNm_f32	1.3999998
k_AsstFWInpLimitHysComp_MtrNm_f32	4.0999999
k_AsstFWNstep_Cnt_u16	2812
k_AsstFWPstep_Cnt_u16	1968
k_RestoreThresh_MtrNm_f32	2.27999997
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_Asst WopiBoundX_HwNm_s4p11[5][1] t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6] t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][9] t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	6144 -12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	
	10240





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432 20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528
	24576
t2 AsstFWUprBoundY MtrNm s4p11[6][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	179
t_AsstFWDefltAssistX_HwNm_u8p8[1]	205
t_AsstFWDefltAssistX_HwNm_u8p8[2]	230
t_AsstFWDefltAssistX_HwNm_u8p8[3]	256 282
t_AsstFWDefltAssistX_HwNm_u8p8[4]	307
t_AsstFWDefltAssistX_HwNm_u8p8[5]	333
t_AsstFWDefltAssistX_HwNm_u8p8[6]	358
t_AsstFWDefltAssistX_HwNm_u8p8[7] t_AsstFWDefltAssistX_HwNm_u8p8[8]	384
t_AsstFWDefitAssistX_HwNm_u8p8[9]	410
t_AsstFWDefltAssistX_HwNm_u8p8[10]	435
t_AsstFWDefitAssistX_HwNm_u8p8[11]	461
t_AsstFWDefltAssistX_HwNm_u8p8[12]	486
t AsstFWDefitAssistX HwNm u8p8[13]	512
t_AsstFWDefitAssistX_HwNm_u8p8[14]	538
t_AsstFWDefitAssistX_HwNm_u8p8[14]  t_AsstFWDefitAssistX_HwNm_u8p8[15]	563
t_AsstFWDefitAssistX_HwNm_u8p8[15]  t_AsstFWDefitAssistX_HwNm_u8p8[16]	589
t_AsstFWDefitAssistX_HwNm_u8p8[17]	614
t_AsstFWDefitAssistX_HwNm_u8p8[17]  t_AsstFWDefitAssistX_HwNm_u8p8[18]	640
t_AsstFWDefltAssistX_HwNm_u8p8[19]	666
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	19046
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	19456
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	20070
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	20890
t AsstFWDefltAssistY MtrNm s4p11[11]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	21299
t AsstFWDefltAssistY MtrNm s4p11[13]	21504
t AsstFWDefltAssistY MtrNm s4p11[14]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	21914
t AsstFWDefltAssistY MtrNm s4p11[16]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	22733
t AsstFWPstepNstepThresh Cnt u16[0]	204
t_AsstFWPstepNstepThresh_Cnt_u16[1]	535
t_AsstFWVehSpd_Kph_u9p7[0]	24960
t_AsstFWVehSpd_Kph_u9p7[1]	25088
t_AsstFWVehSpd_Kph_u9p7[2]	25216
t_AsstFWVehSpd_Kph_u9p7[3]	25344
t_AsstFWVehSpd_Kph_u9p7[4]	25472
t AsstFWVehSpd Kph u9p7[5]	25600
t AsstFWVehSpd Kph u9p7[6]	25728
t_AsstFWVehSpd_Kph_u9p7[7]	25856
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4,0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	77.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	•
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
5 T T_ T_ T_ T_ T_ T_ T_ T_ T_ T	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt Rte Inst Ap AssistFirewall.AssistFirewall Per1 HwTorque HwNm f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tct Rte Inst Ap AssistFirewall.AssistFirewall Per1 HysteresisComp MtrNm f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.769999981	0.769999981 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0	0 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.33099985	6.33099985 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.399999619	0.400000006 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8.32999992	8.32999992 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.769999981	0.769999981 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.84 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.099999
AssistFirewall ActiveKSV M str.K Uls f32	0.0599999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	200
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	6.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.119999997
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	1.5
k_AsstFWInpLimitHysComp_MtrNm_f32	4.30000019
k_AsstFWNstep_Cnt_u16	2688
k_AsstFWPstep_Cnt_u16	2091
k_RestoreThresh_MtrNm_f32	2.28999996
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_Asst WopiBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_Asst WorlboundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	16384
==	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288
	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	26624
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	26624
:2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_Asst WopiBoundY_MtrNm_s4p11[7][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	205
t_AsstFWDefltAssistX_HwNm_u8p8[1]	230
t_AsstFWDefltAssistX_HwNm_u8p8[2]	256
t_AsstFWDefltAssistX_HwNm_u8p8[3]	282
t_AsstFWDefltAssistX_HwNm_u8p8[4]	307
t_AsstFWDefltAssistX_HwNm_u8p8[5]	333
t_AsstFWDefltAssistX_HwNm_u8p8[6]	358
t_AsstFWDefltAssistX_HwNm_u8p8[7]	384
t_AsstFWDefltAssistX_HwNm_u8p8[8]	410
t_AsstFWDefltAssistX_HwNm_u8p8[9]	435
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	461 486
t_AsstFWDefltAssistX_HwNm_u8p8[12]	512
t AsstFWDefltAssistX HwNm u8p8[13]	538
t_AsstFWDefltAssistX_HwNm_u8p8[14]	563
t_AsstFWDefltAssistX_HwNm_u8p8[15]	589
t_AsstFWDefltAssistX_HwNm_u8p8[16]	614
t_AsstFWDefltAssistX_HwNm_u8p8[17]	640
t_AsstFWDefltAssistX_HwNm_u8p8[18]	666
t_AsstFWDefltAssistX_HwNm_u8p8[19]	691
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	20070 20275
t_AsstFWDefltAssistY_MtrNm_s4p11[6] t_AsstFWDefltAssistY_MtrNm_s4p11[7]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	20685
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	22733
t_AsstFWDefltAssistY_MtrNm_s4p11[19] t AsstFWPstepNstepThresh Cnt u16[0]	22938
t_AsstFWPstepNstepThresh_Cnt_u16[1]	0
t_AsstFWVehSpd_Kph_u9p7[0]	27904
t_AsstFWVehSpd_Kph_u9p7[1]	28032
t_AsstFWVehSpd_Kph_u9p7[2]	28160
t_AsstFWVehSpd_Kph_u9p7[3]	28288
t_AsstFWVehSpd_Kph_u9p7[4]	28416
t_AsstFWVehSpd_Kph_u9p7[5]	28544
t_AsstFWVehSpd_Kph_u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7]	28800
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5 2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	88.1999969
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.91400003	2.91400003 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0	0 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.71199989	1.71200001 ± 4.88E-04	<b>~</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.199999809	0.200000003 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>~</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.0480001	2.0480001 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x00	0x00	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Τ					
Actual Function	Count	Expected Function	Count	Result	
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~	
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>	
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	-	
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>	
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	_	

Test Step 2.85 (Repeat Count = 1)	<u> </u>
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.79999995
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	344
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	6.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.7999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.129999995
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.19999981
k_AsstFWInpLimitHFA_MtrNm_f32	1.70000005
k_AsstFWInpLimitHysComp_MtrNm_f32	4.5
k_AsstFWNstep_Cnt_u16	2564
k_AsstFWPstep_Cnt_u16	2214
k_RestoreThresh_MtrNm_f32	3.30999994
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5] t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240 12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-0144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6] t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9] t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_Asst WuprBoundX_HwNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
t2 AsstFWUprBoundX HwNm s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
t2_AsstFWUprBoundX_rwNin_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_Asst WopfboundX_1wNin_s4p11[6][10]	12288
t2_Asst WopfBoundX_1WNm_s4p11[0][10]	-12288
t2_Asst WopfboundX_1wNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_Asst WopfboundX_1wNin_s4p11[7][2]	-6144
t2_Asst WopiboundX_1wNin_s4p11[7][3]	-4096
t2_Asst WopfboundX_1wNin_s4p11[7][4]	-2048
t2_Asst WopibodidA_riwidii_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	16384
t2_AsstrWUprBoundY_MtrNm_s4p11[0][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	20480





Input Value
22528
24576
26624
-8192
-6144
-4096
-2048
0
2048
4096
6144 8192
10240
12288
-14336
-12288
-10240
-8192
-6144
-4096
-2048
0
2048
4096
6144
-16384
-14336
-12288
-10240
-8192
-6144
-4096
-2048
0
2048
4096
-30720 -28672
-26624
-24576
-22528
-20480
-18432
-16384
-14336
-12288
-10240
2048
4096
6144
8192
10240
12288
14336
16384
18432
20480
22528
8192
10240
12288
14336
16384
18432 20480
20480 22528
LEGEU
24576
24576 26624
24576 26624 28672
24576 26624 28672 -10240
24576 26624 28672





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefltAssistX_HwNm_u8p8[0]	230
t_AsstFWDefltAssistX_HwNm_u8p8[1]	256
t_AsstFWDefltAssistX_HwNm_u8p8[2]	282
t_AsstFWDefltAssistX_HwNm_u8p8[3]	307
t_AsstFWDefltAssistX_HwNm_u8p8[4]	333
t_AsstFWDefltAssistX_HwNm_u8p8[5]	358
t_AsstFWDefltAssistX_HwNm_u8p8[6]	384
t_AsstFWDefltAssistX_HwNm_u8p8[7]	410
t_AsstFWDefltAssistX_HwNm_u8p8[8]	435
t_AsstFWDefltAssistX_HwNm_u8p8[9]	461
t_AsstFWDefltAssistX_HwNm_u8p8[10]	486
t_AsstFWDefltAssistX_HwNm_u8p8[11]	512
t_AsstFWDefltAssistX_HwNm_u8p8[12]	538
t_AsstFWDefltAssistX_HwNm_u8p8[13]	563
t_AsstFWDefltAssistX_HwNm_u8p8[14]	589
t_AsstFWDefltAssistX_HwNm_u8p8[15]	614
t_AsstFWDefltAssistX_HwNm_u8p8[16]	640
t_AsstFWDefltAssistX_HwNm_u8p8[17]	666
t_AsstFWDefltAssistX_HwNm_u8p8[18]	691
t_AsstFWDefltAssistX_HwNm_u8p8[19]	717
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	19251 19456
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[2] t_AsstFWDefltAssistY_MtrNm_s4p11[3]	19866
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	20070
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	20275
t_AsstFWDefitAssistY_MtrNm_s4p11[6]	20480
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	20685
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	22733
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	22938
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	23142
t_AsstFWPstepNstepThresh_Cnt_u16[0]	5000
t_AsstFWPstepNstepThresh_Cnt_u16[1]	5000
t_AsstFWVehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1]	30976
t_AsstFWVehSpd_Kph_u9p7[2]	31104
t_AsstFWVehSpd_Kph_u9p7[3]	31232
t_AsstFWVehSpd_Kph_u9p7[4]	31360
t_AsstFWVehSpd_Kph_u9p7[5]	31488
t_AsstFWVehSpd_Kph_u9p7[6]	31616
t_AsstFWVehSpd_Kph_u9p7[7]	31744
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.6500001
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	99.3000031
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lq	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	·
	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	

AssistFirewall\_Per1







7.666ti ii ewaii_i et i	( Table 10 A
Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-6144
	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_riwNin_s4p11[0][10]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	
	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	22528
	1





	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	26624
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	28672
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	2048
	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048
	4096
2 Asst-WuprBoundy MtrNm s4p11[6][10]	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192 -6144
	-8192 -6144 -4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefitAssistX_HwNm_u8p8[0]	256
t_AsstFWDefltAssistX_HwNm_u8p8[1]	282
t_AsstFWDefltAssistX_HwNm_u8p8[2]	307
t_AsstFWDefltAssistX_HwNm_u8p8[3]	333
t_AsstFWDefltAssistX_HwNm_u8p8[4]	358
t_AsstFWDefltAssistX_HwNm_u8p8[5]	384
t_AsstFWDefltAssistX_HwNm_u8p8[6]	410
t_AsstFWDefltAssistX_HwNm_u8p8[7]	435
t_AsstFWDefltAssistX_HwNm_u8p8[8]	461
t_AsstFWDefltAssistX_HwNm_u8p8[9]	486
t_AsstFWDefltAssistX_HwNm_u8p8[10]	512
t_AsstFWDefltAssistX_HwNm_u8p8[11]	538
t_AsstFWDefltAssistX_HwNm_u8p8[12]	563
t_AsstFWDefltAssistX_HwNm_u8p8[13]	589
t_AsstFWDefltAssistX_HwNm_u8p8[14]	614
t_AsstFWDefltAssistX_HwNm_u8p8[15]	640
t_AsstFWDefltAssistX_HwNm_u8p8[16]	666
t_AsstFWDefltAssistX_HwNm_u8p8[17]	691
t_AsstFWDefltAssistX_HwNm_u8p8[18]	717 742
t_AsstFWDefltAssistX_HwNm_u8p8[19]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[0] t_AsstFWDefltAssistY_MtrNm_s4p11[1]	19661
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	20070
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	22733
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	22938
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	23142
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	23347
t_AsstFWPstepNstepThresh_Cnt_u16[0]	207
t_AsstFWPstepNstepThresh_Cnt_u16[1]	547
t_AsstFWVehSpd_Kph_u9p7[0]	33792
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	33920 34048
t_AsstFWVehSpd_Kph_u9p7[3]	34176
t_AsstFWVehSpd_Kph_u9p7[4]	34304
t_AsstFWVehSpd_Kph_u9p7[5]	34432
t AsstFWVehSpd Kph u9p7[6]	34560
t_AsstFWVehSpd_Kph_u9p7[7]	34688
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.78000021
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-4
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	110.099998
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTb$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Igc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.87999995	0.879999995 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	547	547 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.87799978	4.87799978 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-0.200000286	-0.200000003 ± 4.88E-04	<b>~</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.20599985	4.20599985 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.87999995	0.879999995 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>~</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.87 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.099999
AssistFirewall ActiveKSV M str.K Uls f32	0.30000012
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4554
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	6.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0700000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.150000006
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.400001
k_AsstFWInpLimitHFA_MtrNm_f32	2.05999994
k_AsstFWInpLimitHysComp_MtrNm_f32	4.9000001
k_AsstFWNstep_Cnt_u16	2316
k_AsstFWPstep_Cnt_u16	0
k_RestoreThresh_MtrNm_f32	3.32999992
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-6192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2040
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
t2_Asst WopiboundX_HwNm_s4p11[3][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144
t2_Asst WopiBoundX_HwNm_s4p11[3][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0] t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_mwnm_s4p11[4][1] t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2] t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2040
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288
t2 AsstFWUprBoundX HwNm s4p11[5][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2 AsstFWUprBoundX HwNm s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-8192





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6] t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	2048
	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10] t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	10240 -12288
	-12268
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1] t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240
	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3] t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-4096
	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5] t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2046
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	8192
t2_Asst WuprBoundY_MtrNm_s4p11[4][0]	-26624
t2_Asst WoprBoundY_MtrNm_s4p11[4][0]	-24576
t2_Asst WoprboundY_MtrNm_s4p11[4][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	10240
t2 AsstFWUprBoundY MtrNm s4p11[5][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144
	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-0144
	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	282
t_AsstFWDefltAssistX_HwNm_u8p8[1]	307
t_AsstFWDefltAssistX_HwNm_u8p8[2]	333
t_AsstFWDefltAssistX_HwNm_u8p8[3]	358
t_AsstFWDefltAssistX_HwNm_u8p8[4]	384
t_AsstFWDefltAssistX_HwNm_u8p8[5]	410
t_AsstFWDefltAssistX_HwNm_u8p8[6]	435
t_AsstFWDefltAssistX_HwNm_u8p8[7]	461
t_AsstFWDefltAssistX_HwNm_u8p8[8]	486
t_AsstFWDefltAssistX_HwNm_u8p8[9]	512 538
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	563
t_AsstFWDefltAssistX_HwNm_u8p8[12]	589
t AsstFWDefitAssistX HwNm u8p8[13]	614
t_AsstFWDefltAssistX_HwNm_u8p8[14]	640
t_AsstFWDefltAssistX_HwNm_u8p8[15]	666
t_AsstFWDefltAssistX_HwNm_u8p8[16]	691
t_AsstFWDefltAssistX_HwNm_u8p8[17]	717
t_AsstFWDefltAssistX_HwNm_u8p8[18]	742
t_AsstFWDefltAssistX_HwNm_u8p8[19]	768
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[5] t_AsstFWDefltAssistY_MtrNm_s4p11[6]	20685 20890
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22733
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	22938
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	23142
t_AsstFWDefltAssistY_MtrNm_s4p11[18] t_AsstFWDefltAssistY_MtrNm_s4p11[19]	23347 23552
t AsstFWPstepNstepThresh Cnt u16[0]	208
t_AsstFWPstepNstepThresh_Cnt_u16[1]	551
t_AsstFWVehSpd_Kph_u9p7[0]	36736
t_AsstFWVehSpd_Kph_u9p7[1]	36864
t_AsstFWVehSpd_Kph_u9p7[2]	36992
t_AsstFWVehSpd_Kph_u9p7[3]	37120
t_AsstFWVehSpd_Kph_u9p7[4]	37248
t_AsstFWVehSpd_Kph_u9p7[5]	37376
t_AsstFWVehSpd_Kph_u9p7[6]	37504
t_AsstFWVehSpd_Kph_u9p7[7]	37632
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.90999985
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	2
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-6
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	121.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.16999984	2.17000008 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	551	551 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.77799988	5.77799988 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.19999981	6.19999981 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.3349998	3.33500004 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.88 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.7999995
AssistFirewall ActiveKSV M str.K Uls f32	0.059999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	3322
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall CombAsstSV MtrNm M f32	6.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.079999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.0199998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall LwrBoundKSV M str.K Uls f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.15999996
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.7999995
k AsstFWInpLimitHFA MtrNm f32	2.2999995
k_AsstFWInpLimitHysComp_MtrNm_f32	5.0999999
k_AsstFWNstep_Cnt_u16	2192
k_AsstFWPstep_Cnt_u16	5000
k RestoreThresh MtrNm f32	3.33999991
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2 AsstFWUprBoundX HwNm s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2 AsstFWUprBoundX HwNm s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2 AsstFWUprBoundX HwNm s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
t2 AsstFWUprBoundX HwNm s4p11[5][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
t2 AsstFWUprBoundX HwNm s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
and the proposition of the state of the stat	
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
	14336 -14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336 -12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-14336 -12288 -10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-14336 -12288 -10240 -8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-14336 -12288 -10240 -8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-14336 -12288 -10240 -8192 -6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-14336 -12288 -10240 -8192 -6144

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Input Value
2048
4096
6144
-28672
-26624
-24576
-22528
-20480
-18432
-16384
-14336
-12288
-10240
-8192
-30720
-28672
-26624
-24576
-22528
-20480
-18432
-16384
-14336
-12288
-10240
-10240
-8192
-6144
-4096
-2048
0
2048
4096
6144
8192
10240
-24576
-22528
-20480
-18432
-16384
-14336
-12288 -10240
-8192 -8144
-6144 -4096
8192
10240
12288
14336 16384
18432
20480
22528
24576
26624
28672 -12288
-12288 -10240
-10240 -8192
-8192 -6144
-6144 -4096
-4096 -2048
0
2048
4096
6144
6144 8192
6144 8192 -2048
6144 8192





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] t_AsstFWDefltAssistX_HwNm_u8p8[0]	307
t_AsstFWDefltAssistX_HwNm_u8p8[1]	333
t_AsstFWDefltAssistX_HwNm_u8p8[2]	358
t_AsstFWDefltAssistX_HwNm_u8p8[3]	384
t_AsstFWDefltAssistX_HwNm_u8p8[4]	410
t_AsstFWDefltAssistX_HwNm_u8p8[5]	435
t_AsstFWDefltAssistX_HwNm_u8p8[6]	461
t_AsstFWDefltAssistX_HwNm_u8p8[7]	486
t_AsstFWDefltAssistX_HwNm_u8p8[8]	512
t_AsstFWDefltAssistX_HwNm_u8p8[9]	538
t_AsstFWDefltAssistX_HwNm_u8p8[10]	563
t_AsstFWDefltAssistX_HwNm_u8p8[11]	589
t_AsstFWDefltAssistX_HwNm_u8p8[12]	614
t_AsstFWDefltAssistX_HwNm_u8p8[13]	640
t_AsstFWDefltAssistX_HwNm_u8p8[14]	666
t_AsstFWDefltAssistX_HwNm_u8p8[15]	691
t_AsstFWDefltAssistX_HwNm_u8p8[16]	717
t_AsstFWDefltAssistX_HwNm_u8p8[17]	742
t_AsstFWDefltAssistX_HwNm_u8p8[18]	768
t_AsstFWDefltAssistX_HwNm_u8p8[19]	794
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	20685 20890
t_AsstFWDefltAssistY_MtrNm_s4p11[5] t_AsstFWDefltAssistY_MtrNm_s4p11[6]	21094
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	21299
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	21914
t AsstFWDefltAssistY MtrNm s4p11[11]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	22733
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22938
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	23142
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	23347
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	23552
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	23757
t_AsstFWPstepNstepThresh_Cnt_u16[0]	209
t_AsstFWPstepNstepThresh_Cnt_u16[1]	555
t_AsstFWVehSpd_Kph_u9p7[0]	39680
t_AsstFWVehSpd_Kph_u9p7[1]	39808
t_AsstFWVehSpd_Kph_u9p7[2]	39936
t_AsstFWVehSpd_Kph_u9p7[3]	40064
t_AsstFWVehSpd_Kph_u9p7[4]	40192
t_AsstFWVehSpd_Kph_u9p7[5]	40320
t_AsstFWVehSpd_Kph_u9p7[6]	40448
t_AsstFWVehSpd_Kph_u9p7[7]	40576
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.03999996
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	0 2.0999999
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_132.value tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	2.0999999
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	132.300003
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	*
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
, , , , , , , , , , , , , , , , , , , ,	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_Assisti ilewali_Fei1_iviEO_Codiitei_Crit_eridiii

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.63199997	2.63199997 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	555	555 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.55200005	1.55200005 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.5	6.5 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.28399992	4.28399992 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	✓
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	-

Test Step 2.89 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall ActiveKSV M str.K Uls f32	0.019999996
AssistFirewall_ActiveRawAcc_Cnt_M_u16	222
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	6.6999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.029999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	2
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.600000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.170000002
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.9000001
k_AsstFWInpLimitHFA_MtrNm_f32	3.2999995
k_AsstFWInpLimitHysComp_MtrNm_f32	5.30000019
k_AsstFWNstep_Cnt_u16	2000
k AsstFWPstep Cnt u16	2500
k RestoreThresh MtrNm f32	3.3499999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6] t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7] t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][0] t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0
t2_AsstFWUprBoundX_riwNin_s4p11[5][1] t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4] t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5] t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_Asst WopiboundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144
	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-2048
	-2048 0

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-6144 -28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0] t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-22528
t2_Asst Wopibound1_ivitNin_s4p11[2][3] t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-18432
	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6] t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-10304
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7] t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-14330
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9] t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10] t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
tz_Assit WopiBound1_ivitiVini_s4p11[/][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096 6144





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	333
t_AsstFWDefltAssistX_HwNm_u8p8[1]	358
t_AsstFWDefltAssistX_HwNm_u8p8[2]	384
t_AsstFWDefltAssistX_HwNm_u8p8[3]	410
t_AsstFWDefltAssistX_HwNm_u8p8[4]	435
t_AsstFWDefltAssistX_HwNm_u8p8[5]	461
t_AsstFWDefltAssistX_HwNm_u8p8[6]	486
t_AsstFWDefltAssistX_HwNm_u8p8[7]	512
t_AsstFWDefltAssistX_HwNm_u8p8[8]	538
t_AsstFWDefltAssistX_HwNm_u8p8[9]	563
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	589 614
t AsstFWDefitAssistX HwNm u8p8[12]	640
t_AsstFWDefitAssistX_HwNm_u8p8[13]	666
t_AsstFWDefitAssistX_HwNm_u8p8[14]	691
t_AsstFWDefitAssistX_HwNm_u8p8[15]	717
t_AsstFWDefitAssistX_HwNm_u8p8[16]	742
t AsstFWDefltAssistX HwNm u8p8[17]	768
t_AsstFWDefitAssistX_HwNm_u8p8[18]	794
t_AsstFWDefltAssistX_HwNm_u8p8[19]	819
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	22733
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	22938
t_AsstFWDefltAssistY_MtrNm_s4p11[15] t_AsstFWDefltAssistY_MtrNm_s4p11[16]	23142 23347
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	23552
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	23757
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	23962
t_AsstFWPstepNstepThresh_Cnt_u16[0]	210
t_AsstFWPstepNstepThresh_Cnt_u16[1]	559
t_AsstFWVehSpd_Kph_u9p7[0]	42624
t_AsstFWVehSpd_Kph_u9p7[1]	42752
t_AsstFWVehSpd_Kph_u9p7[2]	42880
t_AsstFWVehSpd_Kph_u9p7[3]	43008
t_AsstFWVehSpd_Kph_u9p7[4]	43136
t_AsstFWVehSpd_Kph_u9p7[5]	43264
t_AsstFWVehSpd_Kph_u9p7[6]	43392
t_AsstFWVehSpd_Kph_u9p7[7]	43520
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.17000008
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	143.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_li	· ·
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_Hw1orque_HwNm_f32  tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_Hw1 orque_Hwnm_r32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32
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AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.07800007	1.07799995 ± 4.88E-04	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	559	559 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.37100005	1.37100005 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.4000001	6.4000001 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.34000003	1.34000003 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

τ -				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	_

Test Step 2.90 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.099999
AssistFirewall ActiveKSV M str.K Uls f32	0.100000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	344
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	6.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.40000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.090000036
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4
k_AsstFWInpLimitHFA_MtrNm_f32	4.30000019
k_AsstFWInpLimitHysComp_MtrNm_f32	2
k_AsstFWNstep_Cnt_u16	0
k_AsstFWPstep_Cnt_u16	200
k_RestoreThresh_MtrNm_f32	3.3599999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240





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Name	Input Value	
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192	
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144	
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096	
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0	
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048	
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144	
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192	
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048	
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0	
t2_Asst WopiboundX_HwNm_s4p11[3][1]	2048	
t2_AsstrWUprBoundX_HwNm_s4p11[3][3]	4096	
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192	
	10240	
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]		
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096	
z_AsstFWUprBoundX_HwNm_s4p11[7][3] 2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192 10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]		
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0	
	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	2040	





Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
	4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	8192





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	22528
t_AsstFWDefltAssistX_HwNm_u8p8[0]	358
t_AsstFWDefltAssistX_HwNm_u8p8[1]	384 410
t_AsstFWDefltAssistX_HwNm_u8p8[2]	
t_AsstFWDefltAssistX_HwNm_u8p8[3] t_AsstFWDefltAssistX_HwNm_u8p8[4]	435
t_AsstFWDefltAssistX_HwNm_u8p8[5]	486
t_AsstFWDefltAssistX_HwNm_u8p8[6]	512
t_AsstFWDefitAssistX_HwNm_u8p8[7]	538
t_AsstFWDefltAssistX_HwNm_u8p8[8]	563
t_AsstFWDefltAssistX_HwNm_u8p8[9]	589
t_AsstFWDefltAssistX_HwNm_u8p8[10]	614
t_AsstFWDefltAssistX_HwNm_u8p8[11]	640
t_AsstFWDefltAssistX_HwNm_u8p8[12]	666
t_AsstFWDefitAssistX_HwNm_u8p8[13]	691
t AsstFWDefltAssistX HwNm u8p8[14]	717
t_AsstFWDefitAssistX_HwNm_u8p8[15]	742
t_AsstFWDefltAssistX_HwNm_u8p8[16]	768
t_AsstFWDefitAssistX_HwNm_u8p8[17]	794
t_AsstFWDefitAssistX_HwNm_u8p8[18]	819
t_AsstFWDefltAssistX_HwNm_u8p8[19]	845
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	22733
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	22938
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	23142
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	23347
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	23552
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	23757
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	23962
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	24166
t_AsstFWPstepNstepThresh_Cnt_u16[0]	211
t_AsstFWPstepNstepThresh_Cnt_u16[1]	563
t_AsstFWVehSpd_Kph_u9p7[0]	45568
t_AsstFWVehSpd_Kph_u9p7[1]	45696
t_AsstFWVehSpd_Kph_u9p7[2]	45824
t_AsstFWVehSpd_Kph_u9p7[3]	45952
t_AsstFWVehSpd_Kph_u9p7[4]	46080
t_AsstFWVehSpd_Kph_u9p7[5]	46208
t_AsstFWVehSpd_Kph_u9p7[6]	46336
t_AsstFWVehSpd_Kph_u9p7[7]	46464
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.30000019
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.3999998
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	154.100006
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_left and the property of the p$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

AssistFirewall\_Per1







Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
2 AsstFWUprBoundX HwNm s4p11[4][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
2 AsstFWUprBoundX HwNm s4p11[6][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-16384
	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-12288
	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	10240





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576
t_AsstFWDefltAssistX_HwNm_u8p8[0]	384 410
t_AsstFWDefltAssistX_HwNm_u8p8[1] t_AsstFWDefltAssistX_HwNm_u8p8[2]	435
t_AsstFWDefltAssistX_HwNm_u8p8[3]	461
t_AsstFWDefltAssistX_HwNm_u8p8[4]	486
t_AsstFWDefltAssistX_HwNm_u8p8[5]	512
t_AsstFWDefltAssistX_HwNm_u8p8[6]	538
t_AsstFWDefltAssistX_HwNm_u8p8[7]	563
t_AsstFWDefltAssistX_HwNm_u8p8[8]	589
t_AsstFWDefltAssistX_HwNm_u8p8[9]	614 640
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	666
t AsstFWDefitAssistX HwNm u8p8[12]	691
t_AsstFWDefltAssistX_HwNm_u8p8[13]	717
t_AsstFWDefltAssistX_HwNm_u8p8[14]	742
t_AsstFWDefltAssistX_HwNm_u8p8[15]	768
t_AsstFWDefltAssistX_HwNm_u8p8[16]	794
t_AsstFWDefltAssistX_HwNm_u8p8[17]	819
t_AsstFWDefltAssistX_HwNm_u8p8[18]	845
t_AsstFWDefltAssistX_HwNm_u8p8[19]	870
t_AsstFWDefltAssistY_MtrNm_s4p11[0] t_AsstFWDefltAssistY_MtrNm_s4p11[1]	-205 -184
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	-164
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	-143
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	-123
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	-102
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	-82
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	-61
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	-41
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	-20 0
t_AsstFWDefltAssistY_MtrNm_s4p11[10] t_AsstFWDefltAssistY_MtrNm_s4p11[11]	20
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	41
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	61
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	82
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	102
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	123
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	143
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	164
t_AsstFWDefthAssistY_MtrNm_s4p11[19]	184
t_AsstFWPstepNstepThresh_Cnt_u16[0] t_AsstFWPstepNstepThresh_Cnt_u16[1]	212 567
t_AsstFWVehSpd_Kph_u9p7[0]	1408
t_AsstFWVehSpd_Kph_u9p7[1]	1536
t_AsstFWVehSpd_Kph_u9p7[2]	1664
t_AsstFWVehSpd_Kph_u9p7[3]	1792
t_AsstFWVehSpd_Kph_u9p7[4]	1920
t_AsstFWVehSpd_Kph_u9p7[5]	2048
t_AsstFWVehSpd_Kph_u9p7[6]	2176
t_AsstFWVehSpd_Kph_u9p7[7]	2304 5.42999983
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lqc.value	5.42999983 0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.70000005
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	165.300003
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Itgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
THE THE THE PRODUCT IN WAIT. ASSIST HE WAIT FOR THE PROPERTY INTERNAL INTER	I I I I I I I I I I I I I I I I I I I
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tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

2015-03-23, 11:55:49+0530



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.24000001	2.24000001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	567	567 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	-0.100097656	-0.100097656 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.20200014	5.20200014 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2	2 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3	3 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-0.100097656	-0.100097656 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>~</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>~</b>

T			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.92 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall ActiveKSV M str.K Uls f32	0.30000012
AssistFirewall_ActiveRawAcc_Cnt_M_u16	334
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	7
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0700000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall LwrBoundKSV M str.K Uls f32	0.60000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.109999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.19999981
k_AsstFWInpLimitHFA_MtrNm_f32	6.30000019
k_AsstFWInpLimitHysComp_MtrNm_f32	1
k_AsstFWNstep_Cnt_u16	2500
k_AsstFWPstep_Cnt_u16	21
k_RestoreThresh_MtrNm_f32	3.38000011
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144



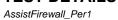


Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192 10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8] t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1] t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336 -12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096 2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6] t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_Asst Wopibound1_Within_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
	-2048
t2 AsstFWUprBoundY MtrNm s4p11[0][2]	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-2048
	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048
	0





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	410
t_AsstFWDefltAssistX_HwNm_u8p8[1]	435
t_AsstFWDefltAssistX_HwNm_u8p8[2]	461
t_AsstFWDefltAssistX_HwNm_u8p8[3]	486
t_AsstFWDefltAssistX_HwNm_u8p8[4]	512
t_AsstFWDefltAssistX_HwNm_u8p8[5]	538
t_AsstFWDefltAssistX_HwNm_u8p8[6] t_AsstFWDefltAssistX_HwNm_u8p8[7]	563 589
t_AsstFWDefitAssistX_HwNm_u8p8[8]	614
t_AsstFWDefltAssistX_HwNm_u8p8[9]	640
t_AsstFWDefltAssistX_HwNm_u8p8[10]	666
t_AsstFWDefltAssistX_HwNm_u8p8[11]	691
t AsstFWDefltAssistX HwNm u8p8[12]	717
t_AsstFWDefltAssistX_HwNm_u8p8[13]	742
t_AsstFWDefltAssistX_HwNm_u8p8[14]	768
t_AsstFWDefltAssistX_HwNm_u8p8[15]	794
t_AsstFWDefltAssistX_HwNm_u8p8[16]	819
t_AsstFWDefltAssistX_HwNm_u8p8[17]	845
t_AsstFWDefltAssistX_HwNm_u8p8[18]	870
t_AsstFWDefltAssistX_HwNm_u8p8[19]	896
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	-143
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	-82
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	-20
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	41
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	102
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	164
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	225 287
t_AsstFWDefltAssistY_MtrNm_s4p11[8] t_AsstFWDefltAssistY_MtrNm_s4p11[9]	348
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	410
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	471
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	532
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	594
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	655
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	717
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	778
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	840
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	901
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	963
t_AsstFWPstepNstepThresh_Cnt_u16[0]	213
t_AsstFWPstepNstepThresh_Cnt_u16[1]	571
t_AsstFWVehSpd_Kph_u9p7[0]	4352
t_AsstFWVehSpd_Kph_u9p7[1]	4480
t_AsstFWVehSpd_Kph_u9p7[2]	4608
t_AsstFWVehSpd_Kph_u9p7[3]	4736
t_AsstFWVehSpd_Kph_u9p7[4]	4864
t_AsstFWVehSpd_Kph_u9p7[5]	4992
t_AsstFWVehSpd_Kph_u9p7[6]	5120
t_AsstFWVehSpd_Kph_u9p7[7]  tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5248 5.55999994
	0.009999994
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2.5999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176.399994
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	
	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_learnerserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverserverser$	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_legt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32$	
	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.07000005	1.07000005 ± 4.88E-04	<b>*</b>
AssistFirewall_ActiveRawAcc_Cnt_M_u16	355	355 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.81680965	5.81681013 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.21899986	6.21899986 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.79999971	2.79999995 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.21999979	4.21999979 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	5.81680965	5.81681013 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~

Τ				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	•

Test Step 2.93 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.79999995
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8118
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.7999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.129999995
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.5
k_AsstFWInpLimitHFA_MtrNm_f32	8.80000019
k_AsstFWInpLimitHysComp_MtrNm_f32	6.38000011
k_AsstFWNstep_Cnt_u16	2192
k_AsstFWPstep_Cnt_u16	2091
k_RestoreThresh_MtrNm_f32	3.3900001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
2 AsstFWUprBoundX HwNm s4p11[5][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	10240

AssistFirewall\_Per1





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
z_AsstFWUprBoundY_MtrNm_s4p11[6][0] 2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
, , , , , , , , , , , , , , , , , , , ,	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	435
t_AsstFWDefltAssistX_HwNm_u8p8[1]	461
t_AsstFWDefltAssistX_HwNm_u8p8[2]	486
t_AsstFWDefltAssistX_HwNm_u8p8[3]	512
t_AsstFWDefltAssistX_HwNm_u8p8[4]	538
t_AsstFWDefltAssistX_HwNm_u8p8[5]	563
t_AsstFWDefltAssistX_HwNm_u8p8[6]	589
t_AsstFWDefltAssistX_HwNm_u8p8[7]	614
t_AsstFWDefltAssistX_HwNm_u8p8[8]	640
t_AsstFWDefltAssistX_HwNm_u8p8[9]	666
t_AsstFWDefltAssistX_HwNm_u8p8[10]	691
t_AsstFWDefltAssistX_HwNm_u8p8[11]	717
t_AsstFWDefltAssistX_HwNm_u8p8[12]	742
t_AsstFWDefltAssistX_HwNm_u8p8[13]	768
t_AsstFWDefltAssistX_HwNm_u8p8[14]	794
t_AsstFWDefltAssistX_HwNm_u8p8[15]	819
t_AsstFWDefltAssistX_HwNm_u8p8[16]	845
t_AsstFWDefltAssistX_HwNm_u8p8[17]	870
t_AsstFWDefltAssistX_HwNm_u8p8[18] t AsstFWDefltAssistX_HwNm_u8p8[19]	896 922
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	2458
t_AsstFWDefitAssistY_MtrNm_s4p11[1]	2662
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2867
t_AsstFWDefitAssistY_MtrNm_s4p11[3]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6144
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	6349
t_AsstFWPstepNstepThresh_Cnt_u16[0] t AsstFWPstepNstepThresh Cnt u16[1]	214
	575
t_AsstFWVehSpd_Kph_u9p7[0] t_AsstFWVehSpd_Kph_u9p7[1]	7296 7424
t_AsstFWVenSpd_kpn_u9p7[1] t_AsstFWVehSpd_kph_u9p7[2]	7552
t_AsstFWVehSpd_Kph_u9p7[3]	7680
t_AsstFWVehSpd_Kph_u9p7[4]	7808
t_AsstFWVehSpd_Kph_u9p7[5]	7936
t AsstFWVehSpd Kph u9p7[6]	8064
t_AsstFWVehSpd_Kph_u9p7[7]	8192
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.17000008
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	143.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.51999998	2.51999998 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	575	575 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.10009766	3.10009766 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.26999998	4.26999998 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.5	3.5 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.03999996	2.03999996 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.10009766	3.10009766 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.94 (Repeat Count = 1)	v
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.099999
AssistFirewall ActiveKSV M str.K Uls f32	0.090000036
AssistFirewall_ActiveRawAcc_Cnt_M_u16	109
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.2000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.079999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.89999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0700000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0099999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4
k_AsstFWInpLimitHFA_MtrNm_f32	2.5
k_AsstFWInpLimitHysComp_MtrNm_f32	3.78999996
k_AsstFWNstep_Cnt_u16	3928
k_AsstFWPstep_Cnt_u16	1107
k_RestoreThresh_MtrNm_f32	1.8999998
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384
	-16384 -14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2 AsstFWUprBoundX HwNm s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2 AsstFWUprBoundX HwNm s4p11[6][3]	-12288
t2 AsstFWUprBoundX HwNm s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
t2_AsstrWUprBoundY_MtrNm_s4p11[0][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	14336





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-2048
2_Asst WopiBoundY_MtrNm_s4p11[4][6]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528
	24576
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144



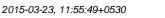


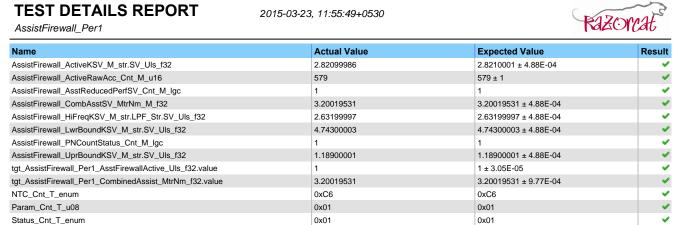
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	461 486
t_AsstFWDefltAssistX_HwNm_u8p8[1] t_AsstFWDefltAssistX_HwNm_u8p8[2]	512
t_AsstFWDefltAssistX_HwNm_u8p8[3]	538
t_AsstFWDefltAssistX_HwNm_u8p8[4]	563
t_AsstFWDefltAssistX_HwNm_u8p8[5]	589
t_AsstFWDefltAssistX_HwNm_u8p8[6]	614
t_AsstFWDefltAssistX_HwNm_u8p8[7]	640
t_AsstFWDefltAssistX_HwNm_u8p8[8]	666
t_AsstFWDefltAssistX_HwNm_u8p8[9]	691
t_AsstFWDefltAssistX_HwNm_u8p8[10]	717
t_AsstFWDefltAssistX_HwNm_u8p8[11]	742
t_AsstFWDefltAssistX_HwNm_u8p8[12]	768
t_AsstFWDefltAssistX_HwNm_u8p8[13]	794
t_AsstFWDefltAssistX_HwNm_u8p8[14]	819
t_AsstFWDefltAssistX_HwNm_u8p8[15]	845
t_AsstFWDefltAssistX_HwNm_u8p8[16]	870
t_AsstFWDefltAssistX_HwNm_u8p8[17]	896
t_AsstFWDefltAssistX_HwNm_u8p8[18]	922
t_AsstFWDefltAssistX_HwNm_u8p8[19]	947
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2662
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2867
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3482 3686
t_AsstFWDefltAssistY_MtrNm_s4p11[5] t_AsstFWDefltAssistY_MtrNm_s4p11[6]	3891
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4710
t AsstFWDefltAssistY MtrNm s4p11[11]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6554
t_AsstFWPstepNstepThresh_Cnt_u16[0]	215
t_AsstFWPstepNstepThresh_Cnt_u16[1]	579
t_AsstFWVehSpd_Kph_u9p7[0]	10240
t_AsstFWVehSpd_Kph_u9p7[1]	10368
t_AsstFWVehSpd_Kph_u9p7[2]	10496
t_AsstFWVehSpd_Kph_u9p7[3]	10624
t_AsstFWVehSpd_Kph_u9p7[4]	10752
t_AsstFWVehSpd_Kph_u9p7[5]	11008
t_AsstFWVehSpd_Kph_u9p7[6]	11008
t_AsstFWVehSpd_Kph_u9p7[7] tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	11136
tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	9
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90.1999969
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

NTC\_Cnt\_T\_enum

Param\_Cnt\_T\_u08

Status\_Cnt\_T\_enum





T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	-
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	_

0xC9

0x01

0x01

0xC9

0x01

0x01

Test Step 2.95 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.099999
AssistFirewall ActiveKSV M str.K Uls f32	0.090000036
AssistFirewall_ActiveRawAcc_Cnt_M_u16	109
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	-8.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.8999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0700000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0099999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4
k_AsstFWInpLimitHFA_MtrNm_f32	2.5
k_AsstFWInpLimitHysComp_MtrNm_f32	3.78999996
k_AsstFWNstep_Cnt_u16	3928
k_AsstFWPstep_Cnt_u16	1107
k_RestoreThresh_MtrNm_f32	1.8999998
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
z_AsstFWUprBoundX_HwNm_s4p11[3][9] 2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
2 AsstFWUprBoundX HwNm s4p11[5][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
2 AsstFWUprBoundX HwNm s4p11[5][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
2 AsstFWUprBoundX HwNm s4p11[6][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	8192
:2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240
	12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	





Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048
· · · · · · · · · · · · · · · · · · ·	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	26624
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][1] 2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096
	8192
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	
	8192 10240 12288





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	22528 24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	486
t_AsstFWDefltAssistX_HwNm_u8p8[1]	512
t_AsstFWDefltAssistX_HwNm_u8p8[2]	538
t_AsstFWDefltAssistX_HwNm_u8p8[3]	563
t_AsstFWDefltAssistX_HwNm_u8p8[4]	589
t_AsstFWDefltAssistX_HwNm_u8p8[5]	614
t_AsstFWDefltAssistX_HwNm_u8p8[6]	640
t_AsstFWDefltAssistX_HwNm_u8p8[7]	666
t_AsstFWDefltAssistX_HwNm_u8p8[8]	691 717
t_AsstFWDefltAssistX_HwNm_u8p8[9] t_AsstFWDefltAssistX_HwNm_u8p8[10]	742
t_AsstFWDefitAssistX_HwNm_u8p8[11]	768
t_AsstFWDefltAssistX_HwNm_u8p8[12]	794
t_AsstFWDefitAssistX_HwNm_u8p8[13]	819
t_AsstFWDefltAssistX_HwNm_u8p8[14]	845
t_AsstFWDefltAssistX_HwNm_u8p8[15]	870
t_AsstFWDefltAssistX_HwNm_u8p8[16]	896
t_AsstFWDefltAssistX_HwNm_u8p8[17]	922
t_AsstFWDefltAssistX_HwNm_u8p8[18]	947
t_AsstFWDefltAssistX_HwNm_u8p8[19]	973
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2867
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3072
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[3] t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3482 3686
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[15] t_AsstFWDefltAssistY_MtrNm_s4p11[16]	5939 6144
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	6349
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6758
t_AsstFWPstepNstepThresh_Cnt_u16[0]	216
t_AsstFWPstepNstepThresh_Cnt_u16[1]	583
t_AsstFWVehSpd_Kph_u9p7[0]	13184
t_AsstFWVehSpd_Kph_u9p7[1]	13312
t_AsstFWVehSpd_Kph_u9p7[2]	13440
t_AsstFWVehSpd_Kph_u9p7[3]	13568
t_AsstFWVehSpd_Kph_u9p7[4]	13696
t_AsstFWVehSpd_Kph_u9p7[5]	13824
t_AsstFWVehSpd_Kph_u9p7[6]	13952
t_AsstFWVehSpd_Kph_u9p7[7]	14080
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	9
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90.3000031
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tot Dto Ingt An AggistEiroughl AggistEiroughl Day MEG County Out	tot AssistEirowall Bort MEC Counter Cat annua
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.82099986	2.8210001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	583	583 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.29980469	3.29980469 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.63199997	2.63199997 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.67299986	4.67299986 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.199	1.199 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.29980469	3.29980469 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.96 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.30000019
AssistFirewall ActiveKSV M str.K Uls f32	0.40000006
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall CombAsstSV MtrNm M f32	8.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.079999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11199999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.3000019
AssistFirewall LwrBoundKSV M str.K Uls f32	0.119999997
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.099999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.219999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.80000019
k AsstFWInpLimitHFA MtrNm f32	6.40999985
k_AsstFWInpLimitHysComp_MtrNm_f32	6.71000004
k_AsstFWNstep_Cnt_u16	4052
k_AsstFWPstep_Cnt_u16	2460
k RestoreThresh MtrNm f32	4.4299983
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2 AsstFWUprBoundX HwNm s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2 AsstFWUprBoundX HwNm s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384
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Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288	
2 AsstFWUprBoundX HwNm s4p11[6][2]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192	
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2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	4096	
	6144	
	· · · ·	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1] 2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1] 2_AsstFWUprBoundY_MtrNm_s4p11[0][2] 2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1] 2_AsstFWUprBoundY_MtrNm_s4p11[0][2] 2_AsstFWUprBoundY_MtrNm_s4p11[0][3] 2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240 12288	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	10240	





Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336
:2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240
	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	26624
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	28672
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
, , , , , , , , , , , , , , , , , , , ,	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096 2040
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	512
t_AsstFWDefltAssistX_HwNm_u8p8[1]	538
t_AsstFWDefltAssistX_HwNm_u8p8[2]	563
t_AsstFWDefltAssistX_HwNm_u8p8[3]	589
t_AsstFWDefltAssistX_HwNm_u8p8[4]	614
t_AsstFWDefltAssistX_HwNm_u8p8[5]	640
t_AsstFWDefltAssistX_HwNm_u8p8[6]	666
t_AsstFWDefltAssistX_HwNm_u8p8[7]	691
t_AsstFWDefltAssistX_HwNm_u8p8[8]	717
t_AsstFWDefltAssistX_HwNm_u8p8[9]	742
t_AsstFWDefltAssistX_HwNm_u8p8[10]	768
t_AsstFWDefltAssistX_HwNm_u8p8[11]	794
t_AsstFWDefltAssistX_HwNm_u8p8[12]	819
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	845 870
t_AsstFWDefitAssistX_HwNm_u8p8[14]  t_AsstFWDefitAssistX_HwNm_u8p8[15]	896
t_AsstFWDefitAssistX_HwNm_u8p8[16]	922
t_AsstFWDefltAssistX_HwNm_u8p8[17]	947
t_AsstFWDefitAssistX_HwNm_u8p8[18]	973
t_AsstFWDefltAssistX_HwNm_u8p8[19]	998
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[11] t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5325 5530
t AsstFWDefltAssistY MtrNm s4p11[13]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6963
t_AsstFWPstepNstepThresh_Cnt_u16[0]	217
t_AsstFWPstepNstepThresh_Cnt_u16[1]	587
t_AsstFWVehSpd_Kph_u9p7[0]	16128
t_AsstFWVehSpd_Kph_u9p7[1]	16256
t_AsstFWVehSpd_Kph_u9p7[2]	16384
t_AsstFWVehSpd_Kph_u9p7[3]	16512
t_AsstFWVehSpd_Kph_u9p7[4]	16640
t_AsstFWVehSpd_Kph_u9p7[5]	16768
t_AsstFWVehSpd_Kph_u9p7[6]	16896
t_AsstFWVehSpd_Kph_u9p7[7]	5 10000001
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	-5.19999981 0
tgt_AssistFireWall_Per1_Deteat_Assist_MtrNm_f32.value	-5.5999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.4000001
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.5999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFi$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-3.18000007	-3.18000007 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	587	587 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.39990234	-3.39990234 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-6.06399965	-6.06400013 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-4.59198856	-4.59198809 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.21799994	2.21799994 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-3.39990234	-3.39990234 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•

T			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.97 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.4000001
AssistFirewall ActiveKSV M str.K Uls f32	0.5
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8610
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	0
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.090000036
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11300004
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.4000001
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.129999995
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.230000004
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.9000001
k_AsstFWInpLimitHFA_MtrNm_f32	6.42000008
k_AsstFWInpLimitHysComp_MtrNm_f32	6.82000017
k_AsstFWNstep_Cnt_u16	4053
k_AsstFWPstep_Cnt_u16	2583
k_RestoreThresh_MtrNm_f32	4.44000006
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2 AsstFWUprBoundX HwNm s4p11[2][2]	-10240
_ , ,	
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
	-2046
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2 AsstFWUprBoundX HwNm s4p11[5][9]	0
_ , ,	
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	4096 6144

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Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240	
:2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048	
	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]		
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	26624	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	28672	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192	
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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	538
t_AsstFWDefltAssistX_HwNm_u8p8[1]	563
t_AsstFWDefltAssistX_HwNm_u8p8[2]	589 614
t_AsstFWDefltAssistX_HwNm_u8p8[3] t AsstFWDefltAssistX_HwNm_u8p8[4]	640
t_AsstFWDefltAssistX_HwNm_u8p8[5]	666
t_AsstFWDefltAssistX_HwNm_u8p8[6]	691
t_AsstFWDefitAssistX_HwNm_u8p8[7]	717
t_AsstFWDefltAssistX_HwNm_u8p8[8]	742
t_AsstFWDefltAssistX_HwNm_u8p8[9]	768
t_AsstFWDefltAssistX_HwNm_u8p8[10]	794
t_AsstFWDefltAssistX_HwNm_u8p8[11]	819
t AsstFWDefltAssistX HwNm u8p8[12]	845
t_AsstFWDefltAssistX_HwNm_u8p8[13]	870
t_AsstFWDefltAssistX_HwNm_u8p8[14]	896
t_AsstFWDefitAssistX_HwNm_u8p8[15]	922
t AsstFWDefltAssistX HwNm u8p8[16]	947
t AsstFWDefltAssistX HwNm u8p8[17]	973
t_AsstFWDefltAssistX_HwNm_u8p8[18]	998
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1024
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7168
t_AsstFWPstepNstepThresh_Cnt_u16[0]	218
t_AsstFWPstepNstepThresh_Cnt_u16[1]	591
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
t_AsstFWVehSpd_Kph_u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.30000019
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.69999981
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.69999981
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	187.100006
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_kte_inst_Ap_assistFirewali.AssistFirewali_Per1_HysteresisComp_intrinm_ts2 tgt_kte_inst_Ap_assistFirewali.AssistFirewali_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	
tul inte inst an assistritewali. Assistritewali Peri Veriiclespeed NDN 132	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-2.70000005	-2.70000005 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	591	591 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.5	-3.5 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-6.28999996	-6.28999996 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-4.63300037	-4.6329999 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.5369997	-5.53700018 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-3.5	-3.5 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.98 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.5
AssistFirewall ActiveKSV M str.K Uls f32	0.60000024
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8733
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.100000001
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11399996
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.80000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.140000001
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.19999981
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.239999995
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5
k_AsstFWInpLimitHFA_MtrNm_f32	6.42999983
k_AsstFWInpLimitHysComp_MtrNm_f32	6.92999983
k_AsstFWNstep_Cnt_u16	3053
k_AsstFWPstep_Cnt_u16	2706
k_RestoreThresh_MtrNm_f32	4.44999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_Asst WopiboundX_1 Willi_s4p 11[4][5] t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2 AsstFWUprBoundX HwNm s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3] t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240 12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	0144

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-8192
	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432
	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-12288 -10240 -8192 -6144





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	563
t_AsstFWDefltAssistX_HwNm_u8p8[1]	589
t_AsstFWDefltAssistX_HwNm_u8p8[2]	614
t_AsstFWDefltAssistX_HwNm_u8p8[3]	640
t_AsstFWDefltAssistX_HwNm_u8p8[4]	666
t_AsstFWDefltAssistX_HwNm_u8p8[5]	691
t_AsstFWDefltAssistX_HwNm_u8p8[6]	717
t_AsstFWDefltAssistX_HwNm_u8p8[7]	742 768
t_AsstFWDefltAssistX_HwNm_u8p8[8] t_AsstFWDefltAssistX_HwNm_u8p8[9]	794
t_AsstFWDefltAssistX_HwNm_u8p8[10]	819
t_AsstFWDefltAssistX_HwNm_u8p8[11]	845
t_AsstFWDefltAssistX_HwNm_u8p8[12]	870
t_AsstFWDefltAssistX_HwNm_u8p8[13]	896
t_AsstFWDefltAssistX_HwNm_u8p8[14]	922
t_AsstFWDefltAssistX_HwNm_u8p8[15]	947
t_AsstFWDefltAssistX_HwNm_u8p8[16]	973
t_AsstFWDefltAssistX_HwNm_u8p8[17]	998
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1050
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3686 3891
t_AsstFWDefltAssistY_MtrNm_s4p11[2] t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[13] t AsstFWDefltAssistY MtrNm s4p11[14]	6144 6349
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6554
t_AsstFWDefitAssistY_MtrNm_s4p11[16]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7373
t_AsstFWPstepNstepThresh_Cnt_u16[0]	219
t_AsstFWPstepNstepThresh_Cnt_u16[1]	595
t_AsstFWVehSpd_Kph_u9p7[0]	22016
t_AsstFWVehSpd_Kph_u9p7[1]	22144
t_AsstFWVehSpd_Kph_u9p7[2]	22272
t_AsstFWVehSpd_Kph_u9p7[3]	22400
t_AsstFWVehSpd_Kph_u9p7[4] t_AsstFWVehSpd_Kph_u9p7[5]	22528
t_AsstFWVenSpd_Kpn_u9p7[5] t AsstFWVehSpd Kph u9p7[6]	22656 22784
t_AsstFWVehSpd_Kph_u9p7[7]	22764
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.4000001
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.67000008
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.5999999
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.67000008
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	198.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_ltgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	
	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
• • • • • • • • • • • • • • • • • • • •	tot AssistFirewall Per1 HwTorque HwNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt AssistFirewall Per1_HysteresisComp_MtrNm_f32
• • • • • • • • • • • • • • • • • • • •	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-2.19999981	-2.20000005 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	595	595 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.60009766	-3.60009766 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-4.05000019	-4.05000019 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.04405499	5.04405451 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.39199972	-5.3920002 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-3.60009766	-3.60009766 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.99 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.5
AssistFirewall ActiveKSV M str.K Uls f32	0.0120000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8856
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.109999999
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11500001
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.9000001
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.150000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.25
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.099999
k_AsstFWInpLimitHFA_MtrNm_f32	6.44000006
k_AsstFWInpLimitHysComp_MtrNm_f32	7.03999996
k_AsstFWNstep_Cnt_u16	2053
k_AsstFWPstep_Cnt_u16	2829
k_RestoreThresh_MtrNm_f32	4.46000004
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240





Name t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	
t2 AsstFWUprBoundX HwNm s4p11[2][1]	Input Value
	-8192
t2 AsstFWUprBoundX HwNm s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2 AsstFWUprBoundX HwNm s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2 AsstFWUprBoundX HwNm s4p11[6][0]	-8192
	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
	-6192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-28672
	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-22528 -20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-22528

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5] t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_Asst WoprBoundY_MtrNm_s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048
t2_Asst WoprBoundY_MtrNm_s4p11[6][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-6144
tz_Assi Wopibound1_WithWin_s4p11[7][2]	-0144

AssistFirewall\_Per1



ASSISTITEWAII_PETT	
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefltAssistX_HwNm_u8p8[0]	589
t_AsstFWDefltAssistX_HwNm_u8p8[1]	614
t_AsstFWDefltAssistX_HwNm_u8p8[2]	640
t_AsstFWDefltAssistX_HwNm_u8p8[3]	666
t_AsstFWDefltAssistX_HwNm_u8p8[4]	691
t_AsstFWDefltAssistX_HwNm_u8p8[5]	717
t_AsstFWDefltAssistX_HwNm_u8p8[6]	742
t_AsstFWDefltAssistX_HwNm_u8p8[7]	768
t_AsstFWDefltAssistX_HwNm_u8p8[8]	794
t_AsstFWDefltAssistX_HwNm_u8p8[9]	819
t_AsstFWDefltAssistX_HwNm_u8p8[10]	845
t_AsstFWDefitAssistX_HwNm_u8p8[11]	870
	896
t_AsstFWDefltAssistX_HwNm_u8p8[12] t AsstFWDefltAssistX_HwNm_u8p8[13]	
, ,	922
t_AsstFWDefltAssistX_HwNm_u8p8[14]	947
t_AsstFWDefltAssistX_HwNm_u8p8[15]	973
t_AsstFWDefltAssistX_HwNm_u8p8[16]	998
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1075
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7578
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t_AsstFWPstepNstepThresh_Cnt_u16[0]	220
t_AsstFWPstepNstepThresh_Cnt_u16[1]	599
t_AsstFWVehSpd_Kph_u9p7[0]	24960
t_AsstFWVehSpd_Kph_u9p7[1]	25088
t_AsstFWVehSpd_Kph_u9p7[2]	25216
t_AsstFWVehSpd_Kph_u9p7[3]	25344
t_AsstFWVehSpd_Kph_u9p7[4]	25472
t_AsstFWVehSpd_Kph_u9p7[5]	25600
t_AsstFWVehSpd_Kph_u9p7[6]	25728
t_AsstFWVehSpd_Kph_u9p7[7]	25856
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.5
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.11000013
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7.32999992
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	209.399994
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Id	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
5	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tot Rte Inst Ap AssistFirewall AssistFirewall Per1 HwTorque HwNm f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.43400002	5.43400002 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	599	599 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.70019531	3.70019531 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.24259996	-5.24259996 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.48147964	5.48147964 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.82499981	5.82499981 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.70019531	3.70019531 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T			<b>✓</b>	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	•

Test Step 2.100 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	5.5999999
AssistFirewall ActiveKSV M str.K UIs f32	0.0130000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8979
AssistFirewall AsstReducedPerfSV Cnt M Igc	0
AssistFirewall CombAsstSV MtrNm M f32	7.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.119999997
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11600006
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall LwrBoundKSV M str.K Uls f32	0.159999996
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.19999981
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.25999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.19999981
k AsstFWInpLimitHFA MtrNm f32	6.44999981
k_AsstFWInpLimitHysComp_MtrNm_f32	7.1500001
k_AsstFWNstep_Cnt_u16	1053
k_AsstFWPstep_Cnt_u16	2952
k RestoreThresh MtrNm f32	4.46999979
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2 AsstFWUprBoundX HwNm s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096 2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096 6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240 -8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6] t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9] t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_Asst WopiBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_Asst WopiodidA_nwin_s4p11[6][1] t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_Asst WopiBoundX_HwNm_s4p11[6][3]	0
t2_Asst WopiBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_Asst WopiBoundX_FWNin_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HWNm_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7] t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-1238
t2_AsstFWUprBoundX_HwNm_s4p11[7][2] t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-102 <del>4</del> 0 -8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_Asst WopiounuX_1Wini_s4p11[7][7] t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_Asst WopiBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096
t2_AsstFWUprBoundX_mwnm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-28672 -26624
	-26524 -24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-24576 -22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-14336





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	18432
	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096
	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-4096 -2048





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	614
t_AsstFWDefltAssistX_HwNm_u8p8[1]	640
t_AsstFWDefltAssistX_HwNm_u8p8[2]	666
t_AsstFWDefltAssistX_HwNm_u8p8[3]	691
t_AsstFWDefltAssistX_HwNm_u8p8[4]	717
t_AsstFWDefltAssistX_HwNm_u8p8[5]	742
t_AsstFWDefltAssistX_HwNm_u8p8[6]	768
t_AsstFWDefltAssistX_HwNm_u8p8[7]	794
t_AsstFWDefltAssistX_HwNm_u8p8[8]	819
t_AsstFWDefltAssistX_HwNm_u8p8[9]	845 870
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	896
t_AsstFWDefltAssistX_HwNm_u8p8[12]	922
t_AsstFWDefltAssistX_HwNm_u8p8[13]	947
t_AsstFWDefltAssistX_HwNm_u8p8[14]	973
t_AsstFWDefltAssistX_HwNm_u8p8[15]	998
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1101
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4710 4915
t_AsstFWDefltAssistY_MtrNm_s4p11[5] t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5120
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[18] t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7578 7782
t AsstFWPstepNstepThresh Cnt u16[0]	221
t_AsstFWPstepNstepThresh_Cnt_u16[1]	603
t_AsstFWVehSpd_Kph_u9p7[0]	27904
t_AsstFWVehSpd_Kph_u9p7[1]	28032
t_AsstFWVehSpd_Kph_u9p7[2]	28160
t_AsstFWVehSpd_Kph_u9p7[3]	28288
t_AsstFWVehSpd_Kph_u9p7[4]	28416
t_AsstFWVehSpd_Kph_u9p7[5]	28544
t_AsstFWVehSpd_Kph_u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7]	28800
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.5999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.19999981
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7.21999979 7.44000006
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	220.5
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	•
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

2015-03-23, 11:55:49+0530



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.52719975	5.52720022 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	603	603 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.79980469	3.79980469 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.31799984	-5.31799984 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.67999983	5.67999983 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.14799976	6.14799976 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.79980469	3.79980469 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.101 (Repeat Count = 1)	v v
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	5.6999981
AssistFirewall ActiveKSV M str.K Uls f32	0.0140000004
AssistFirewall ActiveRawAcc Cnt M u16	9102
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.69999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.129999995
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11699998
AssistFirewall LwrBoundKSV M str.SV Uls f32	6.099999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.170000002
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.30000019
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.270000011
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.3000019
k_AsstFWInpLimitHFA_MtrNm_f32	6.46000004
k_AsstFWInpLimitHysComp_MtrNm_f32	7.26000023
k_AsstFWNstep_Cnt_u16	53
k_AsstFWPstep_Cnt_u16	3075
k_RestoreThresh_MtrNm_f32	4.48000002
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144
= , = = 1	1

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288 14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10] t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_Asst WopisoundX_1wNin_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-12288

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_Asst Wopibound1_intrini_s4p11[1][10] t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
t2_Asst Wopibound1_intrini_s4p11[4][6] t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2046





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	640
t_AsstFWDefltAssistX_HwNm_u8p8[1]	666
t_AsstFWDefltAssistX_HwNm_u8p8[2]	691
t_AsstFWDefltAssistX_HwNm_u8p8[3]	717
t_AsstFWDefltAssistX_HwNm_u8p8[4]	742
t_AsstFWDefltAssistX_HwNm_u8p8[5]	768
t_AsstFWDefltAssistX_HwNm_u8p8[6]	794
t_AsstFWDefltAssistX_HwNm_u8p8[7]	819
t_AsstFWDefltAssistX_HwNm_u8p8[8]	845
t_AsstFWDefltAssistX_HwNm_u8p8[9]	870
t_AsstFWDefltAssistX_HwNm_u8p8[10]	896
t_AsstFWDefltAssistX_HwNm_u8p8[11]	922
t_AsstFWDefltAssistX_HwNm_u8p8[12]	947
t_AsstFWDefltAssistX_HwNm_u8p8[13]	973
t_AsstFWDefltAssistX_HwNm_u8p8[14]	998
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[18] t AsstFWDefltAssistX_HwNm_u8p8[19]	1101 1126
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	4096
t_AsstFWDefitAssistY_MtrNm_s4p11[1]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7987
t_AsstFWPstepNstepThresh_Cnt_u16[0]	222
t_AsstFWPstepNstepThresh_Cnt_u16[1]	607
t_AsstFWVehSpd_Kph_u9p7[0] t_AsstFWVehSpd_Kph_u9p7[1]	30848 30976
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	31104
t_AsstFWVehSpd_Kph_u9p7[3]	31232
t_AsstFWVehSpd_Kph_u9p7[4]	31360
t_AsstFWVehSpd_Kph_u9p7[5]	31488
t AsstFWVehSpd Kph u9p7[6]	31616
t_AsstFWVehSpd_Kph_u9p7[7]	31744
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.69999981
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.88999987
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.32999992
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7.55000019
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	231.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.62019968	5.62020016 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	607	607 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.89990234	3.89990234 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-3.86439991	-3.86439991 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.98903036	6.98903036 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.78900003	3.78900003 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.89990234	3.89990234 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.102 (Repeat Count = 1)	🗸 🗸 - The state of the state
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.80000019
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0149999997
AssistFirewall_ActiveRawAcc_Cnt_M_u16	9225
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.140000001
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11800003
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.19999981
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.180000007
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.4000001
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.280000001
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.4000001
k_AsstFWInpLimitHFA_MtrNm_f32	6.46999979
k_AsstFWInpLimitHysComp_MtrNm_f32	7.36999989
k_AsstFWNstep_Cnt_u16	123
k_AsstFWPstep_Cnt_u16	3198
k_RestoreThresh_MtrNm_f32	4.48999977
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2 AsstFWUprBoundX HwNm s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_1WNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192 -24576
t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-24576
t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-24576 -22528
t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-24576 -22528 -20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-24576 -22528 -20480 -18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-24576 -22528 -20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-24576 -22528 -20480 -18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-24576 -22528 -20480 -18432 -16384

AssistFirewall\_Per1



Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528
t2_Asst WopiBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	12288
t2_Asst WuprBoundY_MtrNm_s4p11[4][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
t2_Asst WopiBoundY_MtrNm_s4p11[7][0]	0
t2_Asst WopiBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	0
t_AsstFWDefltAssistX_HwNm_u8p8[1]	0
t_AsstFWDefltAssistX_HwNm_u8p8[2]	0
t_AsstFWDefltAssistX_HwNm_u8p8[3]	0
t_AsstFWDefltAssistX_HwNm_u8p8[4]	0
t_AsstFWDefltAssistX_HwNm_u8p8[5]	0
t_AsstFWDefltAssistX_HwNm_u8p8[6]	0
t_AsstFWDefltAssistX_HwNm_u8p8[7]	
t_AsstFWDefltAssistX_HwNm_u8p8[8] t_AsstFWDefltAssistX_HwNm_u8p8[9]	0
t_AsstFWDefltAssistX_HwNm_u8p8[10]	0
t_AsstFWDefltAssistX_HwNm_u8p8[11]	0
t_AsstFWDefltAssistX_HwNm_u8p8[12]	0
t_AsstFWDefltAssistX_HwNm_u8p8[13]	0
t_AsstFWDefltAssistX_HwNm_u8p8[14]	0
t_AsstFWDefltAssistX_HwNm_u8p8[15]	0
t_AsstFWDefltAssistX_HwNm_u8p8[16]	0
t_AsstFWDefltAssistX_HwNm_u8p8[17]	0
t_AsstFWDefltAssistX_HwNm_u8p8[18]	0
t_AsstFWDefltAssistX_HwNm_u8p8[19]	0
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6554 6758
t_AsstFWDefltAssistY_MtrNm_s4p11[12] t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6963
t_AsstFWDefitAssistY_MtrNm_s4p11[14]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7373
t AsstFWDefltAssistY_MtrNm_s4p11[16]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	8192
t_AsstFWPstepNstepThresh_Cnt_u16[0]	223
t_AsstFWPstepNstepThresh_Cnt_u16[1]	611
t_AsstFWVehSpd_Kph_u9p7[0]	33792
t_AsstFWVehSpd_Kph_u9p7[1]	33920
t_AsstFWVehSpd_Kph_u9p7[2]	34048
t_AsstFWVehSpd_Kph_u9p7[3]	34176
t_AsstFWVehSpd_Kph_u9p7[4]	34304
t_AsstFWVehSpd_Kph_u9p7[5]	34432
t_AsstFWVehSpd_Kph_u9p7[6]	34560
t_AsstFWVehSpd_Kph_u9p7[7]	34688
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.67000008
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7.65999985
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	222 100007
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	222.199997 tot AccietEirouall Port AcctEirouallActivo Llle f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tot Rte Inst An AssistFirewall AssistFirewall Per1 Defeat Assith Service Cot II	, .g, .co.croman_r or r_boroat_/.co.rbi_Ocrvice_Orit_igo
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt	tot AssistFirewall Per1 HighFregAssist MtrNm f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	,

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.7130003	5.71299982 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	611	611 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	4	4 ± 4.88E-04	✓
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-2.29439998	-2.29439998 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.34399986	6.34399986 ± 4.88E-04	✓
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>~</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.04800034	4.04799986 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4	4 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.103 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.9000001
AssistFirewall ActiveKSV M str.K Uls f32	0.0160000008
AssistFirewall_ActiveRawAcc_Cnt_M_u16	9348
AssistFirewall AsstReducedPerfSV Cnt M Igc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.150000006
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11899996
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.30000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.189999998
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.289999992
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.5
k_AsstFWInpLimitHFA_MtrNm_f32	6.48000002
k_AsstFWInpLimitHysComp_MtrNm_f32	7.48000002
k_AsstFWNstep_Cnt_u16	234
k_AsstFWPstep_Cnt_u16	3321
k RestoreThresh MtrNm f32	5.51000023
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048

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Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-2048	
	-2040	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]		
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384	
	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]		
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-8192	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480 22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	4096
t2_Asst WopiBoundY_MtrNm_s4p11[2][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	14336
t2_Asst WopiBoundY_MtrNm_s4p11[2][7]	16384
t2_Asst WopiBoundY_MtrNm_s4p11[2][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528 0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144
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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefitAssistX_HwNm_u8p8[0]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[1]	2560
t AsstFWDefltAssistX HwNm u8p8[2]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[3]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[4]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[5]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[6]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[7]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[8]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[9]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[10]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[11]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[12]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[13]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[14]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[15] t_AsstFWDefltAssistX_HwNm_u8p8[16]	2560 2560
t_AsstFWDefitAssistX_HwNm_u8p8[16]  t_AsstFWDefitAssistX_HwNm_u8p8[17]	2560
t_AsstFWDefitAssistX_HwNm_u8p8[18]	2560
t_AsstFWDefitAssistX_HwNm_u8p8[19]	2560
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[12] t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6963 7168
t AsstFWDefltAssistY MtrNm s4p11[14]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	8397
t_AsstFWPstepNstepThresh_Cnt_u16[0]	224
t_AsstFWPstepNstepThresh_Cnt_u16[1]	615
t_AsstFWVehSpd_Kph_u9p7[0]	36736
t_AsstFWVehSpd_Kph_u9p7[1]	36864
t_AsstFWVehSpd_Kph_u9p7[2]	36992
t_AsstFWVehSpd_Kph_u9p7[3]	37120
t_AsstFWVehSpd_Kph_u9p7[4]	37248
t_AsstFWVehSpd_Kph_u9p7[5]	37376
t_AsstFWVehSpd_Kph_u9p7[6]	37504
t_AsstFWVehSpd_Kph_u9p7[7]	37632 6.78000034
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	6.78000021 0
tgt_AssistFireWall_Per1_Deteat_Assist_MtrNm_f32.value	7.11000013
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.55000019
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.31999969
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	253.100006
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFirewall\_AssistFi$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.80560017	5.80560017 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	615	615 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	2.20019531	2.20019531 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.33899975	7.33900023 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.19300032	7.19299984 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.32499981	4.32499981 ± 4.88E-04	•
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	2.20019531	2.20019531 ± 9.77E-04	•
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.104 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6
AssistFirewall ActiveKSV M str.K Uls f32	0.0170000009
AssistFirewall_ActiveRawAcc_Cnt_M_u16	9471
AssistFirewall AsstReducedPerfSV Cnt M lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.159999996
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.4000001
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.200000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.300000012
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.5999999
k_AsstFWInpLimitHFA_MtrNm_f32	6.48999977
k_AsstFWInpLimitHysComp_MtrNm_f32	7.59000015
k_AsstFWNstep_Cnt_u16	345
k_AsstFWPstep_Cnt_u16	3444
k_RestoreThresh_MtrNm_f32	5.51999998
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0





Name  12_AsstFWUprBoundX_HwNm_s4p11[2][1]  12_AsstFWUprBoundX_HwNm_s4p11[2][2]  12_AsstFWUprBoundX_HwNm_s4p11[2][3]  12_AsstFWUprBoundX_HwNm_s4p11[2][4]  12_AsstFWUprBoundX_HwNm_s4p11[2][6]  12_AsstFWUprBoundX_HwNm_s4p11[2][7]  12_AsstFWUprBoundX_HwNm_s4p11[2][8]  12_AsstFWUprBoundX_HwNm_s4p11[2][9]  12_AsstFWUprBoundX_HwNm_s4p11[2][9]  12_AsstFWUprBoundX_HwNm_s4p11[2][10]  12_AsstFWUprBoundX_HwNm_s4p11[3][0]  12_AsstFWUprBoundX_HwNm_s4p11[3][1]  12_AsstFWUprBoundX_HwNm_s4p11[3][1]  12_AsstFWUprBoundX_HwNm_s4p11[3][2]  12_AsstFWUprBoundX_HwNm_s4p11[3][6]  12_AsstFWUprBoundX_HwNm_s4p11[3][6]  12_AsstFWUprBoundX_HwNm_s4p11[3][6]  12_AsstFWUprBoundX_HwNm_s4p11[3][7]  12_AsstFWUprBoundX_HwNm_s4p11[3][6]  12_AsstFWUprBoundX_HwNm_s4p11[3][6]  12_AsstFWUprBoundX_HwNm_s4p11[3][6]  12_AsstFWUprBoundX_HwNm_s4p11[3][6]	Input Value 2048 4096 6144 8192 10240 12288 14336 16384 18432 20480 -6144 -4096 -2048 0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2] t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4] t2_AsstFWUprBoundX_HwNm_s4p11[2][5] t2_AsstFWUprBoundX_HwNm_s4p11[2][6] t2_AsstFWUprBoundX_HwNm_s4p11[2][7] t2_AsstFWUprBoundX_HwNm_s4p11[2][8] t2_AsstFWUprBoundX_HwNm_s4p11[2][9] t2_AsstFWUprBoundX_HwNm_s4p11[2][10] t2_AsstFWUprBoundX_HwNm_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][1] t2_AsstFWUprBoundX_HwNm_s4p11[3][1] t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096 6144 8192 10240 12288 14336 16384 18432 20480 -6144 -4096 -2048 0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3] t2_AsstFWUprBoundX_HwNm_s4p11[2][4] t2_AsstFWUprBoundX_HwNm_s4p11[2][6] t2_AsstFWUprBoundX_HwNm_s4p11[2][6] t2_AsstFWUprBoundX_HwNm_s4p11[2][7] t2_AsstFWUprBoundX_HwNm_s4p11[2][8] t2_AsstFWUprBoundX_HwNm_s4p11[2][9] t2_AsstFWUprBoundX_HwNm_s4p11[2][10] t2_AsstFWUprBoundX_HwNm_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][1] t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144 8192 10240 12288 14336 16384 18432 20480 -6144 -4096 -2048 0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4] t2_AsstFWUprBoundX_HwNm_s4p11[2][5] t2_AsstFWUprBoundX_HwNm_s4p11[2][6] t2_AsstFWUprBoundX_HwNm_s4p11[2][7] t2_AsstFWUprBoundX_HwNm_s4p11[2][8] t2_AsstFWUprBoundX_HwNm_s4p11[2][9] t2_AsstFWUprBoundX_HwNm_s4p11[2][10] t2_AsstFWUprBoundX_HwNm_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][1] t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192 10240 12288 14336 16384 18432 20480 -6144 -4096 -2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4] t2_AsstFWUprBoundX_HwNm_s4p11[2][5] t2_AsstFWUprBoundX_HwNm_s4p11[2][6] t2_AsstFWUprBoundX_HwNm_s4p11[2][7] t2_AsstFWUprBoundX_HwNm_s4p11[2][8] t2_AsstFWUprBoundX_HwNm_s4p11[2][9] t2_AsstFWUprBoundX_HwNm_s4p11[2][10] t2_AsstFWUprBoundX_HwNm_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][1] t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240 12288 14336 16384 18432 20480 -6144 -4096 -2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5] t2_AsstFWUprBoundX_HwNm_s4p11[2][6] t2_AsstFWUprBoundX_HwNm_s4p11[2][7] t2_AsstFWUprBoundX_HwNm_s4p11[2][8] t2_AsstFWUprBoundX_HwNm_s4p11[2][9] t2_AsstFWUprBoundX_HwNm_s4p11[2][10] t2_AsstFWUprBoundX_HwNm_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][1] t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240 12288 14336 16384 18432 20480 -6144 -4096 -2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6] t2_AsstFWUprBoundX_HwNm_s4p11[2][7] t2_AsstFWUprBoundX_HwNm_s4p11[2][8] t2_AsstFWUprBoundX_HwNm_s4p11[2][9] t2_AsstFWUprBoundX_HwNm_s4p11[2][10] t2_AsstFWUprBoundX_HwNm_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][1] t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288 14336 16384 18432 20480 -6144 -4096 -2048 0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7] t2_AsstFWUprBoundX_HwNm_s4p11[2][8] t2_AsstFWUprBoundX_HwNm_s4p11[2][9] t2_AsstFWUprBoundX_HwNm_s4p11[2][10] t2_AsstFWUprBoundX_HwNm_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][1] t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	14336 16384 18432 20480 -6144 -4096 -2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8] t2_AsstFWUprBoundX_HwNm_s4p11[2][9] t2_AsstFWUprBoundX_HwNm_s4p11[2][10] t2_AsstFWUprBoundX_HwNm_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][1] t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][3] t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	16384 18432 20480 -6144 -4096 -2048 0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9] t2_AsstFWUprBoundX_HwNm_s4p11[2][10] t2_AsstFWUprBoundX_HwNm_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][1] t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][3] t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][5] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	18432 20480 -6144 -4096 -2048 0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10] t2_AsstFWUprBoundX_HwNm_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][1] t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][3] t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][5] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	20480 -6144 -4096 -2048 0 2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][1] t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][3] t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][5] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-6144 -4096 -2048 0 2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][1] t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][3] t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][5] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096 -2048 0 2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][3] t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][5] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048 0 2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3] t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][5] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0 2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3] t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][5] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][5] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5] t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6] t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][7] t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
	8192
	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-10240
	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2 AsstFWUprBoundX HwNm s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	<b>-8192</b>
	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-6144

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7.00.001 11.0Wall_1 0.11	
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	12288
t2_AsstrWUprBoundY_MtrNm_s4p11[1][4]	14336
	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-8192
	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	4096
10. A (E)A(() D 1)/ A (; ) )	0444
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144 8192





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480 22528
t_AsstFWDefitAssistX_HwNm_u8p8[0]	717
t_AsstFWDefltAssistX_HwNm_u8p8[1]	742
t AsstFWDefltAssistX HwNm u8p8[2]	768
t_AsstFWDefltAssistX_HwNm_u8p8[3]	794
t_AsstFWDefltAssistX_HwNm_u8p8[4]	819
t_AsstFWDefltAssistX_HwNm_u8p8[5]	845
t_AsstFWDefltAssistX_HwNm_u8p8[6]	870
t_AsstFWDefltAssistX_HwNm_u8p8[7]	896
t_AsstFWDefltAssistX_HwNm_u8p8[8]	922
t_AsstFWDefltAssistX_HwNm_u8p8[9]	947
t_AsstFWDefltAssistX_HwNm_u8p8[10]	973
t_AsstFWDefltAssistX_HwNm_u8p8[11]	998
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1126
t_AsstFWDefitAssistX_HwNm_u8p8[17]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1203
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[2] t_AsstFWDefltAssistY_MtrNm_s4p11[3]	5120 5325
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	5530
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5939
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	8602
t_AsstFWPstepNstepThresh_Cnt_u16[0]	225
t_AsstFWPstepNstepThresh_Cnt_u16[1]	619
t_AsstFWVehSpd_Kph_u9p7[0]	39680
t_AsstFWVehSpd_Kph_u9p7[1]	39808
t_AsstFWVehSpd_Kph_u9p7[2]	39936
t_AsstFWVehSpd_Kph_u9p7[3]	40064
t_AsstFWVehSpd_Kph_u9p7[4]	40192
t_AsstFWVehSpd_Kph_u9p7[5] t AsstFWVehSpd Kph u9p7[6]	40320 40448
t_AsstFWVenSpd_Kph_u9p7[6] t_AsstFWVehSpd_Kph_u9p7[7]	40448
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.8899987
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.21999979
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.65999985
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.43000031
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	12.3999996
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.89799976	5.89799976 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	619	619 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.20019531	4.20019531 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.60080051	7.60080004 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.11999989	7.11999989 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-3.8499999	-3.8499999 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4.20019531	4.20019531 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.105 (Repeat Count = 1)	la de la companya de
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.099999
AssistFirewall ActiveKSV M str.K Uls f32	0.0179999992
AssistFirewall_ActiveRawAcc_Cnt_M_u16	9594
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	7.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.170000002
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12100005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.20999993
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.5999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.310000002
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.69999981
k_AsstFWInpLimitHFA_MtrNm_f32	6.5
k_AsstFWInpLimitHysComp_MtrNm_f32	7.69999981
k_AsstFWNstep_Cnt_u16	456
k_AsstFWPstep_Cnt_u16	3567
k_RestoreThresh_MtrNm_f32	5.53000021
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-18432



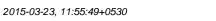


Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[7][0]  2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-12288
	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-4096





Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	0
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	26624
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	28672
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	20480
	22528
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	26624
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][3] 2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144 8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9] 2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336 4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][10] 2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	4096
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Assistrirewaii_Peri	
Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576
_AsstFWDefltAssistX_HwNm_u8p8[0]	742
_AsstFWDefltAssistX_HwNm_u8p8[1]	768
_AsstFWDefltAssistX_HwNm_u8p8[2]	794
_AsstFWDefltAssistX_HwNm_u8p8[3]	819
AsstFWDefltAssistX HwNm u8p8[4]	845
_AsstFWDefitAssistX_HwNm_u8p8[5]	870
_AsstFWDefitAssistX_HwNm_u8p8[6]	896
_AsstFWDefltAssistX_HwNm_u8p8[7]	922
_AsstFWDefltAssistX_HwNm_u8p8[8]	947
_AsstFWDefitAssistX_HwNm_u8p8[9]	973
_AsstFWDefltAssistX_HwNm_u8p8[10]	998
_AsstFWDefltAssistX_HwNm_u8p8[11]	1024
_AsstFWDefltAssistX_HwNm_u8p8[12]	1050
_AsstFWDefltAssistX_HwNm_u8p8[13]	1075
_AsstFWDefltAssistX_HwNm_u8p8[14]	1101
_AsstFWDefltAssistX_HwNm_u8p8[15]	1126
_AsstFWDefltAssistX_HwNm_u8p8[16]	1152
_AsstFWDefltAssistX_HwNm_u8p8[17]	1178
_AsstFWDefltAssistX_HwNm_u8p8[18]	1203
_AsstFWDefltAssistX_HwNm_u8p8[19]	1229
_AsstFWDefltAssistY_MtrNm_s4p11[0]	-205
_AsstFWDefltAssistY_MtrNm_s4p11[1]	-205
_AsstFWDefltAssistY_MtrNm_s4p11[2]	-205
_AsstFWDefltAssistY_MtrNm_s4p11[3]	-205
_AsstFWDefltAssistY_MtrNm_s4p11[4]	-205
_AsstFWDefltAssistY_MtrNm_s4p11[5]	-205
_AsstFWDefltAssistY_MtrNm_s4p11[6]	-205
_AsstFWDefltAssistY_MtrNm_s4p11[7]	-205
_AsstFWDefltAssistY_MtrNm_s4p11[8]	-205
_AsstFWDefltAssistY_MtrNm_s4p11[9]	-205
_AsstFWDefltAssistY_MtrNm_s4p11[10]	-205
_AsstFWDefltAssistY_MtrNm_s4p11[11]	-205
_AsstFWDefltAssistY_MtrNm_s4p11[12]	-205
_AsstFWDefltAssistY_MtrNm_s4p11[13]	-205
AsstFWDefitAssistY MtrNm s4p11[14]	-205
_AsstFWDefitAssistY_MtrNm_s4p11[15]	-205
_AsstFWDefitAssistY_MtrNm_s4p11[16]	-205 -205
_AsstFWDefitAssistY_MtrNm_s4p11[17]	-205
_AsstFWDefltAssistY_MtrNm_s4p11[18]	-205
_AsstFWDefltAssistY_MtrNm_s4p11[19]	-205
_AsstFWPstepNstepThresh_Cnt_u16[0]	226
_AsstFWPstepNstepThresh_Cnt_u16[1]	623
_AsstFWVehSpd_Kph_u9p7[0]	42624
_AsstFWVehSpd_Kph_u9p7[1]	42752
_AsstFWVehSpd_Kph_u9p7[2]	42880
_AsstFWVehSpd_Kph_u9p7[3]	43008
_AsstFWVehSpd_Kph_u9p7[4]	43136
_AsstFWVehSpd_Kph_u9p7[5]	43264
_AsstFWVehSpd_Kph_u9p7[6]	43392
_AsstFWVehSpd_Kph_u9p7[7]	43520
gt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7
gt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
gt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.32999992
gt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.76999998
gt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.0999999
gt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
gt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	19.5
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
goor_rp_rooton nowan.rooton newan_r or r_baseAssistOffia_ivittiVIII_l32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
THE THE THE AN AssistEirowall AssistEirowall Dord CombinedAssist Mitches (22)	tgt_nooioti itewaii_r et i _outrioitteu/Aooiot_WithVIII_102
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tat AssistEirowall Bort Dofoat AsstThi Sonias Cat las
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_It_	
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_Itgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
gt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_legt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32

AssistFirewall\_Per1





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.99020004	5.99020004 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	623	623 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-0.100097656	-0.100097656 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.68900013	5.68900013 ± 4.88E-04	<b>~</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.0250001	7.0250001 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-3.5539999	-3.5539999 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-0.100097656	-0.100097656 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>~</b>
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>~</b>

T			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.106 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.1999981
AssistFirewall ActiveKSV M str.K Uls f32	0.0189999994
AssistFirewall_ActiveRawAcc_Cnt_M_u16	9717
AssistFirewall AsstReducedPerfSV Cnt M lqc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.69999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.180000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12199998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.5999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.219999999
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.69999981
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.319999993
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.80000019
k_AsstFWInpLimitHFA_MtrNm_f32	6.51000023
k_AsstFWInpLimitHysComp_MtrNm_f32	7.80999994
k_AsstFWNstep_Cnt_u16	567
k_AsstFWPstep_Cnt_u16	3690
k_RestoreThresh_MtrNm_f32	5.53999996
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	
	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_Asst WopfboundX_HwNm_s4p11[5][1]	-10240
	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_Asst WopiBoundX_HwNm_s4p11[7][7] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_Asst WopiBoundX_HwNm_s4p11[7][2] t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
. = - , , n.,	18432
t2 AsstFWUprBoundY MtrNm s4p11[6][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	768
t_AsstFWDefltAssistX_HwNm_u8p8[1]	794
t_AsstFWDefltAssistX_HwNm_u8p8[2]	819
t_AsstFWDefltAssistX_HwNm_u8p8[3]	845
t_AsstFWDefltAssistX_HwNm_u8p8[4]	870
t_AsstFWDefltAssistX_HwNm_u8p8[5]	896
t_AsstFWDefltAssistX_HwNm_u8p8[6]	922
t_AsstFWDefltAssistX_HwNm_u8p8[7]	947
t_AsstFWDefltAssistX_HwNm_u8p8[8]	973
t_AsstFWDefltAssistX_HwNm_u8p8[9]	998
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[13] t_AsstFWDefltAssistX_HwNm_u8p8[14]	1101 1126
t_AsstFWDefitAssistX_HwNm_u8p8[14]  t_AsstFWDefitAssistX_HwNm_u8p8[15]	1152
t_AsstFWDefitAssistX_HwNm_u8p8[16]	1178
t_AsstFWDefitAssistX_HwNm_u8p8[17]	1203
t_AsstFWDefitAssistX_HwNm_u8p8[18]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1254
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[11] t_AsstFWDefltAssistY_MtrNm_s4p11[12]	32767 32767
t AsstFWDefltAssistY MtrNm s4p11[13]	32767
t AsstFWDefitAssistY MtrNm s4p11[14]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	32767
t_AsstFWPstepNstepThresh_Cnt_u16[0]	227
t_AsstFWPstepNstepThresh_Cnt_u16[1]	627
t_AsstFWVehSpd_Kph_u9p7[0]	45568
t_AsstFWVehSpd_Kph_u9p7[1]	45696
t_AsstFWVehSpd_Kph_u9p7[2]	45824
t_AsstFWVehSpd_Kph_u9p7[3]	45952
t_AsstFWVehSpd_Kph_u9p7[4]	46080
t_AsstFWVehSpd_Kph_u9p7[5]	46208
t_AsstFWVehSpd_Kph_u9p7[6]	46336
t_AsstFWVehSpd_Kph_u9p7[7]	46464
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	7.11000013
tgt_AssistFirewall_Per1_Deteat_Assist_MtrNm_f32.value  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.44000006
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.88000011
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.19999981
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	26.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.08220005	6.08220005 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	627	627 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.78980017	5.78980017 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.90799999	6.90799999 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-3.23599982	-3.23600006 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.107 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.30000019
AssistFirewall ActiveKSV M str.K Uls f32	0.019999996
AssistFirewall_ActiveRawAcc_Cnt_M_u16	9840
AssistFirewall AsstReducedPerfSV Cnt M lqc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.18999998
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12300003
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.69999981
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.230000004
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.330000013
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.9000001
k_AsstFWInpLimitHFA_MtrNm_f32	6.51999998
k_AsstFWInpLimitHysComp_MtrNm_f32	7.92000008
k_AsstFWNstep_Cnt_u16	678
k_AsstFWPstep_Cnt_u16	3813
k_RestoreThresh_MtrNm_f32	5.55000019
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	0





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048
t2_Asst Wopibound1_MtrNm_s4p11[1][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7] t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1] t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10] t_AsstFWDefltAssistX_HwNm_u8p8[0]	794
t_AsstFWDefitAssistX_HwNm_u8p8[1]	819
t_AsstFWDefltAssistX_HwNm_u8p8[2]	845
t_AsstFWDefltAssistX_HwNm_u8p8[3]	870
t_AsstFWDefltAssistX_HwNm_u8p8[4]	896
t_AsstFWDefltAssistX_HwNm_u8p8[5]	922
t_AsstFWDefltAssistX_HwNm_u8p8[6]	947
t_AsstFWDefltAssistX_HwNm_u8p8[7]	973
t_AsstFWDefltAssistX_HwNm_u8p8[8]	998
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1280
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2458
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2662
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2867
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3277 3482
t_AsstFWDefltAssistY_MtrNm_s4p11[5] t_AsstFWDefltAssistY_MtrNm_s4p11[6]	3686
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	3891
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4506
t AsstFWDefltAssistY MtrNm s4p11[11]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6349
t_AsstFWPstepNstepThresh_Cnt_u16[0]	228
t_AsstFWPstepNstepThresh_Cnt_u16[1]	631
t_AsstFWVehSpd_Kph_u9p7[0]	1408
t_AsstFWVehSpd_Kph_u9p7[1]	1536
t_AsstFWVehSpd_Kph_u9p7[2]	1664
t_AsstFWVehSpd_Kph_u9p7[3]	1792
t_AsstFWVehSpd_Kph_u9p7[4]	1920
t_AsstFWVehSpd_Kph_u9p7[5]	2048
t_AsstFWVehSpd_Kph_u9p7[6]	2176
t_AsstFWVehSpd_Kph_u9p7[7]	2304
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7.21999979
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	0 7.55000019
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.98999977
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.3000019
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	33.099985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
, , , , , , , , , , , , , , , , , , , ,	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_/tosioti irewaii_i eri_iwee_oodiitoi_ont_ondiii

AssistFirewall\_Per1



Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.17400026	6.17399979 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	9162	9162 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.10009766	3.10009766 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.88879967	5.88880014 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.38899994	5.38899994 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.72699976	7.72700024 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.10009766	3.10009766 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T ✓				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>✓</b>

Test Step 2.108 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.4000001
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0209999997
AssistFirewall_ActiveRawAcc_Cnt_M_u16	9963
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.69999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.200000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12399995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.80000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.23999995
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.19999981
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.340000004
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6
k_AsstFWInpLimitHFA_MtrNm_f32	6.53000021
k_AsstFWInpLimitHysComp_MtrNm_f32	8.02999973
k_AsstFWNstep_Cnt_u16	789
k_AsstFWPstep_Cnt_u16	3936
k_RestoreThresh_MtrNm_f32	5.55999994
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_Asst WopiBoundX_HwNm_s4p11[2][4]	-4096
	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10] t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0] t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	
	-4096 2049
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144
, – – 1 1 1 1 1 1 1	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048

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Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048
z_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096
	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144 -4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144
2 AsstFWUprBoundY MtrNm s4p11[5][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-2040
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
1 . 2.3	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480 819
t_AsstFWDefltAssistX_HwNm_u8p8[0]	845
t_AsstFWDefltAssistX_HwNm_u8p8[1] t_AsstFWDefltAssistX_HwNm_u8p8[2]	870
t_AsstFWDefltAssistX_HwNm_u8p8[3]	896
t_AsstFWDefltAssistX_HwNm_u8p8[4]	922
t_AsstFWDefltAssistX_HwNm_u8p8[5]	947
t_AsstFWDefltAssistX_HwNm_u8p8[6]	973
t_AsstFWDefltAssistX_HwNm_u8p8[7]	998
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1306
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	23962
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	24166
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	24371
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	24781 24986
t_AsstFWDefltAssistY_MtrNm_s4p11[5] t_AsstFWDefltAssistY_MtrNm_s4p11[6]	25190
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	25395
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	25600
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	25805
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	26010
t AsstFWDefltAssistY MtrNm s4p11[11]	26214
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	26419
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	26829
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	27034
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	27238
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	27443
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	27648
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	27853
t_AsstFWPstepNstepThresh_Cnt_u16[0]	229
t_AsstFWPstepNstepThresh_Cnt_u16[1]	635
t_AsstFWVehSpd_Kph_u9p7[0]	4352
t_AsstFWVehSpd_Kph_u9p7[1]	4480
t_AsstFWVehSpd_Kph_u9p7[2]	4608
t_AsstFWVehSpd_Kph_u9p7[3]	4736
t_AsstFWVehSpd_Kph_u9p7[4]	4864
t_AsstFWVehSpd_Kph_u9p7[5]	4992
t_AsstFWVehSpd_Kph_u9p7[6]	5120 5248
t_AsstFWVehSpd_Kph_u9p7[7] tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7.32999992
tgt_AssistFirewall_Per1_BaseAssistCmd_intrinm_t32.value tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgc.value	7.32999992 0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.65999985
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8.10000038
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.31999969
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	40.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tot Dto Inst An AssistEirowell AssistEirowell Dorf MEC Counter Cot anum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	ig_noon noman_ren_mee_counter_ona_m

AssistFirewall\_Per1

NTC\_Cnt\_T\_enum

Param\_Cnt\_T\_u08

Status\_Cnt\_T\_enum

NTC\_Cnt\_T\_enum

Param\_Cnt\_T\_u08

Status\_Cnt\_T\_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.2656002	6.2656002 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	9174	9174 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	8.67199993	8.67199993 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.97487545	4.97487497 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8.42559338	8.42559338 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tot AssistFirewall Per1 CombinedAssist MtrNm f32.value	8.80000019	8.80000019 ± 9.77E-04	<b>✓</b>

0xC6

0x01

0x00

0xC9

0x01

0x01

0xC6

0x01

0x00

0xC9

0x01

0x01

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	•

Test Step 2.109 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.5
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0219999999
AssistFirewall_ActiveRawAcc_Cnt_M_u16	10086
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.20999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.125
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.9000001
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.25
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.30000019
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.349999994
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6.099999
k_AsstFWInpLimitHFA_MtrNm_f32	6.53999996
k_AsstFWInpLimitHysComp_MtrNm_f32	8.14000034
k_AsstFWNstep_Cnt_u16	900
k_AsstFWPstep_Cnt_u16	4059
k_RestoreThresh_MtrNm_f32	5.55999994
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240
= , = = = 1 ( x.)	

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9] t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192 10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096 2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144 8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6] t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
tz_Asstr-woprboundX_mwnin_s4p11[7][7] t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240
tz_AsstF-wuprBoundY_wtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240 -8192
tz_AsstF-vvuprBoundY_wtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-2046
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	4096
	T000

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][6] 2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0
	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-30720
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	2048
	4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	8192





Name  12_AsstFWUprBoundY_MtrNm_s4p11[7][4]  12_AsstFWUprBoundY_MtrNm_s4p11[7][5]  12_AsstFWUprBoundY_MtrNm_s4p11[7][6]  12_AsstFWUprBoundY_MtrNm_s4p11[7][7]  12_AsstFWUprBoundY_MtrNm_s4p11[7][8]  12_AsstFWUprBoundY_MtrNm_s4p11[7][9]  12_AsstFWUprBoundY_MtrNm_s4p11[7][9]  12_AsstFWUprBoundY_MtrNm_s4p11[7][10]  1_AsstFWDefltAssistX_HwNm_u8p8[0]	Input Value 10240 12288 14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5] t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10304
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	22528
	845
t_AsstFWDefltAssistX_HwNm_u8p8[1]	870
t_AsstFWDefltAssistX_HwNm_u8p8[2]	896
t_AsstFWDefltAssistX_HwNm_u8p8[3]	922
t_AsstFWDefltAssistX_HwNm_u8p8[4]	947
t_AsstFWDefltAssistX_HwNm_u8p8[5]	973
t_AsstFWDefltAssistX_HwNm_u8p8[6]	998
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1126
t AsstFWDefltAssistX HwNm u8p8[12]	1152
	1178
t_AsstFWDefltAssistX_HwNm_u8p8[13]	
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1331
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	-203
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	-201
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	-199
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	-197
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	-195
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	-193
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	-190
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	-188
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	-186
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	-184
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	-182
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	-180
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	-178
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	-176
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	-174
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	-172
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	-170
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	-168
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	-166
t_AsstFWPstepNstepThresh_Cnt_u16[0]	230
t_AsstFWPstepNstepThresh_Cnt_u16[1]	639
t_AsstFWVehSpd_Kph_u9p7[0]	7296
t_AsstFWVehSpd_Kph_u9p7[1]	7424
t_AsstFWVehSpd_Kph_u9p7[2]	7552
t_AsstFWVehSpd_Kph_u9p7[3]	7680
t_AsstFWVehSpd_Kph_u9p7[4]	7808
t_AsstFWVehSpd_Kph_u9p7[5]	7936
t_AsstFWVehSpd_Kph_u9p7[6]	8064
t_AsstFWVehSpd_Kph_u9p7[7]	8192
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7.44000006
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.76999998
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8.21000004
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.43000031
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	47.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.35699987	6.35699987 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	639	639 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-0.0810546875	-0.0810546875 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	8.94580078	8.94579983 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.42500019	6.42500019 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.21848631	6.21848631 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-0.0810546875	-0.0810546875 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T .			V	
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240 12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][0] t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336 -12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2] t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4] t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0 2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336 -12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7] t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9] t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_Asst WopfboundX_1WNIII_s4p11[5][10] t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_Asst WopiBoundX_HwNm_s4p11[6][0] t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2 AsstFWUprBoundX HwNm s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2 AsstFWUprBoundX HwNm s4p11[7][0]	-2048
t2_Asst WoprBoundX_1WNm_s4p11[7][0] t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_Asst WopiBoundX_HwNm_s4p11[7][7]	14336
t2_Asst WopfboundX_1WNIII_s4p11[7][6] t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	6144
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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-8192 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	16384 18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	4096
	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2] t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144 8192 10240





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576 870
t_AsstFWDefltAssistX_HwNm_u8p8[0]	
t_AsstFWDefltAssistX_HwNm_u8p8[1] t_AsstFWDefltAssistX_HwNm_u8p8[2]	896 922
t_AsstFWDefltAssistX_HwNm_u8p8[3]	947
t_AsstFWDefltAssistX_HwNm_u8p8[4]	973
t_AsstFWDefltAssistX_HwNm_u8p8[5]	998
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1075
t_AsstFWDefitAssistX_HwNm_u8p8[9]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1229
t_AsstFWDefitAssistX_HwNm_u8p8[15]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1280
t_AsstFWDefitAssistX_HwNm_u8p8[17]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1331
t_AsstFWDefitAssistX_HwNm_u8p8[19]	1357
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2458
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2662
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2867
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4506
t AsstFWDefltAssistY MtrNm s4p11[11]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6349
t_AsstFWPstepNstepThresh_Cnt_u16[0]	231
t_AsstFWPstepNstepThresh_Cnt_u16[1]	643
t_AsstFWVehSpd_Kph_u9p7[0]	10240
t_AsstFWVehSpd_Kph_u9p7[1]	10368
t_AsstFWVehSpd_Kph_u9p7[2]	10496
t_AsstFWVehSpd_Kph_u9p7[3]	10624
t_AsstFWVehSpd_Kph_u9p7[4]	10752
t_AsstFWVehSpd_Kph_u9p7[5]	10880
t_AsstFWVehSpd_Kph_u9p7[6]	11008
t_AsstFWVehSpd_Kph_u9p7[7]	11136
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7.55000019
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.88000011
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8.31999969
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.53999996
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	54.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
	And Angiet France II Dard MEG. Country Out.
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.44819975	6.44820023 ± 4.88E-04	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	643	643 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.10009766	3.10009766 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	9.22200012	9.22200012 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.22000027	6.21999979 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.29113674	6.29113674 ± 4.88E-04	<b>~</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.10009766	3.10009766 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	•
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	-

Test Step 2.111 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.6999981
AssistFirewall ActiveKSV M str.K Uls f32	0.0240000002
AssistFirewall_ActiveRawAcc_Cnt_M_u16	10332
AssistFirewall AsstReducedPerfSV Cnt M Iqc	1
AssistFirewall CombAsstSV MtrNm M f32	-7.69999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.230000004
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12699997
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.270000011
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.370000005
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6.30000019
k_AsstFWInpLimitHFA_MtrNm_f32	6.55999994
k_AsstFWInpLimitHysComp_MtrNm_f32	8.35999966
k_AsstFWNstep_Cnt_u16	1122
k_AsstFWPstep_Cnt_u16	4305
k_RestoreThresh_MtrNm_f32	8.80000019
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144

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ASSISTRIEWAII_PELL		THE CITY
Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144	
	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]		
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0	
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0	
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240	
z_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096	
:2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2046
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6] t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	4096 6144
	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10] t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0] t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-26024 -24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	6144
	0.400
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1] t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	8192 10240





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480 22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	26624
t_AsstFWDefitAssistX_HwNm_u8p8[0]	896
t_AsstFWDefltAssistX_HwNm_u8p8[1]	922
t_AsstFWDefltAssistX_HwNm_u8p8[2]	947
t_AsstFWDefltAssistX_HwNm_u8p8[3]	973
t_AsstFWDefltAssistX_HwNm_u8p8[4]	998
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[18] t_AsstFWDefltAssistX_HwNm_u8p8[19]	1357 1382
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	2662
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2867
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3686
t_AsstFWDefitAssistY_MtrNm_s4p11[6]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6349
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	6554
t_AsstFWPstepNstepThresh_Cnt_u16[0]	232
t_AsstFWPstepNstepThresh_Cnt_u16[1]	647
t_AsstFWVehSpd_Kph_u9p7[0] t_AsstFWVehSpd_Kph_u9p7[1]	13184 13312
t_AsstFWVehSpd_Kph_u9p7[2]	13440
t_AsstFWVehSpd_Kph_u9p7[3]	13568
t_AsstFWVehSpd_Kph_u9p7[4]	13696
t_AsstFWVehSpd_Kph_u9p7[5]	13824
t_AsstFWVehSpd_Kph_u9p7[6]	13952
t_AsstFWVehSpd_Kph_u9p7[7]	14080
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7.65999985
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.98999977
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8.43000031
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.64999962
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	61.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_left and the property of the p$	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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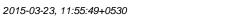


Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.53919983	6.53919983 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	647	647 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.20019531	3.20019531 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	9.50060081	9.50059986 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.83901548	5.83901548 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.31500006	7.31500006 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.20019531	3.20019531 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	✓

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.112 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.80000019
AssistFirewall ActiveKSV M str.K Uls f32	0.0250000004
AssistFirewall_ActiveRawAcc_Cnt_M_u16	10455
AssistFirewall AsstReducedPerfSV Cnt M Iqc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.239999995
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12800002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.19999981
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.280000001
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.5999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.379999995
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6.4000001
k_AsstFWInpLimitHFA_MtrNm_f32	6.57000017
k_AsstFWInpLimitHysComp_MtrNm_f32	8.47000027
k_AsstFWNstep_Cnt_u16	1233
k_AsstFWPstep_Cnt_u16	4428
k_RestoreThresh_MtrNm_f32	4.4000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
2 AsstFWUprBoundX HwNm s4p11[5][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	6144
	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	12288

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-4096 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1] t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096 8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0] t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[/][1] t2_AsstFWUprBoundY_MtrNm_s4p11[/][2]	12288
12_7.000. 17 Opt Double 1 _ INICI 4111_34p 1 1[7][2]	12200
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	14336





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	22528 24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	922
t_AsstFWDefltAssistX_HwNm_u8p8[1]	947
t_AsstFWDefltAssistX_HwNm_u8p8[2]	973
t_AsstFWDefltAssistX_HwNm_u8p8[3]	998
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1152 1178
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1229
t_AsstFWDefitAssistX_HwNm_u8p8[13]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1382
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1408
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2867
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3686 3891
t_AsstFWDefltAssistY_MtrNm_s4p11[5] t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4096
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[18] t AsstFWDefltAssistY_MtrNm_s4p11[19]	6554 6758
t AsstFWPstepNstepThresh Cnt u16[0]	233
t_AsstFWPstepNstepThresh_Cnt_u16[1]	651
t_AsstFWVehSpd_Kph_u9p7[0]	16128
t_AsstFWVehSpd_Kph_u9p7[1]	16256
t_AsstFWVehSpd_Kph_u9p7[2]	16384
t_AsstFWVehSpd_Kph_u9p7[3]	16512
t_AsstFWVehSpd_Kph_u9p7[4]	16640
t_AsstFWVehSpd_Kph_u9p7[5]	16768
t_AsstFWVehSpd_Kph_u9p7[6]	16896
t_AsstFWVehSpd_Kph_u9p7[7]	17024
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7.76999998
tgt_AssistFirewall_Per1_Defeat_AssitTbl_Service_Cnt_lgc.value	0 8.1000038
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8.10000038 8.53999996
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.76000023
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	68.3000031
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.63000011	6.63000011 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	651	651 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.29980469	3.29980469 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	9.7816	9.7816 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.46399975	5.46400023 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8.13199997	8.13199997 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.29980469	3.29980469 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

Τ				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.113 (Repeat Count = 1) Name	Input Value
	-5.3000019
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32 AssistFirewall ActiveKSV M str.K UIs f32	0.40000006
	8487
AssistFirewall_ActiveRawAcc_Cnt_M_u16	
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019 -5.1999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.079999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11199999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.119999997
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.219999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
x_AsstFWInpLimitBaseAsst_MtrNm_f32	4.80000019
c_AsstFWInpLimitHFA_MtrNm_f32	6.40999985
x_AsstFWInpLimitHysComp_MtrNm_f32	6.71000004
<_AsstFWNstep_Cnt_u16	4052
k_AsstFWPstep_Cnt_u16	2460
x_RestoreThresh_MtrNm_f32	4.42999983
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384 18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10] t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_Asst WopiboundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_Asst WoprboundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_Asst WopiboundX_HwNm_s4p11[3][10]	2048
t2 AsstFWUprBoundX HwNm s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0] t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1] t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_riwNrii_s4p11[4][2] t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2 AsstFWUprBoundX HwNm s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	

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Name	Input Value	
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192	
	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]		
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336	
z_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-22528	
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-20480	
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-18432	
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-10240	
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528	
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576	
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384	
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240	
P_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-12288	
2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	-2048 0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefitAssistX_HwNm_u8p8[0]	947
t_AsstFWDefltAssistX_HwNm_u8p8[1]	973
t_AsstFWDefltAssistX_HwNm_u8p8[2]	998
t_AsstFWDefltAssistX_HwNm_u8p8[3]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1382 1408
t_AsstFWDefltAssistX_HwNm_u8p8[18] t_AsstFWDefltAssistX_HwNm_u8p8[19]	1434
t_AsstFWDefitAssistY_MtrNm_s4p11[0]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6963
t_AsstFWPstepNstepThresh_Cnt_u16[0]	234
t_AsstFWPstepNstepThresh_Cnt_u16[1]	655
t_AsstFWVehSpd_Kph_u9p7[0] t_AsstFWVehSpd_Kph_u9p7[1]	19072 19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
t_AsstFWVehSpd_Kph_u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.19999981
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	1
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.5999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.4000001
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.5999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176.100006
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Service\_Cnt\_AsstTbl\_Ser$	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.30000019	-5.30000019 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487	8487 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-16	-16 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-6.06399965	-6.06400013 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019	-5.30000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999	5.0999999 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-16	-16 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.114 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.4000001
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.5
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8610
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	0
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.090000036
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11300004
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.4000001
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.129999995
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.230000004
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.9000001
k_AsstFWInpLimitHFA_MtrNm_f32	6.42000008
k_AsstFWInpLimitHysComp_MtrNm_f32	6.82000017
k_AsstFWNstep_Cnt_u16	4053
k_AsstFWPstep_Cnt_u16	2583
k_RestoreThresh_MtrNm_f32	4.44000006
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
, , , , , , , , , , , , , , , , , , , ,	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0
t2_Asst WopiBoundX_HwNm_s4p11[7][8]	2048
t2_Asst WopiBoundX_HwNm_s4p11[7][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	20480

AssistFirewall Per1

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Input Value t2\_AsstFWUprBoundY\_MtrNm\_s4p11[0][10] 22528 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][0] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][1] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][2] 6144 t2 AsstFWUprBoundY MtrNm s4p11[1][3] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][4] 10240 t2 AsstFWUprBoundY MtrNm s4p11[1][5] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][6] 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][7] 16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][8] 18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][9] 20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[1][10] 22528 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][0] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][1] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][2] 4096 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][3] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][4] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][5] 10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][6] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][7] 14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][8] 16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][9] 18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[2][10] 20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][0] -20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][1] -18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][2] -16384 -14336 t2 AsstFWUprBoundY MtrNm s4p11[3][3] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][4] -12288 t2 AsstFWUprBoundY MtrNm s4p11[3][5] -10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][6] -8192 -6144 t2 AsstFWUprBoundY MtrNm s4p11[3][7] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][8] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][9] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[3][10] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][0] -8192 -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][1] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][2] -4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][3] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][4] 2048 t2 AsstFWUprBoundY MtrNm s4p11[4][5] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][6] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][7] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][8] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][9] 10240  $t2\_AsstFWUprBoundY\_MtrNm\_s4p11[4][10]$ 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][0] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][1] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][2] 6144 t2 AsstFWUprBoundY MtrNm s4p11[5][3] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][4] 10240 t2 AsstFWUprBoundY\_MtrNm\_s4p11[5][5] 12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][6] 14336 t2 AsstFWUprBoundY MtrNm s4p11[5][7] 16384 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][8] 18432 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][9] 20480 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[5][10] 22528 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][0] -12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][1] -10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][2] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][3] -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][4] -4096 -2048 t2 AsstFWUprBoundY\_MtrNm\_s4p11[6][5] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][6] 0 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][7] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][8] 4096 6144 t2 AsstFWUprBoundY MtrNm s4p11[6][9] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[6][10] 8192 t2 AsstFWUprBoundY MtrNm s4p11[7][0] -14336 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][1] -12288 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][2] -10240 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][3] -8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][4] -6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][5] -4096





Name	
2_AssPh/UpBourdy_Mehm set11719   0	
2. ASSP/Wijdeburdy   Methods   1989   4099    -2. ASSP/Wijdeburdy   Methods   1989   1044    -2. ASSP/Wijdeburdy   Methods   1981   1044    -2. ASSP/Wijdeburdy   Methods   1985   1055    -2. ASSP/Wijdeburdy   Methods   1985   1055   1055    -2. ASSP/Wijdeburdy   Methods   1985   1055   1055   1055   1055    -2. ASSP/Wijdeburdy   Methods   1985   1055   1055   1055   1055   1055   1055   1055   1055   1055   1055   1055   1055   1055   1055   1055   1055   1055   1055   1055   1055   1055   1055   1055   1055   1055   1055   1055   1055   1055   1055   1055   1055   1055   1055   1055   1055   1055   1055   1055   1055   1055	
ABSEP/DelThAckest Newth. wide(0)   815	
LASER/POEITASES   ANNIX 19881   846	
LASSP WORTHASSEX, Mehr., 19882  886   LASSP WORTHASSEX, Mehr., 19881  922   LASSP WORTHASSEX, Mehr., 19881  922   LASSP WORTHASSEX, Mehr., 19881  973   PART CARREST, Mehr., 19881  973   PART CARREST, Mehr., 19881  1974   PART CARREST, Mehr., 19881  1975   PART CARREST, Mehr., 19891  1975   PART CARREST, 19891  1975   PAR	
LaseFVDethoses   Ambro, 1988   986     LaseFVDethoses   Ambro, 1988   92     LaseFVDethoses   Ambro, 1988   97     LaseFVDethoses   Ambro, 1988   97     LaseFVDethoses   Ambro, 1988   97     LaseFVDethoses   Ambro, 1988   97     LaseFVDethoses   Ambro, 1988   102     LaseFVDethoses   Ambro, 1988   110     LaseFVDethoses   Ambro, 1988   110     LaseFVDethoses   Ambro, 1988   112     LaseFVDethoses   Ambro, 1988   113     LaseFVDethoses   Ambro, 1988   114     LaseFVDethoses   Ambr	
LASSE/PADERLANDER, Mehra, 195815   97	
LaseFV/DitAssixX, Hahm, usp9(6)	
LassFWDethAssix, Heehn upbgf7  98	
LaseFVDetRickseik, Hehm. up8pt7    988	
LASSIF/WorldAssistX, HwNm. ulps8[1]   1050   1075   LASSIF/WorldAssistX, HwNm. ulps8[1]   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1	
LASSEPWDefitAssisX, HwNm_usp8[10]   1075	
LassiFWDelfassiX HwWm usbg8[13]	
Lasel Woelflassist X Hebra, u698[13]   1152     Lasel Woelflassist X Hebra, u698[13]   1152     Lasel Woelflassist X Hebra, u698[14]   1178     Lasel Woelflassist X Hebra, u698[15]   1203     Lasel Woelflassist X Hebra, u698[15]   1229     Lasel Woelflassist X Hebra, u698[17]   1254     Lasel Woelflassist X Hebra, u698[17]   1254     Lasel Woelflassist X Hebra, u698[18]   1280     Lasel Woelflassist X Hebra, u698[18]   1280     Lasel Woelflassist X Hebra, u698[19]   1306     Lasel Woelflassist X Hebra, u698[19]   1306     Lasel Woelflassist X Hebra, u698[19]   1307     Lasel Woelflassist X Hebra, u698[19]   1308     Lasel Woelflassist X Hebra, u698[19]   1308     Lasel Woelflassist X Hebra, u698[19]   1309     Lasel Woelflassist X Hebra, u699[13]   3891     Lasel Woelflassist X Hebra, u699[13]   3891     Lasel Woelflassist X Hebra, u699[18]   4096     Lasel Woelflassist X Hebra, u699[18]   4096     Lasel Woelflassist X Hebra, u699[19]   4096     Lasel Woelflassist X Hebra,	
LASSIFWDelftAssistX_Hwhm_u8p8[14]   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178   1178	
L. ASSET/WorltAssistX, HwNm. u869[14]  1. ASSET/WorltAssistX, HwNm. u869[15]  1. ASSET/WorltAssistX, HwNm. u869[17]  1. ASSET/WorltAssistX, HwNm. u869[17]  1. ASSET/WorltAssistX, HwNm. u869[18]  1. ASSET/WorltAssistX, HwNm. u869[19]  1. ASSET/WorltAssi	
LASSIFWDettRASSIST, Minkm_ubp8[15]   1203   1229   1229   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224   1224	
LASSIFWDeftAssistX_HwNn_u6p8[15] 1226  LASSIFWDeftAssistX_HwNn_u6p8[15] 1280  LASSIFWDeftAssistX_HwNn_u6p8[15] 1306  LASSIFWDeftAssistY_Mrnn_s4p1[10] 3277  LASSIFWDeftAssistY_Mrnn_s4p1[10] 3482  LASSIFWDeftAssistY_Mrnn_s4p1[10] 3891  LASSIFWDeftAssistY_Mrnn_s4p1[10] 3891  LASSIFWDeftAssistY_Mrnn_s4p1[10] 3891  LASSIFWDeftAssistY_Mrnn_s4p1[10] 4096  LASSIFWDeftAssistY_Mrnn_s4p1[10] 4096  LASSIFWDeftAssistY_Mrnn_s4p1[10] 4500  LASSIFWDeftAssistY_Mrnn_s4p1[10] 4500  LASSIFWDeftAssistY_Mrnn_s4p1[10] 4500  LASSIFWDeftAssistY_Mrnn_s4p1[10] 4500  LASSIFWDeftAssistY_Mrnn_s4p1[10] 4710  LASSIFWDeftAssistY_Mrnn_s4p1[10] 4710  LASSIFWDeftAssistY_Mrnn_s4p1[10] 5120  LASSIFWDeftAssistY_Mrnn_s4p1[10] 5120  LASSIFWDeftAssistY_Mrnn_s4p1[10] 5520  LASSIFWDeftAssistY_Mrnn_s4p1[10] 5530  LASSIFWDeftAssistY_Mrnn_s4p1[10] 5530  LASSIFWDeftAssistY_Mrnn_s4p1[10] 5530  LASSIFWDeftAssistY_Mrnn_s4p1[10] 654  LASSIFWDeftAssistY_Mrnn_s4p1[10] 654  LASSIFWDeftAssistY_Mrnn_s4p1[10] 6554  LASSIFWDeftAssistY_Mrnn_s4p1[10] 6564  LASSIFWDeftAssistY_M	
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LASSIFWDelflAssistY, Minkm_spl1[0] 1306  LASSIFWDelflAssistY, Minkm_spl1[0] 3277  LASSIFWDelflAssistY, Minkm_spl1[0] 3277  LASSIFWDelflAssistY, Minkm_spl1[0] 3482  LASSIFWDelflAssistY, Minkm_spl1[0] 3886  LASSIFWDelflAssistY, Minkm_spl1[0] 4096  LASSIFWDelflAssistY, Minkm_spl1[0] 4096  LASSIFWDelflAssistY, Minkm_spl1[0] 4096  LASSIFWDelflAssistY, Minkm_spl1[0] 4506  LASSIFWDelflAssistY, Minkm_spl1[0] 4506  LASSIFWDelflAssistY, Minkm_spl1[0] 4506  LASSIFWDelflAssistY, Minkm_spl1[0] 4506  LASSIFWDelflAssistY, Minkm_spl1[0] 5120  LASSIFWDelflAssistY, Minkm_spl1[0] 5120  LASSIFWDelflAssistY, Minkm_spl1[1] 5530  LASSIFWDelflAssistY, Minkm_spl1[1] 5734  LASSIFWDelflAssistY, Minkm_spl1[1] 5734  LASSIFWDelflAssistY, Minkm_spl1[1] 5734  LASSIFWDelflAssistY, Minkm_spl1[1] 5734  LASSIFWDelflAssistY, Minkm_spl1[1] 6144  LASSIFWDelflAssistY, Minkm_spl1[1] 6144  LASSIFWDelflAssistY, Minkm_spl1[1] 6154  LASSIFWDelflAssistY, Minkm_spl1[1] 61	
L. AssIFWDelftAssistY_Minm_stp11[0] 3277 L. AssIFWDelftAssistY_Minm_stp11[1] 3482 L. AssIFWDelftAssistY_Minm_stp11[1] 3482 L. AssIFWDelftAssistY_Minm_stp11[2] 3686 L. AssIFWDelftAssistY_Minm_stp11[3] 3891 L. AssIFWDelftAssistY_Minm_stp11[3] 4096 L. AssIFWDelftAssistY_Minm_stp11[6] 4506 L. AssIFWDelftAssistY_Minm_stp11[7] 4710 L. AssIFWDelftAssistY_Minm_stp11[8] 4915 L. AssIFWDelftAssistY_Minm_stp11[9] 5120 L. AssIFWDelftAssistY_Minm_stp11[9] 5120 L. AssIFWDelftAssistY_Minm_stp11[9] 5120 L. AssIFWDelftAssistY_Minm_stp11[1] 5532 L. AssIFWDelftAssistY_Minm_stp11[1] 5530 L. AssIFWDelftAssistY_Minm_stp11[1] 5	
LASSIFWDelflAssistY_Minkm_s4p11() 3482 LASSIFWDelflAssistY_Minkm_s4p11() 3686 LASSIFWDelflAssistY_Minkm_s4p11() 3686 LASSIFWDelflAssistY_Minkm_s4p11() 4096 LASSIFWDelflAssistY_Minkm_s4p11() 4096 LASSIFWDelflAssistY_Minkm_s4p11() 4096 LASSIFWDelflAssistY_Minkm_s4p11() 4096 LASSIFWDelflAssistY_Minkm_s4p11() 4506 LASSIFWDelflAssistY_Minkm_s4p11() 4506 LASSIFWDelflAssistY_Minkm_s4p11() 4506 LASSIFWDelflAssistY_Minkm_s4p11() 5100 LASSIFWDelflAssistY_Minkm_s4p11() 5526 LASSIFWDelflAssistY_Minkm_s4p11() 5526 LASSIFWDelflAssistY_Minkm_s4p11() 5530 LASSIFWDelflAssist	
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LAsstFWDefltAssistY_MtrNm_s4p11[16]       6349         LAsstFWDefltAssistY_MtrNm_s4p11[16]       6554         LAsstFWDefltAssistY_MtrNm_s4p11[17]       6758         LAsstFWDefltAssistY_MtrNm_s4p11[18]       6963         LAsstFWDefltAssistY_MtrNm_s4p11[19]       7168         LAsstFWPstepNstepThresh_Cnt_u16[0]       235         LAsstFWPstepNstepThresh_Cnt_u16[1]       659         LAsstFWehSpd_Kph_u9p7[0]       22016         LAsstFWvehSpd_Kph_u9p7[1]       22144         LAsstFWvehSpd_Kph_u9p7[3]       22400         LAsstFWvehSpd_Kph_u9p7[4]       22528         LAsstFWvehSpd_Kph_u9p7[6]       22784         LAsstFWvehSpd_Kph_u9p7[7]       22912         tgLAsstFirewall_Perf_BaseAssistCmd_MtrNm_f32.value       -5.30000019         tgLAssistFirewall_Perf_BaseAssistCmd_StrNm_f32.value       -5.69999981         tgLAssistFirewall_Perf_HysteresisComp_MtrNm_f32.value       -5.5         tgLAssistFirewall_Perf_HysteresisComp_MtrNm_f32.value       -5.5         tgLAssistFirewall_Perf_HysteresisComp_MtrNm_f32.value       -5.5         tgLAssistFirewall_Perf_HysteresisComp_MtrNm_f32.value       -5.69999981         tgLAssistFirewall_Perf_HysteresisComp_MtrNm_f32.value       -5.69999981	
t_AsstFWDefitAssistY_MtrNm_s4p11[16] 6554  t_AsstFWDefitAssistY_MtrNm_s4p11[17] 6758  t_AsstFWDefitAssistY_MtrNm_s4p11[18] 6963  t_AsstFWDefitAssistY_MtrNm_s4p11[19] 7168  t_AsstFWPstepNstepThresh_Cnt_u16[0] 235  t_AsstFWPstepNstepThresh_Cnt_u16[1] 659  t_AsstFWPstepNstepThresh_Cnt_u16[1] 22016  t_AsstFWehSpd_Kph_u9p7[0] 22144  t_AsstFWehSpd_Kph_u9p7[2] 22272  t_AsstFWehSpd_Kph_u9p7[3] 22400  t_AsstFWehSpd_Kph_u9p7[3] 22528  t_AsstFWehSpd_Kph_u9p7[5] 22666  t_AsstFWOehSpd_Kph_u9p7[6] 22784  t_AsstFWehSpd_Kph_u9p7[6] 22784  t_AsstFWehSpd_Kph_u9p7[7] 22912  tgt_AssisFirewall_Pert_BaseAssistCmd_MtrNm_f32.value 5.3000019  tgt_AssistFirewall_Pert_Defeat_AsstTbl_Service_Cnt_Igc.value 0  tgt_AssistFirewall_Pert_HighFreqAssist_MtrNm_f32.value 5.69999981  tgt_AssistFirewall_Pert_HysteresisComp_MtrNm_f32.value 5.69999981  tgt_AssistFirewall_Pert_HysteresisComp_MtrNm_f32.value 5.69999981  tgt_AssistFirewall_Pert_HysteresisComp_MtrNm_f32.value 5.69999981  tgt_AssistFirewall_Pert_MEC_Counter_Cnt_enum.value 2	
t_AsstFWDefltAssistY_MtrNm_s4p11[17]       6758         t_AsstFWDefltAssistY_MtrNm_s4p11[18]       6963         t_AsstFWDefltAssistY_MtrNm_s4p11[19]       7168         t_AsstFWPstepNstepThresh_Cnt_u16[0]       235         t_AsstFWPstepNstepThresh_Cnt_u16[1]       659         t_AsstFWvehSpd_Kph_u9p7[0]       22016         t_AsstFWvehSpd_Kph_u9p7[1]       22144         t_AsstFWvehSpd_Kph_u9p7[2]       22272         t_AsstFWvehSpd_Kph_u9p7[3]       22400         t_AsstFWvehSpd_Kph_u9p7[4]       22528         t_AsstFWvehSpd_Kph_u9p7[5]       22656         t_AsstFWvehSpd_Kph_u9p7[6]       22784         t_AsstFWvehSpd_Kph_u9p7[7]       22912         tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value       -5.30000019         tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value       -5.69999981         tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value       -5.5         tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value       -5.69999981         tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value       2	
t_AsstFWDefitAssistY_MtrNm_s4p11[18]	
t_AsstFWDefltAssistY_MtrNm_s4p11[19]       7168         t_AsstFWPstepNstepThresh_Cnt_u16[0]       235         t_AsstFWPstepNstepThresh_Cnt_u16[1]       659         t_AsstFWVehSpd_Kph_u9p7[0]       22016         t_AsstFWVehSpd_Kph_u9p7[1]       22144         t_AsstFWVehSpd_Kph_u9p7[2]       22272         t_AsstFWVehSpd_Kph_u9p7[3]       22400         t_AsstFWVehSpd_Kph_u9p7[4]       22528         t_AsstFWVehSpd_Kph_u9p7[5]       22656         t_AsstFWVehSpd_Kph_u9p7[6]       22784         t_AsstFWvehSpd_Kph_u9p7[7]       22912         tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value       -5.30000019         tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value       -5.69999981         tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value       -5.5         tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value       -5.69999981         tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value       2	
t_AsstFWPstepNstepThresh_Cnt_u16[0]       235         t_AsstFWVehSpd_Kph_u9p7[0]       22016         t_AsstFWVehSpd_Kph_u9p7[1]       22144         t_AsstFWVehSpd_Kph_u9p7[2]       22272         t_AsstFWVehSpd_Kph_u9p7[3]       22400         t_AsstFWVehSpd_Kph_u9p7[4]       22528         t_AsstFWVehSpd_Kph_u9p7[5]       22656         t_AsstFWVehSpd_Kph_u9p7[6]       22784         t_AsstFWVehSpd_Kph_u9p7[7]       22912         tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value       -5.30000019         tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value       -5.69999981         tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value       -5.6         tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value       -5.69999981         tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value       2	
t_AsstFWPstepNstepThresh_Cnt_u16[1]       659         t_AsstFWVehSpd_Kph_u9p7[0]       22016         t_AsstFWVehSpd_Kph_u9p7[1]       22144         t_AsstFWVehSpd_Kph_u9p7[2]       22272         t_AsstFWVehSpd_Kph_u9p7[3]       22400         t_AsstFWVehSpd_Kph_u9p7[4]       22528         t_AsstFWVehSpd_Kph_u9p7[5]       22656         t_AsstFWVehSpd_Kph_u9p7[6]       22784         t_AsstFWvehSpd_Kph_u9p7[7]       22912         tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value       -5.30000019         tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value       0         tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value       -5.6999981         tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value       -5.69999981         tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value       -5.69999981         tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value       2	
t_AsstFWVehSpd_Kph_u9p7[0]       22016         t_AsstFWVehSpd_Kph_u9p7[1]       22144         t_AsstFWVehSpd_Kph_u9p7[2]       22272         t_AsstFWVehSpd_Kph_u9p7[3]       22400         t_AsstFWVehSpd_Kph_u9p7[4]       22528         t_AsstFWVehSpd_Kph_u9p7[5]       22656         t_AsstFWVehSpd_Kph_u9p7[6]       22784         t_AsstFWvehSpd_Kph_u9p7[7]       22912         tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value       -5.30000019         tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value       0         tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value       -5.69999981         tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value       -5.5         tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value       -5.69999981         tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value       2	
t_AsstFWVehSpd_Kph_u9p7[1]       22144         t_AsstFWVehSpd_Kph_u9p7[2]       22272         t_AsstFWVehSpd_Kph_u9p7[3]       22400         t_AsstFWVehSpd_Kph_u9p7[4]       22528         t_AsstFWVehSpd_Kph_u9p7[5]       22656         t_AsstFWVehSpd_Kph_u9p7[6]       22784         t_AsstFWvehSpd_Kph_u9p7[7]       22912         tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value       -5.30000019         tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value       0         tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value       -5.69999981         tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value       -5.5         tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value       2	
t_AsstFWVehSpd_Kph_u9p7[2]       22272         t_AsstFWVehSpd_Kph_u9p7[3]       22400         t_AsstFWVehSpd_Kph_u9p7[4]       22528         t_AsstFWVehSpd_Kph_u9p7[5]       22656         t_AsstFWVehSpd_Kph_u9p7[6]       22784         t_AsstFWvehSpd_Kph_u9p7[7]       22912         tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value       -5.30000019         tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value       0         tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value       -5.69999981         tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value       -5.5         tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value       2	
t_AsstFWVehSpd_Kph_u9p7[3]       22400         t_AsstFWVehSpd_Kph_u9p7[4]       22528         t_AsstFWVehSpd_Kph_u9p7[5]       22656         t_AsstFWVehSpd_Kph_u9p7[6]       22784         t_AsstFWvehSpd_Kph_u9p7[7]       22912         tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value       -5.30000019         tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value       0         tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value       -5.69999981         tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value       -5.5         tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value       2	
t_AsstFWVehSpd_Kph_u9p7[4]       22528         t_AsstFWVehSpd_Kph_u9p7[5]       22656         t_AsstFWVehSpd_Kph_u9p7[6]       22784         t_AsstFWVehSpd_Kph_u9p7[7]       22912         tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value       -5.30000019         tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value       0         tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value       -5.69999981         tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value       -5.5         tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value       2	
t_AsstFWVehSpd_Kph_u9p7[5]       22656         t_AsstFWVehSpd_Kph_u9p7[6]       22784         t_AsstFWVehSpd_Kph_u9p7[7]       22912         tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value       -5.30000019         tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value       0         tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value       -5.69999981         tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value       -5.5         tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value       2	
t_AsstFWVehSpd_Kph_u9p7[6]       22784         t_AsstFWVehSpd_Kph_u9p7[7]       22912         tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value       -5.30000019         tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value       0         tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value       -5.69999981         tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value       -5.5         tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value       2	
t_AssiFWVehSpd_Kph_u9p7[7]       22912         tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value       -5.30000019         tgt_AssistFirewall_Per1_Defeat_AssiTbl_Service_Cnt_lgc.value       0         tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value       -5.69999981         tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value       -5.5         tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value       2	
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value -5.30000019  tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value 0  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value -5.69999981  tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value -5.5  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value -5.69999981  tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value 2	
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value 0  tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value -5.69999981  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value -5.69999981  tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value 2	
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value -5.69999981  tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value -5.5  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value -5.69999981  tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value 2	
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value -5.5  tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value -5.69999981  tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value 2	
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value -5.69999981 tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value 2	
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value 2	
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value 187.199997	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall_AssistFirewall_Per1_CombinedAssist_MtrNm_f32 tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lt_tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32 tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32 tgt_AssistFirewall_Per1_HwTorque_HwNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32 tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32 tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32	
Name Actual Value Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32 -2.70000005 -2.70000005 -2.70000005 -2.70000005	•

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveRawAcc_Cnt_M_u16	659	659 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.5	-3.5 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-6.28999996	-6.28999996 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.0880003	-5.08799982 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.19199991	-5.19199991 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-3.5	-3.5 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>~</b>

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.115 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.5
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.600000024
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8733
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.100000001
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11399996
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.80000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.140000001
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.19999981
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.239999995
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5
k AsstFWInpLimitHFA MtrNm f32	6.42999983
k_AsstFWInpLimitHysComp_MtrNm_f32	6.92999983
k_AsstFWNstep_Cnt_u16	3053
k_AsstFWPstep_Cnt_u16	2706
k_RestoreThresh_MtrNm_f32	4.44999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2 AsstFWUprBoundX HwNm s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10] t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	16384 -14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384 -12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0] t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240 -8102
t2_AsstFWUprBoundX_HwNm_s4p11[7][2] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3] t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4] t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2046
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	16384 18432

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Name	Input Value
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	870
t_AsstFWDefltAssistX_HwNm_u8p8[1]	896 922
t_AsstFWDefltAssistX_HwNm_u8p8[2] t AsstFWDefltAssistX HwNm u8p8[3]	947
t_AsstFWDefltAssistX_HwNm_u8p8[4]	973
t_AsstFWDefltAssistX_HwNm_u8p8[5]	998
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1152 1178
t_AsstFWDefltAssistX_HwNm_u8p8[12] t AsstFWDefltAssistX HwNm u8p8[13]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1357
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3891
t_AsstFWDefitAssistY_MtrNm_s4p11[3] t_AsstFWDefitAssistY_MtrNm_s4p11[4]	4096 4301
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6144
t_AsstFWDefitAssistY_MtrNm_s4p11[14] t_AsstFWDefitAssistY_MtrNm_s4p11[15]	6349 6554
t_AsstFWDefitAssistY_MtrNm_s4p11[16]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7373
t_AsstFWPstepNstepThresh_Cnt_u16[0]	236
t_AsstFWPstepNstepThresh_Cnt_u16[1]	663
t_AsstFWVehSpd_Kph_u9p7[0]	24960
t_AsstFWVehSpd_Kph_u9p7[1]	25088
t_AsstFWVehSpd_Kph_u9p7[2]	25216
t_AsstFWVehSpd_Kph_u9p7[3] t_AsstFWVehSpd_Kph_u9p7[4]	25344 25472
t_AsstFWVehSpd_Kph_u9p7[5]	25472 25600
t_AsstFWVehSpd_Kph_u9p7[6]	25728
t_AsstFWVehSpd_Kph_u9p7[7]	25856
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.4000001
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.67000008
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.599999
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.67000008
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	198.300003 tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uis_r32  tgt_Rte_inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_AsstrIrewallActive_Uis_f32 tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_k	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgr_rtto_mot_rp_rtodott newalls todott newall_retr_nysteresiseemp_within_toz	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-2.19999981	-2.20000005 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	663	663 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.60009766	-3.60009766 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-4.05000019	-4.05000019 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.6983614	4.6983614 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.44813251	-5.44813299 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-3.60009766	-3.60009766 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.116 (Repeat Count = 1)	🗸
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.5
AssistFirewall ActiveKSV M str.K Uls f32	0.0120000001
AssistFirewall ActiveRawAcc Cnt M u16	8856
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.109999999
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11500001
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.9000001
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.150000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.25
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	6.44000006
k_AsstFWInpLimitHysComp_MtrNm_f32	7.03999996
k_AsstFWNstep_Cnt_u16	2053
k_AsstFWPstep_Cnt_u16	2829
k_RestoreThresh_MtrNm_f32	4.46000004
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048





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12_AssIFWUprBoundX_HwNm_s4p11[2] 6    12_AssIFWUprBoundX_HwNm_s4p11[2] 6    12_AssIFWUprBoundX_HwNm_s4p11[2] 6    12_AssIFWUprBoundX_HwNm_s4p11[2] 7    12288   12_AssIFWUprBoundX_HwNm_s4p11[2] 7    12288   14336   12_AssIFWUprBoundX_HwNm_s4p11[2] 9    16384   12_AssIFWUprBoundX_HwNm_s4p11[2] 10    18432   12_AssIFWUprBoundX_HwNm_s4p11[3] 0    12_AssIFWUprBoundX_HwNm_s4p11[3] 1    1-10240   12_AssIFWUprBoundX_HwNm_s4p11[3] 2    12_AssIFWUprBoundX_HwNm_s4p11[3] 2    12_AssIFWUprBoundX_HwNm_s4p11[3] 2    12_AssIFWUprBoundX_HwNm_s4p11[3] 3    13_14_14_14_14_14_14_14_14_14_14_14_14_14_	
12_AssIFWUprBoundX_HwNm_s4p11[2] 5    10240	
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12288   1228   12288   12288   12288   12288   12288   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285   12285	
12_AsstFWUprBoundX_HwNm_s4p11[2][8]   14336   12_AsstFWUprBoundX_HwNm_s4p11[2][10]   16384   12_AsstFWUprBoundX_HwNm_s4p11[2][10]   18432   12_AsstFWUprBoundX_HwNm_s4p11[3][0]   1-12288   12_AsstFWUprBoundX_HwNm_s4p11[3][1]   1-10240   12_AsstFWUprBoundX_HwNm_s4p11[3][1]   1-10240   12_AsstFWUprBoundX_HwNm_s4p11[3][2]   8-1812   12_AsstFWUprBoundX_HwNm_s4p11[3][3]   6-1144   12_AsstFWUprBoundX_HwNm_s4p11[3][4]   4-096   12_AsstFWUprBoundX_HwNm_s4p11[3][6]   0   12_AsstFWUprBoundX_HwNm_s4p11[3][6]   0   12_AsstFWUprBoundX_HwNm_s4p11[3][7]   2048   12_AsstFWUprBoundX_HwNm_s4p11[3][8]   4-096   12_AsstFWUprBoundX_HwNm_s4p11[3][8]   4-096   12_AsstFWUprBoundX_HwNm_s4p11[3][9]   6-1144   12_AsstFWUprBoundX_HwNm_s4p11[3][9]   6-12_AsstFWUprBoundX_HwNm_s4p11[4][1]   0   12_AsstFWUprBoundX_HwNm_s4p11[4][1]   0   12_AsstFWUprBoundX_HwNm_s4p11[4][1]   0   12_AsstFWUprBoundX_HwNm_s4p11[4][1]   0   12_AsstFWUprBoundX_HwNm_s4p11[4][2]   2048   12_AsstFWUprBoundX_HwNm_s4p11[4][2]   2048   12_AsstFWUprBoundX_HwNm_s4p11[4][6]   10240   12_AsstFWUprBoundX_HwNm_s4p11[6][6]   1024	
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12. AsstFWUprBoundX. HwNm_s4p11[2][10] 12. AsstFWUprBoundX. HwNm_s4p11[3][1] 12. AsstFWUprBoundX. HwNm_s4p11[3][2] 12. AsstFWUprBoundX. HwNm_s4p11[3][2] 12. AsstFWUprBoundX. HwNm_s4p11[3][3] 13. 6-6144 12. AsstFWUprBoundX. HwNm_s4p11[3][3] 12. AsstFWUprBoundX. HwNm_s4p11[3][4] 12. AsstFWUprBoundX. HwNm_s4p11[3][6] 12. AsstFWUprBoundX. HwNm_s4p11[3][7] 12. AsstFWUprBoundX. HwNm_s4p11[3][7] 12. AsstFWUprBoundX. HwNm_s4p11[3][7] 12. AsstFWUprBoundX. HwNm_s4p11[3][7] 12. AsstFWUprBoundX. HwNm_s4p11[3][8] 12. AsstFWUprBoundX. HwNm_s4p11[3][9] 12. AsstFWUprBoundX. HwNm_s4p11[3][9] 12. AsstFWUprBoundX. HwNm_s4p11[3][9] 12. AsstFWUprBoundX. HwNm_s4p11[4][9] 12. AsstFWUprBoundX. HwNm_s4p11[4][6] 12. AsstFWUprBoundX. HwNm_s4p11[4][6] 12. AsstFWUprBoundX. HwNm_s4p11[4][6] 12. AsstFWUprBoundX. HwNm_s4p11[4][9] 12. AsstFWUprBoundX. HwNm_s4p11[4][9] 13. AsstFWUprBoundX. HwNm_s4p11[4][9] 14. AsstFWUprBoundX. HwNm_s4p11[4][9] 15. AsstFWUprBoundX. HwNm_s4p11[6][9] 16. AsstFWUprBoundX.	
12   AsstFWUprBoundX   HwNm_s4p11[3][0]   12288   12   AsstFWUprBoundX   HwNm_s4p11[3][1]   1-10240   12   AsstFWUprBoundX   HwNm_s4p11[3][2]   8-192   12   AsstFWUprBoundX   HwNm_s4p11[3][3]   6-1144   12   AsstFWUprBoundX   HwNm_s4p11[3][6]   2-048   12   AsstFWUprBoundX   HwNm_s4p11[3][6]   0   12   AsstFWUprBoundX   HwNm_s4p11[3][6]   0   12   AsstFWUprBoundX   HwNm_s4p11[3][7]   2048   12   AsstFWUprBoundX   HwNm_s4p11[3][8]   4096   12   AsstFWUprBoundX   HwNm_s4p11[3][8]   4096   12   AsstFWUprBoundX   HwNm_s4p11[3][9]   6144   12   AsstFWUprBoundX   HwNm_s4p11[3][9]   6144   12   AsstFWUprBoundX   HwNm_s4p11[3][10]   2-2048   12   AsstFWUprBoundX   HwNm_s4p11[4][0]   2-2048   12   AsstFWUprBoundX   HwNm_s4p11[4][0]   2-2048   12   AsstFWUprBoundX   HwNm_s4p11[4][2]   2-2048   12   AsstFWUprBoundX   HwNm_s4p11[4][3]   4096   12   AsstFWUprBoundX   HwNm_s4p11[4][6]   6144   12   AsstFWUprBoundX   HwNm_s4p11[4][6]   6144   12   AsstFWUprBoundX   HwNm_s4p11[4][6]   6144   12   AsstFWUprBoundX   HwNm_s4p11[4][6]   6124   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   6144   614	
12 AsstFWUprBoundX HwNm_s4p11[3][0]       -12288         12 AsstFWUprBoundX HwNm_s4p11[3][1]       -10240         12 AsstFWUprBoundX HwNm_s4p11[3][2]       -8192         12 AsstFWUprBoundX HwNm_s4p11[3][4]       -4096         12 AsstFWUprBoundX HwNm_s4p11[3][6]       -2048         12 AsstFWUprBoundX HwNm_s4p11[3][7]       2048         12 AsstFWUprBoundX HwNm_s4p11[3][8]       0         12 AsstFWUprBoundX HwNm_s4p11[3][8]       4096         12 AsstFWUprBoundX HwNm_s4p11[3][8]       4096         12 AsstFWUprBoundX HwNm_s4p11[3][8]       4096         12 AsstFWUprBoundX HwNm_s4p11[3][9]       6144         12 AsstFWUprBoundX HwNm_s4p11[3][9]       6144         12 AsstFWUprBoundX HwNm_s4p11[4][0]       -2048         12 AsstFWUprBoundX HwNm_s4p11[4][1]       0         12 AsstFWUprBoundX HwNm_s4p11[4][2]       2048         12 AsstFWUprBoundX HwNm_s4p11[4][6]       10240         12 AsstFWUprBoundX HwNm_s4p11[4][6]       10240         12 AsstFWUprBoundX HwNm_s4p11[4][6]       10240         12 AsstFWUprBoundX HwNm_s4p11[4][7]       12288         12 AsstFWUprBoundX HwNm_s4p11[5][6]       16384         12 AsstFWUprBoundX HwNm_s4p11[5][7]       6183         12 AsstFWUprBoundX HwNm_s4p11[5][7]       6194         12 AsstFWUprBoundX HwNm_s4p1	
12_AsstFWUprBoundX_HwNm_s4p11[3][1] -10240 12_AsstFWUprBoundX_HwNm_s4p11[3][2] -8192 12_AsstFWUprBoundX_HwNm_s4p11[3][3] -6144 12_AsstFWUprBoundX_HwNm_s4p11[3][6] -2048 12_AsstFWUprBoundX_HwNm_s4p11[3][6] -2048 12_AsstFWUprBoundX_HwNm_s4p11[3][6] -2048 12_AsstFWUprBoundX_HwNm_s4p11[3][6] -2048 12_AsstFWUprBoundX_HwNm_s4p11[3][7] -2048 12_AsstFWUprBoundX_HwNm_s4p11[3][8] -4096 12_AsstFWUprBoundX_HwNm_s4p11[3][9] -6144 12_AsstFWUprBoundX_HwNm_s4p11[3][10] -2048 12_AsstFWUprBoundX_HwNm_s4p11[3][10] -2048 12_AsstFWUprBoundX_HwNm_s4p11[4][0] -2048 12_AsstFWUprBoundX_HwNm_s4p11[4][1] -0 -2048 12_AsstFWUprBoundX_HwNm_s4p11[4][1] -2048 12_AsstFWUprBoundX_HwNm_s4p11[4][2] -2048 12_AsstFWUprBoundX_HwNm_s4p11[4][6] -2048 12_AsstFWUprBoundX_HwNm_s4p11[6][0] -10240 12_AsstFWUprBoundX_HwNm_s4p11[6][0] -10240 12_AsstFWUprBoundX_HwNm_s4p11[6][1] -8192 12_AsstFWUprBoundX_HwNm_s4p11[6][1] -8192 12_AsstFWUprBoundX_HwNm_s4p11[6][1] -2048 12_AsstFWUprBoundX_HwNm_s4p11[6][1] -2048 12_AsstFWUprBoundX_HwNm_s4p11[6][6] -6144 12_AsstFWUprBoundX_HwNm_s4p11[6][6] -2048 12_AsstFWUprBoundX_HwNm_s4p11[6][6] -2048 12_AsstFWUprBoundX_HwNm_s4p11[6][6] -2048 12_AsstFWUprBoundX_HwNm_s4p11[6][6] -10240 12_Asst	
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12_AsstFWUprBoundX_HwNm_s4p11[3][5]       -4096         12_AsstFWUprBoundX_HwNm_s4p11[3][6]       0         12_AsstFWUprBoundX_HwNm_s4p11[3][7]       2048         12_AsstFWUprBoundX_HwNm_s4p11[3][7]       2048         12_AsstFWUprBoundX_HwNm_s4p11[3][8]       4096         12_AsstFWUprBoundX_HwNm_s4p11[3][9]       6144         12_AsstFWUprBoundX_HwNm_s4p11[3][10]       8192         12_AsstFWUprBoundX_HwNm_s4p11[4][0]       -2048         12_AsstFWUprBoundX_HwNm_s4p11[4][1]       0         12_AsstFWUprBoundX_HwNm_s4p11[4][2]       2048         12_AsstFWUprBoundX_HwNm_s4p11[4][2]       2048         12_AsstFWUprBoundX_HwNm_s4p11[4][3]       4096         12_AsstFWUprBoundX_HwNm_s4p11[4][6]       10240         12_AsstFWUprBoundX_HwNm_s4p11[4][6]       10240         12_AsstFWUprBoundX_HwNm_s4p11[4][6]       10240         12_AsstFWUprBoundX_HwNm_s4p11[4][6]       1436         12_AsstFWUprBoundX_HwNm_s4p11[4][6]       1436         12_AsstFWUprBoundX_HwNm_s4p11[5][1]       18432         12_AsstFWUprBoundX_HwNm_s4p11[5][1]       16384         12_AsstFWUprBoundX_HwNm_s4p11[5][1]       -10240         12_AsstFWUprBoundX_HwNm_s4p11[5][6]       0         12_AsstFWUprBoundX_HwNm_s4p11[5][7]       4096         12_AsstFWUprBoundX_HwNm_s4p11[6][6	
12_AsstFWUprBoundX_HwNm_s4p11[3][6]       -2048         12_AsstFWUprBoundX_HwNm_s4p11[3][7]       2048         12_AsstFWUprBoundX_HwNm_s4p11[3][7]       2048         12_AsstFWUprBoundX_HwNm_s4p11[3][8]       4096         12_AsstFWUprBoundX_HwNm_s4p11[3][9]       6144         12_AsstFWUprBoundX_HwNm_s4p11[4][0]       2048         12_AsstFWUprBoundX_HwNm_s4p11[4][0]       -2048         12_AsstFWUprBoundX_HwNm_s4p11[4][1]       0         12_AsstFWUprBoundX_HwNm_s4p11[4][2]       2048         12_AsstFWUprBoundX_HwNm_s4p11[4][3]       4096         12_AsstFWUprBoundX_HwNm_s4p11[4][4]       6144         12_AsstFWUprBoundX_HwNm_s4p11[4][6]       10240         12_AsstFWUprBoundX_HwNm_s4p11[4][6]       10240         12_AsstFWUprBoundX_HwNm_s4p11[4][6]       14336         12_AsstFWUprBoundX_HwNm_s4p11[4][9]       16384         12_AsstFWUprBoundX_HwNm_s4p11[4][9]       16384         12_AsstFWUprBoundX_HwNm_s4p11[5][1]       8192         12_AsstFWUprBoundX_HwNm_s4p11[5][1]       8192         12_AsstFWUprBoundX_HwNm_s4p11[5][1]       8192         12_AsstFWUprBoundX_HwNm_s4p11[5][6]       2048         12_AsstFWUprBoundX_HwNm_s4p11[5][6]       2048         12_AsstFWUprBoundX_HwNm_s4p11[6][6]       2048         12_AsstFWUprBoundX_HwNm_s4p11[6	
12_AsstFWUprBoundX_HwNm_s4p11[3][7]       2048         12_AsstFWUprBoundX_HwNm_s4p11[3][7]       2048         12_AsstFWUprBoundX_HwNm_s4p11[3][8]       4096         12_AsstFWUprBoundX_HwNm_s4p11[3][9]       6144         12_AsstFWUprBoundX_HwNm_s4p11[3][10]       8192         12_AsstFWUprBoundX_HwNm_s4p11[4][0]       -2048         12_AsstFWUprBoundX_HwNm_s4p11[4][1]       0         12_AsstFWUprBoundX_HwNm_s4p11[4][2]       2048         12_AsstFWUprBoundX_HwNm_s4p11[4][3]       4096         12_AsstFWUprBoundX_HwNm_s4p11[4][6]       6144         12_AsstFWUprBoundX_HwNm_s4p11[4][6]       10240         12_AsstFWUprBoundX_HwNm_s4p11[4][6]       10240         12_AsstFWUprBoundX_HwNm_s4p11[4][6]       10240         12_AsstFWUprBoundX_HwNm_s4p11[4][6]       14336         12_AsstFWUprBoundX_HwNm_s4p11[4][6]       16384         12_AsstFWUprBoundX_HwNm_s4p11[5][6]       16384         12_AsstFWUprBoundX_HwNm_s4p11[5][7]       8192         12_AsstFWUprBoundX_HwNm_s4p11[5][7]       8192         12_AsstFWUprBoundX_HwNm_s4p11[5][6]       2048         12_AsstFWUprBoundX_HwNm_s4p11[5][7]       4096         12_AsstFWUprBoundX_HwNm_s4p11[5][6]       2048         12_AsstFWUprBoundX_HwNm_s4p11[6][7]       4096         12_AsstFWUprBoundX_HwNm_s4p11[	
12_AsstFWUprBoundX_HwNm_s4p11[3][7]       2048         12_AsstFWUprBoundX_HwNm_s4p11[3][8]       4096         12_AsstFWUprBoundX_HwNm_s4p11[3][9]       6144         12_AsstFWUprBoundX_HwNm_s4p11[3][10]       8192         12_AsstFWUprBoundX_HwNm_s4p11[4][0]       -2048         12_AsstFWUprBoundX_HwNm_s4p11[4][1]       0         12_AsstFWUprBoundX_HwNm_s4p11[4][2]       2048         12_AsstFWUprBoundX_HwNm_s4p11[4][2]       2048         12_AsstFWUprBoundX_HwNm_s4p11[4][3]       4096         12_AsstFWUprBoundX_HwNm_s4p11[4][6]       6144         12_AsstFWUprBoundX_HwNm_s4p11[4][6]       10240         12_AsstFWUprBoundX_HwNm_s4p11[4][7]       12288         12_AsstFWUprBoundX_HwNm_s4p11[4][9]       16384         12_AsstFWUprBoundX_HwNm_s4p11[4][9]       16384         12_AsstFWUprBoundX_HwNm_s4p11[5][0]       -10240         12_AsstFWUprBoundX_HwNm_s4p11[5][1]       -8192         12_AsstFWUprBoundX_HwNm_s4p11[5][1]       -8192         12_AsstFWUprBoundX_HwNm_s4p11[5][6]       -6144         12_AsstFWUprBoundX_HwNm_s4p11[5][6]       0         12_AsstFWUprBoundX_HwNm_s4p11[5][6]       2048         12_AsstFWUprBoundX_HwNm_s4p11[5][6]       0         12_AsstFWUprBoundX_HwNm_s4p11[6][6]       -1444         12_AsstFWUprBoundX_HwNm_s4p11[6]	
12_AsstFWUprBoundX_HwNm_s4p11[3][8]       4096         12_AsstFWUprBoundX_HwNm_s4p11[3][9]       6144         12_AsstFWUprBoundX_HwNm_s4p11[3][10]       8192         12_AsstFWUprBoundX_HwNm_s4p11[4][0]       -2048         12_AsstFWUprBoundX_HwNm_s4p11[4][1]       0         12_AsstFWUprBoundX_HwNm_s4p11[4][2]       2048         12_AsstFWUprBoundX_HwNm_s4p11[4][3]       4096         12_AsstFWUprBoundX_HwNm_s4p11[4][6]       6144         12_AsstFWUprBoundX_HwNm_s4p11[4][6]       10240         12_AsstFWUprBoundX_HwNm_s4p11[4][6]       10240         12_AsstFWUprBoundX_HwNm_s4p11[4][7]       12288         12_AsstFWUprBoundX_HwNm_s4p11[4][7]       12288         12_AsstFWUprBoundX_HwNm_s4p11[4][10]       16384         12_AsstFWUprBoundX_HwNm_s4p11[4][10]       18432         12_AsstFWUprBoundX_HwNm_s4p11[5][0]       -10240         12_AsstFWUprBoundX_HwNm_s4p11[5][0]       -10240         12_AsstFWUprBoundX_HwNm_s4p11[5][7]       -8192         12_AsstFWUprBoundX_HwNm_s4p11[5][6]       -6144         12_AsstFWUprBoundX_HwNm_s4p11[5][6]       2048         12_AsstFWUprBoundX_HwNm_s4p11[5][6]       2048         12_AsstFWUprBoundX_HwNm_s4p11[5][6]       6144         12_AsstFWUprBoundX_HwNm_s4p11[6][6]       -16384         12_AsstFWUprBoundX_H	
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]       6144         t2_AsstFWUprBoundX_HwNm_s4p11[3][10]       8192         t2_AsstFWUprBoundX_HwNm_s4p11[4][0]       -2048         t2_AsstFWUprBoundX_HwNm_s4p11[4][1]       0         t2_AsstFWUprBoundX_HwNm_s4p11[4][2]       2048         t2_AsstFWUprBoundX_HwNm_s4p11[4][3]       4096         t2_AsstFWUprBoundX_HwNm_s4p11[4][4]       6144         t2_AsstFWUprBoundX_HwNm_s4p11[4][5]       8192         t2_AsstFWUprBoundX_HwNm_s4p11[4][6]       10240         t2_AsstFWUprBoundX_HwNm_s4p11[4][7]       12288         t2_AsstFWUprBoundX_HwNm_s4p11[4][7]       12288         t2_AsstFWUprBoundX_HwNm_s4p11[4][9]       16384         t2_AsstFWUprBoundX_HwNm_s4p11[4][9]       16384         t2_AsstFWUprBoundX_HwNm_s4p11[5][0]       -10240         t2_AsstFWUprBoundX_HwNm_s4p11[5][0]       -10240         t2_AsstFWUprBoundX_HwNm_s4p11[5][1]       -8192         t2_AsstFWUprBoundX_HwNm_s4p11[5][6]       -6144         t2_AsstFWUprBoundX_HwNm_s4p11[5][6]       2048         t2_AsstFWUprBoundX_HwNm_s4p11[5][6]       2048         t2_AsstFWUprBoundX_HwNm_s4p11[5][6]       2048         t2_AsstFWUprBoundX_HwNm_s4p11[6][6]       6144         t2_AsstFWUprBoundX_HwNm_s4p11[6][6]       -14336         t2_AsstFWUprBoundX_HwNm	
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]       6144         t2_AsstFWUprBoundX_HwNm_s4p11[3][10]       8192         t2_AsstFWUprBoundX_HwNm_s4p11[4][0]       -2048         t2_AsstFWUprBoundX_HwNm_s4p11[4][1]       0         t2_AsstFWUprBoundX_HwNm_s4p11[4][2]       2048         t2_AsstFWUprBoundX_HwNm_s4p11[4][3]       4096         t2_AsstFWUprBoundX_HwNm_s4p11[4][4]       6144         t2_AsstFWUprBoundX_HwNm_s4p11[4][5]       8192         t2_AsstFWUprBoundX_HwNm_s4p11[4][6]       10240         t2_AsstFWUprBoundX_HwNm_s4p11[4][7]       12288         t2_AsstFWUprBoundX_HwNm_s4p11[4][7]       12288         t2_AsstFWUprBoundX_HwNm_s4p11[4][9]       16384         t2_AsstFWUprBoundX_HwNm_s4p11[4][9]       16384         t2_AsstFWUprBoundX_HwNm_s4p11[5][0]       -10240         t2_AsstFWUprBoundX_HwNm_s4p11[5][0]       -10240         t2_AsstFWUprBoundX_HwNm_s4p11[5][1]       -8192         t2_AsstFWUprBoundX_HwNm_s4p11[5][6]       -6144         t2_AsstFWUprBoundX_HwNm_s4p11[5][6]       2048         t2_AsstFWUprBoundX_HwNm_s4p11[5][6]       2048         t2_AsstFWUprBoundX_HwNm_s4p11[5][6]       2048         t2_AsstFWUprBoundX_HwNm_s4p11[6][6]       6144         t2_AsstFWUprBoundX_HwNm_s4p11[6][6]       -14336         t2_AsstFWUprBoundX_HwNm	
12_AsstFWUprBoundX_HwNm_s4p11[3][10]       8192         12_AsstFWUprBoundX_HwNm_s4p11[4][0]       -2048         12_AsstFWUprBoundX_HwNm_s4p11[4][1]       0         12_AsstFWUprBoundX_HwNm_s4p11[4][2]       2048         12_AsstFWUprBoundX_HwNm_s4p11[4][3]       4096         12_AsstFWUprBoundX_HwNm_s4p11[4][4]       6144         12_AsstFWUprBoundX_HwNm_s4p11[4][5]       8192         12_AsstFWUprBoundX_HwNm_s4p11[4][6]       10240         12_AsstFWUprBoundX_HwNm_s4p11[4][7]       12288         12_AsstFWUprBoundX_HwNm_s4p11[4][7]       12288         12_AsstFWUprBoundX_HwNm_s4p11[4][9]       16384         12_AsstFWUprBoundX_HwNm_s4p11[4][9]       16384         12_AsstFWUprBoundX_HwNm_s4p11[5][0]       -10240         12_AsstFWUprBoundX_HwNm_s4p11[5][1]       -8192         12_AsstFWUprBoundX_HwNm_s4p11[5][1]       -8192         12_AsstFWUprBoundX_HwNm_s4p11[5][3]       -4096         12_AsstFWUprBoundX_HwNm_s4p11[5][6]       2048         12_AsstFWUprBoundX_HwNm_s4p11[5][6]       2048         12_AsstFWUprBoundX_HwNm_s4p11[5][6]       2048         12_AsstFWUprBoundX_HwNm_s4p11[6][6]       -144         12_AsstFWUprBoundX_HwNm_s4p11[6][6]       -18432         12_AsstFWUprBoundX_HwNm_s4p11[6][6]       -18432         12_AsstFWUprBoundX_HwN	
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]       -2048         t2_AsstFWUprBoundX_HwNm_s4p11[4][1]       0         t2_AsstFWUprBoundX_HwNm_s4p11[4][2]       2048         t2_AsstFWUprBoundX_HwNm_s4p11[4][3]       4096         t2_AsstFWUprBoundX_HwNm_s4p11[4][4]       6144         t2_AsstFWUprBoundX_HwNm_s4p11[4][5]       8192         t2_AsstFWUprBoundX_HwNm_s4p11[4][6]       10240         t2_AsstFWUprBoundX_HwNm_s4p11[4][7]       12288         t2_AsstFWUprBoundX_HwNm_s4p11[4][8]       14336         t2_AsstFWUprBoundX_HwNm_s4p11[4][9]       16384         t2_AsstFWUprBoundX_HwNm_s4p11[4][0]       18432         t2_AsstFWUprBoundX_HwNm_s4p11[5][0]       -10240         t2_AsstFWUprBoundX_HwNm_s4p11[5][1]       -8192         t2_AsstFWUprBoundX_HwNm_s4p11[5][2]       -6144         t2_AsstFWUprBoundX_HwNm_s4p11[5][3]       -4096         t2_AsstFWUprBoundX_HwNm_s4p11[5][4]       -2048         t2_AsstFWUprBoundX_HwNm_s4p11[5][6]       2048         t2_AsstFWUprBoundX_HwNm_s4p11[5][6]       2048         t2_AsstFWUprBoundX_HwNm_s4p11[5][6]       4096         t2_AsstFWUprBoundX_HwNm_s4p11[6][6]       -144         t2_AsstFWUprBoundX_HwNm_s4p11[6][6]       -144         t2_AsstFWUprBoundX_HwNm_s4p11[6][6]       -16384         t2_AsstFWUprBoundX_HwNm_	
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t2_AsstFWUprBoundX_HwNm_s4p11[4][2] 2048 t2_AsstFWUprBoundX_HwNm_s4p11[4][3] 4096 t2_AsstFWUprBoundX_HwNm_s4p11[4][4] 6144 t2_AsstFWUprBoundX_HwNm_s4p11[4][5] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[4][6] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[4][7] 12288 t2_AsstFWUprBoundX_HwNm_s4p11[4][8] 14336 t2_AsstFWUprBoundX_HwNm_s4p11[4][9] 16384 t2_AsstFWUprBoundX_HwNm_s4p11[4][10] 18432 t2_AsstFWUprBoundX_HwNm_s4p11[5][0] 16384 t2_AsstFWUprBoundX_HwNm_s4p11[5][1] 18432 t2_AsstFWUprBoundX_HwNm_s4p11[5][1] 18432 t2_AsstFWUprBoundX_HwNm_s4p11[5][2] 16144 t2_AsstFWUprBoundX_HwNm_s4p11[5][2] 16144 t2_AsstFWUprBoundX_HwNm_s4p11[5][4] 16248 t2_AsstFWUprBoundX_HwNm_s4p11[5][6] 16248 t2_AsstFWUprBoundX_HwNm_s4p11[5][6] 16248 t2_AsstFWUprBoundX_HwNm_s4p11[5][6] 16248 t2_AsstFWUprBoundX_HwNm_s4p11[5][6] 16248 t2_AsstFWUprBoundX_HwNm_s4p11[5][9] 16249 t2_AsstFWUprBoundX_HwNm_s4p11[6][9] 16240 t2_AsstFWUprBoundX_HwNm_s4p11[6][9] 16240 t2_AsstFWUprBoundX_HwNm_s4p11[6][1] 16240 t2_AsstFWUprBoundX_HwNm_s4p11[6][6] 1644	
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t2_AsstFWUprBoundX_HwNm_s4p11[5][8] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[5][9] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[5][10] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[6][0] -18432 t2_AsstFWUprBoundX_HwNm_s4p11[6][1] -16384 t2_AsstFWUprBoundX_HwNm_s4p11[6][2] -14336 t2_AsstFWUprBoundX_HwNm_s4p11[6][3] -12288 t2_AsstFWUprBoundX_HwNm_s4p11[6][4] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[6][5] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[6][6] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[6][7] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[6][8] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][8] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][9] 0	
t2_AsstFWUprBoundX_HwNm_s4p11[5][9] 8192 t2_AsstFWUprBoundX_HwNm_s4p11[5][10] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[6][0] -18432 t2_AsstFWUprBoundX_HwNm_s4p11[6][1] -16384 t2_AsstFWUprBoundX_HwNm_s4p11[6][2] -14336 t2_AsstFWUprBoundX_HwNm_s4p11[6][3] -12288 t2_AsstFWUprBoundX_HwNm_s4p11[6][4] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[6][5] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[6][6] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[6][7] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[6][8] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][9] 0	
t2_AsstFWUprBoundX_HwNm_s4p11[5][10] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[6][0] -18432 t2_AsstFWUprBoundX_HwNm_s4p11[6][1] -16384 t2_AsstFWUprBoundX_HwNm_s4p11[6][2] -14336 t2_AsstFWUprBoundX_HwNm_s4p11[6][3] -12288 t2_AsstFWUprBoundX_HwNm_s4p11[6][4] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[6][5] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[6][6] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[6][7] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[6][8] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][9] 0	
t2_AsstFWUprBoundX_HwNm_s4p11[5][10] 10240 t2_AsstFWUprBoundX_HwNm_s4p11[6][0] -18432 t2_AsstFWUprBoundX_HwNm_s4p11[6][1] -16384 t2_AsstFWUprBoundX_HwNm_s4p11[6][2] -14336 t2_AsstFWUprBoundX_HwNm_s4p11[6][3] -12288 t2_AsstFWUprBoundX_HwNm_s4p11[6][4] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[6][5] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[6][6] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[6][7] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[6][8] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][9] 0	
t2_AsstFWUprBoundX_HwNm_s4p11[6][0] -18432 t2_AsstFWUprBoundX_HwNm_s4p11[6][1] -16384 t2_AsstFWUprBoundX_HwNm_s4p11[6][2] -14336 t2_AsstFWUprBoundX_HwNm_s4p11[6][3] -12288 t2_AsstFWUprBoundX_HwNm_s4p11[6][4] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[6][5] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[6][6] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[6][7] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[6][8] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][9] 0	
t2_AsstFWUprBoundX_HwNm_s4p11[6][1] -16384 t2_AsstFWUprBoundX_HwNm_s4p11[6][2] -14336 t2_AsstFWUprBoundX_HwNm_s4p11[6][3] -12288 t2_AsstFWUprBoundX_HwNm_s4p11[6][4] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[6][5] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[6][6] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[6][7] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[6][8] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][9] 0	
t2_AsstFWUprBoundX_HwNm_s4p11[6][2] -14336 t2_AsstFWUprBoundX_HwNm_s4p11[6][3] -12288 t2_AsstFWUprBoundX_HwNm_s4p11[6][4] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[6][5] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[6][6] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[6][7] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[6][8] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][9] 0	
t2_AsstFWUprBoundX_HwNm_s4p11[6][3] -12288 t2_AsstFWUprBoundX_HwNm_s4p11[6][4] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[6][5] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[6][6] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[6][7] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[6][8] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][9] 0	
t2_AsstFWUprBoundX_HwNm_s4p11[6][4] -10240 t2_AsstFWUprBoundX_HwNm_s4p11[6][5] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[6][6] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[6][7] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[6][8] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][9] 0	
t2_AsstFWUprBoundX_HwNm_s4p11[6][5] -8192 t2_AsstFWUprBoundX_HwNm_s4p11[6][6] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[6][7] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[6][8] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][9] 0	
t2_AsstFWUprBoundX_HwNm_s4p11[6][6] -6144 t2_AsstFWUprBoundX_HwNm_s4p11[6][7] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[6][8] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][9] 0	
t2_AsstFWUprBoundX_HwNm_s4p11[6][7] -4096 t2_AsstFWUprBoundX_HwNm_s4p11[6][8] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][9] 0	
t2_AsstFWUprBoundX_HwNm_s4p11[6][8] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][9] 0	
t2_AsstFWUprBoundX_HwNm_s4p11[6][8] -2048 t2_AsstFWUprBoundX_HwNm_s4p11[6][9] 0	
t2_AsstFWUprBoundX_HwNm_s4p11[6][9] 0	
ı∠_Assırvv∪prBounax_Hwinm_s4p11[6][10]   2048	
t2_AsstFWUprBoundX_HwNm_s4p11[7][0] -10240	
t2_AsstFWUprBoundX_HwNm_s4p11[7][1] -8192	
t2_AsstFWUprBoundX_HwNm_s4p11[7][2] -6144	
t2_AsstFWUprBoundX_HwNm_s4p11[7][3] -4096	
t2_AsstFWUprBoundX_HwNm_s4p11[7][4] -2048	
t2_AsstFWUprBoundX_HwNm_s4p11[7][5] 0	
t2_AsstFWUprBoundX_HwNm_s4p11[7][7] 4096	
t2_AsstFWUprBoundX_HwNm_s4p11[7][8] 6144	
t2_AsstFWUprBoundX_HwNm_s4p11[7][9] 8192	
t2_AsstFWUprBoundX_HwNm_s4p11[7][10] 10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] 6144	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] 8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] 10240	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] 12288	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] 14336	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5] 16384	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6] 18432	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7] 20480	





Name	
	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192
10. A - (FIA) I - D - ve dV A4-Alex 4 4470703	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	140000
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288
	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10] t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240

AssistFirewall Per1

2015-03-23, 11:55:49+0530



Input Value t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][4] -2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][5] t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][6] 2048 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][7] 4096 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][8] 6144 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][9] 8192 t2\_AsstFWUprBoundY\_MtrNm\_s4p11[7][10] 10240  $t\_AsstFWDefltAssistX\_HwNm\_u8p8[0]$ 896 t\_AsstFWDefltAssistX\_HwNm\_u8p8[1] 922 t AsstFWDefltAssistX HwNm u8p8[2] 947 t\_AsstFWDefltAssistX\_HwNm\_u8p8[3] 973 t\_AsstFWDefltAssistX\_HwNm\_u8p8[4] 998 t\_AsstFWDefltAssistX\_HwNm\_u8p8[5] 1024 t AsstEWDefltAssistX HwNm u8n8[6] 1050 t\_AsstFWDefltAssistX\_HwNm\_u8p8[7] 1075 t AsstFWDefltAssistX\_HwNm\_u8p8[8] 1101 t\_AsstFWDefltAssistX\_HwNm\_u8p8[9] 1126 t AsstFWDefltAssistX HwNm u8p8[10] 1152 t\_AsstFWDefltAssistX\_HwNm\_u8p8[11] 1178 t AsstFWDefltAssistX HwNm u8p8[12] 1203 t\_AsstFWDefltAssistX\_HwNm\_u8p8[13] 1229 t\_AsstFWDefltAssistX\_HwNm\_u8p8[14] 1254 t\_AsstFWDefltAssistX\_HwNm\_u8p8[15] 1280 t\_AsstFWDefltAssistX\_HwNm\_u8p8[16] 1306 t\_AsstFWDefltAssistX\_HwNm\_u8p8[17] 1331 t\_AsstFWDefltAssistX\_HwNm\_u8p8[18] 1357 1382 t\_AsstFWDefltAssistX\_HwNm\_u8p8[19] t\_AsstFWDefltAssistY\_MtrNm\_s4p11[0] 3686 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[1] 3891 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[2] 4096 t AsstFWDefltAssistY MtrNm s4p11[3] 4301 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[4] 4506 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[5] 4710 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[6] 4915 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[7] 5120 t AsstFWDefltAssistY MtrNm s4p11[8] 5325 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[9] 5530 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[10] 5734 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[11] 5939 t AsstFWDefltAssistY MtrNm s4p11[12] 6144 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[13] 6349 t AsstFWDefltAssistY MtrNm s4p11[14] 6554 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[15] 6758 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[16] 6963 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[17] 7168 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[18] 7373 t\_AsstFWDefltAssistY\_MtrNm\_s4p11[19] 7578 t\_AsstFWPstepNstepThresh\_Cnt\_u16[0] 237 t\_AsstFWPstepNstepThresh\_Cnt\_u16[1] 667 27904 t\_AsstFWVehSpd\_Kph\_u9p7[0] t\_AsstFWVehSpd\_Kph\_u9p7[1] 28032 t\_AsstFWVehSpd\_Kph\_u9p7[2] 28160 28288 t\_AsstFWVehSpd\_Kph\_u9p7[3] t\_AsstFWVehSpd\_Kph\_u9p7[4] 28416 t\_AsstFWVehSpd\_Kph\_u9p7[5] 28544 t\_AsstFWVehSpd\_Kph\_u9p7[6] 28672 t AsstFWVehSpd Kph u9p7[7] 28800  $tgt\_AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32.value$ -5.5 tgt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_lgc.value 0 tgt\_AssistFirewall\_Per1\_HighFreqAssist\_MtrNm\_f32.value -5.0999999  $tgt\_AssistFirewall\_Per1\_HwTorque\_HwNm\_f32.value$ 7.11000013 tot AssistFirewall Per1 HysteresisComp MtrNm f32.value 7.32999992  $tgt\_AssistFirewall\_Per1\_MEC\_Counter\_Cnt\_enum.value$ 2 tot AssistFirewall Per1 VehicleSpeed Kph f32.value 209.300003  $tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32$ tgt\_AssistFirewall\_Per1\_AsstFirewallActive\_Uls\_f32 tot Rte Inst Ap AssistFirewall.AssistFirewall Per1 BaseAssistCmd MtrNm f32 tot AssistFirewall Per1 BaseAssistCmd MtrNm f32

AssistFirewall\_Per1







Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2 AsstFWUprBoundX HwNm s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2 AsstFWUprBoundX HwNm s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
to ApotEM/Inchaindy Hushim adot11[7][0]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	
tz_AsstrWUprBoundX_nwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	10240 12288 8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	10240 12288 8192 10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	10240 12288 8192 10240 12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240 12288 8192 10240 12288 14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240 12288 8192 10240 12288 14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240 12288 8192 10240 12288 14336 16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240 12288 8192 10240 12288 14336





t2_AsstFWUprBoundY_MtrNm_s4p11[0][8] t2_AsstFWUprBoundY_MtrNm_s4p11[0][9] t2_AsstFWUprBoundY_MtrNm_s4p11[0][10] t2_AsstFWUprBoundY_MtrNm_s4p11[1][0] t2_AsstFWUprBoundY_MtrNm_s4p11[1][1] t2_AsstFWUprBoundY_MtrNm_s4p11[1][2] t2_AsstFWUprBoundY_MtrNm_s4p11[1][3] t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][7] t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] t2_AsstFWUprBoundY_MtrNm_s4p11[1][0] t2_AsstFWUprBoundY_MtrNm_s4p11[1][0] t2_AsstFWUprBoundY_MtrNm_s4p11[2][0] t2_AsstFWUprBoundY_MtrNm_s4p11[2][0] t2_AsstFWUprBoundY_MtrNm_s4p11[2][1] t2_AsstFWUprBoundY_MtrNm_s4p11[2][2] t2_AsstFWUprBoundY_MtrNm_s4p11[2][3] t2_AsstFWUprBoundY_MtrNm_s4p11[2][4] t2_AsstFWUprBoundY_MtrNm_s4p11[2][4] t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	24576 26624 28672 -6144 -4096 -2048 0 2048 4096 6144 8192 10240 12288 14336 -8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10] t2_AsstFWUprBoundY_MtrNm_s4p11[1][0] t2_AsstFWUprBoundY_MtrNm_s4p11[1][1] t2_AsstFWUprBoundY_MtrNm_s4p11[1][2] t2_AsstFWUprBoundY_MtrNm_s4p11[1][3] t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][7] t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] t2_AsstFWUprBoundY_MtrNm_s4p11[1][0] t2_AsstFWUprBoundY_MtrNm_s4p11[1][0] t2_AsstFWUprBoundY_MtrNm_s4p11[2][0] t2_AsstFWUprBoundY_MtrNm_s4p11[2][1] t2_AsstFWUprBoundY_MtrNm_s4p11[2][1] t2_AsstFWUprBoundY_MtrNm_s4p11[2][2] t2_AsstFWUprBoundY_MtrNm_s4p11[2][3] t2_AsstFWUprBoundY_MtrNm_s4p11[2][3] t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	28672 -6144 -4096 -2048 0 2048 4096 6144 8192 10240 12288 14336 -8192 -6144
12_AsstFWUprBoundY_MtrNm_s4p11[1][0] 12_AsstFWUprBoundY_MtrNm_s4p11[1][1] 12_AsstFWUprBoundY_MtrNm_s4p11[1][2] 12_AsstFWUprBoundY_MtrNm_s4p11[1][3] 12_AsstFWUprBoundY_MtrNm_s4p11[1][6] 12_AsstFWUprBoundY_MtrNm_s4p11[1][6] 12_AsstFWUprBoundY_MtrNm_s4p11[1][7] 12_AsstFWUprBoundY_MtrNm_s4p11[1][8] 12_AsstFWUprBoundY_MtrNm_s4p11[1][8] 12_AsstFWUprBoundY_MtrNm_s4p11[1][9] 12_AsstFWUprBoundY_MtrNm_s4p11[1][0] 12_AsstFWUprBoundY_MtrNm_s4p11[2][0] 12_AsstFWUprBoundY_MtrNm_s4p11[2][0] 12_AsstFWUprBoundY_MtrNm_s4p11[2][1] 12_AsstFWUprBoundY_MtrNm_s4p11[2][2] 12_AsstFWUprBoundY_MtrNm_s4p11[2][3] 12_AsstFWUprBoundY_MtrNm_s4p11[2][3] 12_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144 -4096 -2048 0 2048 4096 6144 8192 10240 12288 14336 -8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1] t2_AsstFWUprBoundY_MtrNm_s4p11[1][2] t2_AsstFWUprBoundY_MtrNm_s4p11[1][3] t2_AsstFWUprBoundY_MtrNm_s4p11[1][4] t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][6] t2_AsstFWUprBoundY_MtrNm_s4p11[1][7] t2_AsstFWUprBoundY_MtrNm_s4p11[1][8] t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] t2_AsstFWUprBoundY_MtrNm_s4p11[1][9] t2_AsstFWUprBoundY_MtrNm_s4p11[1][0] t2_AsstFWUprBoundY_MtrNm_s4p11[2][0] t2_AsstFWUprBoundY_MtrNm_s4p11[2][0] t2_AsstFWUprBoundY_MtrNm_s4p11[2][1] t2_AsstFWUprBoundY_MtrNm_s4p11[2][2] t2_AsstFWUprBoundY_MtrNm_s4p11[2][3] t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-4096 -2048 0 2048 4096 6144 8192 10240 12288 14336 -8192 -6144
12_AsstFWUprBoundY_MtrNm_s4p11[1][2] 12_AsstFWUprBoundY_MtrNm_s4p11[1][3] 12_AsstFWUprBoundY_MtrNm_s4p11[1][4] 12_AsstFWUprBoundY_MtrNm_s4p11[1][6] 12_AsstFWUprBoundY_MtrNm_s4p11[1][6] 12_AsstFWUprBoundY_MtrNm_s4p11[1][7] 12_AsstFWUprBoundY_MtrNm_s4p11[1][8] 12_AsstFWUprBoundY_MtrNm_s4p11[1][9] 12_AsstFWUprBoundY_MtrNm_s4p11[1][10] 12_AsstFWUprBoundY_MtrNm_s4p11[2][0] 12_AsstFWUprBoundY_MtrNm_s4p11[2][0] 12_AsstFWUprBoundY_MtrNm_s4p11[2][1] 12_AsstFWUprBoundY_MtrNm_s4p11[2][2] 12_AsstFWUprBoundY_MtrNm_s4p11[2][3] 12_AsstFWUprBoundY_MtrNm_s4p11[2][3] 12_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-2048 0 2048 4096 6144 8192 10240 12288 14336 -8192 -6144
12_AsstFWUprBoundY_MtrNm_s4p11[1][3] 12_AsstFWUprBoundY_MtrNm_s4p11[1][4] 12_AsstFWUprBoundY_MtrNm_s4p11[1][6] 12_AsstFWUprBoundY_MtrNm_s4p11[1][6] 12_AsstFWUprBoundY_MtrNm_s4p11[1][7] 12_AsstFWUprBoundY_MtrNm_s4p11[1][8] 12_AsstFWUprBoundY_MtrNm_s4p11[1][9] 12_AsstFWUprBoundY_MtrNm_s4p11[1][0] 12_AsstFWUprBoundY_MtrNm_s4p11[2][0] 12_AsstFWUprBoundY_MtrNm_s4p11[2][0] 12_AsstFWUprBoundY_MtrNm_s4p11[2][1] 12_AsstFWUprBoundY_MtrNm_s4p11[2][1] 12_AsstFWUprBoundY_MtrNm_s4p11[2][2] 12_AsstFWUprBoundY_MtrNm_s4p11[2][3] 12_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0 2048 4096 6144 8192 10240 12288 14336 -8192 -6144
12_AsstFWUprBoundY_MtrNm_s4p11[1][4] 12_AsstFWUprBoundY_MtrNm_s4p11[1][6] 12_AsstFWUprBoundY_MtrNm_s4p11[1][6] 12_AsstFWUprBoundY_MtrNm_s4p11[1][7] 12_AsstFWUprBoundY_MtrNm_s4p11[1][8] 12_AsstFWUprBoundY_MtrNm_s4p11[1][9] 12_AsstFWUprBoundY_MtrNm_s4p11[1][10] 12_AsstFWUprBoundY_MtrNm_s4p11[2][0] 12_AsstFWUprBoundY_MtrNm_s4p11[2][1] 12_AsstFWUprBoundY_MtrNm_s4p11[2][1] 12_AsstFWUprBoundY_MtrNm_s4p11[2][2] 12_AsstFWUprBoundY_MtrNm_s4p11[2][3] 12_AsstFWUprBoundY_MtrNm_s4p11[2][3] 12_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048 4096 6144 8192 10240 12288 14336 -8192 -6144
12_AsstFWUprBoundY_MtrNm_s4p11[1][5] 12_AsstFWUprBoundY_MtrNm_s4p11[1][6] 12_AsstFWUprBoundY_MtrNm_s4p11[1][7] 12_AsstFWUprBoundY_MtrNm_s4p11[1][8] 12_AsstFWUprBoundY_MtrNm_s4p11[1][9] 12_AsstFWUprBoundY_MtrNm_s4p11[1][10] 12_AsstFWUprBoundY_MtrNm_s4p11[2][0] 12_AsstFWUprBoundY_MtrNm_s4p11[2][1] 12_AsstFWUprBoundY_MtrNm_s4p11[2][1] 12_AsstFWUprBoundY_MtrNm_s4p11[2][2] 12_AsstFWUprBoundY_MtrNm_s4p11[2][3] 12_AsstFWUprBoundY_MtrNm_s4p11[2][3] 12_AsstFWUprBoundY_MtrNm_s4p11[2][4]	4096 6144 8192 10240 12288 14336 -8192
12_AsstFWUprBoundY_MtrNm_s4p11[1][6] 12_AsstFWUprBoundY_MtrNm_s4p11[1][7] 12_AsstFWUprBoundY_MtrNm_s4p11[1][8] 12_AsstFWUprBoundY_MtrNm_s4p11[1][9] 12_AsstFWUprBoundY_MtrNm_s4p11[1][10] 12_AsstFWUprBoundY_MtrNm_s4p11[2][0] 12_AsstFWUprBoundY_MtrNm_s4p11[2][1] 12_AsstFWUprBoundY_MtrNm_s4p11[2][1] 12_AsstFWUprBoundY_MtrNm_s4p11[2][2] 12_AsstFWUprBoundY_MtrNm_s4p11[2][3] 12_AsstFWUprBoundY_MtrNm_s4p11[2][3] 12_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144 8192 10240 12288 14336 -8192 -6144
i2_AsstFWUprBoundY_MtrNm_s4p11[1][7] i2_AsstFWUprBoundY_MtrNm_s4p11[1][8] i2_AsstFWUprBoundY_MtrNm_s4p11[1][9] i2_AsstFWUprBoundY_MtrNm_s4p11[1][10] i2_AsstFWUprBoundY_MtrNm_s4p11[2][0] i2_AsstFWUprBoundY_MtrNm_s4p11[2][1] i2_AsstFWUprBoundY_MtrNm_s4p11[2][2] i2_AsstFWUprBoundY_MtrNm_s4p11[2][2] i2_AsstFWUprBoundY_MtrNm_s4p11[2][3] i2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192 10240 12288 14336 -8192 -6144
i2_AsstFWUprBoundY_MtrNm_s4p11[1][8] i2_AsstFWUprBoundY_MtrNm_s4p11[1][9] i2_AsstFWUprBoundY_MtrNm_s4p11[1][10] i2_AsstFWUprBoundY_MtrNm_s4p11[2][0] i2_AsstFWUprBoundY_MtrNm_s4p11[2][1] i2_AsstFWUprBoundY_MtrNm_s4p11[2][2] i2_AsstFWUprBoundY_MtrNm_s4p11[2][3] i2_AsstFWUprBoundY_MtrNm_s4p11[2][3] i2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240 12288 14336 -8192 -6144
i2_AsstFWUprBoundY_MtrNm_s4p11[1][9] i2_AsstFWUprBoundY_MtrNm_s4p11[1][10] i2_AsstFWUprBoundY_MtrNm_s4p11[2][0] i2_AsstFWUprBoundY_MtrNm_s4p11[2][1] i2_AsstFWUprBoundY_MtrNm_s4p11[2][2] i2_AsstFWUprBoundY_MtrNm_s4p11[2][3] i2_AsstFWUprBoundY_MtrNm_s4p11[2][3] i2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	12288 14336 -8192 -6144
i2_AsstFWUprBoundY_MtrNm_s4p11[1][10] i2_AsstFWUprBoundY_MtrNm_s4p11[2][0] i2_AsstFWUprBoundY_MtrNm_s4p11[2][1] i2_AsstFWUprBoundY_MtrNm_s4p11[2][2] i2_AsstFWUprBoundY_MtrNm_s4p11[2][3] i2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	14336 -8192 -6144
i2_AsstFWUprBoundY_MtrNm_s4p11[2][0] i2_AsstFWUprBoundY_MtrNm_s4p11[2][1] i2_AsstFWUprBoundY_MtrNm_s4p11[2][2] i2_AsstFWUprBoundY_MtrNm_s4p11[2][3] i2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192 -6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]  2_AsstFWUprBoundY_MtrNm_s4p11[2][1]  2_AsstFWUprBoundY_MtrNm_s4p11[2][2]  2_AsstFWUprBoundY_MtrNm_s4p11[2][3]  2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][1] 2_AsstFWUprBoundY_MtrNm_s4p11[2][2] 2_AsstFWUprBoundY_MtrNm_s4p11[2][3] 2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	
2_AsstFWUprBoundY_MtrNm_s4p11[2][2] 2_AsstFWUprBoundY_MtrNm_s4p11[2][3] 2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	4006
2_AsstFWUprBoundY_MtrNm_s4p11[2][3] 2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-2048
	0
	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][8] 2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-18432
2 AsstFWUprBoundY MtrNm s4p11[4][6]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][1] 2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	
	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
	-4096
:2_AsstFWUprBoundY_MtrNm_s4p11[7][2] :2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048 4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6] t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_Asst WopiBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	922
t_AsstFWDefltAssistX_HwNm_u8p8[1]	947
t_AsstFWDefltAssistX_HwNm_u8p8[2]	973
t_AsstFWDefltAssistX_HwNm_u8p8[3]	998
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[11] t_AsstFWDefltAssistX_HwNm_u8p8[12]	1203 1229
t_AsstFWDefitAssistX_HwNm_u8p8[13]	1254
t_AsstFWDefitAssistX_HwNm_u8p8[14]	1280
t AsstFWDefltAssistX HwNm u8p8[15]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1382
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1408
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5734 5939
t_AsstFWDefltAssistY_MtrNm_s4p11[9] t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6144
t AsstFWDefitAssistY MtrNm s4p11[11]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6554
t AsstFWDefltAssistY MtrNm s4p11[13]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7987
t_AsstFWPstepNstepThresh_Cnt_u16[0]	238
t_AsstFWPstepNstepThresh_Cnt_u16[1]	671
t_AsstFWVehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1]	30976
t_AsstFWVehSpd_Kph_u9p7[2]	31104
t_AsstFWVehSpd_Kph_u9p7[3] t_AsstFWVehSpd_Kph_u9p7[4]	31232 31360
t_AsstFWVehSpd_kph_u9p7[4]	31488
t_AsstFWVehSpd_Kph_u9p7[6]	31616
t_AsstFWVehSpd_Kph_u9p7[7]	31744
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.5999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.19999981
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.21999979
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7.44000006
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	220.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_UIs_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.52719975	5.52720022 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	671	671 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.89990234	3.89990234 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.31799984	-5.31799984 ± 4.88E-04	•
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.4000001	4.4000001 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8.22799969	8.22799969 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	•
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.89990234	3.89990234 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	•
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	•

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-8.80000019
AssistFirewall ActiveKSV M str.K Uls f32	0.00125584798
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0
AssistFirewall AsstReducedPerfSV Cnt M Igc	0
AssistFirewall CombAsstSV MtrNm M f32	-8.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-52.7999992
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00125584798
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00062859
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-8.80000019
AssistFirewall LwrBoundKSV M str.K Uls f32	0.00125584798
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-16
Assisti ilewali_Oprodulukov_M_str.Sv_Ols_i32	0.00125584798
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
<_AsstFWInpLimitBaseAsst_MtrNm_f32	0
AsstFWInpLimitHFA MtrNm f32	0
<pre>&lt;_AsstFWInpLimitHysComp_MtrNm_f32</pre>	0
<_AsstFWNstep_Cnt_u16	0
<pre>c_nest Printerp_cnt_u16</pre>	0
RestoreThresh MtrNm f32	0
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-20480
2 AsstFWUprBoundX HwNm s4p11[0][9]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-20480
2 AsstFWUprBoundX HwNm s4p11[1][6]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	-20480
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-20480





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-20480
	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-20480
, , , , , , , , , , , , , , , , , , , ,	
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-20480
t2 AsstFWUprBoundX HwNm s4p11[7][9]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][9] t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	-20480 -20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-20480 -20480 -32768
t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-20480 -20480 -32768 -32768
t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-20480 -20480 -32768 -32768 -32768
t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-20480 -20480 -32768 -32768
t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-20480 -20480 -32768 -32768 -32768
t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-20480 -20480 -32768 -32768 -32768 -32768
t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-20480 -20480 -32768 -32768 -32768 -32768 -32768 -32768
t2_AsstFWUprBoundX_HwNm_s4p11[7][10] t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-20480 -20480 -32768 -32768 -32768 -32768 -32768





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5] t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-32768 -32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6] t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-32768 -32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-32768
	-32768 -32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-32768 -32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0] t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-32768





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-32768 -32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7] t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	-32768
t_AsstFWDefltAssistX_HwNm_u8p8[0]	0
t_AsstFWDefltAssistX_HwNm_u8p8[1]	0
t_AsstFWDefltAssistX_HwNm_u8p8[2]	0
t_AsstFWDefltAssistX_HwNm_u8p8[3]	0
t_AsstFWDefltAssistX_HwNm_u8p8[4]	0
t_AsstFWDefltAssistX_HwNm_u8p8[5]	0
t_AsstFWDefltAssistX_HwNm_u8p8[6]	0
t_AsstFWDefltAssistX_HwNm_u8p8[7]	0
t_AsstFWDefltAssistX_HwNm_u8p8[8]	0
t_AsstFWDefltAssistX_HwNm_u8p8[9]	0
t_AsstFWDefltAssistX_HwNm_u8p8[10]	0
t_AsstFWDefltAssistX_HwNm_u8p8[11]	0
t_AsstFWDefltAssistX_HwNm_u8p8[12]	0
t_AsstFWDefltAssistX_HwNm_u8p8[13]	0
t_AsstFWDefltAssistX_HwNm_u8p8[14]	0
t_AsstFWDefltAssistX_HwNm_u8p8[15]	0
t_AsstFWDefltAssistX_HwNm_u8p8[16]	0
t_AsstFWDefltAssistX_HwNm_u8p8[17] t_AsstFWDefltAssistX_HwNm_u8p8[18]	0
t_AsstFWDefitAssistX_HwNm_u8p8[19]	0
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	-205
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	-205 0
t_AsstFWPstepNstepThresh_Cnt_u16[0]	0
t_AsstFWPstepNstepThresh_Cnt_u16[1] t AsstFWVehSpd Kph u9p7[0]	0
t_AsstFWVenSpd_Kph_u9p7[1]	0
t_AsstFWVehSpd_Kph_u9p7[2]	0
t_AsstFWVehSpd_Kph_u9p7[3]	0
t_AsstFWVehSpd_Kph_u9p7[4]	0
t_AsstFWVehSpd_Kph_u9p7[5]	0
t_AsstFWVehSpd_Kph_u9p7[6]	0
t_AsstFWVehSpd_Kph_u9p7[7]	0
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-8.80000019
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-8.80000019
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-10
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-8.80000019
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	0
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

AssistFirewall\_Per1





Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-8.78894901	-8.78894901 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0	0 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	0.100097656	0.100097656 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-52.7336922	-52.7336922 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-8.76885509	-8.76885509 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-16	-16 ± 4.88E-04	✓
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	0.100097656	0.100097656 ± 9.77E-04	✓
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	✓
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 2.119 (Repeat Count = 1)	and the second of the second o
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8.80000019
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.715390444
AssistFirewall_ActiveRawAcc_Cnt_M_u16	65535
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	52.7999992
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.715390444
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	2.09537959
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8.80000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.715390444
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	15.9995003
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.715390444
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	8.80000019
k_AsstFWInpLimitHFA_MtrNm_f32	8.80000019
k_AsstFWInpLimitHysComp_MtrNm_f32	8.80000019
k_AsstFWNstep_Cnt_u16	5000
k_AsstFWPstep_Cnt_u16	5000
k_RestoreThresh_MtrNm_f32	8.80000019
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	20480





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	20480
t2 AsstFWUprBoundX HwNm s4p11[2][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	20480
t2 AsstFWUprBoundX HwNm s4p11[3][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2 AsstFWUprBoundX HwNm s4p11[6][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	20480
	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	32767 32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	32767 32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	32767 32767 32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4] t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	32767 32767 32767 32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1] t2_AsstFWUprBoundY_MtrNm_s4p11[0][2] t2_AsstFWUprBoundY_MtrNm_s4p11[0][3] t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	32767 32767 32767

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Namo	Input Value
Name t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	Input Value 32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6] t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	32767 32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7] t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	32767 32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6] t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	32767 32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9] t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	32767
t2_Asst WopfboundY_MtrNm_s4p11[5][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	32767





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	32767 32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	32767
t_AsstFWDefitAssistX_HwNm_u8p8[0]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[1]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[2]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[3]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[4]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[5]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[6]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[7]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[8]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[9]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[10]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[11]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[12]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[13]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[14]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[15]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[16]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[17]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[18]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[19]	2560
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	32767 32767
t_AsstFWDefltAssistY_MtrNm_s4p11[3] t_AsstFWDefltAssistY_MtrNm_s4p11[4]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	32767
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	32767
t_AsstFWPstepNstepThresh_Cnt_u16[0]	5000
t_AsstFWPstepNstepThresh_Cnt_u16[1]	5000
t_AsstFWVehSpd_Kph_u9p7[0]	65408
t_AsstFWVehSpd_Kph_u9p7[1]	65408
t_AsstFWVehSpd_Kph_u9p7[2]	65408 GE408
t_AsstFWVehSpd_Kph_u9p7[3]	65408 65408
t_AsstFWVehSpd_Kph_u9p7[4]	65408 65408
t_AsstFWVehSpd_Kph_u9p7[5] t AsstFWVehSpd Kph u9p7[6]	65408 65408
t_AsstFWVenSpd_Kph_u9p7[7]	65408
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	8.80000019
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	1
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	8.80000019
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	10
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.80000019
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	255
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

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Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8.80000019	8.80000019 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	65535	65535 ± 1	✓
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	26.4000015	26.3999996 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	33.9136925	33.9136925 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8.80000019	8.80000019 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	15.9995003	15.9995003 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	26.4000015	26.3999996 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~

Τ					
Actual Function	Count	Expected Function	Count	Result	
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~	
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•	
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~	

AssistFirewall\_Per1

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Test Case 3: Path test

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#### Specification

AssistFirewall\_Per1

Performance Metrics (With "None" Instrumentation and WithPS Environment)
CPU Cycles:

TC3.1 6628.00 Cycles
TC3.2 6628.00 Cycles
TC3.3 6629.00 Cycles
TC3.4 6629.00 Cycles
TC3.5 6629.00 Cycles
TC3.6 6629.00 Cycles
TC3.7 6629.00 Cycles
TC3.8 6629.00 Cycles
TC3.9 6629.00 Cycles
TC3.10 6629.00 Cycles
TC3.11 6629.00 Cycles
TC3.12 6629.00 Cycles
TC3.13 6629.00 Cycles
TC3.14 6629.00 Cycles
TC3.15 6629.00 Cycles
TC3.16 6629.00 Cycles
TC3.17 6629.00 Cycles
TC3.17 6629.00 Cycles



#### **Description** Vector Description

TS3.1"((HysteresisComp\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitHysComp\_MtrNm\_f32))=False && ((HysteresisComp\_MtrNm\_T\_f32)<=(-k\_AsstFWInpLimitHysComp\_MtrNm\_f32))=False && ((HighFreqAssist\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitHFA\_MtrNm\_f32))=True && ((BaseAssistCmd\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitBaseAsst\_MtrNm\_f32))=False && ((BaseAssistCmd\_MtrNm\_T\_f32)<=(-k\_AsstFWInpLimitBaseAsst\_MtrNm\_f32))=False && ((DefeatAsstTblSvc\_Cnt\_T\_lgc != D\_FALSE\_CNT\_LGC) && (MECCounter\_Cnt\_T\_enum != ProductionMode)) =False && ((LowFreqInput\_MtrNm\_T\_f32)>=( UprBoundFilt\_MtrNm\_T\_f32))=True && DefltAsst\_MtrNm\_T\_f32 = Productionino(et) =False && ((LowFreqInput\_mitNmT\_\_\_132)=( )prBoundarii\_mitNmT\_\_\_132)]=True && DelftAsstLookup\_MtrNm\_T\_f32 \* ((float32)Sign\_f32\_m(HwTorque\_HwNm\_T\_f32))=True && ((LowFreqInput\_MtrNm\_T\_f32) = DelftAsstLookup\_MtrNm\_T\_f32) | ((LowFreqInput\_MtrNm\_T\_f32) | ((LowFreqInput\_MtrNm\_T\_f32) | ((LowFreqInput\_MtrNm\_T\_f32) = DelftAsstLookup\_MtrNm\_T\_f32) | (LowFreqInput\_MtrNm\_T\_f32) | (LowFreqInput\_MtrNm\_T\_f32) | (LowFreqInput\_MtrNm\_T\_f32) | ((AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16) = ((AssistFWPstepNstep\_Cnt\_T\_str.Threshold) - ((AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16) = ((AssistF (TRUE == AssistFirewall\_PNCountStatus\_Cnt\_M\_lgc))=True && (AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32>8.8)=True && (AsstFWActive\_Uls\_T\_f32>1)=True"
TS3.2"((HysteresisComp\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitHysComp\_MtrNm\_f32))=True && ((BaseAssistCmd\_MtrNm\_T\_f32))=True && ((HighFreqAssist\_MtrNm\_T\_f32))=(E\_AsstFWInpLimitHFA\_MtrNm\_f32))=True && ((BaseAssistCmd\_MtrNm\_T\_f32))=True && ((LowFreqInput\_MtrNm\_T\_f32))=True && ((LowFreqInput\_MtrNm\_T\_f32))=True && ((LowFreqInput\_MtrNm\_T\_f32))=True && ((LowFreqInput\_MtrNm\_T\_f32))=True && ((LowFreqInput\_MtrNm\_T\_f32))=True && ((LowFreqInput\_MtrNm\_T\_f32))=True && ((AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16)<((AsstFWPstepNstep\_Cnt\_T\_str.Threshold)-(AsstFWPstepNstep\_Cnt\_T\_str.Pstep)))=False && (AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16)=((AsstFWPstepNstepThresh\_Cnt\_u16[1])
=True && (((Abs\_f32\_m(SumInput\_MtrNm\_T\_f32)-AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32) > k\_RestoreThresh\_MtrNm\_f32) && (AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32>8.8)=True && (AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32>1)=True && (AssistFirewall\_CombAsstSV\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitHysComp\_MtrNm\_f32))=True && ((HighFreqAssist\_MtrNm\_T\_f32))=(k\_AsstFWInpLimitHFA\_MtrNm\_f32))=True && ((BaseAssistCmd\_MtrNm\_T\_f32)=True && ((HighFreqAssist\_MtrNm\_T\_f32))=(k\_AsstFWInpLimitHFA\_MtrNm\_f32))=True && ((BaseAssistCmd\_MtrNm\_T\_f32)=True && ((HighFreqAssist\_MtrNm\_T\_f32))=(k\_AsstFWInpLimitHFA\_MtrNm\_f32))=True && ((BaseAssistCmd\_MtrNm\_T\_f32)=True && ((HighFreqAssist\_MtrNm\_T\_f32))=(k\_AsstFWInpLimitHFA\_MtrNm\_f32))=True && ((BaseAssistCmd\_MtrNm\_T\_f32)=True && ((BaseAssistCmd\_MtrNm\_T\_f32 (TRUE == AssistFirewall\_PNCountStatus\_Cnt\_M\_lgc))=True && (AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32>8.8)=True && ((High-freqAssist\_MtrNm\_ | \_132)>= (K\_AsstF-WinpLimitH-A\_MtrNm\_132))= True && ((BaseAssistCmd\_MtrNm\_ | \_132)>= 1 rue && ((BaseAssistCmd\_MtrNm\_ | \_132)> 1 rue && ((BaseAssistCmd\_MtrNm\_ | \_132)= 1 rue && (BaseAssistCmd\_MtrNm\_ (RastFwicking Library Find of the SastFwing Library Li k\_AsstFWInpLimitHysComp\_MtrNm\_f32))=False && ((HighFreqAssist\_MtrNm\_T\_f32))=(k\_AsstFWInpLimitHFA\_MtrNm\_f32))=True && ((BaseAssistCmd\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitBaseAsst\_MtrNm\_f32))=False && ((BaseAssistCmd\_MtrNm\_T\_f32)>=(-k\_AsstFWInpLimitBaseAsst\_MtrNm\_f32))=False && ((DefeatAsstTblSvc\_Cnt\_T\_lgc != D\_FALSE\_CNT\_LGC) && (MECCounter\_Cnt\_T\_enum != K\_AsstFWInpLimitBaseAsst\_MtrNm\_f32))=False && ((DefeatAsstTblSvc\_Cnt\_T\_lgc != D\_FALSE\_CNT\_LGC) && (MECCounter\_Cnt\_T\_enum ProductionMode)) =False && ((LowFreqInput\_MtrNm\_T\_f32)>=( UprBoundFilt\_MtrNm\_T\_f32))=True && DefltAsst\_MtrNm\_T\_f32 = DefltAsstLookup\_MtrNm\_T\_f32 \* ((Idoat32)Sign\_f32\_m(HwTorque\_HwNm\_T\_f32))=True && ((LowFreqInput\_MtrNm\_T\_f32 > UprBoundFilt\_MtrNm\_T\_f32))=True && ((LowFreqInput\_MtrNm\_T\_f32) || (LowFreqInput\_MtrNm\_T\_f32) > UprBoundFilt\_MtrNm\_T\_f32) >=True && ((AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16)<((AsstFWPstepNstepThestp\_Cnt\_T\_str.Threshold)-(AsstFWPstepNstep\_Cnt\_T\_str.Pstep)))=False && ((AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16)<((AsstFWPstepNstepThresh\_Cnt\_u16[1])=True && (((Abs\_f32\_m(SumInput\_MtrNm\_T\_f32 - AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32) > k\_RestoreThresh\_MtrNm\_f32) && (AssistFirewall\_AsstReducedPerfSV\_Cnt\_M\_lgc == TRUE)) || (TRUE == AssistFirewall\_PNCountStatus\_Cnt\_M\_lgc))=True && (AssitFirewall\_CombAsstSV\_MtrNm\_M\_f32)=8.8)=True && (AssitFWActive\_Uls\_T\_f32>)=1 True" && ((HysteresisComp\_MtrNm\_T\_f32))=False && ((HysteresisComp\_MtrNm\_T\_f32))=False && ((HighFreqAssist\_MtrNm\_T\_f32))=False && ((HighFreqAssist\_MtrNm\_T\_f32))=False && ((HighFreqAssist\_MtrNm\_T\_f32))=False && ((HestarastTblSvc\_Cnt\_T\_lgc!=D\_FALSE\_CNT\_LGC) && (MECCounter\_Cnt\_T\_enum!= ProductionMode)) =False && &&((BaseAssistCmd\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitBaseAsst\_MtrNm\_f32))=True && ((DefeatAsstTblSvc\_Cnt\_T\_lgc != D\_FALSE\_CNT\_LGC) && (MECCounter\_Cnt\_T\_enum != ProductionMode)) =False && ((HysteresisComp\_MtrNm\_T\_f32)>=(-k\_AsstFWInpLimitHysComp\_MtrNm\_f32))=False && ((HysteresisComp\_MtrNm\_T\_f32))=False && ((HighFreqAssist\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitHysComp\_MtrNm\_T\_f32))=False && ((HighFreqAssist\_MtrNm\_f32))=False && ((BaseAssistCmd\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitBaseAsst\_MtrNm\_f32))=False && ((BaseAssistCmd\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitBaseAsst\_MtrNm\_f32))=False && ((DefeatAsstTblSvc\_Cnt\_T\_lgc != D\_FALSE\_CNT\_LGC) && (MECCounter\_Cnt\_T\_enum != ProductionMode)) =False && ((LowFreqInput\_MtrNm\_T\_f32)>=( UprBoundFilt\_MtrNm\_T\_f32))=True && DefitAsst\_Okup\_MtrNm\_T\_f32 \* ((float32)Sign\_f32\_m(HwTorque\_HwNm\_T\_f32))=True && ((LowFreqInput\_MtrNm\_T\_f32) < DetitAsstLookup\_mtrNm\_1\_i32 \* (inoat32)sign\_f32\_m(HwTorque\_HwNm\_1\_f32)=1rue && ( (LowFreqinput\_mtrNm\_1\_f32 > LwrBoundFilt\_MtrNm\_T\_f32 > I) | (LowFreqinput\_MtrNm\_T\_f32 > UprBoundFilt\_MtrNm\_T\_f32 ) =True && ((AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16)<-((AsstFWPstepNstep\_Cnt\_T\_str.Threshold)-(AsstFWPstepNstep\_Cnt\_T\_str.Pstep)))=True && ((AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16) >= t\_AsstFWPstepNstepThresh\_Cnt\_u16[1] )=True && ((AssistFirewall\_ActiveRawAcc\_Cnt\_M\_u16) >= t\_AsstFWPstepNstepThresh\_Cnt\_u16[1] )=True && ((AssistFirewall\_AsstReducedPerfSV\_Cnt\_M\_lgc == TRUE)) || (TRUE == AssistFirewall\_PNCountStatus\_Cnt\_M\_lgc))=True && (AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32>8.8)=False && (AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32>8 (Asstructive\_Uls\_T\_f32<=0)=False"
TS3.6"((HysteresisComp\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitHysComp\_MtrNm\_f32))=True && ((HighFreqAssist\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitHFA\_MtrNm\_f32))=False && ((HighFreqAssist\_MtrNm\_T\_f32)>=(-k\_AsstFWInpLimitHFA\_MtrNm\_T\_f32))=False && ((BaseAssistCmd\_MtrNm\_T\_f32))=False && ((BaseAssistCmd\_MtrNm\_T\_f32))=False && ((DefeatAsstTblSvc\_Cnt\_T\_lgc!= D\_FALSE\_CNT\_LGC) && (MECCounter\_Cnt\_T\_enum != ProductionMode)) =False && ((LowFreqInput\_MtrNm\_T\_f32)>=( UprBoundFilt\_MtrNm\_T\_f32))=False && ((LowFreqInput\_MtrNm\_T\_f32))=true && DefltAsst\_MtrNm\_T\_f32 = DefltAsstLookup\_MtrNm\_T\_f32 \* AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32) > k\_Restore Thresh\_MtrNm\_f32) && (AssistFirewall\_AsstReducedPerfSV\_Cnt\_M\_lgc == TRUE)) || (TRUE == AssistFirewall\_PNCountStatus\_Cnt\_M\_lgc))=True && (AssistFirewall\_CombAsstSV\_MtrNm\_M\_f32>8.8)=True && (AsstFWActive\_Uls\_T\_f32>1)=True" TS3.7"(HysteresisComp\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitHysComp\_MtrNm\_f32))=False && ((HysteresisComp\_MtrNm\_T\_f32)<=(-k\_AsstFWInpLimitHysComp\_MtrNm\_f32))=False ((HighFreqAssist\_MtrNm\_T\_f32)>=(k\_AsstFWInpLimitHFA\_MtrNm\_f32))=False && ((HighFreqAssist\_MtrNm\_T\_f32)<=(-k\_AsstFWInpLimitHFA\_MtrNm\_f32))=False ((High-freqAssist\_MtrNm\_I\_\_132)<=(-k\_Asstr-WinpLimitHFA\_MtrNm\_I32))=False 
&&((BaseAssistCmd\_MtrNm\_T\_f32)>=(k\_Asstr-WinpLimitHFA\_MtrNm\_I32))=True 
&& ((DefeatAsstTblSvc\_Cnt\_T\_lgc != D\_FALSE\_CNT\_LGC) 
&& (MECCounter\_Cnt\_T\_enum != ProductionMode)) 
=False 
&& ((LowFreqInput\_MtrNm\_T\_f32)>=( UprBoundFilt\_MtrNm\_T\_f32))=False 
&& ((LowFreqInput\_MtrNm\_T\_f32))=true 
&& DefltAsst\_MtrNm\_T\_f32 
= DefltAsstLookup\_MtrNm\_T\_f32 
\* ((float32)Sign\_f32\_m(HwTorque\_HwNm\_T\_f32))=False 
&& ((LowFreqInput\_MtrNm\_T\_f32 < LwrBoundFilt\_MtrNm\_T\_f32) || (LowFreqInput\_MtrNm\_T\_f32 > UprBoundFilt\_MtrNm\_T\_f32) )=True





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&&((AssistFirewall_ActiveRawAcc_Cnt_M_u16)<((AsstFWPstepNstep_Cnt_T_str.Threshold)-(AsstFWPstepNstep_Cnt_T_str.Pstep)))=False &&
        (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[1])=False && (AssistFirewall_CombAsstSV_MtrNm_M_f32<=-8.8)=True&& (((Abs_f32_m(SumInput_MtrNm_T_f32 - AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) ||
      (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=True && (AsstFWActive_Uls_T_f32>1)=True"
   (AsstFWActive_UIS_1_32>1)=1rue*
TS3.8""((HysteresisComp_MtrNm_T_f32))=(k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HysteresisComp_MtrNm_T_f32)<=(-k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=False && ((HighFreqAssist_MtrNm_T_f32)<=(-k_AsstFWInpLimitHFA_MtrNm_f32))=False && ((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=False && ((DefeatAsstTblSvc_Cnt_T_lgc !=
   D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum!= ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32)>=( UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32)=DefItAsstLookup_MtrNm_T_f32 * ((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32) * ((float32)Sign_f32_m(HwTorque_HwNm_T_f32)) * ((float32)Sign_f32_m(HwTorque_HwNm_T_f32)) * ((float32)Sign_f32_m(
     LwrBoundFilt_MtrNm_T_f32) ||
(LowFreqInput_MtrNm_T_f32 > UprBoundFilt_MtrNm_T_f32) )=FALSE
&&((AssistFirewall_ActiveRawAcc_Cnt_M_u16)>((AsstFWPstepNstep_Cnt_T_str.Nstep)=True && (AssistFirewall_ActiveRawAcc_Cnt_M_u16)
     &&((AssistFirewall_ActiveRawAcc_cnt_m_u1o)>((AsstFwPstepNstep_cnt_1_str.Nstep)=1fue && (AssistFirewall_ActiveRawAcc_cnt_m_u16)> = t_AsstFWPstepNstepThresh_Cnt_u16[0])=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32<=-8.8)=True&& (((Abs_f32_m(SumInput_MtrNm_T_f32 - AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32<=-8.8)=False && (AssistFirewall_CT_f32>1)=True*"
 "TS3.9"((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=True && ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=True && ((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((BaseAssistCmd_MtrNm_T_f32)<=(-k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((DefeatAsstTblSvc_Cnt_T_lgc!= D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32)>=( UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32)>=( UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32) = UprBoundFilt_MtrNm_T_f32) = UprBoundFilt_MtrNm_T_f32 = UprBoundFilt_MtrNm_T_f32) = UprBoundFilt_MtrNm_T_f32 = UprBoundFilt_MtrNm_T_f32) = True && ((AssistFirewall_ActiveRawAcc_Cnt_M_u16) > (AssistFirewall_ActiveRawAcc_Cnt_M_u16) > (AssistFirewall_ActiveRawAc
     &&(((Assistr-irewall_ActiveRawAcc_Cnt_M_u16)<((Assit-WPstepnstep_Cnt_1_str.Pstep)))=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16)>= t_AsstFWPstepnStep_Cnt_u16[1])=True && (AssistFirewall_CombAsstSV_MtrNm_u16])=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32<=-8.8)=True&& (((Abs_f32_m(SumInput_MtrNm_T_f32 - AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=True && (AssistFirewall_Comp_MtrNm_T_f32)=False && ((HysteresisComp_MtrNm_T_f32)>=(-
     k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))= False && ((HighFreqAssist_MtrNm_T_f32)<=(-k_AsstFWInpLimitHFA_MtrNm_f32))=False && ((HighFreqAssist_MtrNm_T_f32)<=(-k_AsstFWInpLimitHFA_MtrNm_f32))=False && ((DefeatAsstTblSvc_Cnt_T_lgc !=
     D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32)>=( UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=True && DefitAsst_MtrNm_T_f32 = DefitAsstLookup_MtrNm_T_f32 *
 UprBoundFilt_MtrNm_T_f32)=True && DeftHasst_MtrNm_T_f32 = DeftHasstLookup_MtrNm_T_f32 * ((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32 < LwrBoundFilt_MtrNm_T_f32) || ((LowFreqInput_MtrNm_T_f32 > UprBoundFilt_MtrNm_T_f32))=True && (((AssistFirewall_ActiveRawAcc_Cnt_M_u16)<(((AsstFWPstepNstep_Cnt_T_str.Threshold)-(AsstFWPstepNstep_Cnt_T_str.Pstep)))=True && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 > t_AsstFWPstepNstepThresh_Cnt_u16[1])=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 > t_AsstFWPstepNstepThresh_Cnt_u16[0])=True && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 > t_AsstFWPstepNstepThresh_Cnt_u16[0])=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32<) > k_RestoreThresh_MtrNm_T_f32 & AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_132) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32<-8.8)=False && (Assi
        (AsstFWActive_Uls_T_f32>1)=True
 (AsstFWActive_Uls_T_f32>1)=True"

TS3.11"((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=True &&
((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=True &&
((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHsaseAsst_MtrNm_f32))=False && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False &&
((LowFreqInput_MtrNm_T_f32)>=( UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32)</br>
((Host32)Sign_f32_m(HwTorque_HwNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32) & ((HwTorque_HwNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32) & ((HwTorque_HwNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32) & ((HwTorque_HwNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32) & ((LowFreqInput
     ZasstrWestepNstepThresh_Cnt_u16[0] =False && (Assistrilewall_ActiveRawAcc_Cnt_M_u16 > t_AsstrWPstepNstepThresh_Cnt_u16[0] =False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 > t_AsstFWPstepNstepThresh_Cnt_u16[0] =True && (AssistFirewall_CombAsstSV_MtrNm_M_f32<-8.8)=True&& (((Abs_f32_m(SumInput_MtrNm_T_f32 - AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>-8.8)=False && (AssistFirewall_CombAsstSV_MtrNm_M_f32<-8.8)=False && (AssistFirewall_CombAsstSV_MtrNm_M_f32<-8.8)=False && (AssistFirewall_CombAsstSV_MtrNm_M_f32-8.8)=False && (AssistFirewal
     (AsstrwActive_Dis_1=js2*)=False && (AsstrwActive_Dis_1=js2<=)=False
TS3.12"((HysteresisComp_MtrNm_T_f32))=[k_AsstFWInpLimitHysComp_MtrNm_T_f32)]=False && ((HysteresisComp_MtrNm_T_f32)=(-k_AsstFWInpLimitHysComp_MtrNm_T_f32))=False && ((HighFreqAssist_MtrNm_T_f32))=True
&&((HighFreqAssist_MtrNm_T_f32)<=(-k_AsstFWInpLimitHFA_MtrNm_f32))=False && ((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((BaseAssistCmd_MtrNm_T_f32)<=(-k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((LowFreqInput_MtrNm_T_f32)>=(-typBoundFilt_MtrNm_T_f32)=False && ((LowFreqInput_MtrNm_T_f32)>=(-typBoundFilt_MtrNm_T_f32)*
     UprBoundFilt_MtrNm_T_f32))=True && DefitAsst_MtrNm_T_f32 = DefitAsstLookup_MtrNm_T_f32 * ((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32 < LwrBoundFilt_MtrNm_T_f32) || (LowFreqInput_MtrNm_T_f32 > UprBoundFilt_MtrNm_T_f32) )=False
(LowFreqInput_MtrNm_T_32 > UprBoundFilt_MtrNm_T_32))=False && ((AssistFirewall_ActiveRawAcc_Cnt_M_u16)<((AsstFWPstepNstep_Cnt_T_str.Threshold)-(AsstFWPstepNstep_Cnt_T_str.Pstep)))=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstep_Cnt_T_str.Threshold)-(AsstFWPstepNstep_Cnt_T_str.Pstep)))=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[1])=True && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[0])=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32<=-8.8)=True&& (((Ass_{32}_m(SumInput_MtrNm_T_f32 - AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32<=-8.8)=False && ((HighFreqAssist_MtrNm_T_f32))=False && ((HighFreqAssist_MtrNm_T_f32))=False && ((HighFreqAssist_MtrNm_T_f32))=False && ((Interface))=False && ((DefeatAsstTblSvc_Cnt_T_lgc!=D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum!= ProductionMode))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32)=-(-UprBoundFilt_MtrNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32) <=(-UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32))=False && ((L
```



Test Step 3.1 (Repeat Count = 1)	✓
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.090000036
AssistFirewall_ActiveRawAcc_Cnt_M_u16	109
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.89999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0700000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0099999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4
k_AsstFWInpLimitHFA_MtrNm_f32	2.5
k_AsstFWInpLimitHysComp_MtrNm_f32	3.78999996
k_AsstFWNstep_Cnt_u16	3928
k_AsstFWPstep_Cnt_u16	1107
k_RestoreThresh_MtrNm_f32	1.89999998
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096

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Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
	-2046
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096 0
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192 -6144
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432
:2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
:2_AsstFWUprBoundX_HwNm_s4p11[7][1] :2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-16364
2_73311 W OPI DOUIIUA_ITWINIII_54P I 1[7][2]	
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-26624
	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-10240
	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384
	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240
	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-28672
	-26624
t2 Asst-WuprBoundy MtrNm s4b11151121	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3] t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-24576 -22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3] t2_AsstFWUprBoundY_MtrNm_s4p11[5][4] t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-24576 -22528 -20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3] t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-24576 -22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3] t2_AsstFWUprBoundY_MtrNm_s4p11[5][4] t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-24576 -22528 -20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3] t2_AsstFWUprBoundY_MtrNm_s4p11[5][4] t2_AsstFWUprBoundY_MtrNm_s4p11[5][5] t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-24576 -22528 -20480 -18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3] t2_AsstFWUprBoundY_MtrNm_s4p11[5][4] t2_AsstFWUprBoundY_MtrNm_s4p11[5][5] t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7] t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-24576 -22528 -20480 -18432 -16384 -14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3] t2_AsstFWUprBoundY_MtrNm_s4p11[5][4] t2_AsstFWUprBoundY_MtrNm_s4p11[5][5] t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-24576 -22528 -20480 -18432 -16384





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	
t_AsstFWDefltAssistX_HwNm_u8p8[0]	26
t_AsstFWDefltAssistX_HwNm_u8p8[1]	51
t_AsstFWDefltAssistX_HwNm_u8p8[2]	77
t_AsstFWDefltAssistX_HwNm_u8p8[3]	102
t_AsstFWDefltAssistX_HwNm_u8p8[4]	128
t_AsstFWDefltAssistX_HwNm_u8p8[5]	154
t_AsstFWDefltAssistX_HwNm_u8p8[6]	179
t_AsstFWDefltAssistX_HwNm_u8p8[7]	205
t_AsstFWDefltAssistX_HwNm_u8p8[8]	230
t_AsstFWDefltAssistX_HwNm_u8p8[9]	256
t_AsstFWDefltAssistX_HwNm_u8p8[10]	282
t_AsstFWDefltAssistX_HwNm_u8p8[11]	307
t_AsstFWDefltAssistX_HwNm_u8p8[12]	333
	358
t_AsstFWDefltAssistX_HwNm_u8p8[13]	
t_AsstFWDefltAssistX_HwNm_u8p8[14]	384
t_AsstFWDefltAssistX_HwNm_u8p8[15]	410
t_AsstFWDefltAssistX_HwNm_u8p8[16]	435
t_AsstFWDefltAssistX_HwNm_u8p8[17]	461
t_AsstFWDefltAssistX_HwNm_u8p8[18]	486
t_AsstFWDefltAssistX_HwNm_u8p8[19]	512
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-204
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	0
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144
t AsstFWDefltAssistY MtrNm s4p11[7]	8192
, .,	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720
t_AsstFWPstepNstepThresh_Cnt_u16[0]	0
t_AsstFWPstepNstepThresh_Cnt_u16[1]	0
t_AsstFWVehSpd_Kph_u9p7[0]	1408
t_AsstFWVehSpd_Kph_u9p7[1]	1536
t_AsstFWVehSpd_Kph_u9p7[2]	1664
	1792
t_AsstFWVehSpd_Kph_u9p7[3]	
t_AsstFWVehSpd_Kph_u9p7[3] t_AsstFWVehSpd_Kph_u9p7[4]	1920
t_AsstFWVehSpd_Kph_u9p7[3] t_AsstFWVehSpd_Kph_u9p7[4] t_AsstFWVehSpd_Kph_u9p7[5]	1920 2048
t_AsstFWVehSpd_Kph_u9p7[3] t_AsstFWVehSpd_Kph_u9p7[4]	1920 2048 2176
t_AsstFWVehSpd_Kph_u9p7[3] t_AsstFWVehSpd_Kph_u9p7[4] t_AsstFWVehSpd_Kph_u9p7[5]	1920 2048





Name	Input Value		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	9		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	Jls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_Mt	rNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_Mt	rNm_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.AssistFirewall.Ass$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Ser	vice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mtr	Nm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_	32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.82099986	2.8210001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0	0 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.9920001	1.99199998 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.2329998	5.2329998 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.11900008	1.11899996 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	-

T (0) 00/D (0)	
Test Step 3.2 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0399999991
AssistFirewall_ActiveRawAcc_Cnt_M_u16	6500
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.14999998
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0299999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.39999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0199999996
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00499999989
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3
k_AsstFWInpLimitHFA_MtrNm_f32	1.5
k_AsstFWInpLimitHysComp_MtrNm_f32	1.10000002
k_AsstFWNstep_Cnt_u16	4548
k_AsstFWPstep_Cnt_u16	492
k_RestoreThresh_MtrNm_f32	1.3999998
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2 AsstFWUprBoundX HwNm s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
tz_AsstFWUprBoundX_HwNm_s4p11[7][1] t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240 -8192
	-0192

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Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
2 AsstFWUprBoundY MtrNm s4p11[1][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][4] 2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
z_AsstFWUprBoundY_MtrNm_s4p11[1][5] 2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	22528
2 AsstFWUprBoundY MtrNm s4p11[3][8]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	26624
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	28672
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-10240
= -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1 -1	
2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-8192





Namo	Input Value
Name	Input Value -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10] t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7] t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9] t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	102
t_AsstFWDefitAssistX_HwNm_u8p8[1]	128
t_AsstFWDefitAssistX_HwNm_u8p8[2]	154
t_AsstFWDefltAssistX_HwNm_u8p8[3]	179
t_AsstFWDefltAssistX_HwNm_u8p8[4]	205
t_AsstFWDefltAssistX_HwNm_u8p8[5]	230
t_AsstFWDefltAssistX_HwNm_u8p8[6]	256
t_AsstFWDefltAssistX_HwNm_u8p8[7]	282
t_AsstFWDefltAssistX_HwNm_u8p8[8]	307
t_AsstFWDefltAssistX_HwNm_u8p8[9]	333
· · · · · · · · · · · · · · · · · · ·	358
t_AsstFWDefltAssistX_HwNm_u8p8[10] t_AsstFWDefltAssistX_HwNm_u8p8[11]	384
t_AsstFWDefltAssistX_HwNm_u8p8[12]	410
t_AsstFWDefltAssistX_HwNm_u8p8[13]	435
t_AsstFWDefltAssistX_HwNm_u8p8[14]	461
t_AsstFWDefltAssistX_HwNm_u8p8[15]	486
t_AsstFWDefltAssistX_HwNm_u8p8[16]	512
t_AsstFWDefltAssistX_HwNm_u8p8[17]	538
t_AsstFWDefltAssistX_HwNm_u8p8[18]	563
t_AsstFWDefltAssistX_HwNm_u8p8[19]	589
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	6144
t AsstFWDefitAssistY MtrNm s4p11[6]	6144
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefitAssistY_MtrNm_s4p11[11]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12288
t_AsstFWDefitAssistY_MtrNm_s4p11[13]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	16384
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	20480
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	20480
t_AsstFWPstepNstepThresh_Cnt_u16[0]	125
t_AsstFWPstepNstepThresh_Cnt_u16[1]	219
t_AsstFWVehSpd_Kph_u9p7[0]	10240
t_AsstFWVehSpd_Kph_u9p7[1]	10368
t_AsstFWVehSpd_Kph_u9p7[2]	10496
t_AsstFWVehSpd_Kph_u9p7[3]	10624
t_AsstFWVehSpd_Kph_u9p7[4]	10752
L_ASSII W VEIISPU_RPII_U3P/141	
	10880
t_AsstFWVehSpd_Kph_u9p7[5] t_AsstFWVehSpd_Kph_u9p7[6]	10880 11008





Name	Input Value		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4.0999999		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	40		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	_Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_N	ltrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_N	/trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	le tgt_AssistFirewall_Per1_Defeat_AsstTbl_Se	ervice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mi	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm	_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_N	/ltrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph	n_f32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.76000023	5.76000023 ± 4.88E-04	<b>✓</b>
AssistFirewall_ActiveRawAcc_Cnt_M_u16	219	219 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	-
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.01800013	5.01800013 ± 4.88E-04	-
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8.03999996	8.03999996 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.97000003	3.97000003 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>→</b>
NTC_Cnt_T_enum	0xC9	0xC9	-
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	•

Τ				V
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	•

Name	Input Value
	· ·
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1000
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.16999996
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.60000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0399999991
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00700000022
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1
k_AsstFWInpLimitHFA_MtrNm_f32	1.89999998
k_AsstFWInpLimitHysComp_MtrNm_f32	2.5
k_AsstFWNstep_Cnt_u16	4300
k_AsstFWPstep_Cnt_u16	738
k_RestoreThresh_MtrNm_f32	1.60000002
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2 AsstFWUprBoundX HwNm s4p11[0][5]	2048





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144
	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2046 0
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
:2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144

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Input Value
-4096
-2048
0
2048
4096
6144
8192 10240
12288
-20480
-18432
-16384
-14336
-12288
-10240
-8192
-6144
-4096
-2048
0
-28672
-26624
-24576
-22528
-20480
-18432
-16384
-14336
-12288
-10240
-8192
-30720
-28672
-26624
-24576 -22528
-22526 -20480
-18432
-16384
-14336
-12288
-10240
-14336
-12288
-10240
-8192
-6144
-4096
-2048
0
2048
4096
6144
-6144
-4096
-2048
0
2048
4096
6144
8192
10240
12288
14336 -20480
-18432
-10 <del>4</del> 02
16394
-16384 -1/336
-14336
-14336 -12288
-14336 -12288 -10240
-14336 -12288





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t AsstFWDefltAssistX HwNm u8p8[0]	154
t_AsstFWDefitAssistX_HwNm_u8p8[1]	179
	205
t_AsstFWDefltAssistX_HwNm_u8p8[2]	230
t_AsstFWDefltAssistX_HwNm_u8p8[3]	
t_AsstFWDefltAssistX_HwNm_u8p8[4]	256
t_AsstFWDefltAssistX_HwNm_u8p8[5]	282
t_AsstFWDefltAssistX_HwNm_u8p8[6]	307
t_AsstFWDefltAssistX_HwNm_u8p8[7]	333
t_AsstFWDefltAssistX_HwNm_u8p8[8]	358
t_AsstFWDefltAssistX_HwNm_u8p8[9]	384
t_AsstFWDefltAssistX_HwNm_u8p8[10]	410
t_AsstFWDefltAssistX_HwNm_u8p8[11]	435
t_AsstFWDefltAssistX_HwNm_u8p8[12]	461
t_AsstFWDefltAssistX_HwNm_u8p8[13]	486
t_AsstFWDefltAssistX_HwNm_u8p8[14]	512
t_AsstFWDefltAssistX_HwNm_u8p8[15]	538
t_AsstFWDefltAssistX_HwNm_u8p8[16]	563
t_AsstFWDefltAssistX_HwNm_u8p8[17]	589
t_AsstFWDefltAssistX_HwNm_u8p8[18]	614
t_AsstFWDefltAssistX_HwNm_u8p8[19]	640
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	10240
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	10240
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	10240
t_AsstFWDefitAssistY_MtrNm_s4p11[6]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720
t_AsstFWPstepNstepThresh_Cnt_u16[0]	127
t_AsstFWPstepNstepThresh_Cnt_u16[1]	227
t_AsstFWVehSpd_Kph_u9p7[0]	16128
t_AsstFWVehSpd_Kph_u9p7[1]	
	16256 16384
t_AsstFWVehSpd_Kph_u9p7[2]	16384
t_AsstFWVehSpd_Kph_u9p7[2] t_AsstFWVehSpd_Kph_u9p7[3]	16384 16512
t_AsstFWVehSpd_Kph_u9p7[2] t_AsstFWVehSpd_Kph_u9p7[3] t_AsstFWVehSpd_Kph_u9p7[4]	16384 16512 16640
t_AsstFWVehSpd_Kph_u9p7[2] t_AsstFWVehSpd_Kph_u9p7[3]	16384 16512



Name	Input Value		
t_AsstFWVehSpd_Kph_u9p7[7]	17024		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-8.80000019		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	6		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	60		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_Mt	rNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Se	rvice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mtr	Nm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_	f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph	_f32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7.51999998	7.51999998 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	227	227 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	~
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.73000002	6.73000002 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.51200008	2.51200008 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.95800018	5.95800018 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T .				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>✓</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 3.4 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.019999996
AssistFirewall_ActiveRawAcc_Cnt_M_u16	200
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.13
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0099999978
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.20000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00899999961
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00300000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.20000005
k_AsstFWInpLimitHFA_MtrNm_f32	1.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	3
k_AsstFWNstep_Cnt_u16	4796
k_AsstFWPstep_Cnt_u16	246
k_RestoreThresh_MtrNm_f32	1.20000005
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192

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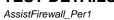


Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2 AsstFWUprBoundX HwNm s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_Asst WopiBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7] t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
	-2046 0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0.
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-16384
	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-22528
:2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-20480
12_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-14336





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	51
t_AsstFWDefltAssistX_HwNm_u8p8[1]	77
t_AsstFWDefltAssistX_HwNm_u8p8[2]	102
t_AsstFWDefltAssistX_HwNm_u8p8[3]	128
t_AsstFWDefltAssistX_HwNm_u8p8[4]	154
t_AsstFWDefltAssistX_HwNm_u8p8[5]	179
t_AsstFWDefltAssistX_HwNm_u8p8[6]	205
	230
t_AsstFWDefltAssistX_HwNm_u8p8[7]	
t_AsstFWDefltAssistX_HwNm_u8p8[8]	256
t_AsstFWDefltAssistX_HwNm_u8p8[9]	282
t_AsstFWDefltAssistX_HwNm_u8p8[10]	307
t_AsstFWDefltAssistX_HwNm_u8p8[11]	333
t_AsstFWDefltAssistX_HwNm_u8p8[12]	358
t_AsstFWDefltAssistX_HwNm_u8p8[13]	384
t_AsstFWDefltAssistX_HwNm_u8p8[14]	410
t_AsstFWDefltAssistX_HwNm_u8p8[15]	435
t_AsstFWDefltAssistX_HwNm_u8p8[16]	461
t_AsstFWDefltAssistX_HwNm_u8p8[17]	486
t_AsstFWDefltAssistX_HwNm_u8p8[18]	512
t_AsstFWDefltAssistX_HwNm_u8p8[19]	538
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	0
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8192
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	12288
· · ·	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720
t_AsstFWPstepNstepThresh_Cnt_u16[0]	123
t_AsstFWPstepNstepThresh_Cnt_u16[1]	211
	I are a
t_AsstFWVehSpd_Kph_u9p7[0]	4352
t_AsstFWVehSpd_Kph_u9p7[0] t_AsstFWVehSpd_Kph_u9p7[1]	4352 4480
t_AsstFWVehSpd_Kph_u9p7[1]	4480
t_AsstFWVehSpd_Kph_u9p7[1] t_AsstFWVehSpd_Kph_u9p7[2]	4480 4608



Name	Input Value		
t_AsstFWVehSpd_Kph_u9p7[6]	5120		
t_AsstFWVehSpd_Kph_u9p7[7]	5248		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	8.80000019		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2.20000005		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	2		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	20		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_M	trNm_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32$	tgt_AssistFirewall_Per1_CombinedAssist_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_I	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Se	rvice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_	<u>f</u> 32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph	_f32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.92000008	3.92000008 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	211	211 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.02399993	3.02399993 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.01800013	6.01800013 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.98199999	1.98199999 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	<b>~</b>
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	<b>~</b>
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>~</b>
Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	Rte Call AssistFirewall Per1 CP1 CheckpointReached	1	<b>✓</b>

Test Step 3.5 (Repeat Count = 1)	· ·
Name	Input Value
AssistFirewall ActiveKSV M str.SV Uls f32	-5.3000019
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.40000006
AssistFirewall ActiveRawAcc Cnt M u16	8487
AssistFirewall AsstReducedPerfSV Cnt M lgc	1
AssistFirewall CombAsstSV MtrNm M f32	8.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.1999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.079999982
AssistFirewall HiFreqKSV M str.CF Uls f32	1.11199999
AssistFirewall LwrBoundKSV M str.SV Uls f32	-5.30000019
AssistFirewall LwrBoundKSV M str.K Uls f32	0.11999997
AssistFirewall PNCountStatus Cnt M lqc	1
AssistFirewall UprBoundKSV M str.SV Uls f32	5,099999
AssistFirewall UprBoundKSV M str.K Uls f32	0.21999999
Rte Inst Ap AssistFirewall	tqt Rte Inst Ap AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.80000019
k AsstFWInpLimitHFA MtrNm f32	6.40999985
k AsstFWInpLimitHysComp MtrNm f32	6.71000004
k AsstFWNstep Cnt u16	4052
k_AsstFWPstep_Cnt_u16	2460
k RestoreThresh MtrNm f32	4.42999983
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
	14336
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
:2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
	0
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336

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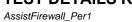


710010tt 110Wdfi_1 Cl 1	(10.10.10.10.10.10.10.10.10.10.10.10.10.1
Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5] t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
t2_Asst WopiBoundY_MtrNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
12_ASSIF VV Upribound t_ivitinin_s4p i ijojjuj	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1] t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1] t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1] t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048 0





Name	Input Value	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240	
:2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048	
	0	
2_AsstFWUprBoundY_MtrNm_s4p11[6][3]		
2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192	
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288	
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336	
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192	
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144	
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096	
2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048	
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0	
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048	
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096	
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144	
2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240	
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288	
t_AsstFWDefltAssistX_HwNm_u8p8[0]	333	
t_AsstFWDefltAssistX_HwNm_u8p8[1]	358	
:_AsstFWDefltAssistX_HwNm_u8p8[2]	384	
:_AsstFWDefltAssistX_HwNm_u8p8[3]	410	
:_AsstFWDefltAssistX_HwNm_u8p8[4]	435	
:_AsstFWDefltAssistX_HwNm_u8p8[5]	461	
:_AsstFWDefltAssistX_HwNm_u8p8[6]	486	
:_AsstFWDefltAssistX_HwNm_u8p8[7]	512	
t_AsstFWDefltAssistX_HwNm_u8p8[8]	538	
t_AsstFWDefltAssistX_HwNm_u8p8[9]	563	
t_AsstFWDefltAssistX_HwNm_u8p8[10]	589	
t_AsstFWDefitAssistX_HwNm_u8p8[11]	614	
:_AsstFWDefitAssistX_HwNm_u8p8[12]	640	
t_AsstFWDefltAssistX_HwNm_u8p8[13]	666	
t_AsstFWDefltAssistX_HwNm_u8p8[14]	691	
t_AsstFWDefltAssistX_HwNm_u8p8[15]	717	
t_AsstFWDefltAssistX_HwNm_u8p8[16]	742	
:_AsstFWDefltAssistX_HwNm_u8p8[17]	768	
:_AsstFWDefltAssistX_HwNm_u8p8[18]	794	
:_AsstFWDefltAssistX_HwNm_u8p8[19]	819	
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-204	
:_AsstFWDefltAssistY_MtrNm_s4p11[1]	0	
_AsstFWDefltAssistY_MtrNm_s4p11[2]	2048	
_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096	
_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096	
:_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144	
:_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144	
:_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192	
:_AsstFWDefltAssistY_MtrNm_s4p11[8]	8192	
:_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240	
_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288	
:_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336	
:_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384	
:_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432	
AsstFWDefltAssistY_MtrNm_s4p11[14]	20480	
:_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528	
_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576	
_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624	
_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672	
:_AsstFWDefitAssistY_MtrNm_s4p11[19]	30720	
:_AsstFWPstepNstepThresh_Cnt_u16[0]	134	
	255	
:_AsstFWPstepNstepThresh_Cnt_u16[1]		
:_AsstFWVehSpd_Kph_u9p7[0]	36736	
t_AsstFWVehSpd_Kph_u9p7[1]	36864	
t_AsstFWVehSpd_Kph_u9p7[2]	36992	
t_AsstFWVehSpd_Kph_u9p7[3]	37120	
t_AsstFWVehSpd_Kph_u9p7[4]	37248	





Name	Input Value		
t_AsstFWVehSpd_Kph_u9p7[5]	37376		
t_AsstFWVehSpd_Kph_u9p7[6]	37504		
t_AsstFWVehSpd_Kph_u9p7[7]	37632		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.19999981		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	1		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.5999999		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.4000001		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.5999999		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	_Uls_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32$	tgt_AssistFirewall_Per1_BaseAssistCmd_M	trNm_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32$	tgt_AssistFirewall_Per1_CombinedAssist_N	ltrNm_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cnt\_Service\_Cn$	_lt_tgt_AssistFirewall_Per1_Defeat_AsstTbl_Se	ervice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mt	rNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_	_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_N	ftrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt	_enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph	_f32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.30000019	-5.30000019 ± 4.88E-04	<b>~</b>
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487	8487 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-16	-16 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-6.06399965	-6.06399965 ± 4.88E-04	-
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019	-5.30000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	-
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999	5.0999999 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	<b>~</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-16	-16 ± 9.77E-04	<b>~</b>
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC6	0xC6	•
Param_Cnt_T_u08	0x01	0x01	-
Status_Cnt_T_enum	0x00	0x00	<b>✓</b>

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	•

Test Step 3.6 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	2.20000005
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0799999982
AssistFirewall_ActiveRawAcc_Cnt_M_u16	106
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.19000006
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0700000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00899999961
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3
k_AsstFWInpLimitHFA_MtrNm_f32	1.29999995
k_AsstFWInpLimitHysComp_MtrNm_f32	3.29999995
k_AsstFWNstep_Cnt_u16	4052
k_AsstFWPstep_Cnt_u16	984
k_RestoreThresh_MtrNm_f32	1.79999995
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096





Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
z_AsstFWUprBoundX_HwNm_s4p11[2][2] 2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][5] 2_AsstFWUprBoundX_HwNm_s4p11[2][6]	
	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048
z_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	
z_AsstFWUprBoundX_HwNm_s4p11[4][10]  2 AsstFWUprBoundX HwNm s4p11[5][0]	2048
	0
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	
	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240 12288
2_AsstFWUprBoundX_HwNm_s4p11[6][7] 2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0] t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-16384 -14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-14330
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240
t2_Asst Wopibound1_within_s4p11[0][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-18432 -16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5] t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-14330
t2_Asst Wopibound1_within_s4p11[2][7] t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-8192
t2 AsstFWUprBoundY MtrNm s4p11[2][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	<sup>-</sup> ∠U <del>4</del> 0





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	286/2
t_AsstFWDefltAssistX_HwNm_u8p8[0]	205
t_AsstFWDefltAssistX_HwNm_u8p8[1]	
t_AsstFWDefltAssistX_HwNm_u8p8[2]	256
t_AsstFWDefltAssistX_HwNm_u8p8[3]	282
t_AsstFWDefltAssistX_HwNm_u8p8[4]	307
t_AsstFWDefltAssistX_HwNm_u8p8[5]	333
t_AsstFWDefltAssistX_HwNm_u8p8[6]	358
t_AsstFWDefltAssistX_HwNm_u8p8[7]	384
t_AsstFWDefltAssistX_HwNm_u8p8[8]	410
t_AsstFWDefltAssistX_HwNm_u8p8[9]	435
t_AsstFWDefltAssistX_HwNm_u8p8[10]	461
t_AsstFWDefltAssistX_HwNm_u8p8[11]	486
t_AsstFWDefltAssistX_HwNm_u8p8[12]	512
t_AsstFWDefltAssistX_HwNm_u8p8[13]	538
t_AsstFWDefltAssistX_HwNm_u8p8[14]	563
t_AsstFWDefltAssistX_HwNm_u8p8[15]	589
t_AsstFWDefltAssistX_HwNm_u8p8[16]	614
t_AsstFWDefltAssistX_HwNm_u8p8[17]	640
t_AsstFWDefltAssistX_HwNm_u8p8[18]	666
t_AsstFWDefltAssistX_HwNm_u8p8[19]	691
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-204
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	0
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720
t_AsstFWPstepNstepThresh_Cnt_u16[0]	129
t_AsstFWPstepNstepThresh_Cnt_u16[1]	235
t_AsstFWVehSpd_Kph_u9p7[0]	22016
t_AsstFWVehSpd_Kph_u9p7[1]	22144
t_AsstFWVehSpd_Kph_u9p7[2]	22272
t_AsstFWVehSpd_Kph_u9p7[3]	22400
t_AsstFWVehSpd_Kph_u9p7[4]	22528
t_AsstFWVehSpd_Kph_u9p7[5]	22656



Name	Input Value		
t_AsstFWVehSpd_Kph_u9p7[6]	22784		
t_AsstFWVehSpd_Kph_u9p7[7]	22912		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	0		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	80		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	_Ulsf32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_M	ltrNm_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_Inst\_Ap\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_AssistFirewall\_Per1\_Defeat\_AsstTbl\_Service\_Cnt\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_Defeat\_AssistFirewall\_Per1\_De$	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Se	ervice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mt	rNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_	_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32		
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	2.02400017	2.02399993 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	235	235 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.46399999	1.46399999 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.33400011	4.33400011 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.9460001	7.9460001 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	<b>✓</b>

Test Step 3.7 (Repeat Count = 1)	
	Innut Value
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0060000005
AssistFirewall_ActiveRawAcc_Cnt_M_u16	115
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.29999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0599999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.090000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.029999993
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.4000001
k_AsstFWInpLimitHFA_MtrNm_f32	2.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	4.76999998
k_AsstFWNstep_Cnt_u16	3680
k_AsstFWPstep_Cnt_u16	1353
k_RestoreThresh_MtrNm_f32	2.0999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
, , , , , , , , , , , , , , , , , , , ,	
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	
	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	
t2_AsstFWUprBoundX_HwNm_s4p11[6][5] t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5] t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	
t2_AsstFWUprBoundX_HwNm_s4p11[6][5] t2_AsstFWUprBoundX_HwNm_s4p11[6][6] t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240
	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-4096
	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	
	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0] t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0] t2_AsstFWUprBoundY_MtrNm_s4p11[5][1] t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0] t2_AsstFWUprBoundY_MtrNm_s4p11[5][1] t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192 -6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10] t2_AsstFWUprBoundY_MtrNm_s4p11[5][0] t2_AsstFWUprBoundY_MtrNm_s4p11[5][1] t2_AsstFWUprBoundY_MtrNm_s4p11[5][2] t2_AsstFWUprBoundY_MtrNm_s4p11[5][3] t2_AsstFWUprBoundY_MtrNm_s4p11[5][4] t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-8192 -6144





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
:_AsstFWDefltAssistX_HwNm_u8p8[0]	282
:_AsstFWDefltAssistX_HwNm_u8p8[1]	307
:_AsstFWDefltAssistX_HwNm_u8p8[2]	333
:_AsstFWDefltAssistX_HwNm_u8p8[3]	358
_AsstFWDefltAssistX_HwNm_u8p8[4]	384
:_AsstFWDefltAssistX_HwNm_u8p8[5]	410
:_AsstFWDefltAssistX_HwNm_u8p8[6]	435
t_AsstFWDefltAssistX_HwNm_u8p8[7]	461
t_AsstFWDefltAssistX_HwNm_u8p8[8]	486
:_AsstFWDefltAssistX_HwNm_u8p8[9]	512
t_AsstFWDefltAssistX_HwNm_u8p8[10]	538
t_AsstFWDefltAssistX_HwNm_u8p8[11]	563
t_AsstFWDefltAssistX_HwNm_u8p8[12]	589
t_AsstFWDefltAssistX_HwNm_u8p8[13]	614
:_AsstFWDefltAssistX_HwNm_u8p8[14]	640
:_AsstFWDefltAssistX_HwNm_u8p8[15]	666
:_AsstFWDefltAssistX_HwNm_u8p8[16]	691
:_AsstFWDefltAssistX_HwNm_u8p8[17]	717
:_AsstFWDefltAssistX_HwNm_u8p8[18]	742
:_AsstFWDefltAssistX_HwNm_u8p8[19]	768
:_AsstFWDefltAssistY_MtrNm_s4p11[0]	4096
_AsstFWDefltAssistY_MtrNm_s4p11[1]	4096
_AsstFWDefltAssistY_MtrNm_s4p11[2]	4096
:_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144
_AsstFWDefltAssistY_MtrNm_s4p11[7]	12288
:_AsstFWDefltAssistY_MtrNm_s4p11[8]	12288
:_AsstFWDefltAssistY_MtrNm_s4p11[9]	12288
:_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
_AsstFWDefltAssistY_MtrNm_s4p11[11]	12288
:_AsstFWDefltAssistY_MtrNm_s4p11[12]	12288
_AsstFWDefltAssistY_MtrNm_s4p11[13]	16384
_AsstFWDefltAssistY_MtrNm_s4p11[14]	16384
_AsstFWDefltAssistY_MtrNm_s4p11[15]	16384
_AsstFWDefltAssistY_MtrNm_s4p11[16]	20480
:_AsstFWDefltAssistY_MtrNm_s4p11[17]	20480
:_AsstFWDefltAssistY_MtrNm_s4p11[18]	20480
:_AsstFWDefltAssistY_MtrNm_s4p11[19]	20480
:_AsstFWPstepNstepThresh_Cnt_u16[0]	132
:_AsstFWPstepNstepThresh_Cnt_u16[1]	247
t_AsstFWVehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1]	30976
t_AsstFWVehSpd_Kph_u9p7[2]	31104
t_AsstFWVehSpd_Kph_u9p7[3]	31232
t_AsstFWVehSpd_Kph_u9p7[4]	31360





Name	Input Value		
t_AsstFWVehSpd_Kph_u9p7[5]	31488		
t_AsstFWVehSpd_Kph_u9p7[6]	31616		
t_AsstFWVehSpd_Kph_u9p7[7]	31744		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-10		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3.0999999		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	22		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_t	Jls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_Mtr	Nm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_Mt	rNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lq	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Ser	vice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mtrl	Nm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f	32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_Mt	rNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_	enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_	<u>f</u> 32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.06939983	5.06939983 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	247	247 ± 1	~
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019	-8.80000019 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.25	4.25 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.459999979	0.460000008 ± 4.88E-04	•
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.85699987	2.85700011 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-8.80000019	-8.80000019 ± 9.77E-04	~
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status Cnt T enum	0x01	0x01	<b>✓</b>

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 3.8 (Repeat Count = 1)	· · · · · · · · · · · · · · · · · · ·
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4797
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.019999996
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.5
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.60000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00899999961
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.7999995
k_AsstFWInpLimitHFA_MtrNm_f32	3.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	3.29999995
k_AsstFWNstep_Cnt_u16	4551
k_AsstFWPstep_Cnt_u16	2337
k_RestoreThresh_MtrNm_f32	6.9000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_Asst WoprBoundX_1WNIII_s4p11[2][1] t2 AsstFWUprBoundX HwNm s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6192 -6144
	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2 AsstFWUprBoundX HwNm s4p11[5][2]	-10240
t2 AsstFWUprBoundX HwNm s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][0] 2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
2 AsstFWUprBoundY MtrNm s4p11[3][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-24576
ادر المحادث ا	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-20480
z_AsstFWUprBoundY_MtrNm_s4p11[4][2] 2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	16384
	18432





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4] t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	282
t_AsstFWDefltAssistX_HwNm_u8p8[1]	307
t_AsstFWDefltAssistX_HwNm_u8p8[2]	333
t_AsstFWDefltAssistX_HwNm_u8p8[3]	358
t_AsstFWDefltAssistX_HwNm_u8p8[4]	384
t_AsstFWDefltAssistX_HwNm_u8p8[5]	410
t_AsstFWDefltAssistX_HwNm_u8p8[6] t_AsstFWDefltAssistX_HwNm_u8p8[7]	435 461
t_AsstFWDefitAssistX_HwNm_u8p8[8]	486
t_AsstFWDefltAssistX_HwNm_u8p8[9]	512
t_AsstFWDefltAssistX_HwNm_u8p8[10]	538
t_AsstFWDefltAssistX_HwNm_u8p8[11]	563
t_AsstFWDefltAssistX_HwNm_u8p8[12]	589
t_AsstFWDefltAssistX_HwNm_u8p8[13]	614
t_AsstFWDefltAssistX_HwNm_u8p8[14]	640
t_AsstFWDefltAssistX_HwNm_u8p8[15]	666
t_AsstFWDefltAssistX_HwNm_u8p8[16]	691
t_AsstFWDefltAssistX_HwNm_u8p8[17]	717
t_AsstFWDefltAssistX_HwNm_u8p8[18]	742
t_AsstFWDefltAssistX_HwNm_u8p8[19]	768
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[11] t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384 18432
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	20480
t_AsstFWDefitAssistY_MtrNm_s4p11[14]	22528
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	30720
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720
t_AsstFWPstepNstepThresh_Cnt_u16[0]	170
t_AsstFWPstepNstepThresh_Cnt_u16[1]	399
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
	19456

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Name	Input Value		
t_AsstFWVehSpd_Kph_u9p7[4]	19584		
t_AsstFWVehSpd_Kph_u9p7[5]	19712		
t_AsstFWVehSpd_Kph_u9p7[6]	19840		
t_AsstFWVehSpd_Kph_u9p7[7]	19968		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.0999999		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-9		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	77		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	_Uls_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_BaseAssistCmd\_MtrNm\_f32$	tgt_AssistFirewall_Per1_BaseAssistCmd_N	ltrNm_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_CombinedAssist\_MtrNm\_f32$	tgt_AssistFirewall_Per1_CombinedAssist_N	/trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	lt tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm	_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall.AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cni	t_enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph	n_f32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.98000002	1.98000002 ± 4.88E-04	•
AssistFirewall_ActiveRawAcc_Cnt_M_u16	246	246 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0	<b>✓</b>
AssistFirewall_CombAsstSV_MtrNm_M_f32	4	4 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.15799999	1.15799999 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-6.19999981	-6.19999981 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	<b>✓</b>
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.90100002	7.90100002 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	<b>✓</b>
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4	4 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param Cnt T u08	0x01	0x01	<b>•</b>
	UXUT	UXUT	

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	•
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	•

Test Step 3.9 (Repeat Count = 1)		
Name	Input Value	
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7	
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0500000007	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	800	
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.15999997	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0399999991	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.5	
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.10000002	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0299999993	
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5	
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00600000005	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2	
k_AsstFWInpLimitHFA_MtrNm_f32	1.70000005	
k_AsstFWInpLimitHysComp_MtrNm_f32	2.0999999	
k_AsstFWNstep_Cnt_u16	4424	
k_AsstFWPstep_Cnt_u16	615	
k_RestoreThresh_MtrNm_f32	1.5	
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240	
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192	

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Name	Input Value	
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0	
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096	
	6144	
2_AsstFWUprBoundX_HwNm_s4p11[0][8]		
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0	
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432	
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480	
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096	
z_AsstFWUprBoundX_HwNm_s4p11[2][2] 2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0	
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288	
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0	
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096	
	6144	
2_AsstFWUprBoundX_HwNm_s4p11[3][9]		
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384	
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0	
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048	
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096	
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144	
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240	
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288	
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432	
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384	
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336	
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288	
	-10240	
2_AsstFWUprBoundX_HwNm_s4p11[6][4]		
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192	
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144	
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096	
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048	

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-6192
	-0144
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-30720
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-14330
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192 -6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-22528
:2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-20480
	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	
2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-14336





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2] t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	128
t_AsstFWDefltAssistX_HwNm_u8p8[1]	154
t_AsstFWDefltAssistX_HwNm_u8p8[2]	179
t_AsstFWDefltAssistX_HwNm_u8p8[3] t_AsstFWDefltAssistX_HwNm_u8p8[4]	205 230
t_AsstFWDefitAssistX_HwNm_u8p8[5]	256
t_AsstFWDefitAssistX_HwNm_u8p8[6]	282
t_AsstFWDefitAssistX_HwNm_u8p8[7]	307
t_AsstFWDefltAssistX_HwNm_u8p8[8]	333
t_AsstFWDefltAssistX_HwNm_u8p8[9]	358
t_AsstFWDefltAssistX_HwNm_u8p8[10]	384
t_AsstFWDefltAssistX_HwNm_u8p8[11]	410
t_AsstFWDefltAssistX_HwNm_u8p8[12]	435
t_AsstFWDefltAssistX_HwNm_u8p8[13]	461
t_AsstFWDefltAssistX_HwNm_u8p8[14]	486
t_AsstFWDefltAssistX_HwNm_u8p8[15]	512
t_AsstFWDefltAssistX_HwNm_u8p8[16]	538
t_AsstFWDefltAssistX_HwNm_u8p8[17]	563
t_AsstFWDefltAssistX_HwNm_u8p8[18]	589
t_AsstFWDefltAssistX_HwNm_u8p8[19]	614
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[5]  t_AsstFWDefltAssistY_MtrNm_s4p11[6]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	12288 12288
t_AsstFWDefltAssistY_MtrNm_s4p11[7] t_AsstFWDefltAssistY_MtrNm_s4p11[8]	14336
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	14336
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	14336
t_AsstFWDefitAssistY_MtrNm_s4p11[11]	18432
t_AsstFWDefitAssistY_MtrNm_s4p11[12]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	28672
t_AsstFWPstepNstepThresh_Cnt_u16[0]	126
t_AsstFWPstepNstepThresh_Cnt_u16[1]	223
t_AsstFWVehSpd_Kph_u9p7[0]	13184
t_AsstFWVehSpd_Kph_u9p7[1]	13312
t_AsstFWVehSpd_Kph_u9p7[2]	13440





Name	Input Value		
t_AsstFWVehSpd_Kph_u9p7[3]	13568		
t_AsstFWVehSpd_Kph_u9p7[4]	13696		
t_AsstFWVehSpd_Kph_u9p7[5]	13824		
t AsstFWVehSpd Kph u9p7[6]	13952		
t_AsstFWVehSpd_Kph_u9p7[7]	14080		
tgt AssistFirewall Per1 BaseAssistCmd MtrNm f32.value	-5		
tgt AssistFirewall Per1 Defeat AsstTbl Service Cnt Igc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	50		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_Mi	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_le	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Se	rvice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mti	rNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_	f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_M	ltrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_	_enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph	_f32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.6500001	6.6500001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	223	223 ± 1	•
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	•
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.83199978	5.83199978 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.39700007	1.39699996 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.96400023	4.96400023 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	•
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~

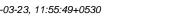
Т				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	<b>✓</b>
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	•

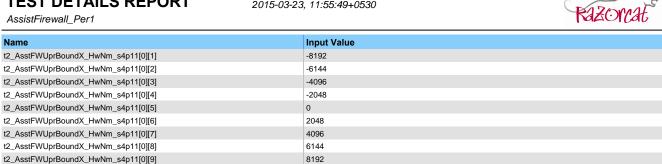
Test Step 3.10 (Repeat Count = 1)		~
Name	Input Value	
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.7999995	
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.100000001	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	344	
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	
AssistFirewall_CombAsstSV_MtrNm_M_f32	6.30000019	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.099999	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.7999995	
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5	
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.0999999	
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.129999995	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.19999981	
k_AsstFWInpLimitHFA_MtrNm_f32	1.70000005	
k_AsstFWInpLimitHysComp_MtrNm_f32	4.5	
k_AsstFWNstep_Cnt_u16	2564	
k_AsstFWPstep_Cnt_u16	2214	
k_RestoreThresh_MtrNm_f32	3.30999994	
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240	

t2\_AsstFWUprBoundX\_HwNm\_s4p11[0][10]

t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][1]

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10240

2048

t2\_AsstFWUprBoundX\_HwNm\_s4p11[1][0] -8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[1][1] -6144 -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[1][2] t2 AsstFWUprBoundX HwNm\_s4p11[1][3] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[1][4] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[1][5] t2\_AsstFWUprBoundX\_HwNm\_s4p11[1][6] 4096

t2\_AsstFWUprBoundX\_HwNm\_s4p11[1][7] 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[1][8] 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[1][9] 10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[1][10]

12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][0] 0 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][1] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][2] 4096

t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][3] 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][4] 8192 10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][5] t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][6] 12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][7] 14336

t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][8] 16384 18432 t2 AsstFWUprBoundX HwNm s4p11[2][9] t2\_AsstFWUprBoundX\_HwNm\_s4p11[2][10] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][0] -12288 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][1] -10240

t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][2] -8192 t2 AsstFWUprBoundX HwNm s4p11[3][3] -6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][4] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][5] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][6]

t2 AsstFWUprBoundX HwNm s4p11[3][7] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][8] 4096 t2 AsstFWUprBoundX HwNm s4p11[3][9] 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[3][10] 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][0] 0

t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][2] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][3] 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][4] 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][5] 10240 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][6] 12288

t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][7] 14336 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][8] 16384 t2 AsstFWUprBoundX HwNm s4p11[4][9] 18432 t2\_AsstFWUprBoundX\_HwNm\_s4p11[4][10] 20480 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][0] -10240

t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][1] -8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][2] -6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][3] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][4] -2048

t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][5] 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][6] t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][7] 4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][8] 6144

t2 AsstFWUprBoundX HwNm s4p11[5][9] 8192 t2\_AsstFWUprBoundX\_HwNm\_s4p11[5][10] 10240 -8192 t2 AsstFWUprBoundX HwNm s4p11[6][0] t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][1] -6144

t2 AsstFWUprBoundX HwNm s4p11[6][2] -4096 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][3] -2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][4] 0

 $t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][5]$ 2048 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][6] 6144 t2\_AsstFWUprBoundX\_HwNm\_s4p11[6][7]

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8] t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10] t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-12288
t2_Asst Wopiobulid1_ivitifil1_s4p11[2][1] t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3] t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-24576 -22528
tz_AsstFWUprBoundY_MtrNm_s4p11[4][4] t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-22528 -20480
	-20480 -18432
	-16432 -16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	
12_AsstFWUprBoundY_MtrNm_s4p11[4][6]  12_AsstFWUprBoundY_MtrNm_s4p11[4][7]  12_AsstFWUprBoundY_MtrNm_s4p11[4][8]  12_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7] t2_AsstFWUprBoundY_MtrNm_s4p11[4][8] t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-14336 -12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7] t2_AsstFWUprBoundY_MtrNm_s4p11[4][8] t2_AsstFWUprBoundY_MtrNm_s4p11[4][9] t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-14336 -12288 -10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7] t2_AsstFWUprBoundY_MtrNm_s4p11[4][8] t2_AsstFWUprBoundY_MtrNm_s4p11[4][9] t2_AsstFWUprBoundY_MtrNm_s4p11[4][10] t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-14336 -12288 -10240 2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7] t2_AsstFWUprBoundY_MtrNm_s4p11[4][8] t2_AsstFWUprBoundY_MtrNm_s4p11[4][9] t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-14336 -12288 -10240





10240 12288 14336
14336
16384
18432
20480
22528
8192
10240 12288
14336
16384
18432
20480
22528
24576
26624
28672
-10240
-8192
-6144
-4096
-2048
0
2048
4096
6144
8192
10240
230
256
282
307
333 358
388
410
435
461
486
512
538
563
589
614
640
666
691
717
-204
0
2048
4096
4096
6144
6144
8192
8192
10240
12288
14336
16384
18432
20480 22528
24576
26624 28672
30720
5000
10000
5000
5000 30848

AssistFirewall\_Per1







Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][9] 2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240 12288
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
	-2048 0
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
tz_AsstFWUprBoundX_HwNm_s4p11[6][2] t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
12_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096

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Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336
	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10] t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048
	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
t2_Asst Wopibound1_within_s4p11[3][7] t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9] t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10] t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144
	-4096





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	128
t_AsstFWDefltAssistX_HwNm_u8p8[1]	154
t_AsstFWDefltAssistX_HwNm_u8p8[2]	179
t_AsstFWDefltAssistX_HwNm_u8p8[3]	205
t_AsstFWDefltAssistX_HwNm_u8p8[4]	230
t_AsstFWDefltAssistX_HwNm_u8p8[5]	256
t_AsstFWDefltAssistX_HwNm_u8p8[6]	282
t_AsstFWDefltAssistX_HwNm_u8p8[7]	307
t_AsstFWDefltAssistX_HwNm_u8p8[8]	333
t_AsstFWDefltAssistX_HwNm_u8p8[9]	358
t_AsstFWDefltAssistX_HwNm_u8p8[10]	384
t_AsstFWDefltAssistX_HwNm_u8p8[11]	410
t_AsstFWDefltAssistX_HwNm_u8p8[12]	435
t_AsstFWDefltAssistX_HwNm_u8p8[13]	461
t_AsstFWDefltAssistX_HwNm_u8p8[14]	486
t_AsstFWDefltAssistX_HwNm_u8p8[15]	512
t_AsstFWDefltAssistX_HwNm_u8p8[16]	538
t_AsstFWDefltAssistX_HwNm_u8p8[17]	563
t_AsstFWDefltAssistX_HwNm_u8p8[18]	589
t_AsstFWDefltAssistX_HwNm_u8p8[19]	614
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4096
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12288
· · · · ·	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	16384
	16384
L_ASSIF WDelitassist f_ivitinin_ s4p1 i [ 15]	
t_AsstFWDefltAssistY_MtrNm_s4p11[15] t_AsstFWDefltAssistY_MtrNm_s4p11[16]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[16] t_AsstFWDefltAssistY_MtrNm_s4p11[17]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[16] t_AsstFWDefltAssistY_MtrNm_s4p11[17] t_AsstFWDefltAssistY_MtrNm_s4p11[18]	20480 20480
t_AsstFWDefltAssistY_MtrNm_s4p11[16] t_AsstFWDefltAssistY_MtrNm_s4p11[17] t_AsstFWDefltAssistY_MtrNm_s4p11[18] t_AsstFWDefltAssistY_MtrNm_s4p11[19]	20480 20480 20480
t_AsstFWDefltAssistY_MtrNm_s4p11[16] t_AsstFWDefltAssistY_MtrNm_s4p11[17] t_AsstFWDefltAssistY_MtrNm_s4p11[18]	20480 20480
t_AsstFWDefltAssistY_MtrNm_s4p11[16] t_AsstFWDefltAssistY_MtrNm_s4p11[17] t_AsstFWDefltAssistY_MtrNm_s4p11[18] t_AsstFWDefltAssistY_MtrNm_s4p11[19]	20480 20480 20480





Name	Input Value		
t_AsstFWVehSpd_Kph_u9p7[1]	19200		
t_AsstFWVehSpd_Kph_u9p7[2]	19328		
t_AsstFWVehSpd_Kph_u9p7[3]	19456		
t_AsstFWVehSpd_Kph_u9p7[4]	19584		
t_AsstFWVehSpd_Kph_u9p7[5]	19712		
t_AsstFWVehSpd_Kph_u9p7[6]	19840		
t_AsstFWVehSpd_Kph_u9p7[7]	19968		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-3		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.0999999		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	123		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_Mt	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lo	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Se	rvice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_Mtr	·Nm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_	f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_	_enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph	_f32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.99000001	0.99000001 ± 4.88E-04	~
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0	0 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.19999981	8.19999981 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.30499983	4.30499983 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-1	-1 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.15699983	3.15700006 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.99000001	0.99000001 ± 3.05E-05	•
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.19999981	8.19999981 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x00	0x00	~
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x00	0x00	<b>V</b>

Τ				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	-

Test Step 3.12 (Repeat Count = 1)	
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0099999978
AssistFirewall_ActiveRawAcc_Cnt_M_u16	112
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00899999961
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00800000038
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00200000009
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	2.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	4.28000021
k_AsstFWNstep_Cnt_u16	3804
k_AsstFWPstep_Cnt_u16	1230





Name	Input Value
k_RestoreThresh_MtrNm_f32	2
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6] t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-14336 -12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	4096
12_AsstFWUprBoundX_HwNm_s4p11[4][10]	6144
12_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
ız_AsstFWUprBoundX_HwNm_s4p11[5][1] ı2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14330 -12288
tz_AsstFWUprBoundX_HwNm_s4p11[5][2] t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4] t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
	-6192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5] t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144 -4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-14336
tz_Asstr Wopibodild1_WithVill_sap11[4][5]	-12288
	-12Z00
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6] t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6] t2_AsstFWUprBoundY_MtrNm_s4p11[4][7] t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-10240 -8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6] t2_AsstFWUprBoundY_MtrNm_s4p11[4][7] t2_AsstFWUprBoundY_MtrNm_s4p11[4][8] t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-10240 -8192 -6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6] t2_AsstFWUprBoundY_MtrNm_s4p11[4][7] t2_AsstFWUprBoundY_MtrNm_s4p11[4][8] t2_AsstFWUprBoundY_MtrNm_s4p11[4][9] t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-10240 -8192 -6144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6] t2_AsstFWUprBoundY_MtrNm_s4p11[4][7] t2_AsstFWUprBoundY_MtrNm_s4p11[4][8] t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-10240 -8192 -6144





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4] t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096 -2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8] t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	256
t_AsstFWDefltAssistX_HwNm_u8p8[1]	282
t_AsstFWDefltAssistX_HwNm_u8p8[2] t_AsstFWDefltAssistX_HwNm_u8p8[3]	307 333
t_AsstFWDefitAssistX_HwNm_u8p8[4]	358
t_AsstFWDefltAssistX_HwNm_u8p8[5]	384
t_AsstFWDefltAssistX_HwNm_u8p8[6]	410
t_AsstFWDefltAssistX_HwNm_u8p8[7]	435
t_AsstFWDefltAssistX_HwNm_u8p8[8]	461
t_AsstFWDefltAssistX_HwNm_u8p8[9]	486
t_AsstFWDefltAssistX_HwNm_u8p8[10]	512
t_AsstFWDefltAssistX_HwNm_u8p8[11]	538
t_AsstFWDefltAssistX_HwNm_u8p8[12]	563
t_AsstFWDefltAssistX_HwNm_u8p8[13]	589
t_AsstFWDefltAssistX_HwNm_u8p8[14]	614
t_AsstFWDefltAssistX_HwNm_u8p8[15] t_AsstFWDefltAssistX_HwNm_u8p8[16]	640 666
t_AsstFWDefitAssistX_HwNm_u8p8[17]	691
t_AsstFWDefitAssistX_HwNm_u8p8[18]	717
t_AsstFWDefitAssistX_HwNm_u8p8[19]	742
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11] t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12288 14336
t_AsstFWDefitAssistY_MtrNm_s4p11[12]  t_AsstFWDefitAssistY_MtrNm_s4p11[13]	14336
t_AsstFWDefitAssistY_MtrNm_s4p11[13]	14336
t_AsstFWDefitAssistY_MtrNm_s4p11[15]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	18432
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	24576
t_AsstFWPstepNstepThresh_Cnt_u16[0]	131
t_AsstFWPstepNstepThresh_Cnt_u16[1]	243

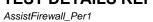
2015-03-23, 11:55:49+0530



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Name	Input Value		
t_AsstFWVehSpd_Kph_u9p7[0]	27904		
t_AsstFWVehSpd_Kph_u9p7[1]	28032		
t_AsstFWVehSpd_Kph_u9p7[2]	28160		
t_AsstFWVehSpd_Kph_u9p7[3]	28288		
t_AsstFWVehSpd_Kph_u9p7[4]	28416		
t_AsstFWVehSpd_Kph_u9p7[5]	28544		
t_AsstFWVehSpd_Kph_u9p7[6]	28672		
t_AsstFWVehSpd_Kph_u9p7[7]	28800		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	10		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_	_Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_M	trNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_M	ltrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_le	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Se	rvice_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt	_enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph	_f32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.97000003	2.97000003 ± 4.88E-04	•
AssistFirewall_ActiveRawAcc_Cnt_M_u16	243	243 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	~
AssistFirewall_CombAsstSV_MtrNm_M_f32	1	1 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.97660005	1.97660005 ± 4.88E-04	~
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0079999	5.0079999 ± 4.88E-04	~
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	~
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	0.987999976	0.987999976 ± 4.88E-04	~
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	~
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	1	1 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	~
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	~
NTC_Cnt_T_enum	0xC9	0xC9	•
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	•

T				<b>✓</b>
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	•

Test Step 3.13 (Repeat Count = 1)	<b>✓</b>
Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	1
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00800000038
AssistFirewall_ActiveRawAcc_Cnt_M_u16	121
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.099999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00899999961
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.03999996
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00600000005
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.099999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0500000007
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3
k_AsstFWInpLimitHFA_MtrNm_f32	4.5
k_AsstFWInpLimitHysComp_MtrNm_f32	5.75
k_AsstFWNstep_Cnt_u16	3432





Name	Input Value
k_AsstFWPstep_Cnt_u16	1599
k_RestoreThresh_MtrNm_f32	2.29999995
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192 10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7] t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144 4000
t2_AsstFWUprBoundX_HwNm_s4p11[4][2] t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096 -2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3] t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2046
t2_AsstrWUprBoundX_HwNm_s4p11[7][5]	2048
t2_Asst WopiBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7] t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8] t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9] t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-14336
t2_Asst WoprBoundY_MtrNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-0144 -4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	0
	2048
t2 AsstFWUprBoundY MtrNm s4p11[4][10]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10] t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5] t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096 6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6] t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192 10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9] t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	333
t_AsstFWDefltAssistX_HwNm_u8p8[1]	358
t_AsstFWDefltAssistX_HwNm_u8p8[2]	384
t_AsstFWDefltAssistX_HwNm_u8p8[3]	410
t_AsstFWDefltAssistX_HwNm_u8p8[4]	435
t_AsstFWDefltAssistX_HwNm_u8p8[5]	461
t_AsstFWDefltAssistX_HwNm_u8p8[6]	486
t_AsstFWDefltAssistX_HwNm_u8p8[7]	512
t_AsstFWDefltAssistX_HwNm_u8p8[8]	538 563
t_AsstFWDefltAssistX_HwNm_u8p8[9] t_AsstFWDefltAssistX_HwNm_u8p8[10]	589
t_AsstFWDefitAssistX_HwNm_u8p8[11]	614
t_AsstFWDefltAssistX_HwNm_u8p8[12]	640
t_AsstFWDefltAssistX_HwNm_u8p8[13]	666
t_AsstFWDefltAssistX_HwNm_u8p8[14]	691
t_AsstFWDefltAssistX_HwNm_u8p8[15]	717
t_AsstFWDefltAssistX_HwNm_u8p8[16]	742
t_AsstFWDefltAssistX_HwNm_u8p8[17]	768
t_AsstFWDefltAssistX_HwNm_u8p8[18]	794
t_AsstFWDefltAssistX_HwNm_u8p8[19]	819
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[1] t_AsstFWDefltAssistY_MtrNm_s4p11[2]	10240 10240
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	10240
t_AsstFWDefitAssistY_MtrNm_s4p11[4]	10240
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14] t_AsstFWDefltAssistY_MtrNm_s4p11[15]	20480 22528
t_AsstFWDefitAssistY_MtrNm_s4p11[16]	24576
t_AsstFWDefitAssistY_MtrNm_s4p11[17]	26624
	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	20012
t_AsstFWDefitAssistY_MtrNm_s4p11[19]	30720

AssistFirewall\_Per1



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Name	Input Value
k_AsstFWNstep_Cnt_u16	4052
k_AsstFWPstep_Cnt_u16	2460
k_RestoreThresh_MtrNm_f32	4.42999983 -14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][0] t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5] t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_Asst WopiBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2 AsstFWUprBoundX HwNm s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0





Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
tz_AsstFWUprBoundY_MtrNm_s4p11[2][7] t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	
	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7] t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
	20480 22528 24576





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288 14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8] t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2_Asst Woproduid1_ivitridii_s4p11[5][9] t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096 947
t_AsstFWDefltAssistX_HwNm_u8p8[0] t_AsstFWDefltAssistX_HwNm_u8p8[1]	947
t_AsstFWDefitAssistX_HwNm_u8p8[2]	998
t_AsstFWDefltAssistX_HwNm_u8p8[3]	998
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1408
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1408
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-204
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	0
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5] t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144 6144
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	8192
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672



Assist frewar_r err				
Name	Input Value			
t_AsstFWPstepNstepThresh_Cnt_u16[0]	234			
t_AsstFWPstepNstepThresh_Cnt_u16[1]	655			
t_AsstFWVehSpd_Kph_u9p7[0]	19072			
t_AsstFWVehSpd_Kph_u9p7[1]	19200			
t_AsstFWVehSpd_Kph_u9p7[2]	19328			
t_AsstFWVehSpd_Kph_u9p7[3]	19456			
t_AsstFWVehSpd_Kph_u9p7[4]	19584			
t_AsstFWVehSpd_Kph_u9p7[5]	19712			
t_AsstFWVehSpd_Kph_u9p7[6]	19840			
t_AsstFWVehSpd_Kph_u9p7[7]	19968			
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.19999981			
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	1			
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.5999999			
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.4000001			
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.5999999			
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0			
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176			
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActi	ve_Uls_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd	_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32			
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_				
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32			
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32				
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_0	Cnt_enum		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_h	(ph_f32		
Name	Actual Value	Expected Value	Result	
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-3.18000007	-3.18000007 ± 4.88E-04	•	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	655	655 ± 1	•	
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	•	
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019	-8.80000019 ± 4.88E-04	•	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-6.06399965	-6.06400013 ± 4.88E-04	•	
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-4.90400028	-4.90399981 ± 4.88E-04	•	
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	•	
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.79002142	2.79002142 ± 4.88E-04	•	
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	•	
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-8.80000019	-8.80000019 ± 9.77E-04	•	
NTC_Cnt_T_enum	0xC6	0xC6	•	
Param_Cnt_T_u08	0x01	0x01	•	
Status_Cnt_T_enum	0x01	0x01	•	
NTC_Cnt_T_enum	0xC9	0xC9	•	
Param_Cnt_T_u08	0x01	0x01	•	
Status_Cnt_T_enum	0x01	0x01	•	

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	•
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	•
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	•

Test Step 3.15 (Repeat Count = 1)		
Name	Input Value	
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.30000019	
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.40000006	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487	
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.19999981	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11199999	
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.119999997	
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.099999	
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.219999999	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.80000019	
k AsstFWInpLimitHFA MtrNm f32	6.40999985	





Name	Input Value
c_AsstFWInpLimitHysComp_MtrNm_f32	6.71000004
c_AsstFWNstep_Cnt_u16	4052
c_AsstFWPstep_Cnt_u16	2460
c_RestoreThresh_MtrNm_f32	4.42999983
2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[1][5] 2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
, , , , , , , , , , , , , , , , , , , ,	4096
2_AsstFWUprBoundX_HwNm_s4p11[1][7]	
2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096 -2048
2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
	6144
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	
2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
2_AsstFWUprBoundX_HwNm_s4p11[5][8] 2_AsstFWUprBoundX_HwNm_s4p11[5][9]	
2_AsstFWUprBoundX_HwNm_s4p11[5][8] 2_AsstFWUprBoundX_HwNm_s4p11[5][9] 2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
2_AsstFWUprBoundX_HwNm_s4p11[5][8] 2_AsstFWUprBoundX_HwNm_s4p11[5][9]	

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Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[0][0] 2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
z_AsstFWUprBoundY_MtrNm_s4p11[0][2] 2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
2_ASSTFWUprBoundY_MtrNm_s4p11[0][3] 2_ASStFWUprBoundY_MtrNm_s4p11[0][4]	
	8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
z_AsstFWUprBoundY_MtrNm_s4p11[2][7] 2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
	14336
2 AsstFWUprBoundY MtrNm s4p11[4][5]	
2_AsstFWUprBoundY_MtrNm_s4p11[4][5] 2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	
2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384





Name	Innuit Value
Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	947
t_AsstFWDefltAssistX_HwNm_u8p8[1]	973
t_AsstFWDefltAssistX_HwNm_u8p8[2]	998
	1024
t_AsstFWDefltAssistX_HwNm_u8p8[3]	
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1331
t_AsstFWDefitAssistX_HwNm_u8p8[16]	1357
t_AsstFWDefitAssistX_HwNm_u8p8[17]	1382
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1408
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1434
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-204
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	0
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefitAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	
	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[13] t_AsstFWDefltAssistY_MtrNm_s4p11[14] t_AsstFWDefltAssistY_MtrNm_s4p11[15]	
t_AsstFWDefltAssistY_MtrNm_s4p11[13] t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[13] t_AsstFWDefltAssistY_MtrNm_s4p11[14] t_AsstFWDefltAssistY_MtrNm_s4p11[15]	20480 22528





Name	Input Value			
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720			
t_AsstFWPstepNstepThresh_Cnt_u16[0]	234			
t_AsstFWPstepNstepThresh_Cnt_u16[1]	655			
t_AsstFWVehSpd_Kph_u9p7[0]	19072			
t_AsstFWVehSpd_Kph_u9p7[1]	19200			
t_AsstFWVehSpd_Kph_u9p7[2]	19328			
t_AsstFWVehSpd_Kph_u9p7[3]	19456			
t_AsstFWVehSpd_Kph_u9p7[4]	19584			
t_AsstFWVehSpd_Kph_u9p7[5]	19712			
t_AsstFWVehSpd_Kph_u9p7[6]	19840			
t_AsstFWVehSpd_Kph_u9p7[7]	19968			
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.19999981			
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	1			
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.5999999			
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.4000001			
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.5999999			
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0			
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176			
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFire	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f3	2 tgt_AssistFirewall_Per1_BaseAss	sistCmd_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f3	tgt_AssistFirewall_Per1_Combine	edAssist_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_C	nt_lc_tgt_AssistFirewall_Per1_Defeat_A	AsstTbl_Service_Cnt_lgc		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	2 tgt_AssistFirewall_Per1_HighFree	Assist_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorqu	ue_HwNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f3	32 tgt_AssistFirewall_Per1_Hysteres	sisComp_MtrNm_f32		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Co	punter_Cnt_enum		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleS	Speed_Kph_f32		
Name	Actual Value	Expected Value	Resul	
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-3.18000007	-3.18000007 ± 4.88E-04		
AssistFirewall ActiveRawAcc Cnt M u16	655	655 ± 1		
AssistFirewall AsstReducedPerfSV Cnt M lgc	1	1		
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019	-8.80000019 ± 4.88E-04		
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-6.06399965	-6.06400013 ± 4.88E-04		
AssistFirewall LwrBoundKSV M str.SV Uls f32	-4.90400028	-4.90399981 ± 4.88E-04		
AssistFirewall PNCountStatus Cnt M lqc	1	1		
AssistFirewall UprBoundKSV M str.SV Uls f32	2.79002142	2.79002142 ± 4.88E-04		
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05		
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-8.80000019	-8.80000019 ± 9.77E-04		
NTC_Cnt_T_enum	0xC6	0xC6		
Param_Cnt_T_u08	0x01	0x01	•	
Status_Cnt_T_enum	0x01	0x01		
NTC_Cnt_T_enum	0xC9	0xC9		
Param_Cnt_T_u08	0x01	0x01	•	

T				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	•
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~

Test Step 3.16 (Repeat Count = 1)		<b>~</b>
Name	Input Value	
AssistFirewall_ActiveKSV_M_str.SV_UIs_f32	4	
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0199999996	
AssistFirewall_ActiveRawAcc_Cnt_M_u16	130	
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.79999995	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3	
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.029999993	
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.07000005	
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6	
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00899999961	
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2	
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0799999982	
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall	
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.9000001	

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Name	Input Value
k_AsstFWInpLimitHFA_MtrNm_f32	1.8999998
k_AsstFWInpLimitHysComp_MtrNm_f32	1.3999998
k_AsstFWNstep_Cnt_u16	3060
k_AsstFWPstep_Cnt_u16	1968
k_RestoreThresh_MtrNm_f32	2.599999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0] t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192 -6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_Asst WoprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048 4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5] t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9] t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384 18432
tz_AsstFWUprBoundX_HwNm_s4p11[4][10] t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-2048
t2_Asst WopiBoundX_HwNm_s4p11[5][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0





Name	Input Value
2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[0][0] 2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
	6144
2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144 8192
2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	
2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-28672
2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-26624
2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-24576
2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-22528
2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-20480
2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-18432
2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-16384
2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-14336
2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144
2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576
2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-12288
2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-10240
2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-8192
	-6144
2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	
	-4096
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	
.2_AsstFWUprBoundY_MtrNm_s4p11[4][4] .2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-2048
2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	





Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240 12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6] t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336 16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8] t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	410
t_AsstFWDefltAssistX_HwNm_u8p8[1]	435
t_AsstFWDefltAssistX_HwNm_u8p8[2]	461
t AsstFWDefltAssistX HwNm u8p8[3]	486
t_AsstFWDefltAssistX_HwNm_u8p8[4]	512
t_AsstFWDefltAssistX_HwNm_u8p8[5]	538
t_AsstFWDefltAssistX_HwNm_u8p8[6]	563
t_AsstFWDefltAssistX_HwNm_u8p8[7]	589
t_AsstFWDefltAssistX_HwNm_u8p8[8]	614
t_AsstFWDefltAssistX_HwNm_u8p8[9]	640
t_AsstFWDefltAssistX_HwNm_u8p8[10]	666
t_AsstFWDefltAssistX_HwNm_u8p8[11]	691
t_AsstFWDefltAssistX_HwNm_u8p8[12]	717
t_AsstFWDefltAssistX_HwNm_u8p8[13]	742
t_AsstFWDefltAssistX_HwNm_u8p8[14]	768
t_AsstFWDefltAssistX_HwNm_u8p8[15]	794
t_AsstFWDefltAssistX_HwNm_u8p8[16]	819
t_AsstFWDefltAssistX_HwNm_u8p8[17]	845
t_AsstFWDefltAssistX_HwNm_u8p8[18]	870
t_AsstFWDefltAssistX_HwNm_u8p8[19]	896
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	5324
t_AsstFWDefitAssistY_MtrNm_s4p11[2]	5529
t_AsstFWDefltAssistY_MtrNm_s4p11[3] t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5734 5939
t_AsstFWDefitAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefitAssistY_MtrNm_s4p11[6]	6348
t_AsstFWDefitAssistY_MtrNm_s4p11[7]	6553
t_AsstFWDefitAssistY_MtrNm_s4p11[8]	6758
t_AsstFWDefitAssistY_MtrNm_s4p11[9]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	7168
t_AsstFWDefitAssistY_MtrNm_s4p11[11]	7372
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	7577
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[15] t_AsstFWDefltAssistY_MtrNm_s4p11[16]	8192 8396

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Assisti ilewaii_r ei i			( CIPC ( COID
Name	Input Value		
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	8806		
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	9011		
t_AsstFWPstepNstepThresh_Cnt_u16[0]	137		
t_AsstFWPstepNstepThresh_Cnt_u16[1]	267		
t_AsstFWVehSpd_Kph_u9p7[0]	45568		
t_AsstFWVehSpd_Kph_u9p7[1]	45696		
t_AsstFWVehSpd_Kph_u9p7[2]	45824		
t_AsstFWVehSpd_Kph_u9p7[3]	45952		
t_AsstFWVehSpd_Kph_u9p7[4]	46080		
t_AsstFWVehSpd_Kph_u9p7[5]	46208		
t_AsstFWVehSpd_Kph_u9p7[6]	46336		
t_AsstFWVehSpd_Kph_u9p7[7]	46464		
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3.0999999		
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0		
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.0999999		
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-2		
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-8.80000019		
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0		
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	77.1999969		
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActiv	re_Uls_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_	MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist	_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_	lt tgt_AssistFirewall_Per1_Defeat_AsstTbl_	Service_Cnt_lgc	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_	MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwN	m_f32	
$tgt\_Rte\_Inst\_Ap\_AssistFirewall\_AssistFirewall\_Per1\_HysteresisComp\_MtrNm\_f32$	tgt_AssistFirewall_Per1_HysteresisComp	_MtrNm_f32	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_0	Cnt_enum	
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_K	ph_f32	
Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.92000008	3.92000008 ± 4.88E-04	<b>✓</b>
AssistFirewall_ActiveRawAcc_Cnt_M_u16	267	267 ± 1	<b>✓</b>
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	-
AssistFirewall_CombAsstSV_MtrNm_M_f32	-2.89990234	-2.89990234 ± 4.88E-04	<b>✓</b>
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.01799989	3.01799989 ± 4.88E-04	<b>✓</b>
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.8829999	5.8829999 ± 4.88E-04	<b>✓</b>
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	-
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.07999992	2.07999992 ± 4.88E-04	<b>✓</b>
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	-
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-2.89990234	-2.89990234 ± 9.77E-04	<b>✓</b>
NTC_Cnt_T_enum	0xC6	0xC6	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	<b>✓</b>
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>
NTC_Cnt_T_enum	0xC9	0xC9	<b>✓</b>
Param_Cnt_T_u08	0x01	0x01	~
Status_Cnt_T_enum	0x01	0x01	<b>✓</b>

T ✓				
Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	~
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	~
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	~
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	~
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	~