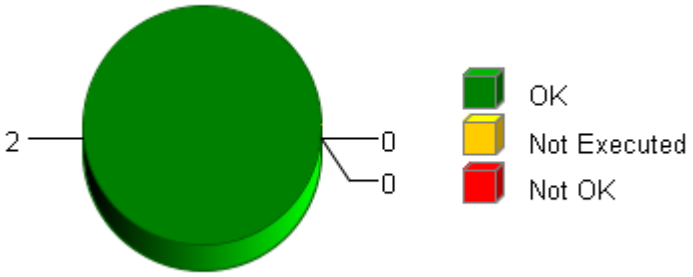
Summary

Total Test Objects:	2
Successful:	2
Failed:	0
Not Executed:	0
Date:	2015-03-23
Time:	11:41:07+0530

Overall Test Object Results (including Coverage)



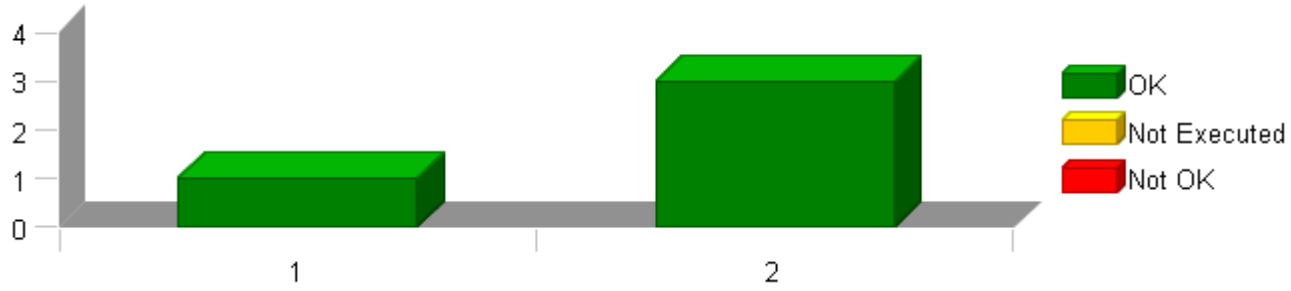
Selected Project Items

Test Object "CBD_UnitTest/AssistFireWall/AssistFirewall_Init1"
Test Object "CBD_UnitTest/AssistFireWall/AssistFirewall_Per1"

Used Test Environments

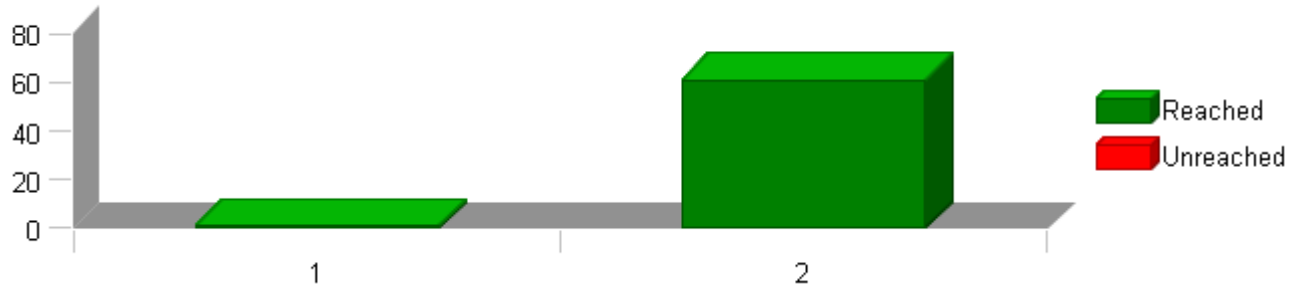
TI TMS 570 PLS UDE (Default)

Test Case Results for Each Test Object (without Coverage)



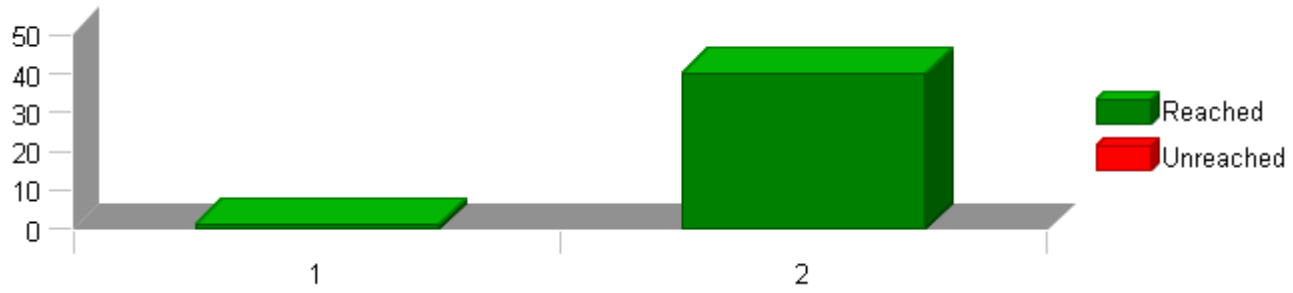
The table above shows each test object on the x axis and the number of test cases of the respective test object on the y axis. Each bar is divided into passed, not executed and failed test cases. The test case results do not take into account any coverage result (i.e. if all test cases of a test object are passed in this table but the coverage is failed, the overall test object result will be failed).

Statement (C0) Coverage: Total Statements for Each Test Object



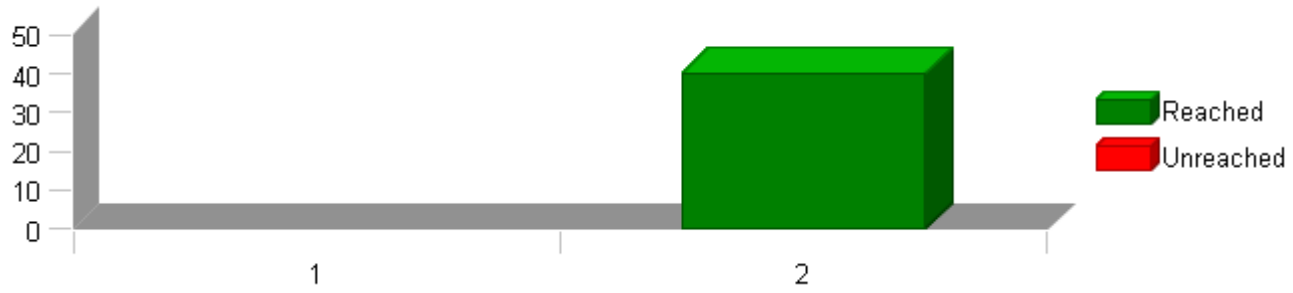
The table above shows each test object on the x axis and the number of statements of the respective test object on the y axis. Each bar is divided into reached statements (i.e. statements that have been executed during the test) and unreached statements.

Branch (C1) Coverage: Total Branches for Each Test Object



The table above shows each test object on the x axis and the number of branches of the respective test object on the y axis. Each bar is divided into reached branches (i.e. branches that have been executed during the test) and unreached branches.

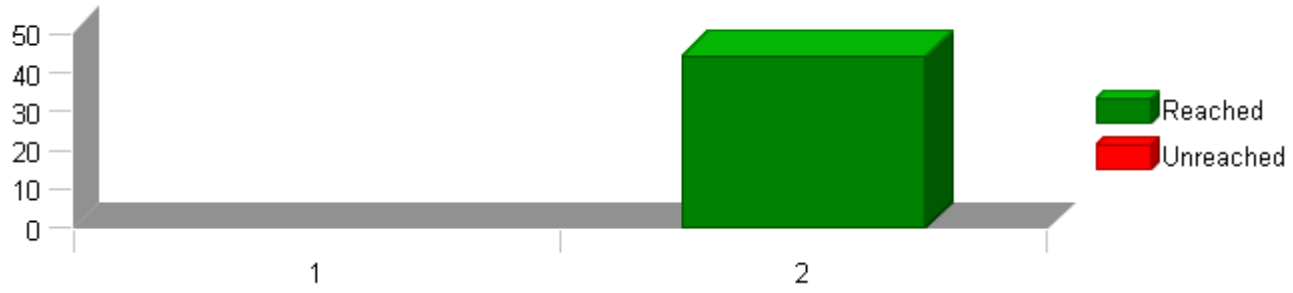
Decision Coverage: Total Decision Outcomes for Each Test Object



The table above shows test objects on the x axis and the number of possible outcomes of all decisions of the respective test object on the y axis. To achieve full DC coverage, each decision must evaluate to both true and false.

Each bar is divided into reached and unreached decision outcomes.

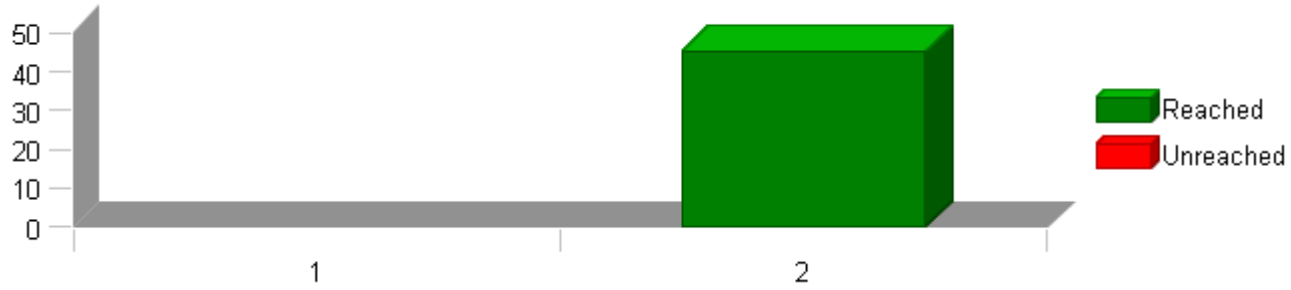
MC/DC Coverage: Total Condition Combinations for Each Test Object



The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MC/DC coverage, each decision requires all contained atomic conditions to evaluate to both true and false independently of all other conditions. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.

MCC Coverage: Total Condition Combinations for Each Test Object



The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MCC coverage, each decision requires all contained atomic conditions to evaluate to all possible combinations of true and false values. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.

Test Object List

The following table lists all test objects with their test case and coverage results. The cumulated results for modules, folders and test collections are also displayed, the indentation within the name column indicates the parent relationship of the elements.

Please note that only test objects are numbered within the first column. This number is referenced on the x axis within the overview charts for test case and coverage results available on previous pages (if included into the report).

No.	Name	C0	C1	DC	MC/DC	MCC	Test Cases	Result
	AssistFirewall	100 %	100 %	100 %	100 %	100 %	4 of 4 passed	✔
	CBD_UnitTest	100 %	100 %	100 %	100 %	100 %	4 of 4 passed	✔
	AssistFireWall	100 %	100 %	100 %	100 %	100 %	4 of 4 passed	✔
1	AssistFirewall_Init1	100 %	100 %	-	-	-	1 of 1 passed	✔
2	AssistFirewall_Per1	100 %	100 %	100 %	100 %	100 %	3 of 3 passed	✔

TEST DETAILS REPORT

Project	AssistFirewall
Module	AssistFireWall
Test Object	AssistFirewall_Per1

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Decision Coverage	100 %
Branch (C1) Coverage	100 %
MCC Coverage	100 %
MC/DC Coverage	100 %

Statistics

Total Testcases	3
Successful	3
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\AssistFirewall
Configuration File	D:\Synergy_Work_Area\AssistFirewall\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	$(PROJECTROOT)\src\Ap_AssistFirewall.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -DBC_ASSISTFIREWALL_FAULTINJECTIONPOINT=STD_OFF -I$(PROJECTROOT)\utp\contract \Ap_AssistFirewall -I$(PROJECTROOT)\utp\contract -I$(PROJECTROOT)\NxtrLib\include -I$(PROJECTROOT)\StdDef\include -I$ (Compiler Install Path)\include
File	$(PROJECTROOT)\NxtrLib\src\interpolation.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -DBC_ASSISTFIREWALL_FAULTINJECTIONPOINT=STD_OFF -I$(PROJECTROOT)\utp\contract \Ap_AssistFirewall -I$(PROJECTROOT)\utp\contract -I$(PROJECTROOT)\NxtrLib\include -I$(PROJECTROOT)\StdDef\include -I$ (Compiler Install Path)\include

Comments/Description/Specification

Name	Text
Module 'AssistFireWall'	**********Unit Test Information********** Name of Tester:Ankita Bhardwaj Code File(s) Under Test:Ap_AssistFirewall.c Code File(s) Version:14 Module Design Document:Assist_Firewall_MDD.docx Module Design Document Version:14 Data Dictionary Version:16 Unit Test Plan Version:11 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.31 Total FLASH Used (Bytes):1568 Total RAM Used (Bytes):79 Total CALS Used (Bytes):480 Special Test Requirements: Test Date:03-23-2015 Comments:"NOTE:1) Inline functions defined in GlobalMacro.h are not Unit Tested. 2)""CBD_Sandbox_dbg.map""map file is embedded for reference. 3) In ""AssistFirewall_Per1"" function, ""Defeat_AsstTbl_Service_Cnt_lgc"" always kept FALSE to make ""if((DefeatAsstTblSvc_Cnt_T_lgc <> D_FALSE_CNT_LGC) And (MECCounter_Cnt_T_enum <> ProductionMode))"" condition FALSE except Boundray Test for variables used in Condition and Path coverage. " **********

Attributes

Name	Value
Compiler Install Path	$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9

Attributes

Name	Value
InitObjDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	$(ProgramFiles)\pls\UDE 3.2
Time Unit	Cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\AssistFirewall\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

TEST DETAILS REPORT

Test Case 1: Metrics Test

Specification

```
Performance Metrics (With "None" Instrumentation
and WithPS Environment)
CPU Cycles:


TC1.1 6628.00 Cycles
TC1.2 6630.00 Cycles
```

Description

Vector description

TS1.1Shortest Execution Path:((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=True && ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=True && ((BaseAssistCmd_MtrNm_T_f32)<=(-k_AsstFWInpLimitBaseAsst_MtrNm_f32))=True && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode))=True
TS1.2"Longest Execution Path:""((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HysteresisComp_MtrNm_T_f32)<=(-k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))= False &&((HighFreqAssist_MtrNm_T_f32)<=(-k_AsstFWInpLimitHFA_MtrNm_f32))=False &&((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((BaseAssistCmd_MtrNm_T_f32)<=(-k_AsstFWInpLimitBaseAsst_MtrNm_f32))=True && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32)>=(UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32)<=(-UprBoundFilt_MtrNm_T_f32))=False && DefltAsst_MtrNm_T_f32 = DefltAsstLookup_MtrNm_T_f32 * ((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32 < LwrBoundFilt_MtrNm_T_f32) || (LowFreqInput_MtrNm_T_f32 > UprBoundFilt_MtrNm_T_f32))=False &&((AssistFirewall_ActiveRawAcc_Cnt_M_u16)<((AssistFirewall_ActiveRawAcc_Cnt_M_u16)>((AsstFWPstepNstep_Cnt_T_str.Nstep)=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[1])=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 > t_AsstFWPstepNstepThresh_Cnt_u16[0])=True && (((Abs_f32_m(SumInput_MtrNm_T_f32 - AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=False && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=False && (AsstFWActive_Uls_T_f32>1)=False && (AsstFWActive_Uls_T_f32<=0)=True ""
"

Test Step 1.1 (Repeat Count = 1)

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.30000019
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.400000006
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11199999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.119999997
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.219999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.80000019
k_AsstFWInpLimitHFA_MtrNm_f32	6.40999985
k_AsstFWInpLimitHysComp_MtrNm_f32	6.71000004
k_AsstFWNstep_Cnt_u16	4052
k_AsstFWPstep_Cnt_u16	2460
k_RestoreThresh_MtrNm_f32	4.42999983
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	947
t_AsstFWDefltAssistX_HwNm_u8p8[1]	973
t_AsstFWDefltAssistX_HwNm_u8p8[2]	998
t_AsstFWDefltAssistX_HwNm_u8p8[3]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1382
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1408
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1434
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	0
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720
t_AsstFWPstepNstepThresh_Cnt_u16[0]	234
t_AsstFWPstepNstepThresh_Cnt_u16[1]	655
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
t_AsstFWVehSpd_Kph_u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7.30000019
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	1
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.19999981
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.4000001
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.30000019	-5.30000019 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487	8487 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	17.9200001	17.9200001 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-3.35039997	-3.35039997 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019	-5.30000019 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999	5.0999999 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	17.9200001	17.9200001 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x00	0x00	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x00	0x00	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 1.2 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-3.4000001
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4797
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0199999996
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.5
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.600000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00899999961
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.79999995
k_AsstFWInpLimitHFA_MtrNm_f32	3.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	3.29999995
k_AsstFWNstep_Cnt_u16	4551
k_AsstFWPstep_Cnt_u16	2337
k_RestoreThresh_MtrNm_f32	6.9000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	282
t_AsstFWDefltAssistX_HwNm_u8p8[1]	307
t_AsstFWDefltAssistX_HwNm_u8p8[2]	333
t_AsstFWDefltAssistX_HwNm_u8p8[3]	358
t_AsstFWDefltAssistX_HwNm_u8p8[4]	384
t_AsstFWDefltAssistX_HwNm_u8p8[5]	410
t_AsstFWDefltAssistX_HwNm_u8p8[6]	435
t_AsstFWDefltAssistX_HwNm_u8p8[7]	461
t_AsstFWDefltAssistX_HwNm_u8p8[8]	486
t_AsstFWDefltAssistX_HwNm_u8p8[9]	512
t_AsstFWDefltAssistX_HwNm_u8p8[10]	538
t_AsstFWDefltAssistX_HwNm_u8p8[11]	563
t_AsstFWDefltAssistX_HwNm_u8p8[12]	589
t_AsstFWDefltAssistX_HwNm_u8p8[13]	614
t_AsstFWDefltAssistX_HwNm_u8p8[14]	640
t_AsstFWDefltAssistX_HwNm_u8p8[15]	666
t_AsstFWDefltAssistX_HwNm_u8p8[16]	691
t_AsstFWDefltAssistX_HwNm_u8p8[17]	717
t_AsstFWDefltAssistX_HwNm_u8p8[18]	742
t_AsstFWDefltAssistX_HwNm_u8p8[19]	768
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	30720
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720
t_AsstFWPstepNstepThresh_Cnt_u16[0]	170
t_AsstFWPstepNstepThresh_Cnt_u16[1]	399
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
t_AsstFWVehSpd_Kph_u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-8.5
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-9
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	77
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-3.06000018	-3.05999994 ± 4.88E-04	✔

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveRawAcc_Cnt_M_u16	246	246 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	0.400000095	0.400000095 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.08599997	1.08600008 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-6.19999981	-6.19999981 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.90100002	7.90100002 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	0.400000095	0.400000095 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x00	0x00	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x00	0x00	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Case 2: Boundary Test ✔

Specification

```
Performance Metrics (With "None" Instrumentation
and WithPS Environment)
CPU Cycles:

TC2.1 6628.00 Cycles
TC2.2 6628.00 Cycles
TC2.3 6629.00 Cycles
TC2.4 6629.00 Cycles
TC2.5 6629.00 Cycles
TC2.6 6629.00 Cycles
TC2.7 6629.00 Cycles
TC2.8 6629.00 Cycles
TC2.9 6629.00 Cycles
TC2.10 6629.00 Cycles
TC2.11 6629.00 Cycles
TC2.12 6629.00 Cycles
TC2.13 6629.00 Cycles
TC2.14 6629.00 Cycles
TC2.15 6629.00 Cycles
TC2.16 6629.00 Cycles
TC2.17 6629.00 Cycles
TC2.18 6629.00 Cycles
TC2.19 6629.00 Cycles
TC2.20 6629.00 Cycles
TC2.21 6629.00 Cycles
TC2.22 6629.00 Cycles
TC2.23 6629.00 Cycles
TC2.24 6629.00 Cycles
TC2.25 6629.00 Cycles
TC2.26 6629.00 Cycles
TC2.27 6629.00 Cycles
TC2.28 6629.00 Cycles
TC2.29 6629.00 Cycles
TC2.30 6629.00 Cycles
TC2.31 6629.00 Cycles
TC2.32 6629.00 Cycles
TC2.33 6629.00 Cycles
TC2.34 6629.00 Cycles
TC2.35 6629.00 Cycles
TC2.36 6629.00 Cycles
TC2.37 6629.00 Cycles
TC2.38 6629.00 Cycles
TC2.39 6629.00 Cycles
TC2.40 6629.00 Cycles
TC2.41 6629.00 Cycles
TC2.42 6629.00 Cycles
TC2.43 6629.00 Cycles
TC2.44 6629.00 Cycles
TC2.45 6629.00 Cycles
TC2.46 6629.00 Cycles
TC2.47 6629.00 Cycles
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TC2.51 6629.00 Cycles
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TC2.66 6629.00 Cycles
TC2.67 6629.00 Cycles
TC2.68 6629.00 Cycles
TC2.69 6629.00 Cycles
TC2.70 6629.00 Cycles
TC2.71 6629.00 Cycles
TC2.72 6629.00 Cycles
TC2.73 6629.00 Cycles
TC2.74 6629.00 Cycles
TC2.75 6629.00 Cycles
TC2.76 6629.00 Cycles
TC2.77 6629.00 Cycles
TC2.78 6629.00 Cycles
TC2.79 6629.00 Cycles
TC2.80 6629.00 Cycles
TC2.81 6629.00 Cycles
TC2.82 6629.00 Cycles
TC2.83 6629.00 Cycles
TC2.84 6629.00 Cycles
TC2.85 6629.00 Cycles
TC2.86 6629.00 Cycles
TC2.87 6629.00 Cycles
TC2.88 6629.00 Cycles
TC2.89 6629.00 Cycles
TC2.90 6629.00 Cycles
TC2.91 6629.00 Cycles
TC2.92 6629.00 Cycles
TC2.93 6629.00 Cycles
TC2.94 6629.00 Cycles
TC2.95 6629.00 Cycles
TC2.96 6629.00 Cycles
TC2.97 6629.00 Cycles
TC2.98 6629.00 Cycles
TC2.99 6629.00 Cycles
TC2.100 6629.00 Cycles
TC2.101 6629.00 Cycles
TC2.102 6629.00 Cycles
TC2.103 6629.00 Cycles
TC2.104 6629.00 Cycles
TC2.105 6629.00 Cycles
TC2.106 6629.00 Cycles
TC2.107 6629.00 Cycles
TC2.108 6629.00 Cycles
TC2.109 6629.00 Cycles
TC2.110 6629.00 Cycles
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TC2.111 6629.00 Cycles
TC2.112 6629.00 Cycles
TC2.113 6629.00 Cycles
TC2.114 6629.00 Cycles
TC2.115 6629.00 Cycles
TC2.116 6629.00 Cycles
TC2.117 6629.00 Cycles
TC2.118 6629.00 Cycles
TC2.119 6629.00 Cycles
```

Description Vector Description

TS2.1BaseAssistCmd_MtrNm_f32 = min
TS2.2BaseAssistCmd_MtrNm_f32 = max
TS2.3BaseAssistCmd_MtrNm_f32 = zero
TS2.4BaseAssistCmd_MtrNm_f32 =pos
TS2.5BaseAssistCmd_MtrNm_f32= neg
TS2.6HighFreqAssist_MtrNm_f32 = min
TS2.7HighFreqAssist_MtrNm_f32 = max
TS2.8HighFreqAssist_MtrNm_f32 = zero
TS2.9HighFreqAssist_MtrNm_f32 = pos
TS2.10HighFreqAssist_MtrNm_f32 = neg
TS2.11HwTorque_HwNm_f32 = min
TS2.12HwTorque_HwNm_f32 = max
TS2.13HwTorque_HwNm_f32 = zero
TS2.14HwTorque_HwNm_f32 = pos
TS2.15HwTorque_HwNm_f32 = neg
TS2.16HysteresisComp_MtrNm_f32 = min
TS2.17HysteresisComp_MtrNm_f32 = max
TS2.18HysteresisComp_MtrNm_f32 = zero
TS2.19HysteresisComp_MtrNm_f32 = pos
TS2.20HysteresisComp_MtrNm_f32 = neg
TS2.21VehicleSpeed_Kph_f32 = min
TS2.22VehicleSpeed_Kph_f32 = max
TS2.23VehicleSpeed_Kph_f32 = mid
TS2.24t_AsstFWVehSpd_Kph_u9p7[8] = min
TS2.25t_AsstFWVehSpd_Kph_u9p7[8] = max
TS2.26t_AsstFWVehSpd_Kph_u9p7[8] = mid
TS2.27t2_AsstFWUprBoundX_HwNm_s4p11[11] = min
TS2.28t2_AsstFWUprBoundX_HwNm_s4p11[11] = max
TS2.29t2_AsstFWUprBoundX_HwNm_s4p11[11] = zero
TS2.30t2_AsstFWUprBoundX_HwNm_s4p11[11] = pos
TS2.31t2_AsstFWUprBoundX_HwNm_s4p11[11] = neg
TS2.32t2_AsstFWUprBoundY_MtrNm_s4p11[11] = min
TS2.33t2_AsstFWUprBoundY_MtrNm_s4p11[11] = max
TS2.34t2_AsstFWUprBoundY_MtrNm_s4p11[11] = zero
TS2.35t2_AsstFWUprBoundY_MtrNm_s4p11[11] = pos
TS2.36t2_AsstFWUprBoundY_MtrNm_s4p11[11] = neg
TS2.37AssistFirewall_UprBoundKSV_M_str.SV = min
TS2.38AssistFirewall_UprBoundKSV_M_str.SV = max
TS2.39AssistFirewall_UprBoundKSV_M_str.SV= zero
TS2.40AssistFirewall_UprBoundKSV_M_str.SV.SV = pos
TS2.41AssistFirewall_UprBoundKSV_M_str.SV.SV = neg
TS2.42AssistFirewall_UprBoundKSV_M_str.K= min
TS2.43AssistFirewall_UprBoundKSV_M_str.K= max
TS2.44AssistFirewall_UprBoundKSV_M_str.K.K = mid
TS2.45AssistFirewall_LwrBoundKSV_M_str.SV= min
TS2.46AssistFirewall_LwrBoundKSV_M_str.SV= max
TS2.47AssistFirewall_LwrBoundKSV_M_str.SV= zero
TS2.48AssistFirewall_LwrBoundKSV_M_str.SV= pos
TS2.49AssistFirewall_LwrBoundKSV_M_str.SV = neg
TS2.50AssistFirewall_LwrBoundKSV_M_str.K= min
TS2.51AssistFirewall_LwrBoundKSV_M_str.K= max
TS2.52AssistFirewall_LwrBoundKSV_M_str.K= mid
TS2.53AssistFirewall_ActiveKSV_M_str.SV = min
TS2.54AssistFirewall_ActiveKSV_M_str.SV = max
TS2.55AssistFirewall_ActiveKSV_M_str.SV = zero
TS2.56AssistFirewall_ActiveKSV_M_str.SV= pos
TS2.57AssistFirewall_ActiveKSV_M_str.SV= neg
TS2.58AssistFirewall_ActiveKSV_M_str.K= min
TS2.59AssistFirewall_ActiveKSV_M_str.K= max
TS2.60AssistFirewall_ActiveKSV_M_str.K= mid
TS2.61AssistFirewall_HiFreqKSV_M_str.LPF.SV = min
TS2.62AssistFirewall_HiFreqKSV_M_str.LPF.SV = max
TS2.63AssistFirewall_HiFreqKSV_M_str.LPF.SV= zero
TS2.64AssistFirewall_HiFreqKSV_M_str.LPF.SV= pos
TS2.65AssistFirewall_HiFreqKSV_M_str.LPF.SV= neg
TS2.66AssistFirewall_HiFreqKSV_M_str.LPF.K= min
TS2.67AssistFirewall_HiFreqKSV_M_str.LPF.K= max
TS2.68AssistFirewall_HiFreqKSV_M_str.LPF.K= mid
TS2.69AssistFirewall_HiFreqKSV_M_str.CF = min
TS2.70AssistFirewall_HiFreqKSV_M_str.CF = max
TS2.71AssistFirewall_HiFreqKSV_M_str.CF=mid
TS2.72k_AsstFWInpLimitHysComp_MtrNm_f32 = min
TS2.73k_AsstFWInpLimitHysComp_MtrNm_f32 = max
TS2.74k_AsstFWInpLimitHysComp_MtrNm_f32 = mid
TS2.75k_AsstFWInpLimitHFA_MtrNm_f32 = min
TS2.76k_AsstFWInpLimitHFA_MtrNm_f32 = max
TS2.77k_AsstFWInpLimitHFA_MtrNm_f32 = mid
TS2.78k_AsstFWInpLimitBaseAsst_MtrNm_f32 = min
TS2.79k_AsstFWInpLimitBaseAsst_MtrNm_f32 =max
TS2.80k_AsstFWInpLimitBaseAsst_MtrNm_f32 = mid
TS2.81AssistFirewall_ActiveRawAcc_Cnt_M_u16 = min
TS2.82AssistFirewall_ActiveRawAcc_Cnt_M_u16= max
TS2.83AssistFirewall_ActiveRawAcc_Cnt_M_u16 = mid
TS2.84t_AsstFWPstepNstepThresh_Cnt_u16[2] = min
TS2.85t_AsstFWPstepNstepThresh_Cnt_u16[2] = max
TS2.86t_AsstFWPstepNstepThresh_Cnt_u16[2] =mid
TS2.87k_AsstFWPstep_Cnt_u16 = min
TS2.88k_AsstFWPstep_Cnt_u16 = max
TS2.89k_AsstFWPstep_Cnt_u16 = mid
TS2.90k_AsstFWNstep_Cnt_u16 = min
TS2.91k_AsstFWNstep_Cnt_u16 = max
TS2.92k_AsstFWNstep_Cnt_u16 = mid
TS2.93AssistFirewall_PNCountStatus_Cnt_M_lgc = FASLE
TS2.94AssistFirewall_PNCountStatus_Cnt_M_lgc= TRUE

TS2.95AssistFirewall_CombAsstSV_MtrNm_M_f32 = min
TS2.96AssistFirewall_CombAsstSV_MtrNm_M_f32 = max
TS2.97AssistFirewall_CombAsstSV_MtrNm_M_f32= zero
TS2.98AssistFirewall_CombAsstSV_MtrNm_M_f32 = pos
TS2.99AssistFirewall_CombAsstSV_MtrNm_M_f32= neg
TS2.100AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc = FALSE
TS2.101AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc= TRUE
TS2.102t_AsstFWDefltAssistX_HwNm_u8p8[20]= min
TS2.103t_AsstFWDefltAssistX_HwNm_u8p8[20] = max
TS2.104t_AsstFWDefltAssistX_HwNm_u8p8[20] =mid
TS2.105t_AsstFWDefltAssistY_MtrNm_s4p11[20] = min
TS2.106t_AsstFWDefltAssistY_MtrNm_s4p11[20] = max
TS2.107t_AsstFWDefltAssistY_MtrNm_s4p11[20] = zero
TS2.108t_AsstFWDefltAssistY_MtrNm_s4p11[20] = pos
TS2.109t_AsstFWDefltAssistY_MtrNm_s4p11[20] = neg
TS2.110k_RestoreThresh_MtrNm_f32 = min
TS2.111k_RestoreThresh_MtrNm_f32 = max
TS2.112k_RestoreThresh_MtrNm_f32 = mid
TS2.113Defeat_AsstTbl_Service_Cnt_lgc==>Max
TS2.114Defeat_AsstTbl_Service_Cnt_lgc==Min
TS2.115MEC_Counter_Cnt_enum==>Min
TS2.116MEC_Counter_Cnt_enum==>Max
TS2.117MEC_Counter_Cnt_enum==>Pos
TS2.118All min
TS2.119All Max

Test Step 2.1 (Repeat Count = 1)

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0900000036
AssistFirewall_ActiveRawAcc_Cnt_M_u16	109
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.89999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0700000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00999999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4
k_AsstFWInpLimitHFA_MtrNm_f32	2.5
k_AsstFWInpLimitHysComp_MtrNm_f32	3.78999996
k_AsstFWNstep_Cnt_u16	3928
k_AsstFWPstep_Cnt_u16	1107
k_RestoreThresh_MtrNm_f32	1.89999998
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	26
t_AsstFWDefltAssistX_HwNm_u8p8[1]	51

TEST DETAILS REPORT

Name	Input Value
t_AsstFWDefltAssistX_HwNm_u8p8[2]	77
t_AsstFWDefltAssistX_HwNm_u8p8[3]	102
t_AsstFWDefltAssistX_HwNm_u8p8[4]	128
t_AsstFWDefltAssistX_HwNm_u8p8[5]	154
t_AsstFWDefltAssistX_HwNm_u8p8[6]	179
t_AsstFWDefltAssistX_HwNm_u8p8[7]	205
t_AsstFWDefltAssistX_HwNm_u8p8[8]	230
t_AsstFWDefltAssistX_HwNm_u8p8[9]	256
t_AsstFWDefltAssistX_HwNm_u8p8[10]	282
t_AsstFWDefltAssistX_HwNm_u8p8[11]	307
t_AsstFWDefltAssistX_HwNm_u8p8[12]	333
t_AsstFWDefltAssistX_HwNm_u8p8[13]	358
t_AsstFWDefltAssistX_HwNm_u8p8[14]	384
t_AsstFWDefltAssistX_HwNm_u8p8[15]	410
t_AsstFWDefltAssistX_HwNm_u8p8[16]	435
t_AsstFWDefltAssistX_HwNm_u8p8[17]	461
t_AsstFWDefltAssistX_HwNm_u8p8[18]	486
t_AsstFWDefltAssistX_HwNm_u8p8[19]	512
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	-184
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	-164
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	-143
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	-123
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	-102
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	-82
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	-61
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	-41
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	-20
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	0
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	20
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	41
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	61
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	82
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	102
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	123
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	143
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	164
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	184
t_AsstFWPstepNstepThresh_Cnt_u16[0]	0
t_AsstFWPstepNstepThresh_Cnt_u16[1]	0
t_AsstFWVehSpd_Kph_u9p7[0]	1408
t_AsstFWVehSpd_Kph_u9p7[1]	1536
t_AsstFWVehSpd_Kph_u9p7[2]	1664
t_AsstFWVehSpd_Kph_u9p7[3]	1792
t_AsstFWVehSpd_Kph_u9p7[4]	1920
t_AsstFWVehSpd_Kph_u9p7[5]	2048
t_AsstFWVehSpd_Kph_u9p7[6]	2176
t_AsstFWVehSpd_Kph_u9p7[7]	2304
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-8.80000019
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	9
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90.1999969
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.82099986	2.8210001 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0	0 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	0.08984375	0.08984375 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.9920001	1.99199998 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.2329998	5.2329998 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.11900008	1.11899996 ± 4.88E-04	✔

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	0.08984375	0.08984375 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.2 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0199999996
AssistFirewall_ActiveRawAcc_Cnt_M_u16	200
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.13
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00999999978
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.20000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00899999961
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00300000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.20000005
k_AsstFWInpLimitHFA_MtrNm_f32	1.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	3
k_AsstFWNstep_Cnt_u16	4796
k_AsstFWPstep_Cnt_u16	246
k_RestoreThresh_MtrNm_f32	1.20000005
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	51

TEST DETAILS REPORT

Name	Input Value
t_AsstFWDefltAssistX_HwNm_u8p8[1]	77
t_AsstFWDefltAssistX_HwNm_u8p8[2]	102
t_AsstFWDefltAssistX_HwNm_u8p8[3]	128
t_AsstFWDefltAssistX_HwNm_u8p8[4]	154
t_AsstFWDefltAssistX_HwNm_u8p8[5]	179
t_AsstFWDefltAssistX_HwNm_u8p8[6]	205
t_AsstFWDefltAssistX_HwNm_u8p8[7]	230
t_AsstFWDefltAssistX_HwNm_u8p8[8]	256
t_AsstFWDefltAssistX_HwNm_u8p8[9]	282
t_AsstFWDefltAssistX_HwNm_u8p8[10]	307
t_AsstFWDefltAssistX_HwNm_u8p8[11]	333
t_AsstFWDefltAssistX_HwNm_u8p8[12]	358
t_AsstFWDefltAssistX_HwNm_u8p8[13]	384
t_AsstFWDefltAssistX_HwNm_u8p8[14]	410
t_AsstFWDefltAssistX_HwNm_u8p8[15]	435
t_AsstFWDefltAssistX_HwNm_u8p8[16]	461
t_AsstFWDefltAssistX_HwNm_u8p8[17]	486
t_AsstFWDefltAssistX_HwNm_u8p8[18]	512
t_AsstFWDefltAssistX_HwNm_u8p8[19]	538
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	-143
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	-82
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	-20
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	41
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	102
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	164
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	225
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	287
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	348
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	410
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	471
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	532
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	594
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	655
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	717
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	778
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	840
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	901
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	963
t_AsstFWPstepNstepThresh_Cnt_u16[0]	123
t_AsstFWPstepNstepThresh_Cnt_u16[1]	211
t_AsstFWVehSpd_Kph_u9p7[0]	4352
t_AsstFWVehSpd_Kph_u9p7[1]	4480
t_AsstFWVehSpd_Kph_u9p7[2]	4608
t_AsstFWVehSpd_Kph_u9p7[3]	4736
t_AsstFWVehSpd_Kph_u9p7[4]	4864
t_AsstFWVehSpd_Kph_u9p7[5]	4992
t_AsstFWVehSpd_Kph_u9p7[6]	5120
t_AsstFWVehSpd_Kph_u9p7[7]	5248
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	8.80000019
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2.20000005
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	20.1000004
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.92000008	3.92000008 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	211	211 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	0.439941406	0.439941406 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.02399993	3.02399993 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.01800013	6.01800013 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.98199999	1.98199999 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	0.439941406	0.439941406 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.3 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0299999993
AssistFirewall_ActiveRawAcc_Cnt_M_u16	400
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.13999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0199999996
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.29999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00999999978
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00400000019
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.20000005
k_AsstFWInpLimitHFA_MtrNm_f32	1.39999998
k_AsstFWInpLimitHysComp_MtrNm_f32	4
k_AsstFWNstep_Cnt_u16	4672
k_AsstFWPstep_Cnt_u16	369
k_RestoreThresh_MtrNm_f32	1.29999995
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240

TEST DETAILS REPORT

Name	Input Value
t_AsstFWDefltAssistX_HwNm_u8p8[0]	77
t_AsstFWDefltAssistX_HwNm_u8p8[1]	102
t_AsstFWDefltAssistX_HwNm_u8p8[2]	128
t_AsstFWDefltAssistX_HwNm_u8p8[3]	154
t_AsstFWDefltAssistX_HwNm_u8p8[4]	179
t_AsstFWDefltAssistX_HwNm_u8p8[5]	205
t_AsstFWDefltAssistX_HwNm_u8p8[6]	230
t_AsstFWDefltAssistX_HwNm_u8p8[7]	256
t_AsstFWDefltAssistX_HwNm_u8p8[8]	282
t_AsstFWDefltAssistX_HwNm_u8p8[9]	307
t_AsstFWDefltAssistX_HwNm_u8p8[10]	333
t_AsstFWDefltAssistX_HwNm_u8p8[11]	358
t_AsstFWDefltAssistX_HwNm_u8p8[12]	384
t_AsstFWDefltAssistX_HwNm_u8p8[13]	410
t_AsstFWDefltAssistX_HwNm_u8p8[14]	435
t_AsstFWDefltAssistX_HwNm_u8p8[15]	461
t_AsstFWDefltAssistX_HwNm_u8p8[16]	486
t_AsstFWDefltAssistX_HwNm_u8p8[17]	512
t_AsstFWDefltAssistX_HwNm_u8p8[18]	538
t_AsstFWDefltAssistX_HwNm_u8p8[19]	563
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2458
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2662
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2867
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6349
t_AsstFWPstepNstepThresh_Cnt_u16[0]	124
t_AsstFWPstepNstepThresh_Cnt_u16[1]	215
t_AsstFWVehSpd_Kph_u9p7[0]	7296
t_AsstFWVehSpd_Kph_u9p7[1]	7424
t_AsstFWVehSpd_Kph_u9p7[2]	7552
t_AsstFWVehSpd_Kph_u9p7[3]	7680
t_AsstFWVehSpd_Kph_u9p7[4]	7808
t_AsstFWVehSpd_Kph_u9p7[5]	7936
t_AsstFWVehSpd_Kph_u9p7[6]	8064
t_AsstFWVehSpd_Kph_u9p7[7]	8192
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	0
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	30.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4.8499999	4.8499999 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	215	215 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.10009766	3.10009766 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0079999	4.0079999 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.01999998	7.01999998 ± 4.88E-04	✔

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.97600007	2.97600007 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.10009766	3.10009766 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.4 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0399999991
AssistFirewall_ActiveRawAcc_Cnt_M_u16	6500
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.14999998
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0299999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.39999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0199999996
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00499999989
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3
k_AsstFWInpLimitHFA_MtrNm_f32	1.5
k_AsstFWInpLimitHysComp_MtrNm_f32	1.10000002
k_AsstFWNstep_Cnt_u16	4548
k_AsstFWPstep_Cnt_u16	492
k_RestoreThresh_MtrNm_f32	1.39999998
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240

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Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	102
t_AsstFWDefltAssistX_HwNm_u8p8[1]	128
t_AsstFWDefltAssistX_HwNm_u8p8[2]	154
t_AsstFWDefltAssistX_HwNm_u8p8[3]	179
t_AsstFWDefltAssistX_HwNm_u8p8[4]	205
t_AsstFWDefltAssistX_HwNm_u8p8[5]	230
t_AsstFWDefltAssistX_HwNm_u8p8[6]	256
t_AsstFWDefltAssistX_HwNm_u8p8[7]	282
t_AsstFWDefltAssistX_HwNm_u8p8[8]	307
t_AsstFWDefltAssistX_HwNm_u8p8[9]	333
t_AsstFWDefltAssistX_HwNm_u8p8[10]	358
t_AsstFWDefltAssistX_HwNm_u8p8[11]	384
t_AsstFWDefltAssistX_HwNm_u8p8[12]	410
t_AsstFWDefltAssistX_HwNm_u8p8[13]	435
t_AsstFWDefltAssistX_HwNm_u8p8[14]	461
t_AsstFWDefltAssistX_HwNm_u8p8[15]	486
t_AsstFWDefltAssistX_HwNm_u8p8[16]	512
t_AsstFWDefltAssistX_HwNm_u8p8[17]	538
t_AsstFWDefltAssistX_HwNm_u8p8[18]	563
t_AsstFWDefltAssistX_HwNm_u8p8[19]	589
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2662
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2867
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6554
t_AsstFWPstepNstepThresh_Cnt_u16[0]	125
t_AsstFWPstepNstepThresh_Cnt_u16[1]	219
t_AsstFWVehSpd_Kph_u9p7[0]	10240
t_AsstFWVehSpd_Kph_u9p7[1]	10368
t_AsstFWVehSpd_Kph_u9p7[2]	10496
t_AsstFWVehSpd_Kph_u9p7[3]	10624
t_AsstFWVehSpd_Kph_u9p7[4]	10752
t_AsstFWVehSpd_Kph_u9p7[5]	10880
t_AsstFWVehSpd_Kph_u9p7[6]	11008
t_AsstFWVehSpd_Kph_u9p7[7]	11136
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.5
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	40.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.76000023	5.76000023 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	219	219 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.20019531	3.20019531 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.01800013	5.01800013 ± 4.88E-04	✔

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Name	Actual Value	Expected Value	Result
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8.03999996	8.03999996 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.97000003	3.97000003 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.20019531	3.20019531 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.5 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0500000007
AssistFirewall_ActiveRawAcc_Cnt_M_u16	800
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.15999997
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0399999991
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.5
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0299999993
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00600000005
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2
k_AsstFWInpLimitHFA_MtrNm_f32	1.70000005
k_AsstFWInpLimitHysComp_MtrNm_f32	2.0999999
k_AsstFWNstep_Cnt_u16	4424
k_AsstFWPstep_Cnt_u16	615
k_RestoreThresh_MtrNm_f32	1.5
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-28672

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	128
t_AsstFWDefltAssistX_HwNm_u8p8[1]	154
t_AsstFWDefltAssistX_HwNm_u8p8[2]	179
t_AsstFWDefltAssistX_HwNm_u8p8[3]	205
t_AsstFWDefltAssistX_HwNm_u8p8[4]	230
t_AsstFWDefltAssistX_HwNm_u8p8[5]	256
t_AsstFWDefltAssistX_HwNm_u8p8[6]	282
t_AsstFWDefltAssistX_HwNm_u8p8[7]	307
t_AsstFWDefltAssistX_HwNm_u8p8[8]	333
t_AsstFWDefltAssistX_HwNm_u8p8[9]	358
t_AsstFWDefltAssistX_HwNm_u8p8[10]	384
t_AsstFWDefltAssistX_HwNm_u8p8[11]	410
t_AsstFWDefltAssistX_HwNm_u8p8[12]	435
t_AsstFWDefltAssistX_HwNm_u8p8[13]	461
t_AsstFWDefltAssistX_HwNm_u8p8[14]	486
t_AsstFWDefltAssistX_HwNm_u8p8[15]	512
t_AsstFWDefltAssistX_HwNm_u8p8[16]	538
t_AsstFWDefltAssistX_HwNm_u8p8[17]	563
t_AsstFWDefltAssistX_HwNm_u8p8[18]	589
t_AsstFWDefltAssistX_HwNm_u8p8[19]	614
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2867
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6758
t_AsstFWPstepNstepThresh_Cnt_u16[0]	126
t_AsstFWPstepNstepThresh_Cnt_u16[1]	223
t_AsstFWVehSpd_Kph_u9p7[0]	13184
t_AsstFWVehSpd_Kph_u9p7[1]	13312
t_AsstFWVehSpd_Kph_u9p7[2]	13440
t_AsstFWVehSpd_Kph_u9p7[3]	13568
t_AsstFWVehSpd_Kph_u9p7[4]	13696
t_AsstFWVehSpd_Kph_u9p7[5]	13824
t_AsstFWVehSpd_Kph_u9p7[6]	13952
t_AsstFWVehSpd_Kph_u9p7[7]	14080
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.5
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	50.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.6500001	6.6500001 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	223	223 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.29980469	3.29980469 ± 4.88E-04	✔

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.83199978	5.83199978 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.39700007	1.39699996 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.96400023	4.96400023 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.29980469	3.29980469 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.6 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1000
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.16999996
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.60000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0399999991
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00700000022
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1
k_AsstFWInpLimitHFA_MtrNm_f32	1.89999998
k_AsstFWInpLimitHysComp_MtrNm_f32	2.5
k_AsstFWNstep_Cnt_u16	4300
k_AsstFWPstep_Cnt_u16	738
k_RestoreThresh_MtrNm_f32	1.60000002
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-28672

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	154
t_AsstFWDefltAssistX_HwNm_u8p8[1]	179
t_AsstFWDefltAssistX_HwNm_u8p8[2]	205
t_AsstFWDefltAssistX_HwNm_u8p8[3]	230
t_AsstFWDefltAssistX_HwNm_u8p8[4]	256
t_AsstFWDefltAssistX_HwNm_u8p8[5]	282
t_AsstFWDefltAssistX_HwNm_u8p8[6]	307
t_AsstFWDefltAssistX_HwNm_u8p8[7]	333
t_AsstFWDefltAssistX_HwNm_u8p8[8]	358
t_AsstFWDefltAssistX_HwNm_u8p8[9]	384
t_AsstFWDefltAssistX_HwNm_u8p8[10]	410
t_AsstFWDefltAssistX_HwNm_u8p8[11]	435
t_AsstFWDefltAssistX_HwNm_u8p8[12]	461
t_AsstFWDefltAssistX_HwNm_u8p8[13]	486
t_AsstFWDefltAssistX_HwNm_u8p8[14]	512
t_AsstFWDefltAssistX_HwNm_u8p8[15]	538
t_AsstFWDefltAssistX_HwNm_u8p8[16]	563
t_AsstFWDefltAssistX_HwNm_u8p8[17]	589
t_AsstFWDefltAssistX_HwNm_u8p8[18]	614
t_AsstFWDefltAssistX_HwNm_u8p8[19]	640
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6963
t_AsstFWPstepNstepThresh_Cnt_u16[0]	127
t_AsstFWPstepNstepThresh_Cnt_u16[1]	227
t_AsstFWVehSpd_Kph_u9p7[0]	16128
t_AsstFWVehSpd_Kph_u9p7[1]	16256
t_AsstFWVehSpd_Kph_u9p7[2]	16384
t_AsstFWVehSpd_Kph_u9p7[3]	16512
t_AsstFWVehSpd_Kph_u9p7[4]	16640
t_AsstFWVehSpd_Kph_u9p7[5]	16768
t_AsstFWVehSpd_Kph_u9p7[6]	16896
t_AsstFWVehSpd_Kph_u9p7[7]	17024
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-8.80000019
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	6
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	60.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7.51999998	7.51999998 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	227	227 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.39990234	3.39990234 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.73000002	6.73000002 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.51200008	2.51200008 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.95800018	5.95800018 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.39990234	3.39990234 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.7 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1000
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.17999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.60000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0399999991
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00700000022
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1
k_AsstFWInpLimitHFA_MtrNm_f32	1.89999998
k_AsstFWInpLimitHysComp_MtrNm_f32	2.5
k_AsstFWNstep_Cnt_u16	4300
k_AsstFWPstep_Cnt_u16	738
k_RestoreThresh_MtrNm_f32	1.70000005
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	179
t_AsstFWDefltAssistX_HwNm_u8p8[1]	205
t_AsstFWDefltAssistX_HwNm_u8p8[2]	230
t_AsstFWDefltAssistX_HwNm_u8p8[3]	256
t_AsstFWDefltAssistX_HwNm_u8p8[4]	282
t_AsstFWDefltAssistX_HwNm_u8p8[5]	307
t_AsstFWDefltAssistX_HwNm_u8p8[6]	333
t_AsstFWDefltAssistX_HwNm_u8p8[7]	358
t_AsstFWDefltAssistX_HwNm_u8p8[8]	384
t_AsstFWDefltAssistX_HwNm_u8p8[9]	410
t_AsstFWDefltAssistX_HwNm_u8p8[10]	435
t_AsstFWDefltAssistX_HwNm_u8p8[11]	461
t_AsstFWDefltAssistX_HwNm_u8p8[12]	486
t_AsstFWDefltAssistX_HwNm_u8p8[13]	512
t_AsstFWDefltAssistX_HwNm_u8p8[14]	538
t_AsstFWDefltAssistX_HwNm_u8p8[15]	563
t_AsstFWDefltAssistX_HwNm_u8p8[16]	589
t_AsstFWDefltAssistX_HwNm_u8p8[17]	614
t_AsstFWDefltAssistX_HwNm_u8p8[18]	640
t_AsstFWDefltAssistX_HwNm_u8p8[19]	666
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7168
t_AsstFWPstepNstepThresh_Cnt_u16[0]	128
t_AsstFWPstepNstepThresh_Cnt_u16[1]	231
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
t_AsstFWVehSpd_Kph_u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	8.80000019
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	6
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	60.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7.51999998	7.51999998 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	231	231 ± 1	✔

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.5	3.5 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.92000008	6.92000008 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.47200012	2.47199988 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.95800018	5.95800018 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.5	3.5 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.8 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0799999982
AssistFirewall_ActiveRawAcc_Cnt_M_u16	106
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.19000006
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0700000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00899999961
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3
k_AsstFWInpLimitHFA_MtrNm_f32	1.29999995
k_AsstFWInpLimitHysComp_MtrNm_f32	3.29999995
k_AsstFWNstep_Cnt_u16	4052
k_AsstFWPstep_Cnt_u16	984
k_RestoreThresh_MtrNm_f32	1.79999995
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	205
t_AsstFWDefltAssistX_HwNm_u8p8[1]	230
t_AsstFWDefltAssistX_HwNm_u8p8[2]	256
t_AsstFWDefltAssistX_HwNm_u8p8[3]	282
t_AsstFWDefltAssistX_HwNm_u8p8[4]	307
t_AsstFWDefltAssistX_HwNm_u8p8[5]	333
t_AsstFWDefltAssistX_HwNm_u8p8[6]	358
t_AsstFWDefltAssistX_HwNm_u8p8[7]	384
t_AsstFWDefltAssistX_HwNm_u8p8[8]	410
t_AsstFWDefltAssistX_HwNm_u8p8[9]	435
t_AsstFWDefltAssistX_HwNm_u8p8[10]	461
t_AsstFWDefltAssistX_HwNm_u8p8[11]	486
t_AsstFWDefltAssistX_HwNm_u8p8[12]	512
t_AsstFWDefltAssistX_HwNm_u8p8[13]	538
t_AsstFWDefltAssistX_HwNm_u8p8[14]	563
t_AsstFWDefltAssistX_HwNm_u8p8[15]	589
t_AsstFWDefltAssistX_HwNm_u8p8[16]	614
t_AsstFWDefltAssistX_HwNm_u8p8[17]	640
t_AsstFWDefltAssistX_HwNm_u8p8[18]	666
t_AsstFWDefltAssistX_HwNm_u8p8[19]	691
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7373
t_AsstFWPstepNstepThresh_Cnt_u16[0]	129
t_AsstFWPstepNstepThresh_Cnt_u16[1]	235
t_AsstFWVehSpd_Kph_u9p7[0]	22016
t_AsstFWVehSpd_Kph_u9p7[1]	22144
t_AsstFWVehSpd_Kph_u9p7[2]	22272
t_AsstFWVehSpd_Kph_u9p7[3]	22400
t_AsstFWVehSpd_Kph_u9p7[4]	22528
t_AsstFWVehSpd_Kph_u9p7[5]	22656
t_AsstFWVehSpd_Kph_u9p7[6]	22784
t_AsstFWVehSpd_Kph_u9p7[7]	22912
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	0
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	80.1999969
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.02400017	2.02399993 ± 4.88E-04	✔

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveRawAcc_Cnt_M_u16	235	235 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.60009766	3.60009766 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.46399999	1.46399999 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.33400011	4.33400011 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.9460001	7.9460001 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.60009766	3.60009766 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.9 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0900000036
AssistFirewall_ActiveRawAcc_Cnt_M_u16	109
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.89999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0700000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00999999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4
k_AsstFWInpLimitHFA_MtrNm_f32	2.5
k_AsstFWInpLimitHysComp_MtrNm_f32	3.78999996
k_AsstFWNstep_Cnt_u16	3928
k_AsstFWPstep_Cnt_u16	1107
k_RestoreThresh_MtrNm_f32	1.89999998
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	230
t_AsstFWDefltAssistX_HwNm_u8p8[1]	256
t_AsstFWDefltAssistX_HwNm_u8p8[2]	282
t_AsstFWDefltAssistX_HwNm_u8p8[3]	307
t_AsstFWDefltAssistX_HwNm_u8p8[4]	333
t_AsstFWDefltAssistX_HwNm_u8p8[5]	358
t_AsstFWDefltAssistX_HwNm_u8p8[6]	384
t_AsstFWDefltAssistX_HwNm_u8p8[7]	410
t_AsstFWDefltAssistX_HwNm_u8p8[8]	435
t_AsstFWDefltAssistX_HwNm_u8p8[9]	461
t_AsstFWDefltAssistX_HwNm_u8p8[10]	486
t_AsstFWDefltAssistX_HwNm_u8p8[11]	512
t_AsstFWDefltAssistX_HwNm_u8p8[12]	538
t_AsstFWDefltAssistX_HwNm_u8p8[13]	563
t_AsstFWDefltAssistX_HwNm_u8p8[14]	589
t_AsstFWDefltAssistX_HwNm_u8p8[15]	614
t_AsstFWDefltAssistX_HwNm_u8p8[16]	640
t_AsstFWDefltAssistX_HwNm_u8p8[17]	666
t_AsstFWDefltAssistX_HwNm_u8p8[18]	691
t_AsstFWDefltAssistX_HwNm_u8p8[19]	717
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7578
t_AsstFWPstepNstepThresh_Cnt_u16[0]	130
t_AsstFWPstepNstepThresh_Cnt_u16[1]	239
t_AsstFWVehSpd_Kph_u9p7[0]	24960
t_AsstFWVehSpd_Kph_u9p7[1]	25088
t_AsstFWVehSpd_Kph_u9p7[2]	25216
t_AsstFWVehSpd_Kph_u9p7[3]	25344
t_AsstFWVehSpd_Kph_u9p7[4]	25472
t_AsstFWVehSpd_Kph_u9p7[5]	25600
t_AsstFWVehSpd_Kph_u9p7[6]	25728
t_AsstFWVehSpd_Kph_u9p7[7]	25856
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.5
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	9
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90.0100021
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.82099986	2.8210001 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	239	239 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.70019531	3.70019531 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.63199997	2.63199997 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.2329998	5.2329998 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.11900008	1.11899996 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.70019531	3.70019531 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.10 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00999999978
AssistFirewall_ActiveRawAcc_Cnt_M_u16	112
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00899999961
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00800000038
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00200000009
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	2.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	4.28000021
k_AsstFWNstep_Cnt_u16	3804
k_AsstFWPstep_Cnt_u16	1230
k_RestoreThresh_MtrNm_f32	2
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-18432

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	256
t_AsstFWDefltAssistX_HwNm_u8p8[1]	282
t_AsstFWDefltAssistX_HwNm_u8p8[2]	307
t_AsstFWDefltAssistX_HwNm_u8p8[3]	333
t_AsstFWDefltAssistX_HwNm_u8p8[4]	358
t_AsstFWDefltAssistX_HwNm_u8p8[5]	384
t_AsstFWDefltAssistX_HwNm_u8p8[6]	410
t_AsstFWDefltAssistX_HwNm_u8p8[7]	435
t_AsstFWDefltAssistX_HwNm_u8p8[8]	461
t_AsstFWDefltAssistX_HwNm_u8p8[9]	486
t_AsstFWDefltAssistX_HwNm_u8p8[10]	512
t_AsstFWDefltAssistX_HwNm_u8p8[11]	538
t_AsstFWDefltAssistX_HwNm_u8p8[12]	563
t_AsstFWDefltAssistX_HwNm_u8p8[13]	589
t_AsstFWDefltAssistX_HwNm_u8p8[14]	614
t_AsstFWDefltAssistX_HwNm_u8p8[15]	640
t_AsstFWDefltAssistX_HwNm_u8p8[16]	666
t_AsstFWDefltAssistX_HwNm_u8p8[17]	691
t_AsstFWDefltAssistX_HwNm_u8p8[18]	717
t_AsstFWDefltAssistX_HwNm_u8p8[19]	742
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7782
t_AsstFWPstepNstepThresh_Cnt_u16[0]	131
t_AsstFWPstepNstepThresh_Cnt_u16[1]	243
t_AsstFWVehSpd_Kph_u9p7[0]	27904
t_AsstFWVehSpd_Kph_u9p7[1]	28032
t_AsstFWVehSpd_Kph_u9p7[2]	28160
t_AsstFWVehSpd_Kph_u9p7[3]	28288
t_AsstFWVehSpd_Kph_u9p7[4]	28416
t_AsstFWVehSpd_Kph_u9p7[5]	28544
t_AsstFWVehSpd_Kph_u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7]	28800
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.5
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	10.1999998
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.97000003	2.97000003 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	243	243 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.89990234	1.89990234 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.97660005	1.97660005 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0079999	5.0079999 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	0.987999976	0.987999976 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	1.89990234	1.89990234 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.11 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00600000005
AssistFirewall_ActiveRawAcc_Cnt_M_u16	115
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.29999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0599999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0900000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0299999993
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.4000001
k_AsstFWInpLimitHFA_MtrNm_f32	2.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	4.76999998
k_AsstFWNstep_Cnt_u16	3680
k_AsstFWPstep_Cnt_u16	1353
k_RestoreThresh_MtrNm_f32	2.0999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	4096

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	282
t_AsstFWDefltAssistX_HwNm_u8p8[1]	307
t_AsstFWDefltAssistX_HwNm_u8p8[2]	333
t_AsstFWDefltAssistX_HwNm_u8p8[3]	358
t_AsstFWDefltAssistX_HwNm_u8p8[4]	384
t_AsstFWDefltAssistX_HwNm_u8p8[5]	410
t_AsstFWDefltAssistX_HwNm_u8p8[6]	435
t_AsstFWDefltAssistX_HwNm_u8p8[7]	461
t_AsstFWDefltAssistX_HwNm_u8p8[8]	486
t_AsstFWDefltAssistX_HwNm_u8p8[9]	512
t_AsstFWDefltAssistX_HwNm_u8p8[10]	538
t_AsstFWDefltAssistX_HwNm_u8p8[11]	563
t_AsstFWDefltAssistX_HwNm_u8p8[12]	589
t_AsstFWDefltAssistX_HwNm_u8p8[13]	614
t_AsstFWDefltAssistX_HwNm_u8p8[14]	640
t_AsstFWDefltAssistX_HwNm_u8p8[15]	666
t_AsstFWDefltAssistX_HwNm_u8p8[16]	691
t_AsstFWDefltAssistX_HwNm_u8p8[17]	717
t_AsstFWDefltAssistX_HwNm_u8p8[18]	742
t_AsstFWDefltAssistX_HwNm_u8p8[19]	768
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7987
t_AsstFWPstepNstepThresh_Cnt_u16[0]	132
t_AsstFWPstepNstepThresh_Cnt_u16[1]	247
t_AsstFWVehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1]	30976
t_AsstFWVehSpd_Kph_u9p7[2]	31104
t_AsstFWVehSpd_Kph_u9p7[3]	31232
t_AsstFWVehSpd_Kph_u9p7[4]	31360
t_AsstFWVehSpd_Kph_u9p7[5]	31488
t_AsstFWVehSpd_Kph_u9p7[6]	31616
t_AsstFWVehSpd_Kph_u9p7[7]	31744
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-10
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	22.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.06939983	5.06939983 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	247	247 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.89990234	-3.89990234 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.25	4.25 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.459999979	0.460000008 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.85699987	2.85700011 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-3.89990234	-3.89990234 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.12 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00700000022
AssistFirewall_ActiveRawAcc_Cnt_M_u16	118
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.39999998
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00800000038
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.02999997
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00499999989
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0399999991
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.70000005
k_AsstFWInpLimitHFA_MtrNm_f32	2.5
k_AsstFWInpLimitHysComp_MtrNm_f32	5.26000023
k_AsstFWNstep_Cnt_u16	3556
k_AsstFWPstep_Cnt_u16	1476
k_RestoreThresh_MtrNm_f32	2.20000005
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefltAssistX_HwNm_u8p8[0]	307
t_AsstFWDefltAssistX_HwNm_u8p8[1]	333
t_AsstFWDefltAssistX_HwNm_u8p8[2]	358
t_AsstFWDefltAssistX_HwNm_u8p8[3]	384
t_AsstFWDefltAssistX_HwNm_u8p8[4]	410
t_AsstFWDefltAssistX_HwNm_u8p8[5]	435
t_AsstFWDefltAssistX_HwNm_u8p8[6]	461
t_AsstFWDefltAssistX_HwNm_u8p8[7]	486
t_AsstFWDefltAssistX_HwNm_u8p8[8]	512
t_AsstFWDefltAssistX_HwNm_u8p8[9]	538
t_AsstFWDefltAssistX_HwNm_u8p8[10]	563
t_AsstFWDefltAssistX_HwNm_u8p8[11]	589
t_AsstFWDefltAssistX_HwNm_u8p8[12]	614
t_AsstFWDefltAssistX_HwNm_u8p8[13]	640
t_AsstFWDefltAssistX_HwNm_u8p8[14]	666
t_AsstFWDefltAssistX_HwNm_u8p8[15]	691
t_AsstFWDefltAssistX_HwNm_u8p8[16]	717
t_AsstFWDefltAssistX_HwNm_u8p8[17]	742
t_AsstFWDefltAssistX_HwNm_u8p8[18]	768
t_AsstFWDefltAssistX_HwNm_u8p8[19]	794
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	8192
t_AsstFWPstepNstepThresh_Cnt_u16[0]	133
t_AsstFWPstepNstepThresh_Cnt_u16[1]	251
t_AsstFWVehSpd_Kph_u9p7[0]	33792
t_AsstFWVehSpd_Kph_u9p7[1]	33920
t_AsstFWVehSpd_Kph_u9p7[2]	34048
t_AsstFWVehSpd_Kph_u9p7[3]	34176
t_AsstFWVehSpd_Kph_u9p7[4]	34304
t_AsstFWVehSpd_Kph_u9p7[5]	34432
t_AsstFWVehSpd_Kph_u9p7[6]	34560
t_AsstFWVehSpd_Kph_u9p7[7]	34688
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2.20000005
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	10
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	33.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.05730009	6.05730009 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	251	251 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	4	4 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.13119984	5.13119984 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.00999999	2.00999999 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.17600012	4.17600012 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4	4 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.13 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00800000038
AssistFirewall_ActiveRawAcc_Cnt_M_u16	121
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00899999961
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.03999996
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00600000005
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0500000007
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3
k_AsstFWInpLimitHFA_MtrNm_f32	4.5
k_AsstFWInpLimitHysComp_MtrNm_f32	5.75
k_AsstFWNstep_Cnt_u16	3432
k_AsstFWPstep_Cnt_u16	1599
k_RestoreThresh_MtrNm_f32	2.29999995
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	333
t_AsstFWDefltAssistX_HwNm_u8p8[1]	358
t_AsstFWDefltAssistX_HwNm_u8p8[2]	384
t_AsstFWDefltAssistX_HwNm_u8p8[3]	410
t_AsstFWDefltAssistX_HwNm_u8p8[4]	435
t_AsstFWDefltAssistX_HwNm_u8p8[5]	461
t_AsstFWDefltAssistX_HwNm_u8p8[6]	486
t_AsstFWDefltAssistX_HwNm_u8p8[7]	512
t_AsstFWDefltAssistX_HwNm_u8p8[8]	538
t_AsstFWDefltAssistX_HwNm_u8p8[9]	563
t_AsstFWDefltAssistX_HwNm_u8p8[10]	589
t_AsstFWDefltAssistX_HwNm_u8p8[11]	614
t_AsstFWDefltAssistX_HwNm_u8p8[12]	640
t_AsstFWDefltAssistX_HwNm_u8p8[13]	666
t_AsstFWDefltAssistX_HwNm_u8p8[14]	691
t_AsstFWDefltAssistX_HwNm_u8p8[15]	717
t_AsstFWDefltAssistX_HwNm_u8p8[16]	742
t_AsstFWDefltAssistX_HwNm_u8p8[17]	768
t_AsstFWDefltAssistX_HwNm_u8p8[18]	794
t_AsstFWDefltAssistX_HwNm_u8p8[19]	819
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	8397
t_AsstFWPstepNstepThresh_Cnt_u16[0]	134
t_AsstFWPstepNstepThresh_Cnt_u16[1]	255
t_AsstFWVehSpd_Kph_u9p7[0]	36736
t_AsstFWVehSpd_Kph_u9p7[1]	36864
t_AsstFWVehSpd_Kph_u9p7[2]	36992
t_AsstFWVehSpd_Kph_u9p7[3]	37120
t_AsstFWVehSpd_Kph_u9p7[4]	37248
t_AsstFWVehSpd_Kph_u9p7[5]	37376
t_AsstFWVehSpd_Kph_u9p7[6]	37504
t_AsstFWVehSpd_Kph_u9p7[7]	37632
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	0
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	44.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	12288

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	0

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	358
t_AsstFWDefltAssistX_HwNm_u8p8[1]	384
t_AsstFWDefltAssistX_HwNm_u8p8[2]	410
t_AsstFWDefltAssistX_HwNm_u8p8[3]	435
t_AsstFWDefltAssistX_HwNm_u8p8[4]	461
t_AsstFWDefltAssistX_HwNm_u8p8[5]	486
t_AsstFWDefltAssistX_HwNm_u8p8[6]	512
t_AsstFWDefltAssistX_HwNm_u8p8[7]	538
t_AsstFWDefltAssistX_HwNm_u8p8[8]	563
t_AsstFWDefltAssistX_HwNm_u8p8[9]	589
t_AsstFWDefltAssistX_HwNm_u8p8[10]	614
t_AsstFWDefltAssistX_HwNm_u8p8[11]	640
t_AsstFWDefltAssistX_HwNm_u8p8[12]	666
t_AsstFWDefltAssistX_HwNm_u8p8[13]	691
t_AsstFWDefltAssistX_HwNm_u8p8[14]	717
t_AsstFWDefltAssistX_HwNm_u8p8[15]	742
t_AsstFWDefltAssistX_HwNm_u8p8[16]	768
t_AsstFWDefltAssistX_HwNm_u8p8[17]	794
t_AsstFWDefltAssistX_HwNm_u8p8[18]	819
t_AsstFWDefltAssistX_HwNm_u8p8[19]	845
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	8602
t_AsstFWPstepNstepThresh_Cnt_u16[0]	135
t_AsstFWPstepNstepThresh_Cnt_u16[1]	259
t_AsstFWVehSpd_Kph_u9p7[0]	39680
t_AsstFWVehSpd_Kph_u9p7[1]	39808
t_AsstFWVehSpd_Kph_u9p7[2]	39936
t_AsstFWVehSpd_Kph_u9p7[3]	40064
t_AsstFWVehSpd_Kph_u9p7[4]	40192
t_AsstFWVehSpd_Kph_u9p7[5]	40320
t_AsstFWVehSpd_Kph_u9p7[6]	40448
t_AsstFWVehSpd_Kph_u9p7[7]	40576
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5.5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	55.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.98199999	1.98199999 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	259	259 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.20019531	4.20019531 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.07500005	1.07500005 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.97550011	3.97550011 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.27399969	6.27400017 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4.20019531	4.20019531 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.15 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00999999978
AssistFirewall_ActiveRawAcc_Cnt_M_u16	127
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.70000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0199999996
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.05999994
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00800000038
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0700000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.5999999
k_AsstFWInpLimitHFA_MtrNm_f32	1.60000002
k_AsstFWInpLimitHysComp_MtrNm_f32	6.73000002
k_AsstFWNstep_Cnt_u16	3184
k_AsstFWPstep_Cnt_u16	1845
k_RestoreThresh_MtrNm_f32	2.5
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	14336

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	384
t_AsstFWDefltAssistX_HwNm_u8p8[1]	410
t_AsstFWDefltAssistX_HwNm_u8p8[2]	435
t_AsstFWDefltAssistX_HwNm_u8p8[3]	461
t_AsstFWDefltAssistX_HwNm_u8p8[4]	486
t_AsstFWDefltAssistX_HwNm_u8p8[5]	512
t_AsstFWDefltAssistX_HwNm_u8p8[6]	538
t_AsstFWDefltAssistX_HwNm_u8p8[7]	563
t_AsstFWDefltAssistX_HwNm_u8p8[8]	589
t_AsstFWDefltAssistX_HwNm_u8p8[9]	614
t_AsstFWDefltAssistX_HwNm_u8p8[10]	640
t_AsstFWDefltAssistX_HwNm_u8p8[11]	666
t_AsstFWDefltAssistX_HwNm_u8p8[12]	691
t_AsstFWDefltAssistX_HwNm_u8p8[13]	717
t_AsstFWDefltAssistX_HwNm_u8p8[14]	742
t_AsstFWDefltAssistX_HwNm_u8p8[15]	768
t_AsstFWDefltAssistX_HwNm_u8p8[16]	794
t_AsstFWDefltAssistX_HwNm_u8p8[17]	819
t_AsstFWDefltAssistX_HwNm_u8p8[18]	845
t_AsstFWDefltAssistX_HwNm_u8p8[19]	870
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	8806
t_AsstFWPstepNstepThresh_Cnt_u16[0]	136
t_AsstFWPstepNstepThresh_Cnt_u16[1]	263
t_AsstFWVehSpd_Kph_u9p7[0]	42624
t_AsstFWVehSpd_Kph_u9p7[1]	42752
t_AsstFWVehSpd_Kph_u9p7[2]	42880
t_AsstFWVehSpd_Kph_u9p7[3]	43008
t_AsstFWVehSpd_Kph_u9p7[4]	43136
t_AsstFWVehSpd_Kph_u9p7[5]	43264
t_AsstFWVehSpd_Kph_u9p7[6]	43392
t_AsstFWVehSpd_Kph_u9p7[7]	43520
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2.20000005
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.69999981
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	66.4000015
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	16384

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	410
t_AsstFWDefltAssistX_HwNm_u8p8[1]	435
t_AsstFWDefltAssistX_HwNm_u8p8[2]	461
t_AsstFWDefltAssistX_HwNm_u8p8[3]	486
t_AsstFWDefltAssistX_HwNm_u8p8[4]	512
t_AsstFWDefltAssistX_HwNm_u8p8[5]	538
t_AsstFWDefltAssistX_HwNm_u8p8[6]	563
t_AsstFWDefltAssistX_HwNm_u8p8[7]	589
t_AsstFWDefltAssistX_HwNm_u8p8[8]	614
t_AsstFWDefltAssistX_HwNm_u8p8[9]	640
t_AsstFWDefltAssistX_HwNm_u8p8[10]	666
t_AsstFWDefltAssistX_HwNm_u8p8[11]	691
t_AsstFWDefltAssistX_HwNm_u8p8[12]	717
t_AsstFWDefltAssistX_HwNm_u8p8[13]	742
t_AsstFWDefltAssistX_HwNm_u8p8[14]	768
t_AsstFWDefltAssistX_HwNm_u8p8[15]	794
t_AsstFWDefltAssistX_HwNm_u8p8[16]	819
t_AsstFWDefltAssistX_HwNm_u8p8[17]	845
t_AsstFWDefltAssistX_HwNm_u8p8[18]	870
t_AsstFWDefltAssistX_HwNm_u8p8[19]	896
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	9011
t_AsstFWPstepNstepThresh_Cnt_u16[0]	137
t_AsstFWPstepNstepThresh_Cnt_u16[1]	267
t_AsstFWVehSpd_Kph_u9p7[0]	45568
t_AsstFWVehSpd_Kph_u9p7[1]	45696
t_AsstFWVehSpd_Kph_u9p7[2]	45824
t_AsstFWVehSpd_Kph_u9p7[3]	45952
t_AsstFWVehSpd_Kph_u9p7[4]	46080
t_AsstFWVehSpd_Kph_u9p7[5]	46208
t_AsstFWVehSpd_Kph_u9p7[6]	46336
t_AsstFWVehSpd_Kph_u9p7[7]	46464
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-8.80000019
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	77.1999969
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.92000008	3.92000008 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	267	267 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-2.89990234	-2.89990234 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.01799989	3.01799989 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.8829999	5.8829999 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.07999992	2.07999992 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-2.89990234	-2.89990234 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.17 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0299999993
AssistFirewall_ActiveRawAcc_Cnt_M_u16	133
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.89999998
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0399999991
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.08000004
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00999999978
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0900000036
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.19999981
k_AsstFWInpLimitHFA_MtrNm_f32	2
k_AsstFWInpLimitHysComp_MtrNm_f32	1.70000005
k_AsstFWNstep_Cnt_u16	2936
k_AsstFWPstep_Cnt_u16	2091
k_RestoreThresh_MtrNm_f32	2.70000005
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	18432

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	8192

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	22528
t_AsstFWDefltAssistX_HwNm_u8p8[0]	435
t_AsstFWDefltAssistX_HwNm_u8p8[1]	461
t_AsstFWDefltAssistX_HwNm_u8p8[2]	486
t_AsstFWDefltAssistX_HwNm_u8p8[3]	512
t_AsstFWDefltAssistX_HwNm_u8p8[4]	538
t_AsstFWDefltAssistX_HwNm_u8p8[5]	563
t_AsstFWDefltAssistX_HwNm_u8p8[6]	589
t_AsstFWDefltAssistX_HwNm_u8p8[7]	614
t_AsstFWDefltAssistX_HwNm_u8p8[8]	640
t_AsstFWDefltAssistX_HwNm_u8p8[9]	666
t_AsstFWDefltAssistX_HwNm_u8p8[10]	691
t_AsstFWDefltAssistX_HwNm_u8p8[11]	717
t_AsstFWDefltAssistX_HwNm_u8p8[12]	742
t_AsstFWDefltAssistX_HwNm_u8p8[13]	768
t_AsstFWDefltAssistX_HwNm_u8p8[14]	794
t_AsstFWDefltAssistX_HwNm_u8p8[15]	819
t_AsstFWDefltAssistX_HwNm_u8p8[16]	845
t_AsstFWDefltAssistX_HwNm_u8p8[17]	870
t_AsstFWDefltAssistX_HwNm_u8p8[18]	896
t_AsstFWDefltAssistX_HwNm_u8p8[19]	922
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	9216
t_AsstFWPstepNstepThresh_Cnt_u16[0]	138
t_AsstFWPstepNstepThresh_Cnt_u16[1]	271
t_AsstFWVehSpd_Kph_u9p7[0]	27904
t_AsstFWVehSpd_Kph_u9p7[1]	28032
t_AsstFWVehSpd_Kph_u9p7[2]	28160
t_AsstFWVehSpd_Kph_u9p7[3]	28288
t_AsstFWVehSpd_Kph_u9p7[4]	28416
t_AsstFWVehSpd_Kph_u9p7[5]	28544
t_AsstFWVehSpd_Kph_u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7]	28800
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.80000019
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	88.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4.8499999	4.8499999 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	271	271 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.89990234	-3.89990234 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.11199999	4.11199999 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.8499999	6.8499999 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.91000009	2.91000009 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-3.89990234	-3.89990234 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.18 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0399999991
AssistFirewall_ActiveRawAcc_Cnt_M_u16	136
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.09000003
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0199999996
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.100000001
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.5
k_AsstFWInpLimitHFA_MtrNm_f32	2.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	2.0999999
k_AsstFWNstep_Cnt_u16	2812
k_AsstFWPstep_Cnt_u16	2214
k_RestoreThresh_MtrNm_f32	2.79999995
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	20480

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	10240

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576
t_AsstFWDefltAssistX_HwNm_u8p8[0]	461
t_AsstFWDefltAssistX_HwNm_u8p8[1]	486
t_AsstFWDefltAssistX_HwNm_u8p8[2]	512
t_AsstFWDefltAssistX_HwNm_u8p8[3]	538
t_AsstFWDefltAssistX_HwNm_u8p8[4]	563
t_AsstFWDefltAssistX_HwNm_u8p8[5]	589
t_AsstFWDefltAssistX_HwNm_u8p8[6]	614
t_AsstFWDefltAssistX_HwNm_u8p8[7]	640
t_AsstFWDefltAssistX_HwNm_u8p8[8]	666
t_AsstFWDefltAssistX_HwNm_u8p8[9]	691
t_AsstFWDefltAssistX_HwNm_u8p8[10]	717
t_AsstFWDefltAssistX_HwNm_u8p8[11]	742
t_AsstFWDefltAssistX_HwNm_u8p8[12]	768
t_AsstFWDefltAssistX_HwNm_u8p8[13]	794
t_AsstFWDefltAssistX_HwNm_u8p8[14]	819
t_AsstFWDefltAssistX_HwNm_u8p8[15]	845
t_AsstFWDefltAssistX_HwNm_u8p8[16]	870
t_AsstFWDefltAssistX_HwNm_u8p8[17]	896
t_AsstFWDefltAssistX_HwNm_u8p8[18]	922
t_AsstFWDefltAssistX_HwNm_u8p8[19]	947
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	9421
t_AsstFWPstepNstepThresh_Cnt_u16[0]	139
t_AsstFWPstepNstepThresh_Cnt_u16[1]	275
t_AsstFWVehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1]	30976
t_AsstFWVehSpd_Kph_u9p7[2]	31104
t_AsstFWVehSpd_Kph_u9p7[3]	31232
t_AsstFWVehSpd_Kph_u9p7[4]	31360
t_AsstFWVehSpd_Kph_u9p7[5]	31488
t_AsstFWVehSpd_Kph_u9p7[6]	31616
t_AsstFWVehSpd_Kph_u9p7[7]	31744
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	0
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	99.3000031
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.76000023	5.76000023 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	275	275 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.60009766	-4.60009766 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.07499981	5.07499981 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.65999985	7.65999985 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.9000001	3.9000001 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-4.60009766	-4.60009766 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.19 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0500000007
AssistFirewall_ActiveRawAcc_Cnt_M_u16	139
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0599999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0299999993
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.200000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.80000019
k_AsstFWInpLimitHFA_MtrNm_f32	2.4000001
k_AsstFWInpLimitHysComp_MtrNm_f32	2.43000007
k_AsstFWNstep_Cnt_u16	2688
k_AsstFWPstep_Cnt_u16	2337
k_RestoreThresh_MtrNm_f32	2.9000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	22528

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	12288

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	26624
t_AsstFWDefltAssistX_HwNm_u8p8[0]	486
t_AsstFWDefltAssistX_HwNm_u8p8[1]	512
t_AsstFWDefltAssistX_HwNm_u8p8[2]	538
t_AsstFWDefltAssistX_HwNm_u8p8[3]	563
t_AsstFWDefltAssistX_HwNm_u8p8[4]	589
t_AsstFWDefltAssistX_HwNm_u8p8[5]	614
t_AsstFWDefltAssistX_HwNm_u8p8[6]	640
t_AsstFWDefltAssistX_HwNm_u8p8[7]	666
t_AsstFWDefltAssistX_HwNm_u8p8[8]	691
t_AsstFWDefltAssistX_HwNm_u8p8[9]	717
t_AsstFWDefltAssistX_HwNm_u8p8[10]	742
t_AsstFWDefltAssistX_HwNm_u8p8[11]	768
t_AsstFWDefltAssistX_HwNm_u8p8[12]	794
t_AsstFWDefltAssistX_HwNm_u8p8[13]	819
t_AsstFWDefltAssistX_HwNm_u8p8[14]	845
t_AsstFWDefltAssistX_HwNm_u8p8[15]	870
t_AsstFWDefltAssistX_HwNm_u8p8[16]	896
t_AsstFWDefltAssistX_HwNm_u8p8[17]	922
t_AsstFWDefltAssistX_HwNm_u8p8[18]	947
t_AsstFWDefltAssistX_HwNm_u8p8[19]	973
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	9626
t_AsstFWPstepNstepThresh_Cnt_u16[0]	140
t_AsstFWPstepNstepThresh_Cnt_u16[1]	279
t_AsstFWVehSpd_Kph_u9p7[0]	33792
t_AsstFWVehSpd_Kph_u9p7[1]	33920
t_AsstFWVehSpd_Kph_u9p7[2]	34048
t_AsstFWVehSpd_Kph_u9p7[3]	34176
t_AsstFWVehSpd_Kph_u9p7[4]	34304
t_AsstFWVehSpd_Kph_u9p7[5]	34432
t_AsstFWVehSpd_Kph_u9p7[6]	34560
t_AsstFWVehSpd_Kph_u9p7[7]	34688
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	123.099998
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.6500001	6.6500001 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	279	279 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.70019531	-4.70019531 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.21780014	6.21780014 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.76700002	0.76700002 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.80000019	4.80000019 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-4.70019531	-4.70019531 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.20 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	142
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.29999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0700000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.20000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0399999991
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.300000012
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	2.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	2.77999997
k_AsstFWNstep_Cnt_u16	2564
k_AsstFWPstep_Cnt_u16	2460
k_RestoreThresh_MtrNm_f32	3
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	14336

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	512
t_AsstFWDefltAssistX_HwNm_u8p8[1]	538
t_AsstFWDefltAssistX_HwNm_u8p8[2]	563
t_AsstFWDefltAssistX_HwNm_u8p8[3]	589
t_AsstFWDefltAssistX_HwNm_u8p8[4]	614
t_AsstFWDefltAssistX_HwNm_u8p8[5]	640
t_AsstFWDefltAssistX_HwNm_u8p8[6]	666
t_AsstFWDefltAssistX_HwNm_u8p8[7]	691
t_AsstFWDefltAssistX_HwNm_u8p8[8]	717
t_AsstFWDefltAssistX_HwNm_u8p8[9]	742
t_AsstFWDefltAssistX_HwNm_u8p8[10]	768
t_AsstFWDefltAssistX_HwNm_u8p8[11]	794
t_AsstFWDefltAssistX_HwNm_u8p8[12]	819
t_AsstFWDefltAssistX_HwNm_u8p8[13]	845
t_AsstFWDefltAssistX_HwNm_u8p8[14]	870
t_AsstFWDefltAssistX_HwNm_u8p8[15]	896
t_AsstFWDefltAssistX_HwNm_u8p8[16]	922
t_AsstFWDefltAssistX_HwNm_u8p8[17]	947
t_AsstFWDefltAssistX_HwNm_u8p8[18]	973
t_AsstFWDefltAssistX_HwNm_u8p8[19]	998
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	9830
t_AsstFWPstepNstepThresh_Cnt_u16[0]	141
t_AsstFWPstepNstepThresh_Cnt_u16[1]	283
t_AsstFWVehSpd_Kph_u9p7[0]	36736
t_AsstFWVehSpd_Kph_u9p7[1]	36864
t_AsstFWVehSpd_Kph_u9p7[2]	36992
t_AsstFWVehSpd_Kph_u9p7[3]	37120
t_AsstFWVehSpd_Kph_u9p7[4]	37248
t_AsstFWVehSpd_Kph_u9p7[5]	37376
t_AsstFWVehSpd_Kph_u9p7[6]	37504
t_AsstFWVehSpd_Kph_u9p7[7]	37632
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-6
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	234.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7.51999998	7.51999998 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	283	283 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.79980469	-4.79980469 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.56739998	6.56739998 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.19200015	2.19199991 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.79999971	1.79999995 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-4.79980469	-4.79980469 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.21 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0700000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	123
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.39999998
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	8
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.29999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0500000007
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.400000006
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.4000001
k_AsstFWInpLimitHFA_MtrNm_f32	2.79999995
k_AsstFWInpLimitHysComp_MtrNm_f32	3.13000011
k_AsstFWNstep_Cnt_u16	2440
k_AsstFWPstep_Cnt_u16	2583
k_RestoreThresh_MtrNm_f32	3.0999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	0

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	538
t_AsstFWDefltAssistX_HwNm_u8p8[1]	563
t_AsstFWDefltAssistX_HwNm_u8p8[2]	589
t_AsstFWDefltAssistX_HwNm_u8p8[3]	614
t_AsstFWDefltAssistX_HwNm_u8p8[4]	640
t_AsstFWDefltAssistX_HwNm_u8p8[5]	666
t_AsstFWDefltAssistX_HwNm_u8p8[6]	691
t_AsstFWDefltAssistX_HwNm_u8p8[7]	717
t_AsstFWDefltAssistX_HwNm_u8p8[8]	742
t_AsstFWDefltAssistX_HwNm_u8p8[9]	768
t_AsstFWDefltAssistX_HwNm_u8p8[10]	794
t_AsstFWDefltAssistX_HwNm_u8p8[11]	819
t_AsstFWDefltAssistX_HwNm_u8p8[12]	845
t_AsstFWDefltAssistX_HwNm_u8p8[13]	870
t_AsstFWDefltAssistX_HwNm_u8p8[14]	896
t_AsstFWDefltAssistX_HwNm_u8p8[15]	922
t_AsstFWDefltAssistX_HwNm_u8p8[16]	947
t_AsstFWDefltAssistX_HwNm_u8p8[17]	973
t_AsstFWDefltAssistX_HwNm_u8p8[18]	998
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1024
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	10035
t_AsstFWPstepNstepThresh_Cnt_u16[0]	142
t_AsstFWPstepNstepThresh_Cnt_u16[1]	287
t_AsstFWVehSpd_Kph_u9p7[0]	39680
t_AsstFWVehSpd_Kph_u9p7[1]	39808
t_AsstFWVehSpd_Kph_u9p7[2]	39936
t_AsstFWVehSpd_Kph_u9p7[3]	40064
t_AsstFWVehSpd_Kph_u9p7[4]	40192
t_AsstFWVehSpd_Kph_u9p7[5]	40320
t_AsstFWVehSpd_Kph_u9p7[6]	40448
t_AsstFWVehSpd_Kph_u9p7[7]	40576
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-7
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	0
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.023	1.023 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	287	287 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.89990234	-4.89990234 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.90399981	7.90399981 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.79499984	2.79500008 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.19999981	2.20000005 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-4.89990234	-4.89990234 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.22 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0799999982
AssistFirewall_ActiveRawAcc_Cnt_M_u16	246
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0900000036
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.39999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.5
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.69999981
k_AsstFWInpLimitHFA_MtrNm_f32	3
k_AsstFWInpLimitHysComp_MtrNm_f32	3.48000002
k_AsstFWNstep_Cnt_u16	2316
k_AsstFWPstep_Cnt_u16	2706
k_RestoreThresh_MtrNm_f32	3.20000005
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	563
t_AsstFWDefltAssistX_HwNm_u8p8[1]	589
t_AsstFWDefltAssistX_HwNm_u8p8[2]	614
t_AsstFWDefltAssistX_HwNm_u8p8[3]	640
t_AsstFWDefltAssistX_HwNm_u8p8[4]	666
t_AsstFWDefltAssistX_HwNm_u8p8[5]	691
t_AsstFWDefltAssistX_HwNm_u8p8[6]	717
t_AsstFWDefltAssistX_HwNm_u8p8[7]	742
t_AsstFWDefltAssistX_HwNm_u8p8[8]	768
t_AsstFWDefltAssistX_HwNm_u8p8[9]	794
t_AsstFWDefltAssistX_HwNm_u8p8[10]	819
t_AsstFWDefltAssistX_HwNm_u8p8[11]	845
t_AsstFWDefltAssistX_HwNm_u8p8[12]	870
t_AsstFWDefltAssistX_HwNm_u8p8[13]	896
t_AsstFWDefltAssistX_HwNm_u8p8[14]	922
t_AsstFWDefltAssistX_HwNm_u8p8[15]	947
t_AsstFWDefltAssistX_HwNm_u8p8[16]	973
t_AsstFWDefltAssistX_HwNm_u8p8[17]	998
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1050
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	10240
t_AsstFWPstepNstepThresh_Cnt_u16[0]	143
t_AsstFWPstepNstepThresh_Cnt_u16[1]	291
t_AsstFWVehSpd_Kph_u9p7[0]	42624
t_AsstFWVehSpd_Kph_u9p7[1]	42752
t_AsstFWVehSpd_Kph_u9p7[2]	42880
t_AsstFWVehSpd_Kph_u9p7[3]	43008
t_AsstFWVehSpd_Kph_u9p7[4]	43136
t_AsstFWVehSpd_Kph_u9p7[5]	43264
t_AsstFWVehSpd_Kph_u9p7[6]	43392
t_AsstFWVehSpd_Kph_u9p7[7]	43520
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	255
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.02400017	2.02399993 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	291	291 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5	-5 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.81100011	1.81099999 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.61399984	3.61400008 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1	1 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-5	-5 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.23 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00600000005
AssistFirewall_ActiveRawAcc_Cnt_M_u16	369
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.60000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0599999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0900000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0299999993
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6
k_AsstFWInpLimitHFA_MtrNm_f32	3.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	3.82999992
k_AsstFWNstep_Cnt_u16	2192
k_AsstFWPstep_Cnt_u16	2829
k_RestoreThresh_MtrNm_f32	3.29999995
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	589
t_AsstFWDefltAssistX_HwNm_u8p8[1]	614
t_AsstFWDefltAssistX_HwNm_u8p8[2]	640
t_AsstFWDefltAssistX_HwNm_u8p8[3]	666
t_AsstFWDefltAssistX_HwNm_u8p8[4]	691
t_AsstFWDefltAssistX_HwNm_u8p8[5]	717
t_AsstFWDefltAssistX_HwNm_u8p8[6]	742
t_AsstFWDefltAssistX_HwNm_u8p8[7]	768
t_AsstFWDefltAssistX_HwNm_u8p8[8]	794
t_AsstFWDefltAssistX_HwNm_u8p8[9]	819
t_AsstFWDefltAssistX_HwNm_u8p8[10]	845
t_AsstFWDefltAssistX_HwNm_u8p8[11]	870
t_AsstFWDefltAssistX_HwNm_u8p8[12]	896
t_AsstFWDefltAssistX_HwNm_u8p8[13]	922
t_AsstFWDefltAssistX_HwNm_u8p8[14]	947
t_AsstFWDefltAssistX_HwNm_u8p8[15]	973
t_AsstFWDefltAssistX_HwNm_u8p8[16]	998
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1075
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	10445
t_AsstFWPstepNstepThresh_Cnt_u16[0]	144
t_AsstFWPstepNstepThresh_Cnt_u16[1]	295
t_AsstFWVehSpd_Kph_u9p7[0]	45568
t_AsstFWVehSpd_Kph_u9p7[1]	45696
t_AsstFWVehSpd_Kph_u9p7[2]	45824
t_AsstFWVehSpd_Kph_u9p7[3]	45952
t_AsstFWVehSpd_Kph_u9p7[4]	46080
t_AsstFWVehSpd_Kph_u9p7[5]	46208
t_AsstFWVehSpd_Kph_u9p7[6]	46336
t_AsstFWVehSpd_Kph_u9p7[7]	46464
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-10
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	22.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.06939983	5.06939983 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	295	295 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.10009766	-5.10009766 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.46600008	4.46600008 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.459999979	0.460000008 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.85699987	2.85700011 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-5.10009766	-5.10009766 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.24 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	492
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.70000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00899999961
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.60000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0799999982
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0599999987
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6.30000019
k_AsstFWInpLimitHFA_MtrNm_f32	3.4000001
k_AsstFWInpLimitHysComp_MtrNm_f32	4.17999983
k_AsstFWNstep_Cnt_u16	2068
k_AsstFWPstep_Cnt_u16	2952
k_RestoreThresh_MtrNm_f32	3.4000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	6144

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefltAssistX_HwNm_u8p8[0]	614
t_AsstFWDefltAssistX_HwNm_u8p8[1]	640
t_AsstFWDefltAssistX_HwNm_u8p8[2]	666
t_AsstFWDefltAssistX_HwNm_u8p8[3]	691
t_AsstFWDefltAssistX_HwNm_u8p8[4]	717
t_AsstFWDefltAssistX_HwNm_u8p8[5]	742
t_AsstFWDefltAssistX_HwNm_u8p8[6]	768
t_AsstFWDefltAssistX_HwNm_u8p8[7]	794
t_AsstFWDefltAssistX_HwNm_u8p8[8]	819
t_AsstFWDefltAssistX_HwNm_u8p8[9]	845
t_AsstFWDefltAssistX_HwNm_u8p8[10]	870
t_AsstFWDefltAssistX_HwNm_u8p8[11]	896
t_AsstFWDefltAssistX_HwNm_u8p8[12]	922
t_AsstFWDefltAssistX_HwNm_u8p8[13]	947
t_AsstFWDefltAssistX_HwNm_u8p8[14]	973
t_AsstFWDefltAssistX_HwNm_u8p8[15]	998
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1101
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	10650
t_AsstFWPstepNstepThresh_Cnt_u16[0]	145
t_AsstFWPstepNstepThresh_Cnt_u16[1]	299
t_AsstFWVehSpd_Kph_u9p7[0]	0
t_AsstFWVehSpd_Kph_u9p7[1]	0
t_AsstFWVehSpd_Kph_u9p7[2]	0
t_AsstFWVehSpd_Kph_u9p7[3]	0
t_AsstFWVehSpd_Kph_u9p7[4]	0
t_AsstFWVehSpd_Kph_u9p7[5]	0
t_AsstFWVehSpd_Kph_u9p7[6]	0
t_AsstFWVehSpd_Kph_u9p7[7]	0
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	10.1999998
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.85399985	3.85400009 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	299	299 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.29980469	3.29980469 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.17559981	3.17560005 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.61199999	5.61199999 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.18799996	2.18799996 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.29980469	3.29980469 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.25 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00800000038
AssistFirewall_ActiveRawAcc_Cnt_M_u16	615
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.79999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00999999978
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.70000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0900000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0700000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6.5999999
k_AsstFWInpLimitHFA_MtrNm_f32	3.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	4.53000021
k_AsstFWNstep_Cnt_u16	1944
k_AsstFWPstep_Cnt_u16	3075
k_RestoreThresh_MtrNm_f32	3.5
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	640
t_AsstFWDefltAssistX_HwNm_u8p8[1]	666
t_AsstFWDefltAssistX_HwNm_u8p8[2]	691
t_AsstFWDefltAssistX_HwNm_u8p8[3]	717
t_AsstFWDefltAssistX_HwNm_u8p8[4]	742
t_AsstFWDefltAssistX_HwNm_u8p8[5]	768
t_AsstFWDefltAssistX_HwNm_u8p8[6]	794
t_AsstFWDefltAssistX_HwNm_u8p8[7]	819
t_AsstFWDefltAssistX_HwNm_u8p8[8]	845
t_AsstFWDefltAssistX_HwNm_u8p8[9]	870
t_AsstFWDefltAssistX_HwNm_u8p8[10]	896
t_AsstFWDefltAssistX_HwNm_u8p8[11]	922
t_AsstFWDefltAssistX_HwNm_u8p8[12]	947
t_AsstFWDefltAssistX_HwNm_u8p8[13]	973
t_AsstFWDefltAssistX_HwNm_u8p8[14]	998
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1126
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	10854
t_AsstFWPstepNstepThresh_Cnt_u16[0]	146
t_AsstFWPstepNstepThresh_Cnt_u16[1]	303
t_AsstFWVehSpd_Kph_u9p7[0]	65408
t_AsstFWVehSpd_Kph_u9p7[1]	65408
t_AsstFWVehSpd_Kph_u9p7[2]	65408
t_AsstFWVehSpd_Kph_u9p7[3]	65408
t_AsstFWVehSpd_Kph_u9p7[4]	65408
t_AsstFWVehSpd_Kph_u9p7[5]	65408
t_AsstFWVehSpd_Kph_u9p7[6]	65408
t_AsstFWVehSpd_Kph_u9p7[7]	65408
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	20.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.05919981	5.05919981 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	303	303 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.39990234	3.39990234 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.17000008	4.17000008 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.63999987	4.63999987 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.09299994	3.09299994 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.39990234	3.39990234 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.26 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00899999961
AssistFirewall_ActiveRawAcc_Cnt_M_u16	738
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.89999998
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0199999996
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0799999982
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6.9000001
k_AsstFWInpLimitHFA_MtrNm_f32	3.79999995
k_AsstFWInpLimitHysComp_MtrNm_f32	4.88000011
k_AsstFWNstep_Cnt_u16	1820
k_AsstFWPstep_Cnt_u16	3198
k_RestoreThresh_MtrNm_f32	3.5999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	0

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	666
t_AsstFWDefltAssistX_HwNm_u8p8[1]	691
t_AsstFWDefltAssistX_HwNm_u8p8[2]	717
t_AsstFWDefltAssistX_HwNm_u8p8[3]	742
t_AsstFWDefltAssistX_HwNm_u8p8[4]	768
t_AsstFWDefltAssistX_HwNm_u8p8[5]	794
t_AsstFWDefltAssistX_HwNm_u8p8[6]	819
t_AsstFWDefltAssistX_HwNm_u8p8[7]	845
t_AsstFWDefltAssistX_HwNm_u8p8[8]	870
t_AsstFWDefltAssistX_HwNm_u8p8[9]	896
t_AsstFWDefltAssistX_HwNm_u8p8[10]	922
t_AsstFWDefltAssistX_HwNm_u8p8[11]	947
t_AsstFWDefltAssistX_HwNm_u8p8[12]	973
t_AsstFWDefltAssistX_HwNm_u8p8[13]	998
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1152
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	11059
t_AsstFWPstepNstepThresh_Cnt_u16[0]	147
t_AsstFWPstepNstepThresh_Cnt_u16[1]	307
t_AsstFWVehSpd_Kph_u9p7[0]	12800
t_AsstFWVehSpd_Kph_u9p7[1]	12800
t_AsstFWVehSpd_Kph_u9p7[2]	12800
t_AsstFWVehSpd_Kph_u9p7[3]	12800
t_AsstFWVehSpd_Kph_u9p7[4]	12800
t_AsstFWVehSpd_Kph_u9p7[5]	12800
t_AsstFWVehSpd_Kph_u9p7[6]	12800
t_AsstFWVehSpd_Kph_u9p7[7]	12800
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	0.78125
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.04509974	6.04510021 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	307	307 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.89990234	3.89990234 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.2736001	5.2736001 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.69999981	5.69999981 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.17199993	4.17199993 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.89990234	3.89990234 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.27 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00999999978
AssistFirewall_ActiveRawAcc_Cnt_M_u16	861
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-2.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0299999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.89999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00800000038
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0900000036
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	7.19999981
k_AsstFWInpLimitHFA_MtrNm_f32	4
k_AsstFWInpLimitHysComp_MtrNm_f32	5.23000002
k_AsstFWNstep_Cnt_u16	1696
k_AsstFWPstep_Cnt_u16	3321
k_RestoreThresh_MtrNm_f32	3.70000005
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-20480

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	14336

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	691
t_AsstFWDefltAssistX_HwNm_u8p8[1]	717
t_AsstFWDefltAssistX_HwNm_u8p8[2]	742
t_AsstFWDefltAssistX_HwNm_u8p8[3]	768
t_AsstFWDefltAssistX_HwNm_u8p8[4]	794
t_AsstFWDefltAssistX_HwNm_u8p8[5]	819
t_AsstFWDefltAssistX_HwNm_u8p8[6]	845
t_AsstFWDefltAssistX_HwNm_u8p8[7]	870
t_AsstFWDefltAssistX_HwNm_u8p8[8]	896
t_AsstFWDefltAssistX_HwNm_u8p8[9]	922
t_AsstFWDefltAssistX_HwNm_u8p8[10]	947
t_AsstFWDefltAssistX_HwNm_u8p8[11]	973
t_AsstFWDefltAssistX_HwNm_u8p8[12]	998
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1178
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	11264
t_AsstFWPstepNstepThresh_Cnt_u16[0]	148
t_AsstFWPstepNstepThresh_Cnt_u16[1]	311
t_AsstFWVehSpd_Kph_u9p7[0]	1408
t_AsstFWVehSpd_Kph_u9p7[1]	1536
t_AsstFWVehSpd_Kph_u9p7[2]	1664
t_AsstFWVehSpd_Kph_u9p7[3]	1792
t_AsstFWVehSpd_Kph_u9p7[4]	1920
t_AsstFWVehSpd_Kph_u9p7[5]	2048
t_AsstFWVehSpd_Kph_u9p7[6]	2176
t_AsstFWVehSpd_Kph_u9p7[7]	2304
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	40.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.96000004	3.96000004 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	311	311 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.89990234	4.89990234 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.37989998	6.37989998 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.96799994	6.96799994 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.37099981	4.37099981 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4.89990234	4.89990234 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.28 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0199999996
AssistFirewall_ActiveRawAcc_Cnt_M_u16	984
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0399999991
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00899999961
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.100000001
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	7.5
k_AsstFWInpLimitHFA_MtrNm_f32	4.19999981
k_AsstFWInpLimitHysComp_MtrNm_f32	5.57999992
k_AsstFWNstep_Cnt_u16	1572
k_AsstFWPstep_Cnt_u16	3444
k_RestoreThresh_MtrNm_f32	3.79999995
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	20480

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	16384

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	717
t_AsstFWDefltAssistX_HwNm_u8p8[1]	742
t_AsstFWDefltAssistX_HwNm_u8p8[2]	768
t_AsstFWDefltAssistX_HwNm_u8p8[3]	794
t_AsstFWDefltAssistX_HwNm_u8p8[4]	819
t_AsstFWDefltAssistX_HwNm_u8p8[5]	845
t_AsstFWDefltAssistX_HwNm_u8p8[6]	870
t_AsstFWDefltAssistX_HwNm_u8p8[7]	896
t_AsstFWDefltAssistX_HwNm_u8p8[8]	922
t_AsstFWDefltAssistX_HwNm_u8p8[9]	947
t_AsstFWDefltAssistX_HwNm_u8p8[10]	973
t_AsstFWDefltAssistX_HwNm_u8p8[11]	998
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1203
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	11469
t_AsstFWPstepNstepThresh_Cnt_u16[0]	149
t_AsstFWPstepNstepThresh_Cnt_u16[1]	315
t_AsstFWVehSpd_Kph_u9p7[0]	4352
t_AsstFWVehSpd_Kph_u9p7[1]	4480
t_AsstFWVehSpd_Kph_u9p7[2]	4608
t_AsstFWVehSpd_Kph_u9p7[3]	4736
t_AsstFWVehSpd_Kph_u9p7[4]	4864
t_AsstFWVehSpd_Kph_u9p7[5]	4992
t_AsstFWVehSpd_Kph_u9p7[6]	5120
t_AsstFWVehSpd_Kph_u9p7[7]	5248
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	50.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4.9000001	4.9000001 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	315	315 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.60009766	5.60009766 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.08400011	4.08400011 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.9369998	7.9369998 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.38999987	5.38999987 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	5.60009766	5.60009766 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.29 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0299999993
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1107
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-2.29999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00999999978
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.200000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	7.80000019
k_AsstFWInpLimitHFA_MtrNm_f32	4.4000001
k_AsstFWInpLimitHysComp_MtrNm_f32	5.92999983
k_AsstFWNstep_Cnt_u16	1448
k_AsstFWPstep_Cnt_u16	3567
k_RestoreThresh_MtrNm_f32	3.9000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	18432

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	14336

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	742
t_AsstFWDefltAssistX_HwNm_u8p8[1]	768
t_AsstFWDefltAssistX_HwNm_u8p8[2]	794
t_AsstFWDefltAssistX_HwNm_u8p8[3]	819
t_AsstFWDefltAssistX_HwNm_u8p8[4]	845
t_AsstFWDefltAssistX_HwNm_u8p8[5]	870
t_AsstFWDefltAssistX_HwNm_u8p8[6]	896
t_AsstFWDefltAssistX_HwNm_u8p8[7]	922
t_AsstFWDefltAssistX_HwNm_u8p8[8]	947
t_AsstFWDefltAssistX_HwNm_u8p8[9]	973
t_AsstFWDefltAssistX_HwNm_u8p8[10]	998
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1229
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	11674
t_AsstFWPstepNstepThresh_Cnt_u16[0]	150
t_AsstFWPstepNstepThresh_Cnt_u16[1]	319
t_AsstFWVehSpd_Kph_u9p7[0]	7296
t_AsstFWVehSpd_Kph_u9p7[1]	7424
t_AsstFWVehSpd_Kph_u9p7[2]	7552
t_AsstFWVehSpd_Kph_u9p7[3]	7680
t_AsstFWVehSpd_Kph_u9p7[4]	7808
t_AsstFWVehSpd_Kph_u9p7[5]	7936
t_AsstFWVehSpd_Kph_u9p7[6]	8064
t_AsstFWVehSpd_Kph_u9p7[7]	8192
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2.20000005
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-6
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	60.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.82000017	5.82000017 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	319	319 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.70019531	-5.70019531 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.17999983	5.17999983 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.199	1.199 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1	1 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-5.70019531	-5.70019531 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.30 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0399999991
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1230
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-2.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0599999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.02999997
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0199999996
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.300000012
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	8.10000038
k_AsstFWInpLimitHFA_MtrNm_f32	4.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	6.28000021
k_AsstFWNstep_Cnt_u16	1324
k_AsstFWPstep_Cnt_u16	3690
k_RestoreThresh_MtrNm_f32	4
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	768
t_AsstFWDefltAssistX_HwNm_u8p8[1]	794
t_AsstFWDefltAssistX_HwNm_u8p8[2]	819
t_AsstFWDefltAssistX_HwNm_u8p8[3]	845
t_AsstFWDefltAssistX_HwNm_u8p8[4]	870
t_AsstFWDefltAssistX_HwNm_u8p8[5]	896
t_AsstFWDefltAssistX_HwNm_u8p8[6]	922
t_AsstFWDefltAssistX_HwNm_u8p8[7]	947
t_AsstFWDefltAssistX_HwNm_u8p8[8]	973
t_AsstFWDefltAssistX_HwNm_u8p8[9]	998
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1254
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	11878
t_AsstFWPstepNstepThresh_Cnt_u16[0]	151
t_AsstFWPstepNstepThresh_Cnt_u16[1]	323
t_AsstFWVehSpd_Kph_u9p7[0]	10240
t_AsstFWVehSpd_Kph_u9p7[1]	10368
t_AsstFWVehSpd_Kph_u9p7[2]	10496
t_AsstFWVehSpd_Kph_u9p7[3]	10624
t_AsstFWVehSpd_Kph_u9p7[4]	10752
t_AsstFWVehSpd_Kph_u9p7[5]	10880
t_AsstFWVehSpd_Kph_u9p7[6]	11008
t_AsstFWVehSpd_Kph_u9p7[7]	11136
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-7
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	70.1999969
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.71999979	6.71999979 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	323	323 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.79980469	-5.79980469 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.28200006	6.28200006 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.09599996	2.09599996 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.29999995	2.29999995 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-5.79980469	-5.79980469 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.31 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0500000007
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1353
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-2.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0700000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.03999996
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0299999993
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.400000006
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	8.39999962
k_AsstFWInpLimitHFA_MtrNm_f32	4.80000019
k_AsstFWInpLimitHysComp_MtrNm_f32	6.63000011
k_AsstFWNstep_Cnt_u16	1200
k_AsstFWPstep_Cnt_u16	3813
k_RestoreThresh_MtrNm_f32	4.0999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-20480

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	794
t_AsstFWDefltAssistX_HwNm_u8p8[1]	819
t_AsstFWDefltAssistX_HwNm_u8p8[2]	845
t_AsstFWDefltAssistX_HwNm_u8p8[3]	870
t_AsstFWDefltAssistX_HwNm_u8p8[4]	896
t_AsstFWDefltAssistX_HwNm_u8p8[5]	922
t_AsstFWDefltAssistX_HwNm_u8p8[6]	947
t_AsstFWDefltAssistX_HwNm_u8p8[7]	973
t_AsstFWDefltAssistX_HwNm_u8p8[8]	998
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1280
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	12083
t_AsstFWPstepNstepThresh_Cnt_u16[0]	152
t_AsstFWPstepNstepThresh_Cnt_u16[1]	327
t_AsstFWVehSpd_Kph_u9p7[0]	13184
t_AsstFWVehSpd_Kph_u9p7[1]	13312
t_AsstFWVehSpd_Kph_u9p7[2]	13440
t_AsstFWVehSpd_Kph_u9p7[3]	13568
t_AsstFWVehSpd_Kph_u9p7[4]	13696
t_AsstFWVehSpd_Kph_u9p7[5]	13824
t_AsstFWVehSpd_Kph_u9p7[6]	13952
t_AsstFWVehSpd_Kph_u9p7[7]	14080
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	80.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7.5999999	7.5999999 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	327	327 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.89990234	-5.89990234 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.41300011	7.41300011 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.8269999	2.8269999 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.20000005	3.20000005 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-5.89990234	-5.89990234 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.32 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1476
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-2.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	8
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.04999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0399999991
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.5
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2
k_AsstFWInpLimitHFA_MtrNm_f32	5
k_AsstFWInpLimitHysComp_MtrNm_f32	0.200000003
k_AsstFWNstep_Cnt_u16	1076
k_AsstFWPstep_Cnt_u16	3936
k_RestoreThresh_MtrNm_f32	4.19999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-32768

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-32768

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	-32768
t_AsstFWDefltAssistX_HwNm_u8p8[0]	819
t_AsstFWDefltAssistX_HwNm_u8p8[1]	845
t_AsstFWDefltAssistX_HwNm_u8p8[2]	870
t_AsstFWDefltAssistX_HwNm_u8p8[3]	896
t_AsstFWDefltAssistX_HwNm_u8p8[4]	922
t_AsstFWDefltAssistX_HwNm_u8p8[5]	947
t_AsstFWDefltAssistX_HwNm_u8p8[6]	973
t_AsstFWDefltAssistX_HwNm_u8p8[7]	998
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1306
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	12288
t_AsstFWPstepNstepThresh_Cnt_u16[0]	153
t_AsstFWPstepNstepThresh_Cnt_u16[1]	331
t_AsstFWVehSpd_Kph_u9p7[0]	16128
t_AsstFWVehSpd_Kph_u9p7[1]	16256
t_AsstFWVehSpd_Kph_u9p7[2]	16384
t_AsstFWVehSpd_Kph_u9p7[3]	16512
t_AsstFWVehSpd_Kph_u9p7[4]	16640
t_AsstFWVehSpd_Kph_u9p7[5]	16768
t_AsstFWVehSpd_Kph_u9p7[6]	16896
t_AsstFWVehSpd_Kph_u9p7[7]	17024
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-9
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90.1999969
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.03400004	1.03400004 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	331	331 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6	-6 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.93599987	7.93599987 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.57599974	4.57600021 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-4.5	-4.5 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-6	-6 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.33 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0700000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1599
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-2.70000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0900000036
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.05999994
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0500000007
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.600000024
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1
k_AsstFWInpLimitHFA_MtrNm_f32	5.19999981
k_AsstFWInpLimitHysComp_MtrNm_f32	0.230000004
k_AsstFWNstep_Cnt_u16	952
k_AsstFWPstep_Cnt_u16	4059
k_RestoreThresh_MtrNm_f32	4.30000019
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	32767

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	32767

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	32767
t_AsstFWDefltAssistX_HwNm_u8p8[0]	845
t_AsstFWDefltAssistX_HwNm_u8p8[1]	870
t_AsstFWDefltAssistX_HwNm_u8p8[2]	896
t_AsstFWDefltAssistX_HwNm_u8p8[3]	922
t_AsstFWDefltAssistX_HwNm_u8p8[4]	947
t_AsstFWDefltAssistX_HwNm_u8p8[5]	973
t_AsstFWDefltAssistX_HwNm_u8p8[6]	998
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1331
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	8602
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	12493
t_AsstFWPstepNstepThresh_Cnt_u16[0]	154
t_AsstFWPstepNstepThresh_Cnt_u16[1]	335
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
t_AsstFWVehSpd_Kph_u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	11.3000002
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.046	2.046 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	335	335 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.20019531	4.20019531 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.21070004	1.21070004 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.04502439	4.04502439 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	12.7997074	12.7997074 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4.20019531	4.20019531 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.34 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0799999982
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1722
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-2.79999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00800000038
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.07000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0599999987
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.10000002
k_AsstFWInpLimitHFA_MtrNm_f32	5.4000001
k_AsstFWInpLimitHysComp_MtrNm_f32	0.430000007
k_AsstFWNstep_Cnt_u16	828
k_AsstFWPstep_Cnt_u16	4182
k_RestoreThresh_MtrNm_f32	4.4000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	0

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	0

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	0
t_AsstFWDefltAssistX_HwNm_u8p8[0]	870
t_AsstFWDefltAssistX_HwNm_u8p8[1]	896
t_AsstFWDefltAssistX_HwNm_u8p8[2]	922
t_AsstFWDefltAssistX_HwNm_u8p8[3]	947
t_AsstFWDefltAssistX_HwNm_u8p8[4]	973
t_AsstFWDefltAssistX_HwNm_u8p8[5]	998
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1357
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	12698
t_AsstFWPstepNstepThresh_Cnt_u16[0]	155
t_AsstFWPstepNstepThresh_Cnt_u16[1]	339
t_AsstFWVehSpd_Kph_u9p7[0]	22016
t_AsstFWVehSpd_Kph_u9p7[1]	22144
t_AsstFWVehSpd_Kph_u9p7[2]	22272
t_AsstFWVehSpd_Kph_u9p7[3]	22400
t_AsstFWVehSpd_Kph_u9p7[4]	22528
t_AsstFWVehSpd_Kph_u9p7[5]	22656
t_AsstFWVehSpd_Kph_u9p7[6]	22784
t_AsstFWVehSpd_Kph_u9p7[7]	22912
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	22.1000004
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.68000007	3.68000007 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	339	339 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.29980469	-4.29980469 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.21864009	2.21864009 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.73399973	5.73400021 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.03400004	1.03400004 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-4.29980469	-4.29980469 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.35 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0900000036
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1845
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-2.9000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00899999961
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.08000004
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0700000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0700000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	5.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	3.48000002
k_AsstFWNstep_Cnt_u16	704
k_AsstFWPstep_Cnt_u16	4305
k_RestoreThresh_MtrNm_f32	4.5
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	14336

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	896
t_AsstFWDefltAssistX_HwNm_u8p8[1]	922
t_AsstFWDefltAssistX_HwNm_u8p8[2]	947
t_AsstFWDefltAssistX_HwNm_u8p8[3]	973
t_AsstFWDefltAssistX_HwNm_u8p8[4]	998
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1382
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	9011
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	12902
t_AsstFWPstepNstepThresh_Cnt_u16[0]	156
t_AsstFWPstepNstepThresh_Cnt_u16[1]	343
t_AsstFWVehSpd_Kph_u9p7[0]	24960
t_AsstFWVehSpd_Kph_u9p7[1]	25088
t_AsstFWVehSpd_Kph_u9p7[2]	25216
t_AsstFWVehSpd_Kph_u9p7[3]	25344
t_AsstFWVehSpd_Kph_u9p7[4]	25472
t_AsstFWVehSpd_Kph_u9p7[5]	25600
t_AsstFWVehSpd_Kph_u9p7[6]	25728
t_AsstFWVehSpd_Kph_u9p7[7]	25856
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	33.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4.55000019	4.55000019 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	343	343 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.39990234	-4.39990234 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.05022001	4.05022001 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.370000005	0.370000005 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.18600011	2.18600011 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-4.39990234	-4.39990234 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.36 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00499999989
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1968
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	2.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00999999978
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.09000003
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0799999982
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0799999982
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	5.80000019
k_AsstFWInpLimitHysComp_MtrNm_f32	3.82999992
k_AsstFWNstep_Cnt_u16	580
k_AsstFWPstep_Cnt_u16	4428
k_RestoreThresh_MtrNm_f32	4.5999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-6144

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-14336

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	-2048
t_AsstFWDefltAssistX_HwNm_u8p8[0]	922
t_AsstFWDefltAssistX_HwNm_u8p8[1]	947
t_AsstFWDefltAssistX_HwNm_u8p8[2]	973
t_AsstFWDefltAssistX_HwNm_u8p8[3]	998
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1382
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1408
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	9216
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	13107
t_AsstFWPstepNstepThresh_Cnt_u16[0]	157
t_AsstFWPstepNstepThresh_Cnt_u16[1]	347
t_AsstFWVehSpd_Kph_u9p7[0]	27904
t_AsstFWVehSpd_Kph_u9p7[1]	28032
t_AsstFWVehSpd_Kph_u9p7[2]	28160
t_AsstFWVehSpd_Kph_u9p7[3]	28288
t_AsstFWVehSpd_Kph_u9p7[4]	28416
t_AsstFWVehSpd_Kph_u9p7[5]	28544
t_AsstFWVehSpd_Kph_u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7]	28800
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	44.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.96999979	5.96999979 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	347	347 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.89990234	4.89990234 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.03299999	5.03299999 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.63999987	2.6400001 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.51999998	3.51999998 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4.89990234	4.89990234 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.37 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0700000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	3321
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.29999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.9000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00999999978
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0500000007
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-16
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00800000038
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.70000005
k_AsstFWInpLimitHFA_MtrNm_f32	8
k_AsstFWInpLimitHysComp_MtrNm_f32	0.430000007
k_AsstFWNstep_Cnt_u16	4305
k_AsstFWPstep_Cnt_u16	861
k_RestoreThresh_MtrNm_f32	5.69999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-16384

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	947
t_AsstFWDefltAssistX_HwNm_u8p8[1]	973
t_AsstFWDefltAssistX_HwNm_u8p8[2]	998
t_AsstFWDefltAssistX_HwNm_u8p8[3]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1382
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1408
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1434
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	9421
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	13312
t_AsstFWPstepNstepThresh_Cnt_u16[0]	158
t_AsstFWPstepNstepThresh_Cnt_u16[1]	351
t_AsstFWVehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1]	30976
t_AsstFWVehSpd_Kph_u9p7[2]	31104
t_AsstFWVehSpd_Kph_u9p7[3]	31232
t_AsstFWVehSpd_Kph_u9p7[4]	31360
t_AsstFWVehSpd_Kph_u9p7[5]	31488
t_AsstFWVehSpd_Kph_u9p7[6]	31616
t_AsstFWVehSpd_Kph_u9p7[7]	31744
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	40.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.57999992	5.57999992 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	351	351 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6.5	-6.5 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.89330006	6.89330006 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.09499979	5.09499979 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-15.9919996	-15.9919996 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-6.5	-6.5 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.38 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0799999982
AssistFirewall_ActiveRawAcc_Cnt_M_u16	3444
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0199999996
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.02999997
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	15.9995003
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00899999961
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6
k_AsstFWInpLimitHFA_MtrNm_f32	1.29999995
k_AsstFWInpLimitHysComp_MtrNm_f32	3.48000002
k_AsstFWNstep_Cnt_u16	4428
k_AsstFWPstep_Cnt_u16	984
k_RestoreThresh_MtrNm_f32	5.80000019
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-14336

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	22528
t_AsstFWDefltAssistX_HwNm_u8p8[0]	77
t_AsstFWDefltAssistX_HwNm_u8p8[1]	102
t_AsstFWDefltAssistX_HwNm_u8p8[2]	128
t_AsstFWDefltAssistX_HwNm_u8p8[3]	154
t_AsstFWDefltAssistX_HwNm_u8p8[4]	179
t_AsstFWDefltAssistX_HwNm_u8p8[5]	205
t_AsstFWDefltAssistX_HwNm_u8p8[6]	230
t_AsstFWDefltAssistX_HwNm_u8p8[7]	256
t_AsstFWDefltAssistX_HwNm_u8p8[8]	282
t_AsstFWDefltAssistX_HwNm_u8p8[9]	307
t_AsstFWDefltAssistX_HwNm_u8p8[10]	333
t_AsstFWDefltAssistX_HwNm_u8p8[11]	358
t_AsstFWDefltAssistX_HwNm_u8p8[12]	384
t_AsstFWDefltAssistX_HwNm_u8p8[13]	410
t_AsstFWDefltAssistX_HwNm_u8p8[14]	435
t_AsstFWDefltAssistX_HwNm_u8p8[15]	461
t_AsstFWDefltAssistX_HwNm_u8p8[16]	486
t_AsstFWDefltAssistX_HwNm_u8p8[17]	512
t_AsstFWDefltAssistX_HwNm_u8p8[18]	538
t_AsstFWDefltAssistX_HwNm_u8p8[19]	563
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	9626
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	13517
t_AsstFWPstepNstepThresh_Cnt_u16[0]	159
t_AsstFWPstepNstepThresh_Cnt_u16[1]	355
t_AsstFWVehSpd_Kph_u9p7[0]	33792
t_AsstFWVehSpd_Kph_u9p7[1]	33920
t_AsstFWVehSpd_Kph_u9p7[2]	34048
t_AsstFWVehSpd_Kph_u9p7[3]	34176
t_AsstFWVehSpd_Kph_u9p7[4]	34304
t_AsstFWVehSpd_Kph_u9p7[5]	34432
t_AsstFWVehSpd_Kph_u9p7[6]	34560
t_AsstFWVehSpd_Kph_u9p7[7]	34688
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-9
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	50.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4.5999999	4.5999999 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	355	355 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6.60009766	-6.60009766 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.58560002	1.58560002 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.97399998	5.97399998 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	15.7295046	15.7295046 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-6.60009766	-6.60009766 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

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Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.39 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0900000036
AssistFirewall_ActiveRawAcc_Cnt_M_u16	3567
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0299999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.03999996
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0700000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	0
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00999999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	8
k_AsstFWInpLimitHFA_MtrNm_f32	2.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	0.100000001
k_AsstFWNstep_Cnt_u16	4551
k_AsstFWPstep_Cnt_u16	1107
k_RestoreThresh_MtrNm_f32	5.9000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-12288

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	10240

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576
t_AsstFWDefltAssistX_HwNm_u8p8[0]	26
t_AsstFWDefltAssistX_HwNm_u8p8[1]	51
t_AsstFWDefltAssistX_HwNm_u8p8[2]	77
t_AsstFWDefltAssistX_HwNm_u8p8[3]	102
t_AsstFWDefltAssistX_HwNm_u8p8[4]	128
t_AsstFWDefltAssistX_HwNm_u8p8[5]	154
t_AsstFWDefltAssistX_HwNm_u8p8[6]	179
t_AsstFWDefltAssistX_HwNm_u8p8[7]	205
t_AsstFWDefltAssistX_HwNm_u8p8[8]	230
t_AsstFWDefltAssistX_HwNm_u8p8[9]	256
t_AsstFWDefltAssistX_HwNm_u8p8[10]	282
t_AsstFWDefltAssistX_HwNm_u8p8[11]	307
t_AsstFWDefltAssistX_HwNm_u8p8[12]	333
t_AsstFWDefltAssistX_HwNm_u8p8[13]	358
t_AsstFWDefltAssistX_HwNm_u8p8[14]	384
t_AsstFWDefltAssistX_HwNm_u8p8[15]	410
t_AsstFWDefltAssistX_HwNm_u8p8[16]	435
t_AsstFWDefltAssistX_HwNm_u8p8[17]	461
t_AsstFWDefltAssistX_HwNm_u8p8[18]	486
t_AsstFWDefltAssistX_HwNm_u8p8[19]	512
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	9830
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	13722
t_AsstFWPstepNstepThresh_Cnt_u16[0]	160
t_AsstFWPstepNstepThresh_Cnt_u16[1]	359
t_AsstFWVehSpd_Kph_u9p7[0]	36736
t_AsstFWVehSpd_Kph_u9p7[1]	36864
t_AsstFWVehSpd_Kph_u9p7[2]	36992
t_AsstFWVehSpd_Kph_u9p7[3]	37120
t_AsstFWVehSpd_Kph_u9p7[4]	37248
t_AsstFWVehSpd_Kph_u9p7[5]	37376
t_AsstFWVehSpd_Kph_u9p7[6]	37504
t_AsstFWVehSpd_Kph_u9p7[7]	37632
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	60.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-4.55000019	-4.55000019 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	359	359 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.70019531	5.70019531 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.97900009	4.97900009 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.72300005	4.72300005 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-0.109999999	-0.109999999 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	5.70019531	5.70019531 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.40 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	3690
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0399999991
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.04999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0799999982
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0199999996
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	7
k_AsstFWInpLimitHFA_MtrNm_f32	1.39999998
k_AsstFWInpLimitHysComp_MtrNm_f32	1.10000002
k_AsstFWNstep_Cnt_u16	4674
k_AsstFWPstep_Cnt_u16	1230
k_RestoreThresh_MtrNm_f32	6
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-10240

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	51
t_AsstFWDefltAssistX_HwNm_u8p8[1]	77
t_AsstFWDefltAssistX_HwNm_u8p8[2]	102
t_AsstFWDefltAssistX_HwNm_u8p8[3]	128
t_AsstFWDefltAssistX_HwNm_u8p8[4]	154
t_AsstFWDefltAssistX_HwNm_u8p8[5]	179
t_AsstFWDefltAssistX_HwNm_u8p8[6]	205
t_AsstFWDefltAssistX_HwNm_u8p8[7]	230
t_AsstFWDefltAssistX_HwNm_u8p8[8]	256
t_AsstFWDefltAssistX_HwNm_u8p8[9]	282
t_AsstFWDefltAssistX_HwNm_u8p8[10]	307
t_AsstFWDefltAssistX_HwNm_u8p8[11]	333
t_AsstFWDefltAssistX_HwNm_u8p8[12]	358
t_AsstFWDefltAssistX_HwNm_u8p8[13]	384
t_AsstFWDefltAssistX_HwNm_u8p8[14]	410
t_AsstFWDefltAssistX_HwNm_u8p8[15]	435
t_AsstFWDefltAssistX_HwNm_u8p8[16]	461
t_AsstFWDefltAssistX_HwNm_u8p8[17]	486
t_AsstFWDefltAssistX_HwNm_u8p8[18]	512
t_AsstFWDefltAssistX_HwNm_u8p8[19]	538
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	10035
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	13926
t_AsstFWPstepNstepThresh_Cnt_u16[0]	161
t_AsstFWPstepNstepThresh_Cnt_u16[1]	363
t_AsstFWVehSpd_Kph_u9p7[0]	39680
t_AsstFWVehSpd_Kph_u9p7[1]	39808
t_AsstFWVehSpd_Kph_u9p7[2]	39936
t_AsstFWVehSpd_Kph_u9p7[3]	40064
t_AsstFWVehSpd_Kph_u9p7[4]	40192
t_AsstFWVehSpd_Kph_u9p7[5]	40320
t_AsstFWVehSpd_Kph_u9p7[6]	40448
t_AsstFWVehSpd_Kph_u9p7[7]	40576
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	70.4000015
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.939999998	0.939999998 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	363	363 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6.70019531	-6.70019531 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-4.57999992	-4.57999992 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.4920001	5.4920001 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.1500001	5.1500001 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.939999998	0.939999998 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-6.70019531	-6.70019531 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.41 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0900000036
AssistFirewall_ActiveRawAcc_Cnt_M_u16	3813
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.70000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.05999994
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0900000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.200000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2
k_AsstFWInpLimitHFA_MtrNm_f32	1.60000002
k_AsstFWInpLimitHysComp_MtrNm_f32	1.39999998
k_AsstFWNstep_Cnt_u16	3567
k_AsstFWPstep_Cnt_u16	1353
k_RestoreThresh_MtrNm_f32	6.0999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	77
t_AsstFWDefltAssistX_HwNm_u8p8[1]	102
t_AsstFWDefltAssistX_HwNm_u8p8[2]	128
t_AsstFWDefltAssistX_HwNm_u8p8[3]	154
t_AsstFWDefltAssistX_HwNm_u8p8[4]	179
t_AsstFWDefltAssistX_HwNm_u8p8[5]	205
t_AsstFWDefltAssistX_HwNm_u8p8[6]	230
t_AsstFWDefltAssistX_HwNm_u8p8[7]	256
t_AsstFWDefltAssistX_HwNm_u8p8[8]	282
t_AsstFWDefltAssistX_HwNm_u8p8[9]	307
t_AsstFWDefltAssistX_HwNm_u8p8[10]	333
t_AsstFWDefltAssistX_HwNm_u8p8[11]	358
t_AsstFWDefltAssistX_HwNm_u8p8[12]	384
t_AsstFWDefltAssistX_HwNm_u8p8[13]	410
t_AsstFWDefltAssistX_HwNm_u8p8[14]	435
t_AsstFWDefltAssistX_HwNm_u8p8[15]	461
t_AsstFWDefltAssistX_HwNm_u8p8[16]	486
t_AsstFWDefltAssistX_HwNm_u8p8[17]	512
t_AsstFWDefltAssistX_HwNm_u8p8[18]	538
t_AsstFWDefltAssistX_HwNm_u8p8[19]	563
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	14131
t_AsstFWPstepNstepThresh_Cnt_u16[0]	162
t_AsstFWPstepNstepThresh_Cnt_u16[1]	367
t_AsstFWVehSpd_Kph_u9p7[0]	42624
t_AsstFWVehSpd_Kph_u9p7[1]	42752
t_AsstFWVehSpd_Kph_u9p7[2]	42880
t_AsstFWVehSpd_Kph_u9p7[3]	43008
t_AsstFWVehSpd_Kph_u9p7[4]	43136
t_AsstFWVehSpd_Kph_u9p7[5]	43264
t_AsstFWVehSpd_Kph_u9p7[6]	43392
t_AsstFWVehSpd_Kph_u9p7[7]	43520
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	80.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.81999993	1.82000005 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	367	367 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6.89990234	-6.89990234 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.14999998	1.14999998 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.64099979	5.64099979 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.4000001	-5.4000001 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-6.89990234	-6.89990234 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.42 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	3936
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.79999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0599999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.07000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00125584798
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1
k_AsstFWInpLimitHFA_MtrNm_f32	2
k_AsstFWInpLimitHysComp_MtrNm_f32	1.29999995
k_AsstFWNstep_Cnt_u16	3690
k_AsstFWPstep_Cnt_u16	1476
k_RestoreThresh_MtrNm_f32	6.19999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	102
t_AsstFWDefltAssistX_HwNm_u8p8[1]	128
t_AsstFWDefltAssistX_HwNm_u8p8[2]	154
t_AsstFWDefltAssistX_HwNm_u8p8[3]	179
t_AsstFWDefltAssistX_HwNm_u8p8[4]	205
t_AsstFWDefltAssistX_HwNm_u8p8[5]	230
t_AsstFWDefltAssistX_HwNm_u8p8[6]	256
t_AsstFWDefltAssistX_HwNm_u8p8[7]	282
t_AsstFWDefltAssistX_HwNm_u8p8[8]	307
t_AsstFWDefltAssistX_HwNm_u8p8[9]	333
t_AsstFWDefltAssistX_HwNm_u8p8[10]	358
t_AsstFWDefltAssistX_HwNm_u8p8[11]	384
t_AsstFWDefltAssistX_HwNm_u8p8[12]	410
t_AsstFWDefltAssistX_HwNm_u8p8[13]	435
t_AsstFWDefltAssistX_HwNm_u8p8[14]	461
t_AsstFWDefltAssistX_HwNm_u8p8[15]	486
t_AsstFWDefltAssistX_HwNm_u8p8[16]	512
t_AsstFWDefltAssistX_HwNm_u8p8[17]	538
t_AsstFWDefltAssistX_HwNm_u8p8[18]	563
t_AsstFWDefltAssistX_HwNm_u8p8[19]	589
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	10445
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	14336
t_AsstFWPstepNstepThresh_Cnt_u16[0]	163
t_AsstFWPstepNstepThresh_Cnt_u16[1]	371
t_AsstFWVehSpd_Kph_u9p7[0]	45568
t_AsstFWVehSpd_Kph_u9p7[1]	45696
t_AsstFWVehSpd_Kph_u9p7[2]	45824
t_AsstFWVehSpd_Kph_u9p7[3]	45952
t_AsstFWVehSpd_Kph_u9p7[4]	46080
t_AsstFWVehSpd_Kph_u9p7[5]	46208
t_AsstFWVehSpd_Kph_u9p7[6]	46336
t_AsstFWVehSpd_Kph_u9p7[7]	46464
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90.1999969
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.70000005	2.70000005 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	371	371 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	7	7 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.13800001	2.13800001 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.05999994	5.05999994 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	0.99874413	0.99874413 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	7	7 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.43 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.200000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4059
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.9000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0700000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.08000004
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0900000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.715390444
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.10000002
k_AsstFWInpLimitHFA_MtrNm_f32	4
k_AsstFWInpLimitHysComp_MtrNm_f32	2.0999999
k_AsstFWNstep_Cnt_u16	3813
k_AsstFWPstep_Cnt_u16	1599
k_RestoreThresh_MtrNm_f32	6.30000019
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	22528
t_AsstFWDefltAssistX_HwNm_u8p8[0]	128
t_AsstFWDefltAssistX_HwNm_u8p8[1]	154
t_AsstFWDefltAssistX_HwNm_u8p8[2]	179
t_AsstFWDefltAssistX_HwNm_u8p8[3]	205
t_AsstFWDefltAssistX_HwNm_u8p8[4]	230
t_AsstFWDefltAssistX_HwNm_u8p8[5]	256
t_AsstFWDefltAssistX_HwNm_u8p8[6]	282
t_AsstFWDefltAssistX_HwNm_u8p8[7]	307
t_AsstFWDefltAssistX_HwNm_u8p8[8]	333
t_AsstFWDefltAssistX_HwNm_u8p8[9]	358
t_AsstFWDefltAssistX_HwNm_u8p8[10]	384
t_AsstFWDefltAssistX_HwNm_u8p8[11]	410
t_AsstFWDefltAssistX_HwNm_u8p8[12]	435
t_AsstFWDefltAssistX_HwNm_u8p8[13]	461
t_AsstFWDefltAssistX_HwNm_u8p8[14]	486
t_AsstFWDefltAssistX_HwNm_u8p8[15]	512
t_AsstFWDefltAssistX_HwNm_u8p8[16]	538
t_AsstFWDefltAssistX_HwNm_u8p8[17]	563
t_AsstFWDefltAssistX_HwNm_u8p8[18]	589
t_AsstFWDefltAssistX_HwNm_u8p8[19]	614
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	10650
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	14541
t_AsstFWPstepNstepThresh_Cnt_u16[0]	164
t_AsstFWPstepNstepThresh_Cnt_u16[1]	375
t_AsstFWVehSpd_Kph_u9p7[0]	1408
t_AsstFWVehSpd_Kph_u9p7[1]	1536
t_AsstFWVehSpd_Kph_u9p7[2]	1664
t_AsstFWVehSpd_Kph_u9p7[3]	1792
t_AsstFWVehSpd_Kph_u9p7[4]	1920
t_AsstFWVehSpd_Kph_u9p7[5]	2048
t_AsstFWVehSpd_Kph_u9p7[6]	2176
t_AsstFWVehSpd_Kph_u9p7[7]	2304
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	11.1000004
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.20000005	3.20000005 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	375	375 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.10009766	7.10009766 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.22399998	3.22399998 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.82562494	5.82562494 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.95528805	1.95528805 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	7.10009766	7.10009766 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.44 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.300000012
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4182
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.09000003
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.5
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.20000005
k_AsstFWInpLimitHFA_MtrNm_f32	5
k_AsstFWInpLimitHysComp_MtrNm_f32	2.29999995
k_AsstFWNstep_Cnt_u16	3936
k_AsstFWPstep_Cnt_u16	1722
k_RestoreThresh_MtrNm_f32	6.4000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	10240

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576
t_AsstFWDefltAssistX_HwNm_u8p8[0]	154
t_AsstFWDefltAssistX_HwNm_u8p8[1]	179
t_AsstFWDefltAssistX_HwNm_u8p8[2]	205
t_AsstFWDefltAssistX_HwNm_u8p8[3]	230
t_AsstFWDefltAssistX_HwNm_u8p8[4]	256
t_AsstFWDefltAssistX_HwNm_u8p8[5]	282
t_AsstFWDefltAssistX_HwNm_u8p8[6]	307
t_AsstFWDefltAssistX_HwNm_u8p8[7]	333
t_AsstFWDefltAssistX_HwNm_u8p8[8]	358
t_AsstFWDefltAssistX_HwNm_u8p8[9]	384
t_AsstFWDefltAssistX_HwNm_u8p8[10]	410
t_AsstFWDefltAssistX_HwNm_u8p8[11]	435
t_AsstFWDefltAssistX_HwNm_u8p8[12]	461
t_AsstFWDefltAssistX_HwNm_u8p8[13]	486
t_AsstFWDefltAssistX_HwNm_u8p8[14]	512
t_AsstFWDefltAssistX_HwNm_u8p8[15]	538
t_AsstFWDefltAssistX_HwNm_u8p8[16]	563
t_AsstFWDefltAssistX_HwNm_u8p8[17]	589
t_AsstFWDefltAssistX_HwNm_u8p8[18]	614
t_AsstFWDefltAssistX_HwNm_u8p8[19]	640
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	10854
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	14746
t_AsstFWPstepNstepThresh_Cnt_u16[0]	165
t_AsstFWPstepNstepThresh_Cnt_u16[1]	379
t_AsstFWVehSpd_Kph_u9p7[0]	4352
t_AsstFWVehSpd_Kph_u9p7[1]	4480
t_AsstFWVehSpd_Kph_u9p7[2]	4608
t_AsstFWVehSpd_Kph_u9p7[3]	4736
t_AsstFWVehSpd_Kph_u9p7[4]	4864
t_AsstFWVehSpd_Kph_u9p7[5]	4992
t_AsstFWVehSpd_Kph_u9p7[6]	5120
t_AsstFWVehSpd_Kph_u9p7[7]	5248
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	22.3999996
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.5	3.5 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	379	379 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.20019531	7.20019531 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.28000021	4.28000021 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.9000001	6.9000001 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.5	2.5 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	7.20019531	7.20019531 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.45 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.400000006
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4305
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0900000036
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-8.80000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.200000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00499999989
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.20000005
k_AsstFWInpLimitHFA_MtrNm_f32	2
k_AsstFWInpLimitHysComp_MtrNm_f32	2.5
k_AsstFWNstep_Cnt_u16	4059
k_AsstFWPstep_Cnt_u16	1845
k_RestoreThresh_MtrNm_f32	6.5
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	0

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	12288

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	26624
t_AsstFWDefltAssistX_HwNm_u8p8[0]	179
t_AsstFWDefltAssistX_HwNm_u8p8[1]	205
t_AsstFWDefltAssistX_HwNm_u8p8[2]	230
t_AsstFWDefltAssistX_HwNm_u8p8[3]	256
t_AsstFWDefltAssistX_HwNm_u8p8[4]	282
t_AsstFWDefltAssistX_HwNm_u8p8[5]	307
t_AsstFWDefltAssistX_HwNm_u8p8[6]	333
t_AsstFWDefltAssistX_HwNm_u8p8[7]	358
t_AsstFWDefltAssistX_HwNm_u8p8[8]	384
t_AsstFWDefltAssistX_HwNm_u8p8[9]	410
t_AsstFWDefltAssistX_HwNm_u8p8[10]	435
t_AsstFWDefltAssistX_HwNm_u8p8[11]	461
t_AsstFWDefltAssistX_HwNm_u8p8[12]	486
t_AsstFWDefltAssistX_HwNm_u8p8[13]	512
t_AsstFWDefltAssistX_HwNm_u8p8[14]	538
t_AsstFWDefltAssistX_HwNm_u8p8[15]	563
t_AsstFWDefltAssistX_HwNm_u8p8[16]	589
t_AsstFWDefltAssistX_HwNm_u8p8[17]	614
t_AsstFWDefltAssistX_HwNm_u8p8[18]	640
t_AsstFWDefltAssistX_HwNm_u8p8[19]	666
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	11059
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	14950
t_AsstFWPstepNstepThresh_Cnt_u16[0]	166
t_AsstFWPstepNstepThresh_Cnt_u16[1]	383
t_AsstFWVehSpd_Kph_u9p7[0]	7296
t_AsstFWVehSpd_Kph_u9p7[1]	7424
t_AsstFWVehSpd_Kph_u9p7[2]	7552
t_AsstFWVehSpd_Kph_u9p7[3]	7680
t_AsstFWVehSpd_Kph_u9p7[4]	7808
t_AsstFWVehSpd_Kph_u9p7[5]	7936
t_AsstFWVehSpd_Kph_u9p7[6]	8064
t_AsstFWVehSpd_Kph_u9p7[7]	8192
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	33.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.5999999	3.5999999 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	383	383 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.29980469	7.29980469 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.0630002	5.0630002 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.64000034	-5.63999987 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.99499989	3.99499989 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	7.29980469	7.29980469 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.46 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.5
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4428
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00800000038
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.20000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8.80000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.300000012
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00600000005
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.5
k_AsstFWInpLimitHFA_MtrNm_f32	1
k_AsstFWInpLimitHysComp_MtrNm_f32	2.70000005
k_AsstFWNstep_Cnt_u16	4182
k_AsstFWPstep_Cnt_u16	1968
k_RestoreThresh_MtrNm_f32	6.5999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	14336

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	205
t_AsstFWDefltAssistX_HwNm_u8p8[1]	230
t_AsstFWDefltAssistX_HwNm_u8p8[2]	256
t_AsstFWDefltAssistX_HwNm_u8p8[3]	282
t_AsstFWDefltAssistX_HwNm_u8p8[4]	307
t_AsstFWDefltAssistX_HwNm_u8p8[5]	333
t_AsstFWDefltAssistX_HwNm_u8p8[6]	358
t_AsstFWDefltAssistX_HwNm_u8p8[7]	384
t_AsstFWDefltAssistX_HwNm_u8p8[8]	410
t_AsstFWDefltAssistX_HwNm_u8p8[9]	435
t_AsstFWDefltAssistX_HwNm_u8p8[10]	461
t_AsstFWDefltAssistX_HwNm_u8p8[11]	486
t_AsstFWDefltAssistX_HwNm_u8p8[12]	512
t_AsstFWDefltAssistX_HwNm_u8p8[13]	538
t_AsstFWDefltAssistX_HwNm_u8p8[14]	563
t_AsstFWDefltAssistX_HwNm_u8p8[15]	589
t_AsstFWDefltAssistX_HwNm_u8p8[16]	614
t_AsstFWDefltAssistX_HwNm_u8p8[17]	640
t_AsstFWDefltAssistX_HwNm_u8p8[18]	666
t_AsstFWDefltAssistX_HwNm_u8p8[19]	691
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	11264
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	15155
t_AsstFWPstepNstepThresh_Cnt_u16[0]	167
t_AsstFWPstepNstepThresh_Cnt_u16[1]	387
t_AsstFWVehSpd_Kph_u9p7[0]	10240
t_AsstFWVehSpd_Kph_u9p7[1]	10368
t_AsstFWVehSpd_Kph_u9p7[2]	10496
t_AsstFWVehSpd_Kph_u9p7[3]	10624
t_AsstFWVehSpd_Kph_u9p7[4]	10752
t_AsstFWVehSpd_Kph_u9p7[5]	10880
t_AsstFWVehSpd_Kph_u9p7[6]	11008
t_AsstFWVehSpd_Kph_u9p7[7]	11136
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-6
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	44.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.5	3.5 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	387	387 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.39990234	-7.39990234 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.99039984	5.99039984 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.96000004	4.96000004 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.93400002	4.93400002 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.39990234	-7.39990234 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.47 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.600000024
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4551
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00899999961
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.29999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.400000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00700000022
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.60000002
k_AsstFWInpLimitHFA_MtrNm_f32	4
k_AsstFWInpLimitHysComp_MtrNm_f32	2.9000001
k_AsstFWNstep_Cnt_u16	4305
k_AsstFWPstep_Cnt_u16	2091
k_RestoreThresh_MtrNm_f32	6.69999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	230
t_AsstFWDefltAssistX_HwNm_u8p8[1]	256
t_AsstFWDefltAssistX_HwNm_u8p8[2]	282
t_AsstFWDefltAssistX_HwNm_u8p8[3]	307
t_AsstFWDefltAssistX_HwNm_u8p8[4]	333
t_AsstFWDefltAssistX_HwNm_u8p8[5]	358
t_AsstFWDefltAssistX_HwNm_u8p8[6]	384
t_AsstFWDefltAssistX_HwNm_u8p8[7]	410
t_AsstFWDefltAssistX_HwNm_u8p8[8]	435
t_AsstFWDefltAssistX_HwNm_u8p8[9]	461
t_AsstFWDefltAssistX_HwNm_u8p8[10]	486
t_AsstFWDefltAssistX_HwNm_u8p8[11]	512
t_AsstFWDefltAssistX_HwNm_u8p8[12]	538
t_AsstFWDefltAssistX_HwNm_u8p8[13]	563
t_AsstFWDefltAssistX_HwNm_u8p8[14]	589
t_AsstFWDefltAssistX_HwNm_u8p8[15]	614
t_AsstFWDefltAssistX_HwNm_u8p8[16]	640
t_AsstFWDefltAssistX_HwNm_u8p8[17]	666
t_AsstFWDefltAssistX_HwNm_u8p8[18]	691
t_AsstFWDefltAssistX_HwNm_u8p8[19]	717
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	11469
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	15360
t_AsstFWPstepNstepThresh_Cnt_u16[0]	168
t_AsstFWPstepNstepThresh_Cnt_u16[1]	391
t_AsstFWVehSpd_Kph_u9p7[0]	13184
t_AsstFWVehSpd_Kph_u9p7[1]	13312
t_AsstFWVehSpd_Kph_u9p7[2]	13440
t_AsstFWVehSpd_Kph_u9p7[3]	13568
t_AsstFWVehSpd_Kph_u9p7[4]	13696
t_AsstFWVehSpd_Kph_u9p7[5]	13824
t_AsstFWVehSpd_Kph_u9p7[6]	13952
t_AsstFWVehSpd_Kph_u9p7[7]	14080
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2.20000005
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-7
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	55.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.19999981	3.20000005 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	391	391 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.5	-7.5 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.01350021	7.01350021 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-2	-2 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.92299986	5.92299986 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.5	-7.5 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.48 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.400000006
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4674
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	8
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00999999978
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.39999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00800000038
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.70000005
k_AsstFWInpLimitHFA_MtrNm_f32	2.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	3.0999999
k_AsstFWNstep_Cnt_u16	4428
k_AsstFWPstep_Cnt_u16	2214
k_RestoreThresh_MtrNm_f32	6.80000019
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-18432

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	256
t_AsstFWDefltAssistX_HwNm_u8p8[1]	282
t_AsstFWDefltAssistX_HwNm_u8p8[2]	307
t_AsstFWDefltAssistX_HwNm_u8p8[3]	333
t_AsstFWDefltAssistX_HwNm_u8p8[4]	358
t_AsstFWDefltAssistX_HwNm_u8p8[5]	384
t_AsstFWDefltAssistX_HwNm_u8p8[6]	410
t_AsstFWDefltAssistX_HwNm_u8p8[7]	435
t_AsstFWDefltAssistX_HwNm_u8p8[8]	461
t_AsstFWDefltAssistX_HwNm_u8p8[9]	486
t_AsstFWDefltAssistX_HwNm_u8p8[10]	512
t_AsstFWDefltAssistX_HwNm_u8p8[11]	538
t_AsstFWDefltAssistX_HwNm_u8p8[12]	563
t_AsstFWDefltAssistX_HwNm_u8p8[13]	589
t_AsstFWDefltAssistX_HwNm_u8p8[14]	614
t_AsstFWDefltAssistX_HwNm_u8p8[15]	640
t_AsstFWDefltAssistX_HwNm_u8p8[16]	666
t_AsstFWDefltAssistX_HwNm_u8p8[17]	691
t_AsstFWDefltAssistX_HwNm_u8p8[18]	717
t_AsstFWDefltAssistX_HwNm_u8p8[19]	742
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	11674
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	15565
t_AsstFWPstepNstepThresh_Cnt_u16[0]	169
t_AsstFWPstepNstepThresh_Cnt_u16[1]	395
t_AsstFWVehSpd_Kph_u9p7[0]	16128
t_AsstFWVehSpd_Kph_u9p7[1]	16256
t_AsstFWVehSpd_Kph_u9p7[2]	16384
t_AsstFWVehSpd_Kph_u9p7[3]	16512
t_AsstFWVehSpd_Kph_u9p7[4]	16640
t_AsstFWVehSpd_Kph_u9p7[5]	16768
t_AsstFWVehSpd_Kph_u9p7[6]	16896
t_AsstFWVehSpd_Kph_u9p7[7]	17024
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	66.5
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.659999967	0.660000026 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	395	395 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.60009766	-7.60009766 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.98999977	7.98999977 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-0.25	-0.25 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.91200018	6.91200018 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.659999967	0.660000026 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.60009766	-7.60009766 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.49 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4797
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0199999996
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.5
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.600000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00899999961
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.79999995
k_AsstFWInpLimitHFA_MtrNm_f32	3.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	3.29999995
k_AsstFWNstep_Cnt_u16	4551
k_AsstFWPstep_Cnt_u16	2337
k_RestoreThresh_MtrNm_f32	6.9000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	282
t_AsstFWDefltAssistX_HwNm_u8p8[1]	307
t_AsstFWDefltAssistX_HwNm_u8p8[2]	333
t_AsstFWDefltAssistX_HwNm_u8p8[3]	358
t_AsstFWDefltAssistX_HwNm_u8p8[4]	384
t_AsstFWDefltAssistX_HwNm_u8p8[5]	410
t_AsstFWDefltAssistX_HwNm_u8p8[6]	435
t_AsstFWDefltAssistX_HwNm_u8p8[7]	461
t_AsstFWDefltAssistX_HwNm_u8p8[8]	486
t_AsstFWDefltAssistX_HwNm_u8p8[9]	512
t_AsstFWDefltAssistX_HwNm_u8p8[10]	538
t_AsstFWDefltAssistX_HwNm_u8p8[11]	563
t_AsstFWDefltAssistX_HwNm_u8p8[12]	589
t_AsstFWDefltAssistX_HwNm_u8p8[13]	614
t_AsstFWDefltAssistX_HwNm_u8p8[14]	640
t_AsstFWDefltAssistX_HwNm_u8p8[15]	666
t_AsstFWDefltAssistX_HwNm_u8p8[16]	691
t_AsstFWDefltAssistX_HwNm_u8p8[17]	717
t_AsstFWDefltAssistX_HwNm_u8p8[18]	742
t_AsstFWDefltAssistX_HwNm_u8p8[19]	768
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	11878
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	15770
t_AsstFWPstepNstepThresh_Cnt_u16[0]	170
t_AsstFWPstepNstepThresh_Cnt_u16[1]	399
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
t_AsstFWVehSpd_Kph_u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-9
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	77.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.98000002	1.98000002 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	246	246 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	4	4 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.15799999	1.15799999 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-6.4000001	-6.4000001 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.90100002	7.90100002 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4	4 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x00	0x00	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x00	0x00	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.50 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.5
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4920
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.69999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0299999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.60000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00125584798
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00999999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1.89999998
k_AsstFWInpLimitHFA_MtrNm_f32	1.10000002
k_AsstFWInpLimitHysComp_MtrNm_f32	3.5
k_AsstFWNstep_Cnt_u16	4674
k_AsstFWPstep_Cnt_u16	2460
k_RestoreThresh_MtrNm_f32	7
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	12288

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-4096

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefltAssistX_HwNm_u8p8[0]	307
t_AsstFWDefltAssistX_HwNm_u8p8[1]	333
t_AsstFWDefltAssistX_HwNm_u8p8[2]	358
t_AsstFWDefltAssistX_HwNm_u8p8[3]	384
t_AsstFWDefltAssistX_HwNm_u8p8[4]	410
t_AsstFWDefltAssistX_HwNm_u8p8[5]	435
t_AsstFWDefltAssistX_HwNm_u8p8[6]	461
t_AsstFWDefltAssistX_HwNm_u8p8[7]	486
t_AsstFWDefltAssistX_HwNm_u8p8[8]	512
t_AsstFWDefltAssistX_HwNm_u8p8[9]	538
t_AsstFWDefltAssistX_HwNm_u8p8[10]	563
t_AsstFWDefltAssistX_HwNm_u8p8[11]	589
t_AsstFWDefltAssistX_HwNm_u8p8[12]	614
t_AsstFWDefltAssistX_HwNm_u8p8[13]	640
t_AsstFWDefltAssistX_HwNm_u8p8[14]	666
t_AsstFWDefltAssistX_HwNm_u8p8[15]	691
t_AsstFWDefltAssistX_HwNm_u8p8[16]	717
t_AsstFWDefltAssistX_HwNm_u8p8[17]	742
t_AsstFWDefltAssistX_HwNm_u8p8[18]	768
t_AsstFWDefltAssistX_HwNm_u8p8[19]	794
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	12083
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	15974
t_AsstFWPstepNstepThresh_Cnt_u16[0]	171
t_AsstFWPstepNstepThresh_Cnt_u16[1]	403
t_AsstFWVehSpd_Kph_u9p7[0]	22016
t_AsstFWVehSpd_Kph_u9p7[1]	22144
t_AsstFWVehSpd_Kph_u9p7[2]	22272
t_AsstFWVehSpd_Kph_u9p7[3]	22400
t_AsstFWVehSpd_Kph_u9p7[4]	22528
t_AsstFWVehSpd_Kph_u9p7[5]	22656
t_AsstFWVehSpd_Kph_u9p7[6]	22784
t_AsstFWVehSpd_Kph_u9p7[7]	22912
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	88.0800018
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.54999995	1.54999995 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	403	403 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.89990234	5.89990234 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.31700015	2.31699991 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.99497652	4.99497652 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.08899999	1.08899999 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	5.89990234	5.89990234 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.51 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.79999995
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0900000036
AssistFirewall_ActiveRawAcc_Cnt_M_u16	5043
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0399999991
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.70000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.715390444
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0199999996
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2
k_AsstFWInpLimitHFA_MtrNm_f32	2.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	3.70000005
k_AsstFWNstep_Cnt_u16	3567
k_AsstFWPstep_Cnt_u16	2583
k_RestoreThresh_MtrNm_f32	7.0999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	14336

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	333
t_AsstFWDefltAssistX_HwNm_u8p8[1]	358
t_AsstFWDefltAssistX_HwNm_u8p8[2]	384
t_AsstFWDefltAssistX_HwNm_u8p8[3]	410
t_AsstFWDefltAssistX_HwNm_u8p8[4]	435
t_AsstFWDefltAssistX_HwNm_u8p8[5]	461
t_AsstFWDefltAssistX_HwNm_u8p8[6]	486
t_AsstFWDefltAssistX_HwNm_u8p8[7]	512
t_AsstFWDefltAssistX_HwNm_u8p8[8]	538
t_AsstFWDefltAssistX_HwNm_u8p8[9]	563
t_AsstFWDefltAssistX_HwNm_u8p8[10]	589
t_AsstFWDefltAssistX_HwNm_u8p8[11]	614
t_AsstFWDefltAssistX_HwNm_u8p8[12]	640
t_AsstFWDefltAssistX_HwNm_u8p8[13]	666
t_AsstFWDefltAssistX_HwNm_u8p8[14]	691
t_AsstFWDefltAssistX_HwNm_u8p8[15]	717
t_AsstFWDefltAssistX_HwNm_u8p8[16]	742
t_AsstFWDefltAssistX_HwNm_u8p8[17]	768
t_AsstFWDefltAssistX_HwNm_u8p8[18]	794
t_AsstFWDefltAssistX_HwNm_u8p8[19]	819
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	16179
t_AsstFWPstepNstepThresh_Cnt_u16[0]	172
t_AsstFWPstepNstepThresh_Cnt_u16[1]	407
t_AsstFWVehSpd_Kph_u9p7[0]	24960
t_AsstFWVehSpd_Kph_u9p7[1]	25088
t_AsstFWVehSpd_Kph_u9p7[2]	25216
t_AsstFWVehSpd_Kph_u9p7[3]	25344
t_AsstFWVehSpd_Kph_u9p7[4]	25472
t_AsstFWVehSpd_Kph_u9p7[5]	25600
t_AsstFWVehSpd_Kph_u9p7[6]	25728
t_AsstFWVehSpd_Kph_u9p7[7]	25856
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	99.0299988
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.54799986	2.5480001 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1476	1476 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6.70019531	-6.70019531 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.29199982	3.29200006 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.4462471	-5.4462471 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.296	2.296 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-6.70019531	-6.70019531 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x00	0x00	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.52 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	5166
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.9000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0299999993
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	3.29999995
k_AsstFWInpLimitHysComp_MtrNm_f32	3.9000001
k_AsstFWNstep_Cnt_u16	3690
k_AsstFWPstep_Cnt_u16	2706
k_RestoreThresh_MtrNm_f32	7.19999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	16384

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	0

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	358
t_AsstFWDefltAssistX_HwNm_u8p8[1]	384
t_AsstFWDefltAssistX_HwNm_u8p8[2]	410
t_AsstFWDefltAssistX_HwNm_u8p8[3]	435
t_AsstFWDefltAssistX_HwNm_u8p8[4]	461
t_AsstFWDefltAssistX_HwNm_u8p8[5]	486
t_AsstFWDefltAssistX_HwNm_u8p8[6]	512
t_AsstFWDefltAssistX_HwNm_u8p8[7]	538
t_AsstFWDefltAssistX_HwNm_u8p8[8]	563
t_AsstFWDefltAssistX_HwNm_u8p8[9]	589
t_AsstFWDefltAssistX_HwNm_u8p8[10]	614
t_AsstFWDefltAssistX_HwNm_u8p8[11]	640
t_AsstFWDefltAssistX_HwNm_u8p8[12]	666
t_AsstFWDefltAssistX_HwNm_u8p8[13]	691
t_AsstFWDefltAssistX_HwNm_u8p8[14]	717
t_AsstFWDefltAssistX_HwNm_u8p8[15]	742
t_AsstFWDefltAssistX_HwNm_u8p8[16]	768
t_AsstFWDefltAssistX_HwNm_u8p8[17]	794
t_AsstFWDefltAssistX_HwNm_u8p8[18]	819
t_AsstFWDefltAssistX_HwNm_u8p8[19]	845
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	12493
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	16384
t_AsstFWPstepNstepThresh_Cnt_u16[0]	173
t_AsstFWPstepNstepThresh_Cnt_u16[1]	411
t_AsstFWVehSpd_Kph_u9p7[0]	27904
t_AsstFWVehSpd_Kph_u9p7[1]	28032
t_AsstFWVehSpd_Kph_u9p7[2]	28160
t_AsstFWVehSpd_Kph_u9p7[3]	28288
t_AsstFWVehSpd_Kph_u9p7[4]	28416
t_AsstFWVehSpd_Kph_u9p7[5]	28544
t_AsstFWVehSpd_Kph_u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7]	28800
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	123.010002
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.99000001	0.99000001 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1476	1476 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.70019531	-7.70019531 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.30499983	4.30499983 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-2	-2 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.1869998	3.18700004 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.99000001	0.99000001 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.70019531	-7.70019531 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x00	0x00	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.53 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-8.80000019
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.200000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	5289
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0599999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.89999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0900000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0399999991
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.20000005
k_AsstFWInpLimitHFA_MtrNm_f32	4.4000001
k_AsstFWInpLimitHysComp_MtrNm_f32	4.0999999
k_AsstFWNstep_Cnt_u16	3813
k_AsstFWPstep_Cnt_u16	2829
k_RestoreThresh_MtrNm_f32	7.30000019
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	18432

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	384
t_AsstFWDefltAssistX_HwNm_u8p8[1]	410
t_AsstFWDefltAssistX_HwNm_u8p8[2]	435
t_AsstFWDefltAssistX_HwNm_u8p8[3]	461
t_AsstFWDefltAssistX_HwNm_u8p8[4]	486
t_AsstFWDefltAssistX_HwNm_u8p8[5]	512
t_AsstFWDefltAssistX_HwNm_u8p8[6]	538
t_AsstFWDefltAssistX_HwNm_u8p8[7]	563
t_AsstFWDefltAssistX_HwNm_u8p8[8]	589
t_AsstFWDefltAssistX_HwNm_u8p8[9]	614
t_AsstFWDefltAssistX_HwNm_u8p8[10]	640
t_AsstFWDefltAssistX_HwNm_u8p8[11]	666
t_AsstFWDefltAssistX_HwNm_u8p8[12]	691
t_AsstFWDefltAssistX_HwNm_u8p8[13]	717
t_AsstFWDefltAssistX_HwNm_u8p8[14]	742
t_AsstFWDefltAssistX_HwNm_u8p8[15]	768
t_AsstFWDefltAssistX_HwNm_u8p8[16]	794
t_AsstFWDefltAssistX_HwNm_u8p8[17]	819
t_AsstFWDefltAssistX_HwNm_u8p8[18]	845
t_AsstFWDefltAssistX_HwNm_u8p8[19]	870
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	12698
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	16589
t_AsstFWPstepNstepThresh_Cnt_u16[0]	174
t_AsstFWPstepNstepThresh_Cnt_u16[1]	415
t_AsstFWVehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1]	30976
t_AsstFWVehSpd_Kph_u9p7[2]	31104
t_AsstFWVehSpd_Kph_u9p7[3]	31232
t_AsstFWVehSpd_Kph_u9p7[4]	31360
t_AsstFWVehSpd_Kph_u9p7[5]	31488
t_AsstFWVehSpd_Kph_u9p7[6]	31616
t_AsstFWVehSpd_Kph_u9p7[7]	31744
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	234.050003
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-7.03999996	-7.03999996 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	415	415 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.10009766	8.10009766 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.42399979	5.42399979 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.82999992	6.82999992 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.41599989	4.41599989 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.10009766	8.10009766 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.54 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8.80000019
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.300000012
AssistFirewall_ActiveRawAcc_Cnt_M_u16	5412
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0700000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0500000007
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.29999995
k_AsstFWInpLimitHFA_MtrNm_f32	5.5
k_AsstFWInpLimitHysComp_MtrNm_f32	4.30000019
k_AsstFWNstep_Cnt_u16	3936
k_AsstFWPstep_Cnt_u16	2952
k_RestoreThresh_MtrNm_f32	7.4000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	20480

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	410
t_AsstFWDefltAssistX_HwNm_u8p8[1]	435
t_AsstFWDefltAssistX_HwNm_u8p8[2]	461
t_AsstFWDefltAssistX_HwNm_u8p8[3]	486
t_AsstFWDefltAssistX_HwNm_u8p8[4]	512
t_AsstFWDefltAssistX_HwNm_u8p8[5]	538
t_AsstFWDefltAssistX_HwNm_u8p8[6]	563
t_AsstFWDefltAssistX_HwNm_u8p8[7]	589
t_AsstFWDefltAssistX_HwNm_u8p8[8]	614
t_AsstFWDefltAssistX_HwNm_u8p8[9]	640
t_AsstFWDefltAssistX_HwNm_u8p8[10]	666
t_AsstFWDefltAssistX_HwNm_u8p8[11]	691
t_AsstFWDefltAssistX_HwNm_u8p8[12]	717
t_AsstFWDefltAssistX_HwNm_u8p8[13]	742
t_AsstFWDefltAssistX_HwNm_u8p8[14]	768
t_AsstFWDefltAssistX_HwNm_u8p8[15]	794
t_AsstFWDefltAssistX_HwNm_u8p8[16]	819
t_AsstFWDefltAssistX_HwNm_u8p8[17]	845
t_AsstFWDefltAssistX_HwNm_u8p8[18]	870
t_AsstFWDefltAssistX_HwNm_u8p8[19]	896
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	12902
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	16794
t_AsstFWPstepNstepThresh_Cnt_u16[0]	175
t_AsstFWPstepNstepThresh_Cnt_u16[1]	419
t_AsstFWVehSpd_Kph_u9p7[0]	33792
t_AsstFWVehSpd_Kph_u9p7[1]	33920
t_AsstFWVehSpd_Kph_u9p7[2]	34048
t_AsstFWVehSpd_Kph_u9p7[3]	34176
t_AsstFWVehSpd_Kph_u9p7[4]	34304
t_AsstFWVehSpd_Kph_u9p7[5]	34432
t_AsstFWVehSpd_Kph_u9p7[6]	34560
t_AsstFWVehSpd_Kph_u9p7[7]	34688
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	24.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.15999985	6.15999985 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	419	419 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	6.29980469	6.29980469 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.97399998	5.97399998 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.189999998	0.189999998 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.34499979	5.34499979 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	6.29980469	6.29980469 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.55 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	5535
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.200000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0599999987
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.4000001
k_AsstFWInpLimitHFA_MtrNm_f32	6.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	4.5
k_AsstFWNstep_Cnt_u16	4059
k_AsstFWPstep_Cnt_u16	3075
k_RestoreThresh_MtrNm_f32	7.5
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	22528

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	14336

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	435
t_AsstFWDefltAssistX_HwNm_u8p8[1]	461
t_AsstFWDefltAssistX_HwNm_u8p8[2]	486
t_AsstFWDefltAssistX_HwNm_u8p8[3]	512
t_AsstFWDefltAssistX_HwNm_u8p8[4]	538
t_AsstFWDefltAssistX_HwNm_u8p8[5]	563
t_AsstFWDefltAssistX_HwNm_u8p8[6]	589
t_AsstFWDefltAssistX_HwNm_u8p8[7]	614
t_AsstFWDefltAssistX_HwNm_u8p8[8]	640
t_AsstFWDefltAssistX_HwNm_u8p8[9]	666
t_AsstFWDefltAssistX_HwNm_u8p8[10]	691
t_AsstFWDefltAssistX_HwNm_u8p8[11]	717
t_AsstFWDefltAssistX_HwNm_u8p8[12]	742
t_AsstFWDefltAssistX_HwNm_u8p8[13]	768
t_AsstFWDefltAssistX_HwNm_u8p8[14]	794
t_AsstFWDefltAssistX_HwNm_u8p8[15]	819
t_AsstFWDefltAssistX_HwNm_u8p8[16]	845
t_AsstFWDefltAssistX_HwNm_u8p8[17]	870
t_AsstFWDefltAssistX_HwNm_u8p8[18]	896
t_AsstFWDefltAssistX_HwNm_u8p8[19]	922
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	13107
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	16998
t_AsstFWPstepNstepThresh_Cnt_u16[0]	176
t_AsstFWPstepNstepThresh_Cnt_u16[1]	423
t_AsstFWVehSpd_Kph_u9p7[0]	36736
t_AsstFWVehSpd_Kph_u9p7[1]	36864
t_AsstFWVehSpd_Kph_u9p7[2]	36992
t_AsstFWVehSpd_Kph_u9p7[3]	37120
t_AsstFWVehSpd_Kph_u9p7[4]	37248
t_AsstFWVehSpd_Kph_u9p7[5]	37376
t_AsstFWVehSpd_Kph_u9p7[6]	37504
t_AsstFWVehSpd_Kph_u9p7[7]	37632
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	57.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0	0 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1476	1476 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6.70019531	-6.70019531 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.43200004	1.43200004 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-0.440000057	-0.439999998 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.15399981	6.15399981 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-6.70019531	-6.70019531 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x00	0x00	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.56 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.5
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0700000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	5658
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0900000036
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.02999997
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.300000012
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0700000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.5
k_AsstFWInpLimitHFA_MtrNm_f32	7.69999981
k_AsstFWInpLimitHysComp_MtrNm_f32	4.69999981
k_AsstFWNstep_Cnt_u16	4182
k_AsstFWPstep_Cnt_u16	3198
k_RestoreThresh_MtrNm_f32	7.5999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	461
t_AsstFWDefltAssistX_HwNm_u8p8[1]	486
t_AsstFWDefltAssistX_HwNm_u8p8[2]	512
t_AsstFWDefltAssistX_HwNm_u8p8[3]	538
t_AsstFWDefltAssistX_HwNm_u8p8[4]	563
t_AsstFWDefltAssistX_HwNm_u8p8[5]	589
t_AsstFWDefltAssistX_HwNm_u8p8[6]	614
t_AsstFWDefltAssistX_HwNm_u8p8[7]	640
t_AsstFWDefltAssistX_HwNm_u8p8[8]	666
t_AsstFWDefltAssistX_HwNm_u8p8[9]	691
t_AsstFWDefltAssistX_HwNm_u8p8[10]	717
t_AsstFWDefltAssistX_HwNm_u8p8[11]	742
t_AsstFWDefltAssistX_HwNm_u8p8[12]	768
t_AsstFWDefltAssistX_HwNm_u8p8[13]	794
t_AsstFWDefltAssistX_HwNm_u8p8[14]	819
t_AsstFWDefltAssistX_HwNm_u8p8[15]	845
t_AsstFWDefltAssistX_HwNm_u8p8[16]	870
t_AsstFWDefltAssistX_HwNm_u8p8[17]	896
t_AsstFWDefltAssistX_HwNm_u8p8[18]	922
t_AsstFWDefltAssistX_HwNm_u8p8[19]	947
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	13312
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	17203
t_AsstFWPstepNstepThresh_Cnt_u16[0]	177
t_AsstFWPstepNstepThresh_Cnt_u16[1]	427
t_AsstFWVehSpd_Kph_u9p7[0]	39680
t_AsstFWVehSpd_Kph_u9p7[1]	39808
t_AsstFWVehSpd_Kph_u9p7[2]	39936
t_AsstFWVehSpd_Kph_u9p7[3]	40064
t_AsstFWVehSpd_Kph_u9p7[4]	40192
t_AsstFWVehSpd_Kph_u9p7[5]	40320
t_AsstFWVehSpd_Kph_u9p7[6]	40448
t_AsstFWVehSpd_Kph_u9p7[7]	40576
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	89.0699997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.11499977	5.11499977 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	427	427 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.70019531	-7.70019531 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.58500004	2.58500004 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.46999979	2.47000003 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	0.439999998	0.439999998 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.70019531	-7.70019531 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.57 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.5
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0799999982
AssistFirewall_ActiveRawAcc_Cnt_M_u16	5781
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.200000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.03999996
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.400000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0799999982
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.5999999
k_AsstFWInpLimitHFA_MtrNm_f32	3.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	4.9000001
k_AsstFWNstep_Cnt_u16	4305
k_AsstFWPstep_Cnt_u16	3321
k_RestoreThresh_MtrNm_f32	7.69999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	0

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	486
t_AsstFWDefltAssistX_HwNm_u8p8[1]	512
t_AsstFWDefltAssistX_HwNm_u8p8[2]	538
t_AsstFWDefltAssistX_HwNm_u8p8[3]	563
t_AsstFWDefltAssistX_HwNm_u8p8[4]	589
t_AsstFWDefltAssistX_HwNm_u8p8[5]	614
t_AsstFWDefltAssistX_HwNm_u8p8[6]	640
t_AsstFWDefltAssistX_HwNm_u8p8[7]	666
t_AsstFWDefltAssistX_HwNm_u8p8[8]	691
t_AsstFWDefltAssistX_HwNm_u8p8[9]	717
t_AsstFWDefltAssistX_HwNm_u8p8[10]	742
t_AsstFWDefltAssistX_HwNm_u8p8[11]	768
t_AsstFWDefltAssistX_HwNm_u8p8[12]	794
t_AsstFWDefltAssistX_HwNm_u8p8[13]	819
t_AsstFWDefltAssistX_HwNm_u8p8[14]	845
t_AsstFWDefltAssistX_HwNm_u8p8[15]	870
t_AsstFWDefltAssistX_HwNm_u8p8[16]	896
t_AsstFWDefltAssistX_HwNm_u8p8[17]	922
t_AsstFWDefltAssistX_HwNm_u8p8[18]	947
t_AsstFWDefltAssistX_HwNm_u8p8[19]	973
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	13517
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	17408
t_AsstFWPstepNstepThresh_Cnt_u16[0]	178
t_AsstFWPstepNstepThresh_Cnt_u16[1]	431
t_AsstFWVehSpd_Kph_u9p7[0]	42624
t_AsstFWVehSpd_Kph_u9p7[1]	42752
t_AsstFWVehSpd_Kph_u9p7[2]	42880
t_AsstFWVehSpd_Kph_u9p7[3]	43008
t_AsstFWVehSpd_Kph_u9p7[4]	43136
t_AsstFWVehSpd_Kph_u9p7[5]	43264
t_AsstFWVehSpd_Kph_u9p7[6]	43392
t_AsstFWVehSpd_Kph_u9p7[7]	43520
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	10.1000004
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.05999994	-5.05999994 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	431	431 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.5	8.5 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.53999996	4.53999996 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.26000023	5.26000023 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.84000003	1.84000003 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.5	8.5 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.58 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00125584798
AssistFirewall_ActiveRawAcc_Cnt_M_u16	5904
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.300000012
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.04999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0900000036
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.70000005
k_AsstFWInpLimitHFA_MtrNm_f32	3.4000001
k_AsstFWInpLimitHysComp_MtrNm_f32	5.0999999
k_AsstFWNstep_Cnt_u16	4428
k_AsstFWPstep_Cnt_u16	3444
k_RestoreThresh_MtrNm_f32	7.80000019
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	512
t_AsstFWDefltAssistX_HwNm_u8p8[1]	538
t_AsstFWDefltAssistX_HwNm_u8p8[2]	563
t_AsstFWDefltAssistX_HwNm_u8p8[3]	589
t_AsstFWDefltAssistX_HwNm_u8p8[4]	614
t_AsstFWDefltAssistX_HwNm_u8p8[5]	640
t_AsstFWDefltAssistX_HwNm_u8p8[6]	666
t_AsstFWDefltAssistX_HwNm_u8p8[7]	691
t_AsstFWDefltAssistX_HwNm_u8p8[8]	717
t_AsstFWDefltAssistX_HwNm_u8p8[9]	742
t_AsstFWDefltAssistX_HwNm_u8p8[10]	768
t_AsstFWDefltAssistX_HwNm_u8p8[11]	794
t_AsstFWDefltAssistX_HwNm_u8p8[12]	819
t_AsstFWDefltAssistX_HwNm_u8p8[13]	845
t_AsstFWDefltAssistX_HwNm_u8p8[14]	870
t_AsstFWDefltAssistX_HwNm_u8p8[15]	896
t_AsstFWDefltAssistX_HwNm_u8p8[16]	922
t_AsstFWDefltAssistX_HwNm_u8p8[17]	947
t_AsstFWDefltAssistX_HwNm_u8p8[18]	973
t_AsstFWDefltAssistX_HwNm_u8p8[19]	998
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	13722
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	17613
t_AsstFWPstepNstepThresh_Cnt_u16[0]	179
t_AsstFWPstepNstepThresh_Cnt_u16[1]	435
t_AsstFWVehSpd_Kph_u9p7[0]	45568
t_AsstFWVehSpd_Kph_u9p7[1]	45696
t_AsstFWVehSpd_Kph_u9p7[2]	45824
t_AsstFWVehSpd_Kph_u9p7[3]	45952
t_AsstFWVehSpd_Kph_u9p7[4]	46080
t_AsstFWVehSpd_Kph_u9p7[5]	46208
t_AsstFWVehSpd_Kph_u9p7[6]	46336
t_AsstFWVehSpd_Kph_u9p7[7]	46464
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	40.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4.99372053	4.99372053 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	435	435 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.70019531	-7.70019531 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.75	4.75 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.04999995	3.04999995 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.19000006	2.19000006 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.70019531	-7.70019531 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.59 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.715390444
AssistFirewall_ActiveRawAcc_Cnt_M_u16	6027
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.69999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.400000006
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.05999994
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.600000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00499999989
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.79999995
k_AsstFWInpLimitHFA_MtrNm_f32	3.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	5.30000019
k_AsstFWNstep_Cnt_u16	4551
k_AsstFWPstep_Cnt_u16	3567
k_RestoreThresh_MtrNm_f32	7.9000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefltAssistX_HwNm_u8p8[0]	538
t_AsstFWDefltAssistX_HwNm_u8p8[1]	563
t_AsstFWDefltAssistX_HwNm_u8p8[2]	589
t_AsstFWDefltAssistX_HwNm_u8p8[3]	614
t_AsstFWDefltAssistX_HwNm_u8p8[4]	640
t_AsstFWDefltAssistX_HwNm_u8p8[5]	666
t_AsstFWDefltAssistX_HwNm_u8p8[6]	691
t_AsstFWDefltAssistX_HwNm_u8p8[7]	717
t_AsstFWDefltAssistX_HwNm_u8p8[8]	742
t_AsstFWDefltAssistX_HwNm_u8p8[9]	768
t_AsstFWDefltAssistX_HwNm_u8p8[10]	794
t_AsstFWDefltAssistX_HwNm_u8p8[11]	819
t_AsstFWDefltAssistX_HwNm_u8p8[12]	845
t_AsstFWDefltAssistX_HwNm_u8p8[13]	870
t_AsstFWDefltAssistX_HwNm_u8p8[14]	896
t_AsstFWDefltAssistX_HwNm_u8p8[15]	922
t_AsstFWDefltAssistX_HwNm_u8p8[16]	947
t_AsstFWDefltAssistX_HwNm_u8p8[17]	973
t_AsstFWDefltAssistX_HwNm_u8p8[18]	998
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1024
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	13926
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	17818
t_AsstFWPstepNstepThresh_Cnt_u16[0]	180
t_AsstFWPstepNstepThresh_Cnt_u16[1]	439
t_AsstFWVehSpd_Kph_u9p7[0]	1408
t_AsstFWVehSpd_Kph_u9p7[1]	1536
t_AsstFWVehSpd_Kph_u9p7[2]	1664
t_AsstFWVehSpd_Kph_u9p7[3]	1792
t_AsstFWVehSpd_Kph_u9p7[4]	1920
t_AsstFWVehSpd_Kph_u9p7[5]	2048
t_AsstFWVehSpd_Kph_u9p7[6]	2176
t_AsstFWVehSpd_Kph_u9p7[7]	2304
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2.20000005
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	50.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.70765734	1.70765722 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	439	439 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.70019531	8.70019531 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.51999998	6.51999998 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.44000006	5.44000006 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.9849999	3.9849999 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.70019531	8.70019531 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.60 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.5
AssistFirewall_ActiveRawAcc_Cnt_M_u16	6150
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.5
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.07000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0900000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00600000005
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.9000001
k_AsstFWInpLimitHFA_MtrNm_f32	3.79999995
k_AsstFWInpLimitHysComp_MtrNm_f32	5.5
k_AsstFWNstep_Cnt_u16	4674
k_AsstFWPstep_Cnt_u16	3690
k_RestoreThresh_MtrNm_f32	8
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	563
t_AsstFWDefltAssistX_HwNm_u8p8[1]	589
t_AsstFWDefltAssistX_HwNm_u8p8[2]	614
t_AsstFWDefltAssistX_HwNm_u8p8[3]	640
t_AsstFWDefltAssistX_HwNm_u8p8[4]	666
t_AsstFWDefltAssistX_HwNm_u8p8[5]	691
t_AsstFWDefltAssistX_HwNm_u8p8[6]	717
t_AsstFWDefltAssistX_HwNm_u8p8[7]	742
t_AsstFWDefltAssistX_HwNm_u8p8[8]	768
t_AsstFWDefltAssistX_HwNm_u8p8[9]	794
t_AsstFWDefltAssistX_HwNm_u8p8[10]	819
t_AsstFWDefltAssistX_HwNm_u8p8[11]	845
t_AsstFWDefltAssistX_HwNm_u8p8[12]	870
t_AsstFWDefltAssistX_HwNm_u8p8[13]	896
t_AsstFWDefltAssistX_HwNm_u8p8[14]	922
t_AsstFWDefltAssistX_HwNm_u8p8[15]	947
t_AsstFWDefltAssistX_HwNm_u8p8[16]	973
t_AsstFWDefltAssistX_HwNm_u8p8[17]	998
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1050
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	14131
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	18022
t_AsstFWPstepNstepThresh_Cnt_u16[0]	181
t_AsstFWPstepNstepThresh_Cnt_u16[1]	443
t_AsstFWVehSpd_Kph_u9p7[0]	4352
t_AsstFWVehSpd_Kph_u9p7[1]	4480
t_AsstFWVehSpd_Kph_u9p7[2]	4608
t_AsstFWVehSpd_Kph_u9p7[3]	4736
t_AsstFWVehSpd_Kph_u9p7[4]	4864
t_AsstFWVehSpd_Kph_u9p7[5]	4992
t_AsstFWVehSpd_Kph_u9p7[6]	5120
t_AsstFWVehSpd_Kph_u9p7[7]	5248
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	60.4000015
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.5	3.5 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1476	1476 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.70019531	7.70019531 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.85000014	1.85000002 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.26999998	1.26999998 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.96999979	4.96999979 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	7.70019531	7.70019531 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x00	0x00	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.61 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	6273
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-4.9000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-52.7999992
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.600000024
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.08000004
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00700000022
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3
k_AsstFWInpLimitHFA_MtrNm_f32	4
k_AsstFWInpLimitHysComp_MtrNm_f32	5.69999981
k_AsstFWNstep_Cnt_u16	3567
k_AsstFWPstep_Cnt_u16	3813
k_RestoreThresh_MtrNm_f32	8.10000038
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	0

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	589
t_AsstFWDefltAssistX_HwNm_u8p8[1]	614
t_AsstFWDefltAssistX_HwNm_u8p8[2]	640
t_AsstFWDefltAssistX_HwNm_u8p8[3]	666
t_AsstFWDefltAssistX_HwNm_u8p8[4]	691
t_AsstFWDefltAssistX_HwNm_u8p8[5]	717
t_AsstFWDefltAssistX_HwNm_u8p8[6]	742
t_AsstFWDefltAssistX_HwNm_u8p8[7]	768
t_AsstFWDefltAssistX_HwNm_u8p8[8]	794
t_AsstFWDefltAssistX_HwNm_u8p8[9]	819
t_AsstFWDefltAssistX_HwNm_u8p8[10]	845
t_AsstFWDefltAssistX_HwNm_u8p8[11]	870
t_AsstFWDefltAssistX_HwNm_u8p8[12]	896
t_AsstFWDefltAssistX_HwNm_u8p8[13]	922
t_AsstFWDefltAssistX_HwNm_u8p8[14]	947
t_AsstFWDefltAssistX_HwNm_u8p8[15]	973
t_AsstFWDefltAssistX_HwNm_u8p8[16]	998
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1075
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	18227
t_AsstFWPstepNstepThresh_Cnt_u16[0]	182
t_AsstFWPstepNstepThresh_Cnt_u16[1]	447
t_AsstFWVehSpd_Kph_u9p7[0]	7296
t_AsstFWVehSpd_Kph_u9p7[1]	7424
t_AsstFWVehSpd_Kph_u9p7[2]	7552
t_AsstFWVehSpd_Kph_u9p7[3]	7680
t_AsstFWVehSpd_Kph_u9p7[4]	7808
t_AsstFWVehSpd_Kph_u9p7[5]	7936
t_AsstFWVehSpd_Kph_u9p7[6]	8064
t_AsstFWVehSpd_Kph_u9p7[7]	8192
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	70.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7.19999981	7.19999981 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	447	447 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.70019531	8.70019531 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-16.3199997	-16.3199997 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.0999999	2.0999999 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.96500015	5.96500015 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.70019531	8.70019531 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.62 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.5
AssistFirewall_ActiveRawAcc_Cnt_M_u16	6396
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	52.7999992
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0900000036
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.09000003
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.200000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00800000038
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	4.19999981
k_AsstFWInpLimitHysComp_MtrNm_f32	5.9000001
k_AsstFWNstep_Cnt_u16	3690
k_AsstFWPstep_Cnt_u16	3936
k_RestoreThresh_MtrNm_f32	8.19999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	12288

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	614
t_AsstFWDefltAssistX_HwNm_u8p8[1]	640
t_AsstFWDefltAssistX_HwNm_u8p8[2]	666
t_AsstFWDefltAssistX_HwNm_u8p8[3]	691
t_AsstFWDefltAssistX_HwNm_u8p8[4]	717
t_AsstFWDefltAssistX_HwNm_u8p8[5]	742
t_AsstFWDefltAssistX_HwNm_u8p8[6]	768
t_AsstFWDefltAssistX_HwNm_u8p8[7]	794
t_AsstFWDefltAssistX_HwNm_u8p8[8]	819
t_AsstFWDefltAssistX_HwNm_u8p8[9]	845
t_AsstFWDefltAssistX_HwNm_u8p8[10]	870
t_AsstFWDefltAssistX_HwNm_u8p8[11]	896
t_AsstFWDefltAssistX_HwNm_u8p8[12]	922
t_AsstFWDefltAssistX_HwNm_u8p8[13]	947
t_AsstFWDefltAssistX_HwNm_u8p8[14]	973
t_AsstFWDefltAssistX_HwNm_u8p8[15]	998
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1101
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	14541
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	18432
t_AsstFWPstepNstepThresh_Cnt_u16[0]	183
t_AsstFWPstepNstepThresh_Cnt_u16[1]	451
t_AsstFWVehSpd_Kph_u9p7[0]	10240
t_AsstFWVehSpd_Kph_u9p7[1]	10368
t_AsstFWVehSpd_Kph_u9p7[2]	10496
t_AsstFWVehSpd_Kph_u9p7[3]	10624
t_AsstFWVehSpd_Kph_u9p7[4]	10752
t_AsstFWVehSpd_Kph_u9p7[5]	10880
t_AsstFWVehSpd_Kph_u9p7[6]	11008
t_AsstFWVehSpd_Kph_u9p7[7]	11136
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	80.1999969
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.550000012	0.550000012 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	451	451 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	48.9570007	48.9570007 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.2734375	2.2734375 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.00349998	7.00349998 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.550000012	0.550000012 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.63 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0900000036
AssistFirewall_ActiveRawAcc_Cnt_M_u16	6519
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	0
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.100000001
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.70000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.300000012
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00899999961
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.20000005
k_AsstFWInpLimitHFA_MtrNm_f32	4.4000001
k_AsstFWInpLimitHysComp_MtrNm_f32	6.0999999
k_AsstFWNstep_Cnt_u16	3813
k_AsstFWPstep_Cnt_u16	4059
k_RestoreThresh_MtrNm_f32	8.30000019
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	14336

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	640
t_AsstFWDefltAssistX_HwNm_u8p8[1]	666
t_AsstFWDefltAssistX_HwNm_u8p8[2]	691
t_AsstFWDefltAssistX_HwNm_u8p8[3]	717
t_AsstFWDefltAssistX_HwNm_u8p8[4]	742
t_AsstFWDefltAssistX_HwNm_u8p8[5]	768
t_AsstFWDefltAssistX_HwNm_u8p8[6]	794
t_AsstFWDefltAssistX_HwNm_u8p8[7]	819
t_AsstFWDefltAssistX_HwNm_u8p8[8]	845
t_AsstFWDefltAssistX_HwNm_u8p8[9]	870
t_AsstFWDefltAssistX_HwNm_u8p8[10]	896
t_AsstFWDefltAssistX_HwNm_u8p8[11]	922
t_AsstFWDefltAssistX_HwNm_u8p8[12]	947
t_AsstFWDefltAssistX_HwNm_u8p8[13]	973
t_AsstFWDefltAssistX_HwNm_u8p8[14]	998
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1126
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	14746
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	18637
t_AsstFWPstepNstepThresh_Cnt_u16[0]	184
t_AsstFWPstepNstepThresh_Cnt_u16[1]	455
t_AsstFWVehSpd_Kph_u9p7[0]	13184
t_AsstFWVehSpd_Kph_u9p7[1]	13312
t_AsstFWVehSpd_Kph_u9p7[2]	13440
t_AsstFWVehSpd_Kph_u9p7[3]	13568
t_AsstFWVehSpd_Kph_u9p7[4]	13696
t_AsstFWVehSpd_Kph_u9p7[5]	13824
t_AsstFWVehSpd_Kph_u9p7[6]	13952
t_AsstFWVehSpd_Kph_u9p7[7]	14080
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-6
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.00200009	2.00200009 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	455	455 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019	-8.80000019 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.03000009	1.02999997 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-0.200000286	-0.200000003 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.9369998	7.9369998 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-8.80000019	-8.80000019 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.64 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	6642
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00499999989
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.400000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00999999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.29999995
k_AsstFWInpLimitHFA_MtrNm_f32	4.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	6.30000019
k_AsstFWNstep_Cnt_u16	3936
k_AsstFWPstep_Cnt_u16	4182
k_RestoreThresh_MtrNm_f32	8.39999962
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	16384

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	22528
t_AsstFWDefltAssistX_HwNm_u8p8[0]	666
t_AsstFWDefltAssistX_HwNm_u8p8[1]	691
t_AsstFWDefltAssistX_HwNm_u8p8[2]	717
t_AsstFWDefltAssistX_HwNm_u8p8[3]	742
t_AsstFWDefltAssistX_HwNm_u8p8[4]	768
t_AsstFWDefltAssistX_HwNm_u8p8[5]	794
t_AsstFWDefltAssistX_HwNm_u8p8[6]	819
t_AsstFWDefltAssistX_HwNm_u8p8[7]	845
t_AsstFWDefltAssistX_HwNm_u8p8[8]	870
t_AsstFWDefltAssistX_HwNm_u8p8[9]	896
t_AsstFWDefltAssistX_HwNm_u8p8[10]	922
t_AsstFWDefltAssistX_HwNm_u8p8[11]	947
t_AsstFWDefltAssistX_HwNm_u8p8[12]	973
t_AsstFWDefltAssistX_HwNm_u8p8[13]	998
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1152
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	14950
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	18842
t_AsstFWPstepNstepThresh_Cnt_u16[0]	185
t_AsstFWPstepNstepThresh_Cnt_u16[1]	459
t_AsstFWVehSpd_Kph_u9p7[0]	16128
t_AsstFWVehSpd_Kph_u9p7[1]	16256
t_AsstFWVehSpd_Kph_u9p7[2]	16384
t_AsstFWVehSpd_Kph_u9p7[3]	16512
t_AsstFWVehSpd_Kph_u9p7[4]	16640
t_AsstFWVehSpd_Kph_u9p7[5]	16768
t_AsstFWVehSpd_Kph_u9p7[6]	16896
t_AsstFWVehSpd_Kph_u9p7[7]	17024
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-7
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	11.1999998
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.78999996	2.78999996 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	459	459 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019	-8.80000019 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.52099991	5.52099991 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-1.4000001	-1.39999998 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.09899998	1.09899998 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-8.80000019	-8.80000019 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.65 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.79999995
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.200000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	6765
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0399999991
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.89999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0199999996
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.4000001
k_AsstFWInpLimitHFA_MtrNm_f32	4.80000019
k_AsstFWInpLimitHysComp_MtrNm_f32	6.5
k_AsstFWNstep_Cnt_u16	4059
k_AsstFWPstep_Cnt_u16	4305
k_RestoreThresh_MtrNm_f32	8.5
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	18432

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	10240

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576
t_AsstFWDefltAssistX_HwNm_u8p8[0]	691
t_AsstFWDefltAssistX_HwNm_u8p8[1]	717
t_AsstFWDefltAssistX_HwNm_u8p8[2]	742
t_AsstFWDefltAssistX_HwNm_u8p8[3]	768
t_AsstFWDefltAssistX_HwNm_u8p8[4]	794
t_AsstFWDefltAssistX_HwNm_u8p8[5]	819
t_AsstFWDefltAssistX_HwNm_u8p8[6]	845
t_AsstFWDefltAssistX_HwNm_u8p8[7]	870
t_AsstFWDefltAssistX_HwNm_u8p8[8]	896
t_AsstFWDefltAssistX_HwNm_u8p8[9]	922
t_AsstFWDefltAssistX_HwNm_u8p8[10]	947
t_AsstFWDefltAssistX_HwNm_u8p8[11]	973
t_AsstFWDefltAssistX_HwNm_u8p8[12]	998
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1178
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	15155
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	19046
t_AsstFWPstepNstepThresh_Cnt_u16[0]	186
t_AsstFWPstepNstepThresh_Cnt_u16[1]	463
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
t_AsstFWVehSpd_Kph_u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	22.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.24000001	2.24000001 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	463	463 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019	-8.80000019 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-4.8039999	-4.8039999 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-3	-3 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.1960001	2.1960001 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-8.80000019	-8.80000019 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.66 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.300000012
AssistFirewall_ActiveRawAcc_Cnt_M_u16	6888
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00125584798
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.600000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0299999993
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.5
k_AsstFWInpLimitHFA_MtrNm_f32	5
k_AsstFWInpLimitHysComp_MtrNm_f32	6.69999981
k_AsstFWNstep_Cnt_u16	4182
k_AsstFWPstep_Cnt_u16	4428
k_RestoreThresh_MtrNm_f32	8.60000038
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	0

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	717
t_AsstFWDefltAssistX_HwNm_u8p8[1]	742
t_AsstFWDefltAssistX_HwNm_u8p8[2]	768
t_AsstFWDefltAssistX_HwNm_u8p8[3]	794
t_AsstFWDefltAssistX_HwNm_u8p8[4]	819
t_AsstFWDefltAssistX_HwNm_u8p8[5]	845
t_AsstFWDefltAssistX_HwNm_u8p8[6]	870
t_AsstFWDefltAssistX_HwNm_u8p8[7]	896
t_AsstFWDefltAssistX_HwNm_u8p8[8]	922
t_AsstFWDefltAssistX_HwNm_u8p8[9]	947
t_AsstFWDefltAssistX_HwNm_u8p8[10]	973
t_AsstFWDefltAssistX_HwNm_u8p8[11]	998
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1203
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	15360
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	19251
t_AsstFWPstepNstepThresh_Cnt_u16[0]	187
t_AsstFWPstepNstepThresh_Cnt_u16[1]	467
t_AsstFWVehSpd_Kph_u9p7[0]	22016
t_AsstFWVehSpd_Kph_u9p7[1]	22144
t_AsstFWVehSpd_Kph_u9p7[2]	22272
t_AsstFWVehSpd_Kph_u9p7[3]	22400
t_AsstFWVehSpd_Kph_u9p7[4]	22528
t_AsstFWVehSpd_Kph_u9p7[5]	22656
t_AsstFWVehSpd_Kph_u9p7[6]	22784
t_AsstFWVehSpd_Kph_u9p7[7]	22912
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-9
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	33.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.769999981	0.769999981 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	467	467 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019	-8.80000019 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.00891638	7.00891638 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-0.800000191	-0.800000012 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.88699985	2.88700008 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.769999981	0.769999981 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-8.80000019	-8.80000019 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.67 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	7011
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	8
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.715390444
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0900000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0399999991
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.5999999
k_AsstFWInpLimitHFA_MtrNm_f32	5.19999981
k_AsstFWInpLimitHysComp_MtrNm_f32	6.9000001
k_AsstFWNstep_Cnt_u16	4305
k_AsstFWPstep_Cnt_u16	4551
k_RestoreThresh_MtrNm_f32	8.69999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-18432

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	742
t_AsstFWDefltAssistX_HwNm_u8p8[1]	768
t_AsstFWDefltAssistX_HwNm_u8p8[2]	794
t_AsstFWDefltAssistX_HwNm_u8p8[3]	819
t_AsstFWDefltAssistX_HwNm_u8p8[4]	845
t_AsstFWDefltAssistX_HwNm_u8p8[5]	870
t_AsstFWDefltAssistX_HwNm_u8p8[6]	896
t_AsstFWDefltAssistX_HwNm_u8p8[7]	922
t_AsstFWDefltAssistX_HwNm_u8p8[8]	947
t_AsstFWDefltAssistX_HwNm_u8p8[9]	973
t_AsstFWDefltAssistX_HwNm_u8p8[10]	998
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1229
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	15565
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	19456
t_AsstFWPstepNstepThresh_Cnt_u16[0]	188
t_AsstFWPstepNstepThresh_Cnt_u16[1]	471
t_AsstFWVehSpd_Kph_u9p7[0]	24960
t_AsstFWVehSpd_Kph_u9p7[1]	25088
t_AsstFWVehSpd_Kph_u9p7[2]	25216
t_AsstFWVehSpd_Kph_u9p7[3]	25344
t_AsstFWVehSpd_Kph_u9p7[4]	25472
t_AsstFWVehSpd_Kph_u9p7[5]	25600
t_AsstFWVehSpd_Kph_u9p7[6]	25728
t_AsstFWVehSpd_Kph_u9p7[7]	25856
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	44.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.57999992	6.57999992 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	471	471 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.60009766	7.60009766 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	9.28770256	9.28770256 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.36999989	7.36999989 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.97599983	3.97600007 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	7.60009766	7.60009766 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.68 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0700000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	7134
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.5
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.04999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0500000007
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.70000005
k_AsstFWInpLimitHFA_MtrNm_f32	5.4000001
k_AsstFWInpLimitHysComp_MtrNm_f32	7.0999999
k_AsstFWNstep_Cnt_u16	4428
k_AsstFWPstep_Cnt_u16	4674
k_RestoreThresh_MtrNm_f32	1.12
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-16384

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	768
t_AsstFWDefltAssistX_HwNm_u8p8[1]	794
t_AsstFWDefltAssistX_HwNm_u8p8[2]	819
t_AsstFWDefltAssistX_HwNm_u8p8[3]	845
t_AsstFWDefltAssistX_HwNm_u8p8[4]	870
t_AsstFWDefltAssistX_HwNm_u8p8[5]	896
t_AsstFWDefltAssistX_HwNm_u8p8[6]	922
t_AsstFWDefltAssistX_HwNm_u8p8[7]	947
t_AsstFWDefltAssistX_HwNm_u8p8[8]	973
t_AsstFWDefltAssistX_HwNm_u8p8[9]	998
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1254
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	15770
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	19661
t_AsstFWPstepNstepThresh_Cnt_u16[0]	189
t_AsstFWPstepNstepThresh_Cnt_u16[1]	475
t_AsstFWVehSpd_Kph_u9p7[0]	27904
t_AsstFWVehSpd_Kph_u9p7[1]	28032
t_AsstFWVehSpd_Kph_u9p7[2]	28160
t_AsstFWVehSpd_Kph_u9p7[3]	28288
t_AsstFWVehSpd_Kph_u9p7[4]	28416
t_AsstFWVehSpd_Kph_u9p7[5]	28544
t_AsstFWVehSpd_Kph_u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7]	28800
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	55.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-14336

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	8192

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	22528
t_AsstFWDefltAssistX_HwNm_u8p8[0]	794
t_AsstFWDefltAssistX_HwNm_u8p8[1]	819
t_AsstFWDefltAssistX_HwNm_u8p8[2]	845
t_AsstFWDefltAssistX_HwNm_u8p8[3]	870
t_AsstFWDefltAssistX_HwNm_u8p8[4]	896
t_AsstFWDefltAssistX_HwNm_u8p8[5]	922
t_AsstFWDefltAssistX_HwNm_u8p8[6]	947
t_AsstFWDefltAssistX_HwNm_u8p8[7]	973
t_AsstFWDefltAssistX_HwNm_u8p8[8]	998
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1280
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	15974
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	19866
t_AsstFWPstepNstepThresh_Cnt_u16[0]	190
t_AsstFWPstepNstepThresh_Cnt_u16[1]	479
t_AsstFWVehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1]	30976
t_AsstFWVehSpd_Kph_u9p7[2]	31104
t_AsstFWVehSpd_Kph_u9p7[3]	31232
t_AsstFWVehSpd_Kph_u9p7[4]	31360
t_AsstFWVehSpd_Kph_u9p7[5]	31488
t_AsstFWVehSpd_Kph_u9p7[6]	31616
t_AsstFWVehSpd_Kph_u9p7[7]	31744
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	66.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.01200008	1.01199996 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	479	479 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.79980469	-7.79980469 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.9000001	2.9000001 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.76000023	3.75999999 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.89400005	4.89400005 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-7.79980469	-7.79980469 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.70 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00999999978
AssistFirewall_ActiveRawAcc_Cnt_M_u16	7380
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.200000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	2.09537959
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.300000012
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0700000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.9000001
k_AsstFWInpLimitHFA_MtrNm_f32	5.80000019
k_AsstFWInpLimitHysComp_MtrNm_f32	7.5
k_AsstFWNstep_Cnt_u16	4674
k_AsstFWPstep_Cnt_u16	4920
k_RestoreThresh_MtrNm_f32	1.13999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-12288

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	10240

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576
t_AsstFWDefltAssistX_HwNm_u8p8[0]	819
t_AsstFWDefltAssistX_HwNm_u8p8[1]	845
t_AsstFWDefltAssistX_HwNm_u8p8[2]	870
t_AsstFWDefltAssistX_HwNm_u8p8[3]	896
t_AsstFWDefltAssistX_HwNm_u8p8[4]	922
t_AsstFWDefltAssistX_HwNm_u8p8[5]	947
t_AsstFWDefltAssistX_HwNm_u8p8[6]	973
t_AsstFWDefltAssistX_HwNm_u8p8[7]	998
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1306
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	16179
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	20070
t_AsstFWPstepNstepThresh_Cnt_u16[0]	191
t_AsstFWPstepNstepThresh_Cnt_u16[1]	483
t_AsstFWVehSpd_Kph_u9p7[0]	33792
t_AsstFWVehSpd_Kph_u9p7[1]	33920
t_AsstFWVehSpd_Kph_u9p7[2]	34048
t_AsstFWVehSpd_Kph_u9p7[3]	34176
t_AsstFWVehSpd_Kph_u9p7[4]	34304
t_AsstFWVehSpd_Kph_u9p7[5]	34432
t_AsstFWVehSpd_Kph_u9p7[6]	34560
t_AsstFWVehSpd_Kph_u9p7[7]	34688
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	77.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.17799997	2.17799997 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	483	483 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.70019531	8.70019531 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.46000004	4.46000004 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.06999969	6.07000017 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.80999994	6.80999994 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.70019531	8.70019531 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.71 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0199999996
AssistFirewall_ActiveRawAcc_Cnt_M_u16	7503
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.9000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.300000012
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.5
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.400000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0799999982
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4
k_AsstFWInpLimitHFA_MtrNm_f32	6
k_AsstFWInpLimitHysComp_MtrNm_f32	7.69999981
k_AsstFWNstep_Cnt_u16	2812
k_AsstFWPstep_Cnt_u16	1476
k_RestoreThresh_MtrNm_f32	1.14999998
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-10240

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	12288

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	26624
t_AsstFWDefltAssistX_HwNm_u8p8[0]	845
t_AsstFWDefltAssistX_HwNm_u8p8[1]	870
t_AsstFWDefltAssistX_HwNm_u8p8[2]	896
t_AsstFWDefltAssistX_HwNm_u8p8[3]	922
t_AsstFWDefltAssistX_HwNm_u8p8[4]	947
t_AsstFWDefltAssistX_HwNm_u8p8[5]	973
t_AsstFWDefltAssistX_HwNm_u8p8[6]	998
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1331
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	20275
t_AsstFWPstepNstepThresh_Cnt_u16[0]	192
t_AsstFWPstepNstepThresh_Cnt_u16[1]	487
t_AsstFWVehSpd_Kph_u9p7[0]	36736
t_AsstFWVehSpd_Kph_u9p7[1]	36864
t_AsstFWVehSpd_Kph_u9p7[2]	36992
t_AsstFWVehSpd_Kph_u9p7[3]	37120
t_AsstFWVehSpd_Kph_u9p7[4]	37248
t_AsstFWVehSpd_Kph_u9p7[5]	37376
t_AsstFWVehSpd_Kph_u9p7[6]	37504
t_AsstFWVehSpd_Kph_u9p7[7]	37632
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	88.0699997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.03799987	3.03800011 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	487	487 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	8	8 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.47000027	6.46999979 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.05999994	4.05999994 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	0.852000058	0.851999998 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8	8 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.72 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	7626
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.400000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0900000036
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	6.19999981
k_AsstFWInpLimitHysComp_MtrNm_f32	0
k_AsstFWNstep_Cnt_u16	2688
k_AsstFWPstep_Cnt_u16	1599
k_RestoreThresh_MtrNm_f32	1.15999997
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	14336

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	870
t_AsstFWDefltAssistX_HwNm_u8p8[1]	896
t_AsstFWDefltAssistX_HwNm_u8p8[2]	922
t_AsstFWDefltAssistX_HwNm_u8p8[3]	947
t_AsstFWDefltAssistX_HwNm_u8p8[4]	973
t_AsstFWDefltAssistX_HwNm_u8p8[5]	998
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1357
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	16589
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	20480
t_AsstFWPstepNstepThresh_Cnt_u16[0]	193
t_AsstFWPstepNstepThresh_Cnt_u16[1]	491
t_AsstFWVehSpd_Kph_u9p7[0]	39680
t_AsstFWVehSpd_Kph_u9p7[1]	39808
t_AsstFWVehSpd_Kph_u9p7[2]	39936
t_AsstFWVehSpd_Kph_u9p7[3]	40064
t_AsstFWVehSpd_Kph_u9p7[4]	40192
t_AsstFWVehSpd_Kph_u9p7[5]	40320
t_AsstFWVehSpd_Kph_u9p7[6]	40448
t_AsstFWVehSpd_Kph_u9p7[7]	40576
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.6500001
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	99.0500031
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.78999996	2.78999996 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	491	491 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.10009766	8.10009766 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.1500001	4.1500001 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5	5 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.82099986	1.82099998 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.10009766	8.10009766 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.73 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.79999995
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.200000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	7749
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0599999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.89999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.100000001
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.19999981
k_AsstFWInpLimitHFA_MtrNm_f32	6.4000001
k_AsstFWInpLimitHysComp_MtrNm_f32	8.80000019
k_AsstFWNstep_Cnt_u16	2564
k_AsstFWPstep_Cnt_u16	1722
k_RestoreThresh_MtrNm_f32	1.16999996
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	896
t_AsstFWDefltAssistX_HwNm_u8p8[1]	922
t_AsstFWDefltAssistX_HwNm_u8p8[2]	947
t_AsstFWDefltAssistX_HwNm_u8p8[3]	973
t_AsstFWDefltAssistX_HwNm_u8p8[4]	998
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1382
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	16794
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	20685
t_AsstFWPstepNstepThresh_Cnt_u16[0]	194
t_AsstFWPstepNstepThresh_Cnt_u16[1]	495
t_AsstFWVehSpd_Kph_u9p7[0]	42624
t_AsstFWVehSpd_Kph_u9p7[1]	42752
t_AsstFWVehSpd_Kph_u9p7[2]	42880
t_AsstFWVehSpd_Kph_u9p7[3]	43008
t_AsstFWVehSpd_Kph_u9p7[4]	43136
t_AsstFWVehSpd_Kph_u9p7[5]	43264
t_AsstFWVehSpd_Kph_u9p7[6]	43392
t_AsstFWVehSpd_Kph_u9p7[7]	43520
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.78000021
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-4
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	110.019997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.24000001	2.24000001 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	495	495 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.20019531	8.20019531 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.87199974	4.87200022 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6	6 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.78999996	2.78999996 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.20019531	8.20019531 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.74 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.300000012
AssistFirewall_ActiveRawAcc_Cnt_M_u16	7872
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0700000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.600000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.109999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.30000019
k_AsstFWInpLimitHFA_MtrNm_f32	6.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	6.38000011
k_AsstFWNstep_Cnt_u16	2440
k_AsstFWPstep_Cnt_u16	1845
k_RestoreThresh_MtrNm_f32	1.17999995
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	922
t_AsstFWDefltAssistX_HwNm_u8p8[1]	947
t_AsstFWDefltAssistX_HwNm_u8p8[2]	973
t_AsstFWDefltAssistX_HwNm_u8p8[3]	998
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1382
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1408
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	16998
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	20890
t_AsstFWPstepNstepThresh_Cnt_u16[0]	195
t_AsstFWPstepNstepThresh_Cnt_u16[1]	499
t_AsstFWVehSpd_Kph_u9p7[0]	45568
t_AsstFWVehSpd_Kph_u9p7[1]	45696
t_AsstFWVehSpd_Kph_u9p7[2]	45824
t_AsstFWVehSpd_Kph_u9p7[3]	45952
t_AsstFWVehSpd_Kph_u9p7[4]	46080
t_AsstFWVehSpd_Kph_u9p7[5]	46208
t_AsstFWVehSpd_Kph_u9p7[6]	46336
t_AsstFWVehSpd_Kph_u9p7[7]	46464
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.90999985
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-6
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	121.029999
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.769999981	0.769999981 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	499	499 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.70019531	8.70019531 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.69399977	5.69399977 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7	7 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.75899982	3.75900006 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.769999981	0.769999981 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.70019531	8.70019531 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.75 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	7995
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.400000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.119999997
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.4000001
k_AsstFWInpLimitHFA_MtrNm_f32	0
k_AsstFWInpLimitHysComp_MtrNm_f32	4
k_AsstFWNstep_Cnt_u16	2316
k_AsstFWPstep_Cnt_u16	1968
k_RestoreThresh_MtrNm_f32	1.19000006
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	947
t_AsstFWDefltAssistX_HwNm_u8p8[1]	973
t_AsstFWDefltAssistX_HwNm_u8p8[2]	998
t_AsstFWDefltAssistX_HwNm_u8p8[3]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1382
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1408
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1434
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	17203
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	21094
t_AsstFWPstepNstepThresh_Cnt_u16[0]	196
t_AsstFWPstepNstepThresh_Cnt_u16[1]	503
t_AsstFWVehSpd_Kph_u9p7[0]	1408
t_AsstFWVehSpd_Kph_u9p7[1]	1536
t_AsstFWVehSpd_Kph_u9p7[2]	1664
t_AsstFWVehSpd_Kph_u9p7[3]	1792
t_AsstFWVehSpd_Kph_u9p7[4]	1920
t_AsstFWVehSpd_Kph_u9p7[5]	2048
t_AsstFWVehSpd_Kph_u9p7[6]	2176
t_AsstFWVehSpd_Kph_u9p7[7]	2304
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.03999996
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	132.039993
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.91400003	2.91400003 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	503	503 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.43200004	1.43200004 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5	5 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.96799994	4.96799994 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.76 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.79999995
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8118
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.129999995
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.5
k_AsstFWInpLimitHFA_MtrNm_f32	8.80000019
k_AsstFWInpLimitHysComp_MtrNm_f32	6.38000011
k_AsstFWNstep_Cnt_u16	2192
k_AsstFWPstep_Cnt_u16	2091
k_RestoreThresh_MtrNm_f32	2.21000004
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	0

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefltAssistX_HwNm_u8p8[0]	128
t_AsstFWDefltAssistX_HwNm_u8p8[1]	154
t_AsstFWDefltAssistX_HwNm_u8p8[2]	179
t_AsstFWDefltAssistX_HwNm_u8p8[3]	205
t_AsstFWDefltAssistX_HwNm_u8p8[4]	230
t_AsstFWDefltAssistX_HwNm_u8p8[5]	256
t_AsstFWDefltAssistX_HwNm_u8p8[6]	282
t_AsstFWDefltAssistX_HwNm_u8p8[7]	307
t_AsstFWDefltAssistX_HwNm_u8p8[8]	333
t_AsstFWDefltAssistX_HwNm_u8p8[9]	358
t_AsstFWDefltAssistX_HwNm_u8p8[10]	384
t_AsstFWDefltAssistX_HwNm_u8p8[11]	410
t_AsstFWDefltAssistX_HwNm_u8p8[12]	435
t_AsstFWDefltAssistX_HwNm_u8p8[13]	461
t_AsstFWDefltAssistX_HwNm_u8p8[14]	486
t_AsstFWDefltAssistX_HwNm_u8p8[15]	512
t_AsstFWDefltAssistX_HwNm_u8p8[16]	538
t_AsstFWDefltAssistX_HwNm_u8p8[17]	563
t_AsstFWDefltAssistX_HwNm_u8p8[18]	589
t_AsstFWDefltAssistX_HwNm_u8p8[19]	614
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	17408
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	21299
t_AsstFWPstepNstepThresh_Cnt_u16[0]	197
t_AsstFWPstepNstepThresh_Cnt_u16[1]	507
t_AsstFWVehSpd_Kph_u9p7[0]	4352
t_AsstFWVehSpd_Kph_u9p7[1]	4480
t_AsstFWVehSpd_Kph_u9p7[2]	4608
t_AsstFWVehSpd_Kph_u9p7[3]	4736
t_AsstFWVehSpd_Kph_u9p7[4]	4864
t_AsstFWVehSpd_Kph_u9p7[5]	4992
t_AsstFWVehSpd_Kph_u9p7[6]	5120
t_AsstFWVehSpd_Kph_u9p7[7]	5248
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.17000008
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	143.059998
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.51999998	2.51999998 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	507	507 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.26999998	4.26999998 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.5	5.5 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.51999998	1.51999998 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.77 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.200000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8241
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0599999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.89999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.600000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.140000001
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.5999999
k_AsstFWInpLimitHFA_MtrNm_f32	3.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	6.48999977
k_AsstFWNstep_Cnt_u16	2812
k_AsstFWPstep_Cnt_u16	2214
k_RestoreThresh_MtrNm_f32	2.22000003
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	26
t_AsstFWDefltAssistX_HwNm_u8p8[1]	51
t_AsstFWDefltAssistX_HwNm_u8p8[2]	77
t_AsstFWDefltAssistX_HwNm_u8p8[3]	102
t_AsstFWDefltAssistX_HwNm_u8p8[4]	128
t_AsstFWDefltAssistX_HwNm_u8p8[5]	154
t_AsstFWDefltAssistX_HwNm_u8p8[6]	179
t_AsstFWDefltAssistX_HwNm_u8p8[7]	205
t_AsstFWDefltAssistX_HwNm_u8p8[8]	230
t_AsstFWDefltAssistX_HwNm_u8p8[9]	256
t_AsstFWDefltAssistX_HwNm_u8p8[10]	282
t_AsstFWDefltAssistX_HwNm_u8p8[11]	307
t_AsstFWDefltAssistX_HwNm_u8p8[12]	333
t_AsstFWDefltAssistX_HwNm_u8p8[13]	358
t_AsstFWDefltAssistX_HwNm_u8p8[14]	384
t_AsstFWDefltAssistX_HwNm_u8p8[15]	410
t_AsstFWDefltAssistX_HwNm_u8p8[16]	435
t_AsstFWDefltAssistX_HwNm_u8p8[17]	461
t_AsstFWDefltAssistX_HwNm_u8p8[18]	486
t_AsstFWDefltAssistX_HwNm_u8p8[19]	512
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	17613
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	21504
t_AsstFWPstepNstepThresh_Cnt_u16[0]	198
t_AsstFWPstepNstepThresh_Cnt_u16[1]	511
t_AsstFWVehSpd_Kph_u9p7[0]	7296
t_AsstFWVehSpd_Kph_u9p7[1]	7424
t_AsstFWVehSpd_Kph_u9p7[2]	7552
t_AsstFWVehSpd_Kph_u9p7[3]	7680
t_AsstFWVehSpd_Kph_u9p7[4]	7808
t_AsstFWVehSpd_Kph_u9p7[5]	7936
t_AsstFWVehSpd_Kph_u9p7[6]	8064
t_AsstFWVehSpd_Kph_u9p7[7]	8192
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.30000019
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.39999998
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	154.300003
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.879999995	0.879999995 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	511	511 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.454	5.454 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.19999981	5.19999981 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.55999994	2.55999994 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.879999995	0.879999995 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.78 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.300000012
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8364
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.69999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0700000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.400000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.150000006
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	0
k_AsstFWInpLimitHFA_MtrNm_f32	1
k_AsstFWInpLimitHysComp_MtrNm_f32	6.5999999
k_AsstFWNstep_Cnt_u16	2688
k_AsstFWPstep_Cnt_u16	2337
k_RestoreThresh_MtrNm_f32	2.23000002
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	0

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	51
t_AsstFWDefltAssistX_HwNm_u8p8[1]	77
t_AsstFWDefltAssistX_HwNm_u8p8[2]	102
t_AsstFWDefltAssistX_HwNm_u8p8[3]	128
t_AsstFWDefltAssistX_HwNm_u8p8[4]	154
t_AsstFWDefltAssistX_HwNm_u8p8[5]	179
t_AsstFWDefltAssistX_HwNm_u8p8[6]	205
t_AsstFWDefltAssistX_HwNm_u8p8[7]	230
t_AsstFWDefltAssistX_HwNm_u8p8[8]	256
t_AsstFWDefltAssistX_HwNm_u8p8[9]	282
t_AsstFWDefltAssistX_HwNm_u8p8[10]	307
t_AsstFWDefltAssistX_HwNm_u8p8[11]	333
t_AsstFWDefltAssistX_HwNm_u8p8[12]	358
t_AsstFWDefltAssistX_HwNm_u8p8[13]	384
t_AsstFWDefltAssistX_HwNm_u8p8[14]	410
t_AsstFWDefltAssistX_HwNm_u8p8[15]	435
t_AsstFWDefltAssistX_HwNm_u8p8[16]	461
t_AsstFWDefltAssistX_HwNm_u8p8[17]	486
t_AsstFWDefltAssistX_HwNm_u8p8[18]	512
t_AsstFWDefltAssistX_HwNm_u8p8[19]	538
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	17818
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	21709
t_AsstFWPstepNstepThresh_Cnt_u16[0]	199
t_AsstFWPstepNstepThresh_Cnt_u16[1]	515
t_AsstFWVehSpd_Kph_u9p7[0]	10240
t_AsstFWVehSpd_Kph_u9p7[1]	10368
t_AsstFWVehSpd_Kph_u9p7[2]	10496
t_AsstFWVehSpd_Kph_u9p7[3]	10624
t_AsstFWVehSpd_Kph_u9p7[4]	10752
t_AsstFWVehSpd_Kph_u9p7[5]	10880
t_AsstFWVehSpd_Kph_u9p7[6]	11008
t_AsstFWVehSpd_Kph_u9p7[7]	11136
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.42999983
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.70000005
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	165.100006
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	77
t_AsstFWDefltAssistX_HwNm_u8p8[1]	102
t_AsstFWDefltAssistX_HwNm_u8p8[2]	128
t_AsstFWDefltAssistX_HwNm_u8p8[3]	154
t_AsstFWDefltAssistX_HwNm_u8p8[4]	179
t_AsstFWDefltAssistX_HwNm_u8p8[5]	205
t_AsstFWDefltAssistX_HwNm_u8p8[6]	230
t_AsstFWDefltAssistX_HwNm_u8p8[7]	256
t_AsstFWDefltAssistX_HwNm_u8p8[8]	282
t_AsstFWDefltAssistX_HwNm_u8p8[9]	307
t_AsstFWDefltAssistX_HwNm_u8p8[10]	333
t_AsstFWDefltAssistX_HwNm_u8p8[11]	358
t_AsstFWDefltAssistX_HwNm_u8p8[12]	384
t_AsstFWDefltAssistX_HwNm_u8p8[13]	410
t_AsstFWDefltAssistX_HwNm_u8p8[14]	435
t_AsstFWDefltAssistX_HwNm_u8p8[15]	461
t_AsstFWDefltAssistX_HwNm_u8p8[16]	486
t_AsstFWDefltAssistX_HwNm_u8p8[17]	512
t_AsstFWDefltAssistX_HwNm_u8p8[18]	538
t_AsstFWDefltAssistX_HwNm_u8p8[19]	563
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	18022
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	21914
t_AsstFWPstepNstepThresh_Cnt_u16[0]	200
t_AsstFWPstepNstepThresh_Cnt_u16[1]	519
t_AsstFWVehSpd_Kph_u9p7[0]	13184
t_AsstFWVehSpd_Kph_u9p7[1]	13312
t_AsstFWVehSpd_Kph_u9p7[2]	13440
t_AsstFWVehSpd_Kph_u9p7[3]	13568
t_AsstFWVehSpd_Kph_u9p7[4]	13696
t_AsstFWVehSpd_Kph_u9p7[5]	13824
t_AsstFWVehSpd_Kph_u9p7[6]	13952
t_AsstFWVehSpd_Kph_u9p7[7]	14080
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.55999994
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2.5999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.63199997	2.63199997 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	519	519 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.68479991	1.68480003 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.5	3.5 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4	4 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.80 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0199999996
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8610
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-5.9000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0299999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	2
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.600000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.170000002
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.5
k_AsstFWInpLimitHFA_MtrNm_f32	3
k_AsstFWInpLimitHysComp_MtrNm_f32	6.80000019
k_AsstFWNstep_Cnt_u16	2440
k_AsstFWPstep_Cnt_u16	1599
k_RestoreThresh_MtrNm_f32	2.25
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	102
t_AsstFWDefltAssistX_HwNm_u8p8[1]	128
t_AsstFWDefltAssistX_HwNm_u8p8[2]	154
t_AsstFWDefltAssistX_HwNm_u8p8[3]	179
t_AsstFWDefltAssistX_HwNm_u8p8[4]	205
t_AsstFWDefltAssistX_HwNm_u8p8[5]	230
t_AsstFWDefltAssistX_HwNm_u8p8[6]	256
t_AsstFWDefltAssistX_HwNm_u8p8[7]	282
t_AsstFWDefltAssistX_HwNm_u8p8[8]	307
t_AsstFWDefltAssistX_HwNm_u8p8[9]	333
t_AsstFWDefltAssistX_HwNm_u8p8[10]	358
t_AsstFWDefltAssistX_HwNm_u8p8[11]	384
t_AsstFWDefltAssistX_HwNm_u8p8[12]	410
t_AsstFWDefltAssistX_HwNm_u8p8[13]	435
t_AsstFWDefltAssistX_HwNm_u8p8[14]	461
t_AsstFWDefltAssistX_HwNm_u8p8[15]	486
t_AsstFWDefltAssistX_HwNm_u8p8[16]	512
t_AsstFWDefltAssistX_HwNm_u8p8[17]	538
t_AsstFWDefltAssistX_HwNm_u8p8[18]	563
t_AsstFWDefltAssistX_HwNm_u8p8[19]	589
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	18227
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	22118
t_AsstFWPstepNstepThresh_Cnt_u16[0]	201
t_AsstFWPstepNstepThresh_Cnt_u16[1]	523
t_AsstFWVehSpd_Kph_u9p7[0]	16128
t_AsstFWVehSpd_Kph_u9p7[1]	16256
t_AsstFWVehSpd_Kph_u9p7[2]	16384
t_AsstFWVehSpd_Kph_u9p7[3]	16512
t_AsstFWVehSpd_Kph_u9p7[4]	16640
t_AsstFWVehSpd_Kph_u9p7[5]	16768
t_AsstFWVehSpd_Kph_u9p7[6]	16896
t_AsstFWVehSpd_Kph_u9p7[7]	17024
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.69000006
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4.5999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	187.300003
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.07800007	1.07799995 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	523	523 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.35900009	1.35899997 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.79999971	2.79999995 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5	5 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.81 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0299999993
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	3.29999995
k_AsstFWInpLimitHysComp_MtrNm_f32	3.9000001
k_AsstFWNstep_Cnt_u16	3690
k_AsstFWPstep_Cnt_u16	2706
k_RestoreThresh_MtrNm_f32	2.25999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	12288

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	14336

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	128
t_AsstFWDefltAssistX_HwNm_u8p8[1]	154
t_AsstFWDefltAssistX_HwNm_u8p8[2]	179
t_AsstFWDefltAssistX_HwNm_u8p8[3]	205
t_AsstFWDefltAssistX_HwNm_u8p8[4]	230
t_AsstFWDefltAssistX_HwNm_u8p8[5]	256
t_AsstFWDefltAssistX_HwNm_u8p8[6]	282
t_AsstFWDefltAssistX_HwNm_u8p8[7]	307
t_AsstFWDefltAssistX_HwNm_u8p8[8]	333
t_AsstFWDefltAssistX_HwNm_u8p8[9]	358
t_AsstFWDefltAssistX_HwNm_u8p8[10]	384
t_AsstFWDefltAssistX_HwNm_u8p8[11]	410
t_AsstFWDefltAssistX_HwNm_u8p8[12]	435
t_AsstFWDefltAssistX_HwNm_u8p8[13]	461
t_AsstFWDefltAssistX_HwNm_u8p8[14]	486
t_AsstFWDefltAssistX_HwNm_u8p8[15]	512
t_AsstFWDefltAssistX_HwNm_u8p8[16]	538
t_AsstFWDefltAssistX_HwNm_u8p8[17]	563
t_AsstFWDefltAssistX_HwNm_u8p8[18]	589
t_AsstFWDefltAssistX_HwNm_u8p8[19]	614
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	22323
t_AsstFWPstepNstepThresh_Cnt_u16[0]	202
t_AsstFWPstepNstepThresh_Cnt_u16[1]	527
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
t_AsstFWVehSpd_Kph_u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	123.099998
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.99000001	0.99000001 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0	0 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.19999981	8.19999981 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.30499983	4.30499983 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-1	-1 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.15699983	3.15700006 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.99000001	0.99000001 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.19999981	8.19999981 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x00	0x00	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x00	0x00	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.82 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-8.80000019
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.200000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	65535
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0599999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.89999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0900000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0399999991
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.20000005
k_AsstFWInpLimitHFA_MtrNm_f32	4.4000001
k_AsstFWInpLimitHysComp_MtrNm_f32	4.0999999
k_AsstFWNstep_Cnt_u16	3813
k_AsstFWPstep_Cnt_u16	2829
k_RestoreThresh_MtrNm_f32	2.26999998
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	14336

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	154
t_AsstFWDefltAssistX_HwNm_u8p8[1]	179
t_AsstFWDefltAssistX_HwNm_u8p8[2]	205
t_AsstFWDefltAssistX_HwNm_u8p8[3]	230
t_AsstFWDefltAssistX_HwNm_u8p8[4]	256
t_AsstFWDefltAssistX_HwNm_u8p8[5]	282
t_AsstFWDefltAssistX_HwNm_u8p8[6]	307
t_AsstFWDefltAssistX_HwNm_u8p8[7]	333
t_AsstFWDefltAssistX_HwNm_u8p8[8]	358
t_AsstFWDefltAssistX_HwNm_u8p8[9]	384
t_AsstFWDefltAssistX_HwNm_u8p8[10]	410
t_AsstFWDefltAssistX_HwNm_u8p8[11]	435
t_AsstFWDefltAssistX_HwNm_u8p8[12]	461
t_AsstFWDefltAssistX_HwNm_u8p8[13]	486
t_AsstFWDefltAssistX_HwNm_u8p8[14]	512
t_AsstFWDefltAssistX_HwNm_u8p8[15]	538
t_AsstFWDefltAssistX_HwNm_u8p8[16]	563
t_AsstFWDefltAssistX_HwNm_u8p8[17]	589
t_AsstFWDefltAssistX_HwNm_u8p8[18]	614
t_AsstFWDefltAssistX_HwNm_u8p8[19]	640
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	18637
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	22528
t_AsstFWPstepNstepThresh_Cnt_u16[0]	203
t_AsstFWPstepNstepThresh_Cnt_u16[1]	531
t_AsstFWVehSpd_Kph_u9p7[0]	22016
t_AsstFWVehSpd_Kph_u9p7[1]	22144
t_AsstFWVehSpd_Kph_u9p7[2]	22272
t_AsstFWVehSpd_Kph_u9p7[3]	22400
t_AsstFWVehSpd_Kph_u9p7[4]	22528
t_AsstFWVehSpd_Kph_u9p7[5]	22656
t_AsstFWVehSpd_Kph_u9p7[6]	22784
t_AsstFWVehSpd_Kph_u9p7[7]	22912
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	234.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-7.03999996	-7.03999996 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	531	531 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.42399979	5.42399979 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.55000019	7.55000019 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.01599979	4.01599979 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.83 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.300000012
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1000
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	6.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0700000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.600000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.109999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4
k_AsstFWInpLimitHFA_MtrNm_f32	1.39999998
k_AsstFWInpLimitHysComp_MtrNm_f32	4.0999999
k_AsstFWNstep_Cnt_u16	2812
k_AsstFWPstep_Cnt_u16	1968
k_RestoreThresh_MtrNm_f32	2.27999997
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	16384

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	179
t_AsstFWDefltAssistX_HwNm_u8p8[1]	205
t_AsstFWDefltAssistX_HwNm_u8p8[2]	230
t_AsstFWDefltAssistX_HwNm_u8p8[3]	256
t_AsstFWDefltAssistX_HwNm_u8p8[4]	282
t_AsstFWDefltAssistX_HwNm_u8p8[5]	307
t_AsstFWDefltAssistX_HwNm_u8p8[6]	333
t_AsstFWDefltAssistX_HwNm_u8p8[7]	358
t_AsstFWDefltAssistX_HwNm_u8p8[8]	384
t_AsstFWDefltAssistX_HwNm_u8p8[9]	410
t_AsstFWDefltAssistX_HwNm_u8p8[10]	435
t_AsstFWDefltAssistX_HwNm_u8p8[11]	461
t_AsstFWDefltAssistX_HwNm_u8p8[12]	486
t_AsstFWDefltAssistX_HwNm_u8p8[13]	512
t_AsstFWDefltAssistX_HwNm_u8p8[14]	538
t_AsstFWDefltAssistX_HwNm_u8p8[15]	563
t_AsstFWDefltAssistX_HwNm_u8p8[16]	589
t_AsstFWDefltAssistX_HwNm_u8p8[17]	614
t_AsstFWDefltAssistX_HwNm_u8p8[18]	640
t_AsstFWDefltAssistX_HwNm_u8p8[19]	666
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	18842
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	22733
t_AsstFWPstepNstepThresh_Cnt_u16[0]	204
t_AsstFWPstepNstepThresh_Cnt_u16[1]	535
t_AsstFWVehSpd_Kph_u9p7[0]	24960
t_AsstFWVehSpd_Kph_u9p7[1]	25088
t_AsstFWVehSpd_Kph_u9p7[2]	25216
t_AsstFWVehSpd_Kph_u9p7[3]	25344
t_AsstFWVehSpd_Kph_u9p7[4]	25472
t_AsstFWVehSpd_Kph_u9p7[5]	25600
t_AsstFWVehSpd_Kph_u9p7[6]	25728
t_AsstFWVehSpd_Kph_u9p7[7]	25856
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	77.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.769999981	0.769999981 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0	0 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.33099985	6.33099985 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.399999619	0.400000006 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8.32999992	8.32999992 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.769999981	0.769999981 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x00	0x00	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.84 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	200
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	6.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.400000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.119999997
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	1.5
k_AsstFWInpLimitHysComp_MtrNm_f32	4.30000019
k_AsstFWNstep_Cnt_u16	2688
k_AsstFWPstep_Cnt_u16	2091
k_RestoreThresh_MtrNm_f32	2.28999996
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	18432

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	205
t_AsstFWDefltAssistX_HwNm_u8p8[1]	230
t_AsstFWDefltAssistX_HwNm_u8p8[2]	256
t_AsstFWDefltAssistX_HwNm_u8p8[3]	282
t_AsstFWDefltAssistX_HwNm_u8p8[4]	307
t_AsstFWDefltAssistX_HwNm_u8p8[5]	333
t_AsstFWDefltAssistX_HwNm_u8p8[6]	358
t_AsstFWDefltAssistX_HwNm_u8p8[7]	384
t_AsstFWDefltAssistX_HwNm_u8p8[8]	410
t_AsstFWDefltAssistX_HwNm_u8p8[9]	435
t_AsstFWDefltAssistX_HwNm_u8p8[10]	461
t_AsstFWDefltAssistX_HwNm_u8p8[11]	486
t_AsstFWDefltAssistX_HwNm_u8p8[12]	512
t_AsstFWDefltAssistX_HwNm_u8p8[13]	538
t_AsstFWDefltAssistX_HwNm_u8p8[14]	563
t_AsstFWDefltAssistX_HwNm_u8p8[15]	589
t_AsstFWDefltAssistX_HwNm_u8p8[16]	614
t_AsstFWDefltAssistX_HwNm_u8p8[17]	640
t_AsstFWDefltAssistX_HwNm_u8p8[18]	666
t_AsstFWDefltAssistX_HwNm_u8p8[19]	691
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	19046
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	22733
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	22938
t_AsstFWPstepNstepThresh_Cnt_u16[0]	0
t_AsstFWPstepNstepThresh_Cnt_u16[1]	0
t_AsstFWVehSpd_Kph_u9p7[0]	27904
t_AsstFWVehSpd_Kph_u9p7[1]	28032
t_AsstFWVehSpd_Kph_u9p7[2]	28160
t_AsstFWVehSpd_Kph_u9p7[3]	28288
t_AsstFWVehSpd_Kph_u9p7[4]	28416
t_AsstFWVehSpd_Kph_u9p7[5]	28544
t_AsstFWVehSpd_Kph_u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7]	28800
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	88.1999969
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.91400003	2.91400003 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0	0 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.71199989	1.71200001 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0.199999809	0.200000003 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.0480001	2.0480001 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x00	0x00	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.85 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.79999995
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	344
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	6.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.129999995
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.19999981
k_AsstFWInpLimitHFA_MtrNm_f32	1.70000005
k_AsstFWInpLimitHysComp_MtrNm_f32	4.5
k_AsstFWNstep_Cnt_u16	2564
k_AsstFWPstep_Cnt_u16	2214
k_RestoreThresh_MtrNm_f32	3.30999994
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	20480

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefltAssistX_HwNm_u8p8[0]	230
t_AsstFWDefltAssistX_HwNm_u8p8[1]	256
t_AsstFWDefltAssistX_HwNm_u8p8[2]	282
t_AsstFWDefltAssistX_HwNm_u8p8[3]	307
t_AsstFWDefltAssistX_HwNm_u8p8[4]	333
t_AsstFWDefltAssistX_HwNm_u8p8[5]	358
t_AsstFWDefltAssistX_HwNm_u8p8[6]	384
t_AsstFWDefltAssistX_HwNm_u8p8[7]	410
t_AsstFWDefltAssistX_HwNm_u8p8[8]	435
t_AsstFWDefltAssistX_HwNm_u8p8[9]	461
t_AsstFWDefltAssistX_HwNm_u8p8[10]	486
t_AsstFWDefltAssistX_HwNm_u8p8[11]	512
t_AsstFWDefltAssistX_HwNm_u8p8[12]	538
t_AsstFWDefltAssistX_HwNm_u8p8[13]	563
t_AsstFWDefltAssistX_HwNm_u8p8[14]	589
t_AsstFWDefltAssistX_HwNm_u8p8[15]	614
t_AsstFWDefltAssistX_HwNm_u8p8[16]	640
t_AsstFWDefltAssistX_HwNm_u8p8[17]	666
t_AsstFWDefltAssistX_HwNm_u8p8[18]	691
t_AsstFWDefltAssistX_HwNm_u8p8[19]	717
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	19251
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	22733
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	22938
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	23142
t_AsstFWPstepNstepThresh_Cnt_u16[0]	5000
t_AsstFWPstepNstepThresh_Cnt_u16[1]	5000
t_AsstFWVehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1]	30976
t_AsstFWVehSpd_Kph_u9p7[2]	31104
t_AsstFWVehSpd_Kph_u9p7[3]	31232
t_AsstFWVehSpd_Kph_u9p7[4]	31360
t_AsstFWVehSpd_Kph_u9p7[5]	31488
t_AsstFWVehSpd_Kph_u9p7[6]	31616
t_AsstFWVehSpd_Kph_u9p7[7]	31744
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.6500001
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	99.3000031
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.61999989	2.61999989 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	2558	2558 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.29799938	3.2980001 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.10500002	4.10500002 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	0	0 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.12699986	3.12700009 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.29799938	3.2980001 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x00	0x00	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.86 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.200000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	2234
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	6.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0599999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.89999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.600000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.140000001
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.30000019
k_AsstFWInpLimitHFA_MtrNm_f32	1.89999998
k_AsstFWInpLimitHysComp_MtrNm_f32	4.69999981
k_AsstFWNstep_Cnt_u16	2440
k_AsstFWPstep_Cnt_u16	2337
k_RestoreThresh_MtrNm_f32	3.31999993
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-18432

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	22528

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	256
t_AsstFWDefltAssistX_HwNm_u8p8[1]	282
t_AsstFWDefltAssistX_HwNm_u8p8[2]	307
t_AsstFWDefltAssistX_HwNm_u8p8[3]	333
t_AsstFWDefltAssistX_HwNm_u8p8[4]	358
t_AsstFWDefltAssistX_HwNm_u8p8[5]	384
t_AsstFWDefltAssistX_HwNm_u8p8[6]	410
t_AsstFWDefltAssistX_HwNm_u8p8[7]	435
t_AsstFWDefltAssistX_HwNm_u8p8[8]	461
t_AsstFWDefltAssistX_HwNm_u8p8[9]	486
t_AsstFWDefltAssistX_HwNm_u8p8[10]	512
t_AsstFWDefltAssistX_HwNm_u8p8[11]	538
t_AsstFWDefltAssistX_HwNm_u8p8[12]	563
t_AsstFWDefltAssistX_HwNm_u8p8[13]	589
t_AsstFWDefltAssistX_HwNm_u8p8[14]	614
t_AsstFWDefltAssistX_HwNm_u8p8[15]	640
t_AsstFWDefltAssistX_HwNm_u8p8[16]	666
t_AsstFWDefltAssistX_HwNm_u8p8[17]	691
t_AsstFWDefltAssistX_HwNm_u8p8[18]	717
t_AsstFWDefltAssistX_HwNm_u8p8[19]	742
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	19456
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	22733
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	22938
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	23142
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	23347
t_AsstFWPstepNstepThresh_Cnt_u16[0]	207
t_AsstFWPstepNstepThresh_Cnt_u16[1]	547
t_AsstFWVehSpd_Kph_u9p7[0]	33792
t_AsstFWVehSpd_Kph_u9p7[1]	33920
t_AsstFWVehSpd_Kph_u9p7[2]	34048
t_AsstFWVehSpd_Kph_u9p7[3]	34176
t_AsstFWVehSpd_Kph_u9p7[4]	34304
t_AsstFWVehSpd_Kph_u9p7[5]	34432
t_AsstFWVehSpd_Kph_u9p7[6]	34560
t_AsstFWVehSpd_Kph_u9p7[7]	34688
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.78000021
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-4
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	110.099998
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.879999995	0.879999995 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	547	547 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.87799978	4.87799978 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-0.200000286	-0.200000003 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.20599985	4.20599985 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.879999995	0.879999995 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.87 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.300000012
AssistFirewall_ActiveRawAcc_Cnt_M_u16	4554
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	6.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0700000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.400000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.150000006
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.4000001
k_AsstFWInpLimitHFA_MtrNm_f32	2.05999994
k_AsstFWInpLimitHysComp_MtrNm_f32	4.9000001
k_AsstFWNstep_Cnt_u16	2316
k_AsstFWPstep_Cnt_u16	0
k_RestoreThresh_MtrNm_f32	3.32999992
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	0

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	282
t_AsstFWDefltAssistX_HwNm_u8p8[1]	307
t_AsstFWDefltAssistX_HwNm_u8p8[2]	333
t_AsstFWDefltAssistX_HwNm_u8p8[3]	358
t_AsstFWDefltAssistX_HwNm_u8p8[4]	384
t_AsstFWDefltAssistX_HwNm_u8p8[5]	410
t_AsstFWDefltAssistX_HwNm_u8p8[6]	435
t_AsstFWDefltAssistX_HwNm_u8p8[7]	461
t_AsstFWDefltAssistX_HwNm_u8p8[8]	486
t_AsstFWDefltAssistX_HwNm_u8p8[9]	512
t_AsstFWDefltAssistX_HwNm_u8p8[10]	538
t_AsstFWDefltAssistX_HwNm_u8p8[11]	563
t_AsstFWDefltAssistX_HwNm_u8p8[12]	589
t_AsstFWDefltAssistX_HwNm_u8p8[13]	614
t_AsstFWDefltAssistX_HwNm_u8p8[14]	640
t_AsstFWDefltAssistX_HwNm_u8p8[15]	666
t_AsstFWDefltAssistX_HwNm_u8p8[16]	691
t_AsstFWDefltAssistX_HwNm_u8p8[17]	717
t_AsstFWDefltAssistX_HwNm_u8p8[18]	742
t_AsstFWDefltAssistX_HwNm_u8p8[19]	768
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	19661
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22733
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	22938
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	23142
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	23347
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	23552
t_AsstFWPstepNstepThresh_Cnt_u16[0]	208
t_AsstFWPstepNstepThresh_Cnt_u16[1]	551
t_AsstFWVehSpd_Kph_u9p7[0]	36736
t_AsstFWVehSpd_Kph_u9p7[1]	36864
t_AsstFWVehSpd_Kph_u9p7[2]	36992
t_AsstFWVehSpd_Kph_u9p7[3]	37120
t_AsstFWVehSpd_Kph_u9p7[4]	37248
t_AsstFWVehSpd_Kph_u9p7[5]	37376
t_AsstFWVehSpd_Kph_u9p7[6]	37504
t_AsstFWVehSpd_Kph_u9p7[7]	37632
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.90999985
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-6
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	121.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.16999984	2.17000008 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	551	551 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.77799988	5.77799988 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.19999981	6.19999981 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.3349998	3.33500004 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.88 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.79999995
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	3322
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	6.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.159999996
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.79999995
k_AsstFWInpLimitHFA_MtrNm_f32	2.29999995
k_AsstFWInpLimitHysComp_MtrNm_f32	5.0999999
k_AsstFWNstep_Cnt_u16	2192
k_AsstFWPstep_Cnt_u16	5000
k_RestoreThresh_MtrNm_f32	3.33999991
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	0

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	307
t_AsstFWDefltAssistX_HwNm_u8p8[1]	333
t_AsstFWDefltAssistX_HwNm_u8p8[2]	358
t_AsstFWDefltAssistX_HwNm_u8p8[3]	384
t_AsstFWDefltAssistX_HwNm_u8p8[4]	410
t_AsstFWDefltAssistX_HwNm_u8p8[5]	435
t_AsstFWDefltAssistX_HwNm_u8p8[6]	461
t_AsstFWDefltAssistX_HwNm_u8p8[7]	486
t_AsstFWDefltAssistX_HwNm_u8p8[8]	512
t_AsstFWDefltAssistX_HwNm_u8p8[9]	538
t_AsstFWDefltAssistX_HwNm_u8p8[10]	563
t_AsstFWDefltAssistX_HwNm_u8p8[11]	589
t_AsstFWDefltAssistX_HwNm_u8p8[12]	614
t_AsstFWDefltAssistX_HwNm_u8p8[13]	640
t_AsstFWDefltAssistX_HwNm_u8p8[14]	666
t_AsstFWDefltAssistX_HwNm_u8p8[15]	691
t_AsstFWDefltAssistX_HwNm_u8p8[16]	717
t_AsstFWDefltAssistX_HwNm_u8p8[17]	742
t_AsstFWDefltAssistX_HwNm_u8p8[18]	768
t_AsstFWDefltAssistX_HwNm_u8p8[19]	794
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	19866
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	22733
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22938
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	23142
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	23347
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	23552
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	23757
t_AsstFWPstepNstepThresh_Cnt_u16[0]	209
t_AsstFWPstepNstepThresh_Cnt_u16[1]	555
t_AsstFWVehSpd_Kph_u9p7[0]	39680
t_AsstFWVehSpd_Kph_u9p7[1]	39808
t_AsstFWVehSpd_Kph_u9p7[2]	39936
t_AsstFWVehSpd_Kph_u9p7[3]	40064
t_AsstFWVehSpd_Kph_u9p7[4]	40192
t_AsstFWVehSpd_Kph_u9p7[5]	40320
t_AsstFWVehSpd_Kph_u9p7[6]	40448
t_AsstFWVehSpd_Kph_u9p7[7]	40576
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.03999996
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	132.300003
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.63199997	2.63199997 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	555	555 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.55200005	1.55200005 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.5	6.5 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.28399992	4.28399992 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.89 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0199999996
AssistFirewall_ActiveRawAcc_Cnt_M_u16	222
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	6.69999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0299999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	2
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.600000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.170000002
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.9000001
k_AsstFWInpLimitHFA_MtrNm_f32	3.29999995
k_AsstFWInpLimitHysComp_MtrNm_f32	5.30000019
k_AsstFWNstep_Cnt_u16	2000
k_AsstFWPstep_Cnt_u16	2500
k_RestoreThresh_MtrNm_f32	3.3499999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	333
t_AsstFWDefltAssistX_HwNm_u8p8[1]	358
t_AsstFWDefltAssistX_HwNm_u8p8[2]	384
t_AsstFWDefltAssistX_HwNm_u8p8[3]	410
t_AsstFWDefltAssistX_HwNm_u8p8[4]	435
t_AsstFWDefltAssistX_HwNm_u8p8[5]	461
t_AsstFWDefltAssistX_HwNm_u8p8[6]	486
t_AsstFWDefltAssistX_HwNm_u8p8[7]	512
t_AsstFWDefltAssistX_HwNm_u8p8[8]	538
t_AsstFWDefltAssistX_HwNm_u8p8[9]	563
t_AsstFWDefltAssistX_HwNm_u8p8[10]	589
t_AsstFWDefltAssistX_HwNm_u8p8[11]	614
t_AsstFWDefltAssistX_HwNm_u8p8[12]	640
t_AsstFWDefltAssistX_HwNm_u8p8[13]	666
t_AsstFWDefltAssistX_HwNm_u8p8[14]	691
t_AsstFWDefltAssistX_HwNm_u8p8[15]	717
t_AsstFWDefltAssistX_HwNm_u8p8[16]	742
t_AsstFWDefltAssistX_HwNm_u8p8[17]	768
t_AsstFWDefltAssistX_HwNm_u8p8[18]	794
t_AsstFWDefltAssistX_HwNm_u8p8[19]	819
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	20070
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	22733
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	22938
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	23142
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	23347
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	23552
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	23757
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	23962
t_AsstFWPstepNstepThresh_Cnt_u16[0]	210
t_AsstFWPstepNstepThresh_Cnt_u16[1]	559
t_AsstFWVehSpd_Kph_u9p7[0]	42624
t_AsstFWVehSpd_Kph_u9p7[1]	42752
t_AsstFWVehSpd_Kph_u9p7[2]	42880
t_AsstFWVehSpd_Kph_u9p7[3]	43008
t_AsstFWVehSpd_Kph_u9p7[4]	43136
t_AsstFWVehSpd_Kph_u9p7[5]	43264
t_AsstFWVehSpd_Kph_u9p7[6]	43392
t_AsstFWVehSpd_Kph_u9p7[7]	43520
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.17000008
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	143.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.07800007	1.07799995 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	559	559 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.37100005	1.37100005 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.4000001	6.4000001 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.34000003	1.34000003 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.90 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	344
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	6.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.400000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0900000036
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4
k_AsstFWInpLimitHFA_MtrNm_f32	4.30000019
k_AsstFWInpLimitHysComp_MtrNm_f32	2
k_AsstFWNstep_Cnt_u16	0
k_AsstFWPstep_Cnt_u16	200
k_RestoreThresh_MtrNm_f32	3.3599999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	22528
t_AsstFWDefltAssistX_HwNm_u8p8[0]	358
t_AsstFWDefltAssistX_HwNm_u8p8[1]	384
t_AsstFWDefltAssistX_HwNm_u8p8[2]	410
t_AsstFWDefltAssistX_HwNm_u8p8[3]	435
t_AsstFWDefltAssistX_HwNm_u8p8[4]	461
t_AsstFWDefltAssistX_HwNm_u8p8[5]	486
t_AsstFWDefltAssistX_HwNm_u8p8[6]	512
t_AsstFWDefltAssistX_HwNm_u8p8[7]	538
t_AsstFWDefltAssistX_HwNm_u8p8[8]	563
t_AsstFWDefltAssistX_HwNm_u8p8[9]	589
t_AsstFWDefltAssistX_HwNm_u8p8[10]	614
t_AsstFWDefltAssistX_HwNm_u8p8[11]	640
t_AsstFWDefltAssistX_HwNm_u8p8[12]	666
t_AsstFWDefltAssistX_HwNm_u8p8[13]	691
t_AsstFWDefltAssistX_HwNm_u8p8[14]	717
t_AsstFWDefltAssistX_HwNm_u8p8[15]	742
t_AsstFWDefltAssistX_HwNm_u8p8[16]	768
t_AsstFWDefltAssistX_HwNm_u8p8[17]	794
t_AsstFWDefltAssistX_HwNm_u8p8[18]	819
t_AsstFWDefltAssistX_HwNm_u8p8[19]	845
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	20275
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	20685
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	20890
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	21094
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	21299
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	21504
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	21709
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	21914
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	22118
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	22323
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	22733
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	22938
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	23142
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	23347
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	23552
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	23757
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	23962
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	24166
t_AsstFWPstepNstepThresh_Cnt_u16[0]	211
t_AsstFWPstepNstepThresh_Cnt_u16[1]	563
t_AsstFWVehSpd_Kph_u9p7[0]	45568
t_AsstFWVehSpd_Kph_u9p7[1]	45696
t_AsstFWVehSpd_Kph_u9p7[2]	45824
t_AsstFWVehSpd_Kph_u9p7[3]	45952
t_AsstFWVehSpd_Kph_u9p7[4]	46080
t_AsstFWVehSpd_Kph_u9p7[5]	46208
t_AsstFWVehSpd_Kph_u9p7[6]	46336
t_AsstFWVehSpd_Kph_u9p7[7]	46464
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.30000019
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.39999998
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	154.100006
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.78999996	2.78999996 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	544	544 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.26499987	4.26499987 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5	5 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.08999991	2.08999991 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.91 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.79999995
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.200000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	2212
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	6.9000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0599999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.89999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.100000001
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	5.30000019
k_AsstFWInpLimitHysComp_MtrNm_f32	1
k_AsstFWNstep_Cnt_u16	5000
k_AsstFWPstep_Cnt_u16	44
k_RestoreThresh_MtrNm_f32	3.36999989
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	10240

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576
t_AsstFWDefltAssistX_HwNm_u8p8[0]	384
t_AsstFWDefltAssistX_HwNm_u8p8[1]	410
t_AsstFWDefltAssistX_HwNm_u8p8[2]	435
t_AsstFWDefltAssistX_HwNm_u8p8[3]	461
t_AsstFWDefltAssistX_HwNm_u8p8[4]	486
t_AsstFWDefltAssistX_HwNm_u8p8[5]	512
t_AsstFWDefltAssistX_HwNm_u8p8[6]	538
t_AsstFWDefltAssistX_HwNm_u8p8[7]	563
t_AsstFWDefltAssistX_HwNm_u8p8[8]	589
t_AsstFWDefltAssistX_HwNm_u8p8[9]	614
t_AsstFWDefltAssistX_HwNm_u8p8[10]	640
t_AsstFWDefltAssistX_HwNm_u8p8[11]	666
t_AsstFWDefltAssistX_HwNm_u8p8[12]	691
t_AsstFWDefltAssistX_HwNm_u8p8[13]	717
t_AsstFWDefltAssistX_HwNm_u8p8[14]	742
t_AsstFWDefltAssistX_HwNm_u8p8[15]	768
t_AsstFWDefltAssistX_HwNm_u8p8[16]	794
t_AsstFWDefltAssistX_HwNm_u8p8[17]	819
t_AsstFWDefltAssistX_HwNm_u8p8[18]	845
t_AsstFWDefltAssistX_HwNm_u8p8[19]	870
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	-184
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	-164
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	-143
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	-123
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	-102
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	-82
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	-61
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	-41
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	-20
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	0
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	20
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	41
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	61
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	82
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	102
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	123
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	143
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	164
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	184
t_AsstFWPstepNstepThresh_Cnt_u16[0]	212
t_AsstFWPstepNstepThresh_Cnt_u16[1]	567
t_AsstFWVehSpd_Kph_u9p7[0]	1408
t_AsstFWVehSpd_Kph_u9p7[1]	1536
t_AsstFWVehSpd_Kph_u9p7[2]	1664
t_AsstFWVehSpd_Kph_u9p7[3]	1792
t_AsstFWVehSpd_Kph_u9p7[4]	1920
t_AsstFWVehSpd_Kph_u9p7[5]	2048
t_AsstFWVehSpd_Kph_u9p7[6]	2176
t_AsstFWVehSpd_Kph_u9p7[7]	2304
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.42999983
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.70000005
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	165.300003
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.24000001	2.24000001 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	567	567 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-0.100097656	-0.100097656 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.20200014	5.20200014 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2	2 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3	3 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-0.100097656	-0.100097656 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.92 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.300000012
AssistFirewall_ActiveRawAcc_Cnt_M_u16	334
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	7
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0700000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00999999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.600000024
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.109999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.19999981
k_AsstFWInpLimitHFA_MtrNm_f32	6.30000019
k_AsstFWInpLimitHysComp_MtrNm_f32	1
k_AsstFWNstep_Cnt_u16	2500
k_AsstFWPstep_Cnt_u16	21
k_RestoreThresh_MtrNm_f32	3.38000011
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	0

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	410
t_AsstFWDefltAssistX_HwNm_u8p8[1]	435
t_AsstFWDefltAssistX_HwNm_u8p8[2]	461
t_AsstFWDefltAssistX_HwNm_u8p8[3]	486
t_AsstFWDefltAssistX_HwNm_u8p8[4]	512
t_AsstFWDefltAssistX_HwNm_u8p8[5]	538
t_AsstFWDefltAssistX_HwNm_u8p8[6]	563
t_AsstFWDefltAssistX_HwNm_u8p8[7]	589
t_AsstFWDefltAssistX_HwNm_u8p8[8]	614
t_AsstFWDefltAssistX_HwNm_u8p8[9]	640
t_AsstFWDefltAssistX_HwNm_u8p8[10]	666
t_AsstFWDefltAssistX_HwNm_u8p8[11]	691
t_AsstFWDefltAssistX_HwNm_u8p8[12]	717
t_AsstFWDefltAssistX_HwNm_u8p8[13]	742
t_AsstFWDefltAssistX_HwNm_u8p8[14]	768
t_AsstFWDefltAssistX_HwNm_u8p8[15]	794
t_AsstFWDefltAssistX_HwNm_u8p8[16]	819
t_AsstFWDefltAssistX_HwNm_u8p8[17]	845
t_AsstFWDefltAssistX_HwNm_u8p8[18]	870
t_AsstFWDefltAssistX_HwNm_u8p8[19]	896
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	-143
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	-82
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	-20
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	41
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	102
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	164
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	225
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	287
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	348
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	410
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	471
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	532
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	594
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	655
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	717
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	778
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	840
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	901
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	963
t_AsstFWPstepNstepThresh_Cnt_u16[0]	213
t_AsstFWPstepNstepThresh_Cnt_u16[1]	571
t_AsstFWVehSpd_Kph_u9p7[0]	4352
t_AsstFWVehSpd_Kph_u9p7[1]	4480
t_AsstFWVehSpd_Kph_u9p7[2]	4608
t_AsstFWVehSpd_Kph_u9p7[3]	4736
t_AsstFWVehSpd_Kph_u9p7[4]	4864
t_AsstFWVehSpd_Kph_u9p7[5]	4992
t_AsstFWVehSpd_Kph_u9p7[6]	5120
t_AsstFWVehSpd_Kph_u9p7[7]	5248
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5.55999994
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2.5999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176.399994
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.07000005	1.07000005 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	355	355 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	5.81680965	5.81681013 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.21899986	6.21899986 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.79999971	2.79999995 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.21999979	4.21999979 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	5.81680965	5.81681013 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x00	0x00	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.93 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.79999995
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8118
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.129999995
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.5
k_AsstFWInpLimitHFA_MtrNm_f32	8.80000019
k_AsstFWInpLimitHysComp_MtrNm_f32	6.38000011
k_AsstFWNstep_Cnt_u16	2192
k_AsstFWPstep_Cnt_u16	2091
k_RestoreThresh_MtrNm_f32	3.3900001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	12288

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	435
t_AsstFWDefltAssistX_HwNm_u8p8[1]	461
t_AsstFWDefltAssistX_HwNm_u8p8[2]	486
t_AsstFWDefltAssistX_HwNm_u8p8[3]	512
t_AsstFWDefltAssistX_HwNm_u8p8[4]	538
t_AsstFWDefltAssistX_HwNm_u8p8[5]	563
t_AsstFWDefltAssistX_HwNm_u8p8[6]	589
t_AsstFWDefltAssistX_HwNm_u8p8[7]	614
t_AsstFWDefltAssistX_HwNm_u8p8[8]	640
t_AsstFWDefltAssistX_HwNm_u8p8[9]	666
t_AsstFWDefltAssistX_HwNm_u8p8[10]	691
t_AsstFWDefltAssistX_HwNm_u8p8[11]	717
t_AsstFWDefltAssistX_HwNm_u8p8[12]	742
t_AsstFWDefltAssistX_HwNm_u8p8[13]	768
t_AsstFWDefltAssistX_HwNm_u8p8[14]	794
t_AsstFWDefltAssistX_HwNm_u8p8[15]	819
t_AsstFWDefltAssistX_HwNm_u8p8[16]	845
t_AsstFWDefltAssistX_HwNm_u8p8[17]	870
t_AsstFWDefltAssistX_HwNm_u8p8[18]	896
t_AsstFWDefltAssistX_HwNm_u8p8[19]	922
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2458
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2662
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2867
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6349
t_AsstFWPstepNstepThresh_Cnt_u16[0]	214
t_AsstFWPstepNstepThresh_Cnt_u16[1]	575
t_AsstFWVehSpd_Kph_u9p7[0]	7296
t_AsstFWVehSpd_Kph_u9p7[1]	7424
t_AsstFWVehSpd_Kph_u9p7[2]	7552
t_AsstFWVehSpd_Kph_u9p7[3]	7680
t_AsstFWVehSpd_Kph_u9p7[4]	780

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.51999998	2.51999998 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	575	575 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.10009766	3.10009766 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.26999998	4.26999998 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3.5	3.5 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.03999996	2.03999996 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.10009766	3.10009766 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.94 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0900000036
AssistFirewall_ActiveRawAcc_Cnt_M_u16	109
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.89999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0700000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00999999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4
k_AsstFWInpLimitHFA_MtrNm_f32	2.5
k_AsstFWInpLimitHysComp_MtrNm_f32	3.78999996
k_AsstFWNstep_Cnt_u16	3928
k_AsstFWPstep_Cnt_u16	1107
k_RestoreThresh_MtrNm_f32	1.89999998
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	14336

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	461
t_AsstFWDefltAssistX_HwNm_u8p8[1]	486
t_AsstFWDefltAssistX_HwNm_u8p8[2]	512
t_AsstFWDefltAssistX_HwNm_u8p8[3]	538
t_AsstFWDefltAssistX_HwNm_u8p8[4]	563
t_AsstFWDefltAssistX_HwNm_u8p8[5]	589
t_AsstFWDefltAssistX_HwNm_u8p8[6]	614
t_AsstFWDefltAssistX_HwNm_u8p8[7]	640
t_AsstFWDefltAssistX_HwNm_u8p8[8]	666
t_AsstFWDefltAssistX_HwNm_u8p8[9]	691
t_AsstFWDefltAssistX_HwNm_u8p8[10]	717
t_AsstFWDefltAssistX_HwNm_u8p8[11]	742
t_AsstFWDefltAssistX_HwNm_u8p8[12]	768
t_AsstFWDefltAssistX_HwNm_u8p8[13]	794
t_AsstFWDefltAssistX_HwNm_u8p8[14]	819
t_AsstFWDefltAssistX_HwNm_u8p8[15]	845
t_AsstFWDefltAssistX_HwNm_u8p8[16]	870
t_AsstFWDefltAssistX_HwNm_u8p8[17]	896
t_AsstFWDefltAssistX_HwNm_u8p8[18]	922
t_AsstFWDefltAssistX_HwNm_u8p8[19]	947
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2662
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2867
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6554
t_AsstFWPstepNstepThresh_Cnt_u16[0]	215
t_AsstFWPstepNstepThresh_Cnt_u16[1]	579
t_AsstFWVehSpd_Kph_u9p7[0]	10240
t_AsstFWVehSpd_Kph_u9p7[1]	10368
t_AsstFWVehSpd_Kph_u9p7[2]	10496
t_AsstFWVehSpd_Kph_u9p7[3]	10624
t_AsstFWVehSpd_Kph_u9p7[4]	10752
t_AsstFWVehSpd_Kph_u9p7[5]	10880
t_AsstFWVehSpd_Kph_u9p7[6]	11008
t_AsstFWVehSpd_Kph_u9p7[7]	11136
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	9
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90.1999969
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.82099986	2.8210001 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	579	579 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.20019531	3.20019531 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.63199997	2.63199997 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.74300003	4.74300003 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.18900001	1.18900001 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.20019531	3.20019531 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.95 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0900000036
AssistFirewall_ActiveRawAcc_Cnt_M_u16	109
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.89999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0700000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00999999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4
k_AsstFWInpLimitHFA_MtrNm_f32	2.5
k_AsstFWInpLimitHysComp_MtrNm_f32	3.78999996
k_AsstFWNstep_Cnt_u16	3928
k_AsstFWPstep_Cnt_u16	1107
k_RestoreThresh_MtrNm_f32	1.89999998
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	16384

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	14336

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	486
t_AsstFWDefltAssistX_HwNm_u8p8[1]	512
t_AsstFWDefltAssistX_HwNm_u8p8[2]	538
t_AsstFWDefltAssistX_HwNm_u8p8[3]	563
t_AsstFWDefltAssistX_HwNm_u8p8[4]	589
t_AsstFWDefltAssistX_HwNm_u8p8[5]	614
t_AsstFWDefltAssistX_HwNm_u8p8[6]	640
t_AsstFWDefltAssistX_HwNm_u8p8[7]	666
t_AsstFWDefltAssistX_HwNm_u8p8[8]	691
t_AsstFWDefltAssistX_HwNm_u8p8[9]	717
t_AsstFWDefltAssistX_HwNm_u8p8[10]	742
t_AsstFWDefltAssistX_HwNm_u8p8[11]	768
t_AsstFWDefltAssistX_HwNm_u8p8[12]	794
t_AsstFWDefltAssistX_HwNm_u8p8[13]	819
t_AsstFWDefltAssistX_HwNm_u8p8[14]	845
t_AsstFWDefltAssistX_HwNm_u8p8[15]	870
t_AsstFWDefltAssistX_HwNm_u8p8[16]	896
t_AsstFWDefltAssistX_HwNm_u8p8[17]	922
t_AsstFWDefltAssistX_HwNm_u8p8[18]	947
t_AsstFWDefltAssistX_HwNm_u8p8[19]	973
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2867
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6758
t_AsstFWPstepNstepThresh_Cnt_u16[0]	216
t_AsstFWPstepNstepThresh_Cnt_u16[1]	583
t_AsstFWVehSpd_Kph_u9p7[0]	13184
t_AsstFWVehSpd_Kph_u9p7[1]	13312
t_AsstFWVehSpd_Kph_u9p7[2]	13440
t_AsstFWVehSpd_Kph_u9p7[3]	13568
t_AsstFWVehSpd_Kph_u9p7[4]	13696
t_AsstFWVehSpd_Kph_u9p7[5]	13824
t_AsstFWVehSpd_Kph_u9p7[6]	13952
t_AsstFWVehSpd_Kph_u9p7[7]	14080
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	9
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90.3000031
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.82099986	2.8210001 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	583	583 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.29980469	3.29980469 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.63199997	2.63199997 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.67299986	4.67299986 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.199	1.199 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.29980469	3.29980469 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.96 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.30000019
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.400000006
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11199999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.119999997
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.219999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.80000019
k_AsstFWInpLimitHFA_MtrNm_f32	6.40999985
k_AsstFWInpLimitHysComp_MtrNm_f32	6.71000004
k_AsstFWNstep_Cnt_u16	4052
k_AsstFWPstep_Cnt_u16	2460
k_RestoreThresh_MtrNm_f32	4.42999983
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	18432

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	512
t_AsstFWDefltAssistX_HwNm_u8p8[1]	538
t_AsstFWDefltAssistX_HwNm_u8p8[2]	563
t_AsstFWDefltAssistX_HwNm_u8p8[3]	589
t_AsstFWDefltAssistX_HwNm_u8p8[4]	614
t_AsstFWDefltAssistX_HwNm_u8p8[5]	640
t_AsstFWDefltAssistX_HwNm_u8p8[6]	666
t_AsstFWDefltAssistX_HwNm_u8p8[7]	691
t_AsstFWDefltAssistX_HwNm_u8p8[8]	717
t_AsstFWDefltAssistX_HwNm_u8p8[9]	742
t_AsstFWDefltAssistX_HwNm_u8p8[10]	768
t_AsstFWDefltAssistX_HwNm_u8p8[11]	794
t_AsstFWDefltAssistX_HwNm_u8p8[12]	819
t_AsstFWDefltAssistX_HwNm_u8p8[13]	845
t_AsstFWDefltAssistX_HwNm_u8p8[14]	870
t_AsstFWDefltAssistX_HwNm_u8p8[15]	896
t_AsstFWDefltAssistX_HwNm_u8p8[16]	922
t_AsstFWDefltAssistX_HwNm_u8p8[17]	947
t_AsstFWDefltAssistX_HwNm_u8p8[18]	973
t_AsstFWDefltAssistX_HwNm_u8p8[19]	998
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6963
t_AsstFWPstepNstepThresh_Cnt_u16[0]	217
t_AsstFWPstepNstepThresh_Cnt_u16[1]	587
t_AsstFWVehSpd_Kph_u9p7[0]	16128
t_AsstFWVehSpd_Kph_u9p7[1]	16256
t_AsstFWVehSpd_Kph_u9p7[2]	16384
t_AsstFWVehSpd_Kph_u9p7[3]	16512
t_AsstFWVehSpd_Kph_u9p7[4]	16640
t_AsstFWVehSpd_Kph_u9p7[5]	16768
t_AsstFWVehSpd_Kph_u9p7[6]	16896
t_AsstFWVehSpd_Kph_u9p7[7]	17024
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.19999981
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.5999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.4000001
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.5999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	538
t_AsstFWDefltAssistX_HwNm_u8p8[1]	563
t_AsstFWDefltAssistX_HwNm_u8p8[2]	589
t_AsstFWDefltAssistX_HwNm_u8p8[3]	614
t_AsstFWDefltAssistX_HwNm_u8p8[4]	640
t_AsstFWDefltAssistX_HwNm_u8p8[5]	666
t_AsstFWDefltAssistX_HwNm_u8p8[6]	691
t_AsstFWDefltAssistX_HwNm_u8p8[7]	717
t_AsstFWDefltAssistX_HwNm_u8p8[8]	742
t_AsstFWDefltAssistX_HwNm_u8p8[9]	768
t_AsstFWDefltAssistX_HwNm_u8p8[10]	794
t_AsstFWDefltAssistX_HwNm_u8p8[11]	819
t_AsstFWDefltAssistX_HwNm_u8p8[12]	845
t_AsstFWDefltAssistX_HwNm_u8p8[13]	870
t_AsstFWDefltAssistX_HwNm_u8p8[14]	896
t_AsstFWDefltAssistX_HwNm_u8p8[15]	922
t_AsstFWDefltAssistX_HwNm_u8p8[16]	947
t_AsstFWDefltAssistX_HwNm_u8p8[17]	973
t_AsstFWDefltAssistX_HwNm_u8p8[18]	998
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1024
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7168
t_AsstFWPstepNstepThresh_Cnt_u16[0]	218
t_AsstFWPstepNstepThresh_Cnt_u16[1]	591
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
t_AsstFWVehSpd_Kph_u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.30000019
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.69999981
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.69999981
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	187.100006
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-2.70000005	-2.70000005 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	591	591 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.5	-3.5 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-6.28999996	-6.28999996 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-4.63300037	-4.6329999 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.5369997	-5.53700018 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-3.5	-3.5 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.98 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.5
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.600000024
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8733
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.100000001
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11399996
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.80000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.140000001
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.19999981
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.239999995
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5
k_AsstFWInpLimitHFA_MtrNm_f32	6.42999983
k_AsstFWInpLimitHysComp_MtrNm_f32	6.92999983
k_AsstFWNstep_Cnt_u16	3053
k_AsstFWPstep_Cnt_u16	2706
k_RestoreThresh_MtrNm_f32	4.44999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	563
t_AsstFWDefltAssistX_HwNm_u8p8[1]	589
t_AsstFWDefltAssistX_HwNm_u8p8[2]	614
t_AsstFWDefltAssistX_HwNm_u8p8[3]	640
t_AsstFWDefltAssistX_HwNm_u8p8[4]	666
t_AsstFWDefltAssistX_HwNm_u8p8[5]	691
t_AsstFWDefltAssistX_HwNm_u8p8[6]	717
t_AsstFWDefltAssistX_HwNm_u8p8[7]	742
t_AsstFWDefltAssistX_HwNm_u8p8[8]	768
t_AsstFWDefltAssistX_HwNm_u8p8[9]	794
t_AsstFWDefltAssistX_HwNm_u8p8[10]	819
t_AsstFWDefltAssistX_HwNm_u8p8[11]	845
t_AsstFWDefltAssistX_HwNm_u8p8[12]	870
t_AsstFWDefltAssistX_HwNm_u8p8[13]	896
t_AsstFWDefltAssistX_HwNm_u8p8[14]	922
t_AsstFWDefltAssistX_HwNm_u8p8[15]	947
t_AsstFWDefltAssistX_HwNm_u8p8[16]	973
t_AsstFWDefltAssistX_HwNm_u8p8[17]	998
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1050
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7373
t_AsstFWPstepNstepThresh_Cnt_u16[0]	219
t_AsstFWPstepNstepThresh_Cnt_u16[1]	595
t_AsstFWVehSpd_Kph_u9p7[0]	22016
t_AsstFWVehSpd_Kph_u9p7[1]	22144
t_AsstFWVehSpd_Kph_u9p7[2]	22272
t_AsstFWVehSpd_Kph_u9p7[3]	22400
t_AsstFWVehSpd_Kph_u9p7[4]	22528
t_AsstFWVehSpd_Kph_u9p7[5]	22656
t_AsstFWVehSpd_Kph_u9p7[6]	22784
t_AsstFWVehSpd_Kph_u9p7[7]	22912
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.4000001
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.67000008
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.5999999
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.67000008
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	198.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-2.19999981	-2.20000005 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	595	595 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.60009766	-3.60009766 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-4.05000019	-4.05000019 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.04405499	5.04405451 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.39199972	-5.3920002 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-3.60009766	-3.60009766 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.99 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.5
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0120000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8856
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.109999999
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11500001
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.9000001
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.150000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.25
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	6.44000006
k_AsstFWInpLimitHysComp_MtrNm_f32	7.03999996
k_AsstFWNstep_Cnt_u16	2053
k_AsstFWPstep_Cnt_u16	2829
k_RestoreThresh_MtrNm_f32	4.46000004
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-16384

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefltAssistX_HwNm_u8p8[0]	589
t_AsstFWDefltAssistX_HwNm_u8p8[1]	614
t_AsstFWDefltAssistX_HwNm_u8p8[2]	640
t_AsstFWDefltAssistX_HwNm_u8p8[3]	666
t_AsstFWDefltAssistX_HwNm_u8p8[4]	691
t_AsstFWDefltAssistX_HwNm_u8p8[5]	717
t_AsstFWDefltAssistX_HwNm_u8p8[6]	742
t_AsstFWDefltAssistX_HwNm_u8p8[7]	768
t_AsstFWDefltAssistX_HwNm_u8p8[8]	794
t_AsstFWDefltAssistX_HwNm_u8p8[9]	819
t_AsstFWDefltAssistX_HwNm_u8p8[10]	845
t_AsstFWDefltAssistX_HwNm_u8p8[11]	870
t_AsstFWDefltAssistX_HwNm_u8p8[12]	896
t_AsstFWDefltAssistX_HwNm_u8p8[13]	922
t_AsstFWDefltAssistX_HwNm_u8p8[14]	947
t_AsstFWDefltAssistX_HwNm_u8p8[15]	973
t_AsstFWDefltAssistX_HwNm_u8p8[16]	998
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1075
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7578
t_AsstFWPstepNstepThresh_Cnt_u16[0]	220
t_AsstFWPstepNstepThresh_Cnt_u16[1]	599
t_AsstFWVehSpd_Kph_u9p7[0]	24960
t_AsstFWVehSpd_Kph_u9p7[1]	25088
t_AsstFWVehSpd_Kph_u9p7[2]	25216
t_AsstFWVehSpd_Kph_u9p7[3]	25344
t_AsstFWVehSpd_Kph_u9p7[4]	25472
t_AsstFWVehSpd_Kph_u9p7[5]	25600
t_AsstFWVehSpd_Kph_u9p7[6]	25728
t_AsstFWVehSpd_Kph_u9p7[7]	25856
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.5
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.11000013
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7.32999992
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	209.399994
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.43400002	5.43400002 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	599	599 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.70019531	3.70019531 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.24259996	-5.24259996 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.48147964	5.48147964 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.82499981	5.82499981 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.70019531	3.70019531 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.100 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.5999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0130000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8979
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.119999997
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11600006
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.159999996
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.19999981
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.25999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.19999981
k_AsstFWInpLimitHFA_MtrNm_f32	6.44999981
k_AsstFWInpLimitHysComp_MtrNm_f32	7.1500001
k_AsstFWNstep_Cnt_u16	1053
k_AsstFWPstep_Cnt_u16	2952
k_RestoreThresh_MtrNm_f32	4.46999979
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-14336

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	614
t_AsstFWDefltAssistX_HwNm_u8p8[1]	640
t_AsstFWDefltAssistX_HwNm_u8p8[2]	666
t_AsstFWDefltAssistX_HwNm_u8p8[3]	691
t_AsstFWDefltAssistX_HwNm_u8p8[4]	717
t_AsstFWDefltAssistX_HwNm_u8p8[5]	742
t_AsstFWDefltAssistX_HwNm_u8p8[6]	768
t_AsstFWDefltAssistX_HwNm_u8p8[7]	794
t_AsstFWDefltAssistX_HwNm_u8p8[8]	819
t_AsstFWDefltAssistX_HwNm_u8p8[9]	845
t_AsstFWDefltAssistX_HwNm_u8p8[10]	870
t_AsstFWDefltAssistX_HwNm_u8p8[11]	896
t_AsstFWDefltAssistX_HwNm_u8p8[12]	922
t_AsstFWDefltAssistX_HwNm_u8p8[13]	947
t_AsstFWDefltAssistX_HwNm_u8p8[14]	973
t_AsstFWDefltAssistX_HwNm_u8p8[15]	998
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1101
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7782
t_AsstFWPstepNstepThresh_Cnt_u16[0]	221
t_AsstFWPstepNstepThresh_Cnt_u16[1]	603
t_AsstFWVehSpd_Kph_u9p7[0]	27904
t_AsstFWVehSpd_Kph_u9p7[1]	28032
t_AsstFWVehSpd_Kph_u9p7[2]	28160
t_AsstFWVehSpd_Kph_u9p7[3]	28288
t_AsstFWVehSpd_Kph_u9p7[4]	28416
t_AsstFWVehSpd_Kph_u9p7[5]	28544
t_AsstFWVehSpd_Kph_u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7]	28800
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.5999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.19999981
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.21999979
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7.44000006
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	220.5
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.52719975	5.52720022 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	603	603 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.79980469	3.79980469 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.31799984	-5.31799984 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.67999983	5.67999983 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.14799976	6.14799976 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.79980469	3.79980469 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.101 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.69999981
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0140000004
AssistFirewall_ActiveRawAcc_Cnt_M_u16	9102
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.69999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.129999995
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11699998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.170000002
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.30000019
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.270000011
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.30000019
k_AsstFWInpLimitHFA_MtrNm_f32	6.46000004
k_AsstFWInpLimitHysComp_MtrNm_f32	7.26000023
k_AsstFWNstep_Cnt_u16	53
k_AsstFWPstep_Cnt_u16	3075
k_RestoreThresh_MtrNm_f32	4.48000002
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-12288

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	640
t_AsstFWDefltAssistX_HwNm_u8p8[1]	666
t_AsstFWDefltAssistX_HwNm_u8p8[2]	691
t_AsstFWDefltAssistX_HwNm_u8p8[3]	717
t_AsstFWDefltAssistX_HwNm_u8p8[4]	742
t_AsstFWDefltAssistX_HwNm_u8p8[5]	768
t_AsstFWDefltAssistX_HwNm_u8p8[6]	794
t_AsstFWDefltAssistX_HwNm_u8p8[7]	819
t_AsstFWDefltAssistX_HwNm_u8p8[8]	845
t_AsstFWDefltAssistX_HwNm_u8p8[9]	870
t_AsstFWDefltAssistX_HwNm_u8p8[10]	896
t_AsstFWDefltAssistX_HwNm_u8p8[11]	922
t_AsstFWDefltAssistX_HwNm_u8p8[12]	947
t_AsstFWDefltAssistX_HwNm_u8p8[13]	973
t_AsstFWDefltAssistX_HwNm_u8p8[14]	998
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1126
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7987
t_AsstFWPstepNstepThresh_Cnt_u16[0]	222
t_AsstFWPstepNstepThresh_Cnt_u16[1]	607
t_AsstFWVehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1]	30976
t_AsstFWVehSpd_Kph_u9p7[2]	31104
t_AsstFWVehSpd_Kph_u9p7[3]	31232
t_AsstFWVehSpd_Kph_u9p7[4]	31360
t_AsstFWVehSpd_Kph_u9p7[5]	31488
t_AsstFWVehSpd_Kph_u9p7[6]	31616
t_AsstFWVehSpd_Kph_u9p7[7]	31744
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.69999981
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.88999987
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.32999992
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7.55000019
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	231.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.62019968	5.62020016 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	607	607 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.89990234	3.89990234 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-3.86439991	-3.86439991 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.98903036	6.98903036 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.78900003	3.78900003 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.89990234	3.89990234 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.102 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.80000019
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0149999997
AssistFirewall_ActiveRawAcc_Cnt_M_u16	9225
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.140000001
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11800003
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.19999981
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.180000007
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.4000001
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.280000001
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.4000001
k_AsstFWInpLimitHFA_MtrNm_f32	6.46999979
k_AsstFWInpLimitHysComp_MtrNm_f32	7.36999989
k_AsstFWNstep_Cnt_u16	123
k_AsstFWPstep_Cnt_u16	3198
k_RestoreThresh_MtrNm_f32	4.48999977
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-10240

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	0
t_AsstFWDefltAssistX_HwNm_u8p8[1]	0
t_AsstFWDefltAssistX_HwNm_u8p8[2]	0
t_AsstFWDefltAssistX_HwNm_u8p8[3]	0
t_AsstFWDefltAssistX_HwNm_u8p8[4]	0
t_AsstFWDefltAssistX_HwNm_u8p8[5]	0
t_AsstFWDefltAssistX_HwNm_u8p8[6]	0
t_AsstFWDefltAssistX_HwNm_u8p8[7]	0
t_AsstFWDefltAssistX_HwNm_u8p8[8]	0
t_AsstFWDefltAssistX_HwNm_u8p8[9]	0
t_AsstFWDefltAssistX_HwNm_u8p8[10]	0
t_AsstFWDefltAssistX_HwNm_u8p8[11]	0
t_AsstFWDefltAssistX_HwNm_u8p8[12]	0
t_AsstFWDefltAssistX_HwNm_u8p8[13]	0
t_AsstFWDefltAssistX_HwNm_u8p8[14]	0
t_AsstFWDefltAssistX_HwNm_u8p8[15]	0
t_AsstFWDefltAssistX_HwNm_u8p8[16]	0
t_AsstFWDefltAssistX_HwNm_u8p8[17]	0
t_AsstFWDefltAssistX_HwNm_u8p8[18]	0
t_AsstFWDefltAssistX_HwNm_u8p8[19]	0
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	8192
t_AsstFWPstepNstepThresh_Cnt_u16[0]	223
t_AsstFWPstepNstepThresh_Cnt_u16[1]	611
t_AsstFWVehSpd_Kph_u9p7[0]	33792
t_AsstFWVehSpd_Kph_u9p7[1]	33920
t_AsstFWVehSpd_Kph_u9p7[2]	34048
t_AsstFWVehSpd_Kph_u9p7[3]	34176
t_AsstFWVehSpd_Kph_u9p7[4]	34304
t_AsstFWVehSpd_Kph_u9p7[5]	34432
t_AsstFWVehSpd_Kph_u9p7[6]	34560
t_AsstFWVehSpd_Kph_u9p7[7]	34688
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.67000008
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7.65999985
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	222.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.7130003	5.71299982 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	611	611 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	4	4 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-2.29439998	-2.29439998 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.34399986	6.34399986 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.04800034	4.04799986 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4	4 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.103 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.9000001
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0160000008
AssistFirewall_ActiveRawAcc_Cnt_M_u16	9348
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.150000006
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11899996
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.30000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.189999998
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.289999992
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.5
k_AsstFWInpLimitHFA_MtrNm_f32	6.48000002
k_AsstFWInpLimitHysComp_MtrNm_f32	7.48000002
k_AsstFWNstep_Cnt_u16	234
k_AsstFWPstep_Cnt_u16	3321
k_RestoreThresh_MtrNm_f32	5.51000023
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[1]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[2]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[3]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[4]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[5]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[6]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[7]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[8]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[9]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[10]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[11]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[12]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[13]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[14]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[15]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[16]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[17]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[18]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[19]	2560
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	8397
t_AsstFWPstepNstepThresh_Cnt_u16[0]	224
t_AsstFWPstepNstepThresh_Cnt_u16[1]	615
t_AsstFWVehSpd_Kph_u9p7[0]	36736
t_AsstFWVehSpd_Kph_u9p7[1]	36864
t_AsstFWVehSpd_Kph_u9p7[2]	36992
t_AsstFWVehSpd_Kph_u9p7[3]	37120
t_AsstFWVehSpd_Kph_u9p7[4]	37248
t_AsstFWVehSpd_Kph_u9p7[5]	37376
t_AsstFWVehSpd_Kph_u9p7[6]	37504
t_AsstFWVehSpd_Kph_u9p7[7]	37632
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.78000021
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.11000013
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.55000019
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.31999969
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	253.100006
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.80560017	5.80560017 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	615	615 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	2.20019531	2.20019531 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.33899975	7.33900023 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.19300032	7.19299984 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.32499981	4.32499981 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	2.20019531	2.20019531 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.104 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0170000009
AssistFirewall_ActiveRawAcc_Cnt_M_u16	9471
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.159999996
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.4000001
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.200000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.300000012
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.5999999
k_AsstFWInpLimitHFA_MtrNm_f32	6.48999977
k_AsstFWInpLimitHysComp_MtrNm_f32	7.59000015
k_AsstFWNstep_Cnt_u16	345
k_AsstFWPstep_Cnt_u16	3444
k_RestoreThresh_MtrNm_f32	5.51999998
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	22528
t_AsstFWDefltAssistX_HwNm_u8p8[0]	717
t_AsstFWDefltAssistX_HwNm_u8p8[1]	742
t_AsstFWDefltAssistX_HwNm_u8p8[2]	768
t_AsstFWDefltAssistX_HwNm_u8p8[3]	794
t_AsstFWDefltAssistX_HwNm_u8p8[4]	819
t_AsstFWDefltAssistX_HwNm_u8p8[5]	845
t_AsstFWDefltAssistX_HwNm_u8p8[6]	870
t_AsstFWDefltAssistX_HwNm_u8p8[7]	896
t_AsstFWDefltAssistX_HwNm_u8p8[8]	922
t_AsstFWDefltAssistX_HwNm_u8p8[9]	947
t_AsstFWDefltAssistX_HwNm_u8p8[10]	973
t_AsstFWDefltAssistX_HwNm_u8p8[11]	998
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1203
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	8397
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	8602
t_AsstFWPstepNstepThresh_Cnt_u16[0]	225
t_AsstFWPstepNstepThresh_Cnt_u16[1]	619
t_AsstFWVehSpd_Kph_u9p7[0]	39680
t_AsstFWVehSpd_Kph_u9p7[1]	39808
t_AsstFWVehSpd_Kph_u9p7[2]	39936
t_AsstFWVehSpd_Kph_u9p7[3]	40064
t_AsstFWVehSpd_Kph_u9p7[4]	40192
t_AsstFWVehSpd_Kph_u9p7[5]	40320
t_AsstFWVehSpd_Kph_u9p7[6]	40448
t_AsstFWVehSpd_Kph_u9p7[7]	40576
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	6.88999987
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.21999979
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.65999985
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.43000031
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	12.3999996
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.89799976	5.89799976 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	619	619 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	4.20019531	4.20019531 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7.60080051	7.60080004 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.11999989	7.11999989 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-3.8499999	-3.8499999 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4.20019531	4.20019531 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.105 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0179999992
AssistFirewall_ActiveRawAcc_Cnt_M_u16	9594
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.170000002
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12100005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.209999993
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.5999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.310000002
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.69999981
k_AsstFWInpLimitHFA_MtrNm_f32	6.5
k_AsstFWInpLimitHysComp_MtrNm_f32	7.69999981
k_AsstFWNstep_Cnt_u16	456
k_AsstFWPstep_Cnt_u16	3567
k_RestoreThresh_MtrNm_f32	5.53000021
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-18432

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	10240

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576
t_AsstFWDefltAssistX_HwNm_u8p8[0]	742
t_AsstFWDefltAssistX_HwNm_u8p8[1]	768
t_AsstFWDefltAssistX_HwNm_u8p8[2]	794
t_AsstFWDefltAssistX_HwNm_u8p8[3]	819
t_AsstFWDefltAssistX_HwNm_u8p8[4]	845
t_AsstFWDefltAssistX_HwNm_u8p8[5]	870
t_AsstFWDefltAssistX_HwNm_u8p8[6]	896
t_AsstFWDefltAssistX_HwNm_u8p8[7]	922
t_AsstFWDefltAssistX_HwNm_u8p8[8]	947
t_AsstFWDefltAssistX_HwNm_u8p8[9]	973
t_AsstFWDefltAssistX_HwNm_u8p8[10]	998
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1229
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	-205
t_AsstFWPstepNstepThresh_Cnt_u16[0]	226
t_AsstFWPstepNstepThresh_Cnt_u16[1]	623
t_AsstFWVehSpd_Kph_u9p7[0]	42624
t_AsstFWVehSpd_Kph_u9p7[1]	42752
t_AsstFWVehSpd_Kph_u9p7[2]	42880
t_AsstFWVehSpd_Kph_u9p7[3]	43008
t_AsstFWVehSpd_Kph_u9p7[4]	43136
t_AsstFWVehSpd_Kph_u9p7[5]	43264
t_AsstFWVehSpd_Kph_u9p7[6]	43392
t_AsstFWVehSpd_Kph_u9p7[7]	43520
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.32999992
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.76999998
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	19.5
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.99020004	5.99020004 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	623	623 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-0.100097656	-0.100097656 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.68900013	5.68900013 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.0250001	7.0250001 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-3.5539999	-3.5539999 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-0.100097656	-0.100097656 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.106 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.19999981
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0189999994
AssistFirewall_ActiveRawAcc_Cnt_M_u16	9717
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.69999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.180000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12199998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.5999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.219999999
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.69999981
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.319999993
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.80000019
k_AsstFWInpLimitHFA_MtrNm_f32	6.51000023
k_AsstFWInpLimitHysComp_MtrNm_f32	7.80999994
k_AsstFWNstep_Cnt_u16	567
k_AsstFWPstep_Cnt_u16	3690
k_RestoreThresh_MtrNm_f32	5.53999996
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	0

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	768
t_AsstFWDefltAssistX_HwNm_u8p8[1]	794
t_AsstFWDefltAssistX_HwNm_u8p8[2]	819
t_AsstFWDefltAssistX_HwNm_u8p8[3]	845
t_AsstFWDefltAssistX_HwNm_u8p8[4]	870
t_AsstFWDefltAssistX_HwNm_u8p8[5]	896
t_AsstFWDefltAssistX_HwNm_u8p8[6]	922
t_AsstFWDefltAssistX_HwNm_u8p8[7]	947
t_AsstFWDefltAssistX_HwNm_u8p8[8]	973
t_AsstFWDefltAssistX_HwNm_u8p8[9]	998
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1254
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	32767
t_AsstFWPstepNstepThresh_Cnt_u16[0]	227
t_AsstFWPstepNstepThresh_Cnt_u16[1]	627
t_AsstFWVehSpd_Kph_u9p7[0]	45568
t_AsstFWVehSpd_Kph_u9p7[1]	45696
t_AsstFWVehSpd_Kph_u9p7[2]	45824
t_AsstFWVehSpd_Kph_u9p7[3]	45952
t_AsstFWVehSpd_Kph_u9p7[4]	46080
t_AsstFWVehSpd_Kph_u9p7[5]	46208
t_AsstFWVehSpd_Kph_u9p7[6]	46336
t_AsstFWVehSpd_Kph_u9p7[7]	46464
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7.11000013
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.44000006
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.88000011
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.19999981
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	26.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.08220005	6.08220005 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	627	627 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.78980017	5.78980017 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.90799999	6.90799999 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-3.23599982	-3.23600006 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.107 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.30000019
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0199999996
AssistFirewall_ActiveRawAcc_Cnt_M_u16	9840
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.189999998
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12300003
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.69999981
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.230000004
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.330000013
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.9000001
k_AsstFWInpLimitHFA_MtrNm_f32	6.51999998
k_AsstFWInpLimitHysComp_MtrNm_f32	7.92000008
k_AsstFWNstep_Cnt_u16	678
k_AsstFWPstep_Cnt_u16	3813
k_RestoreThresh_MtrNm_f32	5.55000019
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	0

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	794
t_AsstFWDefltAssistX_HwNm_u8p8[1]	819
t_AsstFWDefltAssistX_HwNm_u8p8[2]	845
t_AsstFWDefltAssistX_HwNm_u8p8[3]	870
t_AsstFWDefltAssistX_HwNm_u8p8[4]	896
t_AsstFWDefltAssistX_HwNm_u8p8[5]	922
t_AsstFWDefltAssistX_HwNm_u8p8[6]	947
t_AsstFWDefltAssistX_HwNm_u8p8[7]	973
t_AsstFWDefltAssistX_HwNm_u8p8[8]	998
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1280
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2458
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2662
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2867
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6349
t_AsstFWPstepNstepThresh_Cnt_u16[0]	228
t_AsstFWPstepNstepThresh_Cnt_u16[1]	631
t_AsstFWVehSpd_Kph_u9p7[0]	1408
t_AsstFWVehSpd_Kph_u9p7[1]	1536
t_AsstFWVehSpd_Kph_u9p7[2]	1664
t_AsstFWVehSpd_Kph_u9p7[3]	1792
t_AsstFWVehSpd_Kph_u9p7[4]	1920
t_AsstFWVehSpd_Kph_u9p7[5]	2048
t_AsstFWVehSpd_Kph_u9p7[6]	2176
t_AsstFWVehSpd_Kph_u9p7[7]	2304
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7.21999979
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.55000019
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.98999977
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.30000019
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	33.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.17400026	6.17399979 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	9162	9162 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.10009766	3.10009766 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.88879967	5.88880014 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.38899994	5.38899994 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.72699976	7.72700024 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.10009766	3.10009766 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x00	0x00	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.108 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.4000001
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0209999997
AssistFirewall_ActiveRawAcc_Cnt_M_u16	9963
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.69999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.200000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12399995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.80000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.239999995
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.19999981
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.340000004
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6
k_AsstFWInpLimitHFA_MtrNm_f32	6.53000021
k_AsstFWInpLimitHysComp_MtrNm_f32	8.02999973
k_AsstFWNstep_Cnt_u16	789
k_AsstFWPstep_Cnt_u16	3936
k_RestoreThresh_MtrNm_f32	5.55999994
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	819
t_AsstFWDefltAssistX_HwNm_u8p8[1]	845
t_AsstFWDefltAssistX_HwNm_u8p8[2]	870
t_AsstFWDefltAssistX_HwNm_u8p8[3]	896
t_AsstFWDefltAssistX_HwNm_u8p8[4]	922
t_AsstFWDefltAssistX_HwNm_u8p8[5]	947
t_AsstFWDefltAssistX_HwNm_u8p8[6]	973
t_AsstFWDefltAssistX_HwNm_u8p8[7]	998
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1306
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	23962
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	24166
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	24371
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	24781
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	24986
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	25190
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	25395
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	25600
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	25805
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	26010
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	26214
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	26419
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	26829
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	27034
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	27238
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	27443
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	27648
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	27853
t_AsstFWPstepNstepThresh_Cnt_u16[0]	229
t_AsstFWPstepNstepThresh_Cnt_u16[1]	635
t_AsstFWVehSpd_Kph_u9p7[0]	4352
t_AsstFWVehSpd_Kph_u9p7[1]	4480
t_AsstFWVehSpd_Kph_u9p7[2]	4608
t_AsstFWVehSpd_Kph_u9p7[3]	4736
t_AsstFWVehSpd_Kph_u9p7[4]	4864
t_AsstFWVehSpd_Kph_u9p7[5]	4992
t_AsstFWVehSpd_Kph_u9p7[6]	5120
t_AsstFWVehSpd_Kph_u9p7[7]	5248
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7.32999992
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.65999985
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8.10000038
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.31999969
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	40.2000008
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.2656002	6.2656002 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	9174	9174 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	8.67199993	8.67199993 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.97487545	4.97487497 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8.42559338	8.42559338 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x00	0x00	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.109 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.5
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0219999999
AssistFirewall_ActiveRawAcc_Cnt_M_u16	10086
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.209999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.125
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.9000001
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.25
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.30000019
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.349999994
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	6.53999996
k_AsstFWInpLimitHysComp_MtrNm_f32	8.14000034
k_AsstFWNstep_Cnt_u16	900
k_AsstFWPstep_Cnt_u16	4059
k_RestoreThresh_MtrNm_f32	5.55999994
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	22528
t_AsstFWDefltAssistX_HwNm_u8p8[0]	845
t_AsstFWDefltAssistX_HwNm_u8p8[1]	870
t_AsstFWDefltAssistX_HwNm_u8p8[2]	896
t_AsstFWDefltAssistX_HwNm_u8p8[3]	922
t_AsstFWDefltAssistX_HwNm_u8p8[4]	947
t_AsstFWDefltAssistX_HwNm_u8p8[5]	973
t_AsstFWDefltAssistX_HwNm_u8p8[6]	998
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1331
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	-203
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	-201
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	-199
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	-197
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	-195
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	-193
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	-190
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	-188
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	-186
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	-184
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	-182
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	-180
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	-178
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	-176
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	-174
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	-172
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	-170
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	-168
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	-166
t_AsstFWPstepNstepThresh_Cnt_u16[0]	230
t_AsstFWPstepNstepThresh_Cnt_u16[1]	639
t_AsstFWVehSpd_Kph_u9p7[0]	7296
t_AsstFWVehSpd_Kph_u9p7[1]	7424
t_AsstFWVehSpd_Kph_u9p7[2]	7552
t_AsstFWVehSpd_Kph_u9p7[3]	7680
t_AsstFWVehSpd_Kph_u9p7[4]	7808
t_AsstFWVehSpd_Kph_u9p7[5]	7936
t_AsstFWVehSpd_Kph_u9p7[6]	8064
t_AsstFWVehSpd_Kph_u9p7[7]	8192
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7.44000006
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.76999998
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8.21000004
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.43000031
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	47.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.35699987	6.35699987 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	639	639 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-0.0810546875	-0.0810546875 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	8.94580078	8.94579983 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.42500019	6.42500019 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.21848631	6.21848631 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-0.0810546875	-0.0810546875 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.110 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.5999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.023
AssistFirewall_ActiveRawAcc_Cnt_M_u16	10209
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.9000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.219999999
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12600005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.25999999
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.4000001
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.360000014
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6.19999981
k_AsstFWInpLimitHFA_MtrNm_f32	6.55000019
k_AsstFWInpLimitHysComp_MtrNm_f32	8.25
k_AsstFWNstep_Cnt_u16	1011
k_AsstFWPstep_Cnt_u16	4182
k_RestoreThresh_MtrNm_f32	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	10240

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	24576
t_AsstFWDefltAssistX_HwNm_u8p8[0]	870
t_AsstFWDefltAssistX_HwNm_u8p8[1]	896
t_AsstFWDefltAssistX_HwNm_u8p8[2]	922
t_AsstFWDefltAssistX_HwNm_u8p8[3]	947
t_AsstFWDefltAssistX_HwNm_u8p8[4]	973
t_AsstFWDefltAssistX_HwNm_u8p8[5]	998
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1357
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2458
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2662
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2867
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6349
t_AsstFWPstepNstepThresh_Cnt_u16[0]	231
t_AsstFWPstepNstepThresh_Cnt_u16[1]	643
t_AsstFWVehSpd_Kph_u9p7[0]	10240
t_AsstFWVehSpd_Kph_u9p7[1]	10368
t_AsstFWVehSpd_Kph_u9p7[2]	10496
t_AsstFWVehSpd_Kph_u9p7[3]	10624
t_AsstFWVehSpd_Kph_u9p7[4]	10752
t_AsstFWVehSpd_Kph_u9p7[5]	10880
t_AsstFWVehSpd_Kph_u9p7[6]	11008
t_AsstFWVehSpd_Kph_u9p7[7]	11136
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7.55000019
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.88000011
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8.31999969
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.53999996
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	54.2999992
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.44819975	6.44820023 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	643	643 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.10009766	3.10009766 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	9.22200012	9.22200012 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.22000027	6.21999979 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.29113674	6.29113674 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.10009766	3.10009766 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.111 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.69999981
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0240000002
AssistFirewall_ActiveRawAcc_Cnt_M_u16	10332
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.69999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.230000004
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12699997
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.270000011
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.370000005
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6.30000019
k_AsstFWInpLimitHFA_MtrNm_f32	6.55999994
k_AsstFWInpLimitHysComp_MtrNm_f32	8.35999966
k_AsstFWNstep_Cnt_u16	1122
k_AsstFWPstep_Cnt_u16	4305
k_RestoreThresh_MtrNm_f32	8.80000019
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	12288

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	26624
t_AsstFWDefltAssistX_HwNm_u8p8[0]	896
t_AsstFWDefltAssistX_HwNm_u8p8[1]	922
t_AsstFWDefltAssistX_HwNm_u8p8[2]	947
t_AsstFWDefltAssistX_HwNm_u8p8[3]	973
t_AsstFWDefltAssistX_HwNm_u8p8[4]	998
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1382
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2662
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2867
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6554
t_AsstFWPstepNstepThresh_Cnt_u16[0]	232
t_AsstFWPstepNstepThresh_Cnt_u16[1]	647
t_AsstFWVehSpd_Kph_u9p7[0]	13184
t_AsstFWVehSpd_Kph_u9p7[1]	13312
t_AsstFWVehSpd_Kph_u9p7[2]	13440
t_AsstFWVehSpd_Kph_u9p7[3]	13568
t_AsstFWVehSpd_Kph_u9p7[4]	13696
t_AsstFWVehSpd_Kph_u9p7[5]	13824
t_AsstFWVehSpd_Kph_u9p7[6]	13952
t_AsstFWVehSpd_Kph_u9p7[7]	14080
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7.65999985
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	7.98999977
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8.43000031
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.64999962
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	61.0999985
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.53919983	6.53919983 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	647	647 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.20019531	3.20019531 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	9.50060081	9.50059986 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.83901548	5.83901548 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.31500006	7.31500006 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.20019531	3.20019531 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.112 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.80000019
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0250000004
AssistFirewall_ActiveRawAcc_Cnt_M_u16	10455
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-7.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.239999995
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.12800002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	7.19999981
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.280000001
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.5999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.379999995
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	6.4000001
k_AsstFWInpLimitHFA_MtrNm_f32	6.57000017
k_AsstFWInpLimitHysComp_MtrNm_f32	8.47000027
k_AsstFWNstep_Cnt_u16	1233
k_AsstFWPstep_Cnt_u16	4428
k_RestoreThresh_MtrNm_f32	4.4000001
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	12288

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	U

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	922
t_AsstFWDefltAssistX_HwNm_u8p8[1]	947
t_AsstFWDefltAssistX_HwNm_u8p8[2]	973
t_AsstFWDefltAssistX_HwNm_u8p8[3]	998
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1382
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1408
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2867
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6758
t_AsstFWPstepNstepThresh_Cnt_u16[0]	233
t_AsstFWPstepNstepThresh_Cnt_u16[1]	651
t_AsstFWVehSpd_Kph_u9p7[0]	16128
t_AsstFWVehSpd_Kph_u9p7[1]	16256
t_AsstFWVehSpd_Kph_u9p7[2]	16384
t_AsstFWVehSpd_Kph_u9p7[3]	16512
t_AsstFWVehSpd_Kph_u9p7[4]	16640
t_AsstFWVehSpd_Kph_u9p7[5]	16768
t_AsstFWVehSpd_Kph_u9p7[6]	16896
t_AsstFWVehSpd_Kph_u9p7[7]	17024
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	7.76999998
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	8.10000038
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8.53999996
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.76000023
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	68.3000031
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.63000011	6.63000011 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	651	651 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.29980469	3.29980469 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	9.7816	9.7816 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.46399975	5.46400023 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8.13199997	8.13199997 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.29980469	3.29980469 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.113 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.30000019
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.400000006
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11199999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.119999997
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.219999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.80000019
k_AsstFWInpLimitHFA_MtrNm_f32	6.40999985
k_AsstFWInpLimitHysComp_MtrNm_f32	6.71000004
k_AsstFWNstep_Cnt_u16	4052
k_AsstFWPstep_Cnt_u16	2460
k_RestoreThresh_MtrNm_f32	4.42999983
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	14336

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	947
t_AsstFWDefltAssistX_HwNm_u8p8[1]	973
t_AsstFWDefltAssistX_HwNm_u8p8[2]	998
t_AsstFWDefltAssistX_HwNm_u8p8[3]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1382
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1408
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1434
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3072
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	6963
t_AsstFWPstepNstepThresh_Cnt_u16[0]	234
t_AsstFWPstepNstepThresh_Cnt_u16[1]	655
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
t_AsstFWVehSpd_Kph_u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.19999981
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	1
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.5999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.4000001
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.5999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176.100006
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.30000019	-5.30000019 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487	8487 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-16	-16 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-6.06399965	-6.06400013 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019	-5.30000019 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999	5.0999999 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-16	-16 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x00	0x00	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x00	0x00	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.114 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.4000001
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.5
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8610
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	0
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0900000036
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11300004
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.4000001
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.129999995
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.230000004
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.9000001
k_AsstFWInpLimitHFA_MtrNm_f32	6.42000008
k_AsstFWInpLimitHysComp_MtrNm_f32	6.82000017
k_AsstFWNstep_Cnt_u16	4053
k_AsstFWPstep_Cnt_u16	2583
k_RestoreThresh_MtrNm_f32	4.44000006
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	20480

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	819
t_AsstFWDefltAssistX_HwNm_u8p8[1]	845
t_AsstFWDefltAssistX_HwNm_u8p8[2]	870
t_AsstFWDefltAssistX_HwNm_u8p8[3]	896
t_AsstFWDefltAssistX_HwNm_u8p8[4]	922
t_AsstFWDefltAssistX_HwNm_u8p8[5]	947
t_AsstFWDefltAssistX_HwNm_u8p8[6]	973
t_AsstFWDefltAssistX_HwNm_u8p8[7]	998
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1306
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3277
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7168
t_AsstFWPstepNstepThresh_Cnt_u16[0]	235
t_AsstFWPstepNstepThresh_Cnt_u16[1]	659
t_AsstFWVehSpd_Kph_u9p7[0]	22016
t_AsstFWVehSpd_Kph_u9p7[1]	22144
t_AsstFWVehSpd_Kph_u9p7[2]	22272
t_AsstFWVehSpd_Kph_u9p7[3]	22400
t_AsstFWVehSpd_Kph_u9p7[4]	22528
t_AsstFWVehSpd_Kph_u9p7[5]	22656
t_AsstFWVehSpd_Kph_u9p7[6]	22784
t_AsstFWVehSpd_Kph_u9p7[7]	22912
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.30000019
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.69999981
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.69999981
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	187.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-2.70000005	-2.70000005 ± 4.88E-04	✔

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveRawAcc_Cnt_M_u16	659	659 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.5	-3.5 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-6.28999996	-6.28999996 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.0880003	-5.08799982 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.19199991	-5.19199991 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-3.5	-3.5 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.115 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.5
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.600000024
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8733
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.4000001
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.100000001
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11399996
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.80000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.140000001
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.19999981
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.239999995
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5
k_AsstFWInpLimitHFA_MtrNm_f32	6.42999983
k_AsstFWInpLimitHysComp_MtrNm_f32	6.92999983
k_AsstFWNstep_Cnt_u16	3053
k_AsstFWPstep_Cnt_u16	2706
k_RestoreThresh_MtrNm_f32	4.44999981
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	20480

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	870
t_AsstFWDefltAssistX_HwNm_u8p8[1]	896
t_AsstFWDefltAssistX_HwNm_u8p8[2]	922
t_AsstFWDefltAssistX_HwNm_u8p8[3]	947
t_AsstFWDefltAssistX_HwNm_u8p8[4]	973
t_AsstFWDefltAssistX_HwNm_u8p8[5]	998
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1357
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3482
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7373
t_AsstFWPstepNstepThresh_Cnt_u16[0]	236
t_AsstFWPstepNstepThresh_Cnt_u16[1]	663
t_AsstFWVehSpd_Kph_u9p7[0]	24960
t_AsstFWVehSpd_Kph_u9p7[1]	25088
t_AsstFWVehSpd_Kph_u9p7[2]	25216
t_AsstFWVehSpd_Kph_u9p7[3]	25344
t_AsstFWVehSpd_Kph_u9p7[4]	25472
t_AsstFWVehSpd_Kph_u9p7[5]	25600
t_AsstFWVehSpd_Kph_u9p7[6]	25728
t_AsstFWVehSpd_Kph_u9p7[7]	25856
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.4000001
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.67000008
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.5999999
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6.67000008
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	198.300003
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-2.19999981	-2.20000005 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	663	663 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-3.60009766	-3.60009766 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-4.05000019	-4.05000019 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.6983614	4.6983614 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-5.44813251	-5.44813299 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-3.60009766	-3.60009766 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.116 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.5
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0120000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8856
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.109999999
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11500001
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.9000001
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.150000006
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.25
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	6.44000006
k_AsstFWInpLimitHysComp_MtrNm_f32	7.03999996
k_AsstFWNstep_Cnt_u16	2053
k_AsstFWPstep_Cnt_u16	2829
k_RestoreThresh_MtrNm_f32	4.46000004
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	20480

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefltAssistX_HwNm_u8p8[0]	896
t_AsstFWDefltAssistX_HwNm_u8p8[1]	922
t_AsstFWDefltAssistX_HwNm_u8p8[2]	947
t_AsstFWDefltAssistX_HwNm_u8p8[3]	973
t_AsstFWDefltAssistX_HwNm_u8p8[4]	998
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1382
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	3686
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	3891
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7578
t_AsstFWPstepNstepThresh_Cnt_u16[0]	237
t_AsstFWPstepNstepThresh_Cnt_u16[1]	667
t_AsstFWVehSpd_Kph_u9p7[0]	27904
t_AsstFWVehSpd_Kph_u9p7[1]	28032
t_AsstFWVehSpd_Kph_u9p7[2]	28160
t_AsstFWVehSpd_Kph_u9p7[3]	28288
t_AsstFWVehSpd_Kph_u9p7[4]	28416
t_AsstFWVehSpd_Kph_u9p7[5]	28544
t_AsstFWVehSpd_Kph_u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7]	28800
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.5
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.11000013
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7.32999992
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	209.300003
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.43400002	5.43400002 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	667	667 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.70019531	3.70019531 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.24259996	-5.24259996 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.56500006	4.56500006 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.82499981	7.82499981 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.70019531	3.70019531 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.117 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.5999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0130000003
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8979
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	7.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.5999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.119999997
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11600006
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.159999996
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6.19999981
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.25999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	5.19999981
k_AsstFWInpLimitHFA_MtrNm_f32	6.44999981
k_AsstFWInpLimitHysComp_MtrNm_f32	7.1500001
k_AsstFWNstep_Cnt_u16	1053
k_AsstFWPstep_Cnt_u16	2952
k_RestoreThresh_MtrNm_f32	4.46999979
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	22528

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	922
t_AsstFWDefltAssistX_HwNm_u8p8[1]	947
t_AsstFWDefltAssistX_HwNm_u8p8[2]	973
t_AsstFWDefltAssistX_HwNm_u8p8[3]	998
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1382
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1408
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4301
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4506
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4710
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4915
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	5325
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	5530
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	6349
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	6554
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	7373
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	7578
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	7987
t_AsstFWPstepNstepThresh_Cnt_u16[0]	238
t_AsstFWPstepNstepThresh_Cnt_u16[1]	671
t_AsstFWVehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1]	30976
t_AsstFWVehSpd_Kph_u9p7[2]	31104
t_AsstFWVehSpd_Kph_u9p7[3]	31232
t_AsstFWVehSpd_Kph_u9p7[4]	31360
t_AsstFWVehSpd_Kph_u9p7[5]	31488
t_AsstFWVehSpd_Kph_u9p7[6]	31616
t_AsstFWVehSpd_Kph_u9p7[7]	31744
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.5999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.19999981
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	7.21999979
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	7.44000006
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	220.199997
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.52719975	5.52720022 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	671	671 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	3.89990234	3.89990234 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.31799984	-5.31799984 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.4000001	4.4000001 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8.22799969	8.22799969 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	3.89990234	3.89990234 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.118 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-8.80000019
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00125584798
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-52.7999992
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00125584798
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00062859
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-8.80000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00125584798
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-16
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00125584798
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	0
k_AsstFWInpLimitHFA_MtrNm_f32	0
k_AsstFWInpLimitHysComp_MtrNm_f32	0
k_AsstFWNstep_Cnt_u16	0
k_AsstFWPstep_Cnt_u16	0
k_RestoreThresh_MtrNm_f32	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-20480

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	-20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-32768

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-32768

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	-32768
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	-32768
t_AsstFWDefltAssistX_HwNm_u8p8[0]	0
t_AsstFWDefltAssistX_HwNm_u8p8[1]	0
t_AsstFWDefltAssistX_HwNm_u8p8[2]	0
t_AsstFWDefltAssistX_HwNm_u8p8[3]	0
t_AsstFWDefltAssistX_HwNm_u8p8[4]	0
t_AsstFWDefltAssistX_HwNm_u8p8[5]	0
t_AsstFWDefltAssistX_HwNm_u8p8[6]	0
t_AsstFWDefltAssistX_HwNm_u8p8[7]	0
t_AsstFWDefltAssistX_HwNm_u8p8[8]	0
t_AsstFWDefltAssistX_HwNm_u8p8[9]	0
t_AsstFWDefltAssistX_HwNm_u8p8[10]	0
t_AsstFWDefltAssistX_HwNm_u8p8[11]	0
t_AsstFWDefltAssistX_HwNm_u8p8[12]	0
t_AsstFWDefltAssistX_HwNm_u8p8[13]	0
t_AsstFWDefltAssistX_HwNm_u8p8[14]	0
t_AsstFWDefltAssistX_HwNm_u8p8[15]	0
t_AsstFWDefltAssistX_HwNm_u8p8[16]	0
t_AsstFWDefltAssistX_HwNm_u8p8[17]	0
t_AsstFWDefltAssistX_HwNm_u8p8[18]	0
t_AsstFWDefltAssistX_HwNm_u8p8[19]	0
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	-205
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	-205
t_AsstFWPstepNstepThresh_Cnt_u16[0]	0
t_AsstFWPstepNstepThresh_Cnt_u16[1]	0
t_AsstFWVehSpd_Kph_u9p7[0]	0
t_AsstFWVehSpd_Kph_u9p7[1]	0
t_AsstFWVehSpd_Kph_u9p7[2]	0
t_AsstFWVehSpd_Kph_u9p7[3]	0
t_AsstFWVehSpd_Kph_u9p7[4]	0
t_AsstFWVehSpd_Kph_u9p7[5]	0
t_AsstFWVehSpd_Kph_u9p7[6]	0
t_AsstFWVehSpd_Kph_u9p7[7]	0
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-8.80000019
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-8.80000019
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-10
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-8.80000019
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	0
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-8.78894901	-8.78894901 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0	0 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	0.100097656	0.100097656 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-52.7336922	-52.7336922 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-8.76885509	-8.76885509 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	-16	-16 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	0.100097656	0.100097656 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 2.119 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8.80000019
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.715390444
AssistFirewall_ActiveRawAcc_Cnt_M_u16	65535
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	52.7999992
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.715390444
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	2.09537959
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8.80000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.715390444
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	15.9995003
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.715390444
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	8.80000019
k_AsstFWInpLimitHFA_MtrNm_f32	8.80000019
k_AsstFWInpLimitHysComp_MtrNm_f32	8.80000019
k_AsstFWNstep_Cnt_u16	5000
k_AsstFWPstep_Cnt_u16	5000
k_RestoreThresh_MtrNm_f32	8.80000019
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	20480

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	32767

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	32767

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	32767
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	32767
t_AsstFWDefltAssistX_HwNm_u8p8[0]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[1]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[2]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[3]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[4]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[5]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[6]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[7]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[8]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[9]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[10]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[11]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[12]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[13]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[14]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[15]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[16]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[17]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[18]	2560
t_AsstFWDefltAssistX_HwNm_u8p8[19]	2560
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	32767
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	32767
t_AsstFWPstepNstepThresh_Cnt_u16[0]	5000
t_AsstFWPstepNstepThresh_Cnt_u16[1]	5000
t_AsstFWVehSpd_Kph_u9p7[0]	65408
t_AsstFWVehSpd_Kph_u9p7[1]	65408
t_AsstFWVehSpd_Kph_u9p7[2]	65408
t_AsstFWVehSpd_Kph_u9p7[3]	65408
t_AsstFWVehSpd_Kph_u9p7[4]	65408
t_AsstFWVehSpd_Kph_u9p7[5]	65408
t_AsstFWVehSpd_Kph_u9p7[6]	65408
t_AsstFWVehSpd_Kph_u9p7[7]	65408
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	8.80000019
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	1
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	8.80000019
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	10
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8.80000019
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	255
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

TEST DETAILS REPORT

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8.80000019	8.80000019 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	65535	65535 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	26.4000015	26.3999996 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	33.9136925	33.9136925 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8.80000019	8.80000019 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	15.9995003	15.9995003 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	26.4000015	26.3999996 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x00	0x00	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x00	0x00	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Case 3: Path test ✔

TEST DETAILS REPORT

Specification

```
Performance Metrics (With "None" Instrumentation
and WithPS Environment)
CPU Cycles:


TC3.1 6628.00 Cycles
TC3.2 6628.00 Cycles
TC3.3 6629.00 Cycles
TC3.4 6629.00 Cycles
TC3.5 6629.00 Cycles
TC3.6 6629.00 Cycles
TC3.7 6629.00 Cycles
TC3.8 6629.00 Cycles
TC3.9 6629.00 Cycles
TC3.10 6629.00 Cycles
TC3.11 6629.00 Cycles
TC3.12 6629.00 Cycles
TC3.13 6629.00 Cycles
TC3.14 6629.00 Cycles
TC3.15 6629.00 Cycles
TC3.16 6629.00 Cycles
```

Description Vector Description

TS3.1"((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HysteresisComp_MtrNm_T_f32)<=(-k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=True && ((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((BaseAssistCmd_MtrNm_T_f32)<=(-k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32)>=(UprBoundFilt_MtrNm_T_f32))=True && DefltAsst_MtrNm_T_f32 = DefltAsstLookup_MtrNm_T_f32 * ((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32 < LwrBoundFilt_MtrNm_T_f32) ||
(LowFreqInput_MtrNm_T_f32 > UprBoundFilt_MtrNm_T_f32))=True
&&((AssistFirewall_ActiveRawAcc_Cnt_M_u16)<((AsstFWPstepNstep_Cnt_T_str.Threshold)-(AsstFWPstepNstep_Cnt_T_str.Pstep)))=True && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[1])=True && (((Abs_f32_m(SumInput_MtrNm_T_f32 - AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=True && (AsstFWActive_Uls_T_f32>1)=True"
TS3.2"((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=True && ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=True && ((BaseAssistCmd_MtrNm_T_f32)=True &&((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)=False && ((LowFreqInput_MtrNm_T_f32)>=(UprBoundFilt_MtrNm_T_f32))=True && DefltAsst_MtrNm_T_f32 = DefltAsstLookup_MtrNm_T_f32 * ((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32 < LwrBoundFilt_MtrNm_T_f32) ||
(LowFreqInput_MtrNm_T_f32 > UprBoundFilt_MtrNm_T_f32))=True &&
((AssistFirewall_ActiveRawAcc_Cnt_M_u16)<((AsstFWPstepNstep_Cnt_T_str.Threshold)-(AsstFWPstepNstep_Cnt_T_str.Pstep)))=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[1])
=True && (((Abs_f32_m(SumInput_MtrNm_T_f32 - AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=True && (AsstFWActive_Uls_T_f32>1)=True"
TS3.3((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=True && ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=False ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=True && ((BaseAssistCmd_MtrNm_T_f32)=True &&((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode))=True && ((LowFreqInput_MtrNm_T_f32)>=(UprBoundFilt_MtrNm_T_f32))=True &&DefltAsst_MtrNm_T_f32 = DefltAsstLookup_MtrNm_T_f32 * ((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=True && ((AssistFirewall_ActiveRawAcc_Cnt_M_u16)<((AsstFWPstepNstep_Cnt_T_str.Threshold)-(AsstFWPstepNstep_Cnt_T_str.Pstep)))=True &&(AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[1])=True &&(((Abs_f32_m(SumInput_MtrNm_T_f32 - AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=true && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=True && (AsstFWActive_Uls_T_f32>1)=True
TS3.4"((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HysteresisComp_MtrNm_T_f32)<=(-k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=True && ((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=True && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HysteresisComp_MtrNm_T_f32)<=(-k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=True && ((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((BaseAssistCmd_MtrNm_T_f32)<=(-k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32)>=(UprBoundFilt_MtrNm_T_f32))=True && DefltAsst_MtrNm_T_f32 = DefltAsstLookup_MtrNm_T_f32 *((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32 < LwrBoundFilt_MtrNm_T_f32) ||
(LowFreqInput_MtrNm_T_f32 > UprBoundFilt_MtrNm_T_f32))=True &&
((AssistFirewall_ActiveRawAcc_Cnt_M_u16)<((AsstFWPstepNstep_Cnt_T_str.Threshold)-(AsstFWPstepNstep_Cnt_T_str.Pstep)))=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[1])=True && (((Abs_f32_m(SumInput_MtrNm_T_f32 - AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=True && (AsstFWActive_Uls_T_f32>1)=True"
TS3.5"((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HysteresisComp_MtrNm_T_f32)<=(-k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=False && ((HighFreqAssist_MtrNm_T_f32)<=(-k_AsstFWInpLimitHFA_MtrNm_f32))=False &&((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=True && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HysteresisComp_MtrNm_T_f32)<=(-k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=True && ((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((BaseAssistCmd_MtrNm_T_f32)<=(-k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32)>=(UprBoundFilt_MtrNm_T_f32))=True && DefltAsst_MtrNm_T_f32 = DefltAsstLookup_MtrNm_T_f32 * ((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32 < LwrBoundFilt_MtrNm_T_f32) ||
(LowFreqInput_MtrNm_T_f32 > UprBoundFilt_MtrNm_T_f32))=True &&
((AssistFirewall_ActiveRawAcc_Cnt_M_u16)<((AsstFWPstepNstep_Cnt_T_str.Threshold)-(AsstFWPstepNstep_Cnt_T_str.Pstep)))=True &&(AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[1])=True && (((Abs_f32_m(SumInput_MtrNm_T_f32 - AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=False && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=False && (AsstFWActive_Uls_T_f32<=0)=False"
TS3.6"((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=True && ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))=False && ((HighFreqAssist_MtrNm_T_f32)<=(-k_AsstFWInpLimitHFA_MtrNm_f32))=False &&((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((BaseAssistCmd_MtrNm_T_f32)<=(-k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32)>=(UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32)<=(-UprBoundFilt_MtrNm_T_f32))=true && DefltAsst_MtrNm_T_f32 = DefltAsstLookup_MtrNm_T_f32 * ((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32 < LwrBoundFilt_MtrNm_T_f32) ||
(LowFreqInput_MtrNm_T_f32 > UprBoundFilt_MtrNm_T_f32))=True
&&((AssistFirewall_ActiveRawAcc_Cnt_M_u16)<((AsstFWPstepNstep_Cnt_T_str.Threshold)-(AsstFWPstepNstep_Cnt_T_str.Pstep)))=True && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[1])=True && (((Abs_f32_m(SumInput_MtrNm_T_f32 - AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=True && (AsstFWActive_Uls_T_f32>1)=True"
TS3.7"((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HysteresisComp_MtrNm_T_f32)<=(-k_AsstFWInpLimitHysComp_MtrNm_f32))=False ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))= False && ((HighFreqAssist_MtrNm_T_f32)<=(-k_AsstFWInpLimitHFA_MtrNm_f32))=False &&((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=True && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32)>=(UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32)<=(-UprBoundFilt_MtrNm_T_f32))=true && DefltAsst_MtrNm_T_f32 = DefltAsstLookup_MtrNm_T_f32 * ((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32 < LwrBoundFilt_MtrNm_T_f32) ||
(LowFreqInput_MtrNm_T_f32 > UprBoundFilt_MtrNm_T_f32))=True

&&((AssistFirewall_ActiveRawAcc_Cnt_M_u16)<((AsstFWPstepNstep_Cnt_T_str.Threshold)-(AsstFWPstepNstep_Cnt_T_str.Pstep)))=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[1])=False && (AssistFirewall_CombAsstSV_MtrNm_M_f32<=-8.8)=True&& (((Abs_f32_m(SumInput_MtrNm_T_f32 - AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=True && (AsstFWActive_Uls_T_f32>1)=True"

TS3.8"""((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HysteresisComp_MtrNm_T_f32)<=(-k_AsstFWInpLimitHysComp_MtrNm_f32))=False ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))= False && ((HighFreqAssist_MtrNm_T_f32)<=(-k_AsstFWInpLimitHFA_MtrNm_f32))=False &&((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=True && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32)>=(UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32)<=(-UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32)<=(-UprBoundFilt_MtrNm_T_f32))=False && DefltAsst_MtrNm_T_f32 = DefltAsstLookup_MtrNm_T_f32 * ((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32 < LwrBoundFilt_MtrNm_T_f32) ||
(LowFreqInput_MtrNm_T_f32 > UprBoundFilt_MtrNm_T_f32))=FALSE
&&((AssistFirewall_ActiveRawAcc_Cnt_M_u16)>((AsstFWPstepNstep_Cnt_T_str.Nstep)=True && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[1])=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 > t_AsstFWPstepNstepThresh_Cnt_u16[0])=True &&(AssistFirewall_CombAsstSV_MtrNm_M_f32<=-8.8)=True&& (((Abs_f32_m(SumInput_MtrNm_T_f32 - AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=False && (AssistFirewall_CombAsstSV_MtrNm_M_f32<=-8.8)=False && (AsstFWActive_Uls_T_f32>1)=True""
"

TS3.9"((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=True && ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))= True &&((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((BaseAssistCmd_MtrNm_T_f32)<=(-k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32)>=(UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32)<=(-UprBoundFilt_MtrNm_T_f32))=True && DefltAsst_MtrNm_T_f32 = DefltAsstLookup_MtrNm_T_f32 * ((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32 < LwrBoundFilt_MtrNm_T_f32) ||
(LowFreqInput_MtrNm_T_f32 > UprBoundFilt_MtrNm_T_f32))=True
&&(((AssistFirewall_ActiveRawAcc_Cnt_M_u16)<((AsstFWPstepNstep_Cnt_T_str.Threshold)-(AsstFWPstepNstep_Cnt_T_str.Pstep)))=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[1])=True && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 > t_AsstFWPstepNstepThresh_Cnt_u16[0])=True &&(AssistFirewall_CombAsstSV_MtrNm_M_f32<=-8.8)=True&& (((Abs_f32_m(SumInput_MtrNm_T_f32 - AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=True && (AsstFWActive_Uls_T_f32>1)=True"

TS3.10"((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HysteresisComp_MtrNm_T_f32)<=(-k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))= False && ((HighFreqAssist_MtrNm_T_f32)<=(-k_AsstFWInpLimitHFA_MtrNm_f32))=False &&((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=True && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32)>=(UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32)<=(-UprBoundFilt_MtrNm_T_f32))=True && DefltAsst_MtrNm_T_f32 = DefltAsstLookup_MtrNm_T_f32 * ((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32 < LwrBoundFilt_MtrNm_T_f32) ||
(LowFreqInput_MtrNm_T_f32 > UprBoundFilt_MtrNm_T_f32))=True
&&(((AssistFirewall_ActiveRawAcc_Cnt_M_u16)<((AsstFWPstepNstep_Cnt_T_str.Threshold)-(AsstFWPstepNstep_Cnt_T_str.Pstep)))=True && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[1])=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 > t_AsstFWPstepNstepThresh_Cnt_u16[0])=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 > t_AsstFWPstepNstepThresh_Cnt_u16[0])=True &&(AssistFirewall_CombAsstSV_MtrNm_M_f32<=-8.8)=True&& (((Abs_f32_m(SumInput_MtrNm_T_f32 - AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=False && (AssistFirewall_CombAsstSV_MtrNm_M_f32<=-8.8)=False && (AsstFWActive_Uls_T_f32>1)=True"

TS3.11"((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=True && ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))= True &&((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32)>=(UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32)<=(-UprBoundFilt_MtrNm_T_f32))=False && DefltAsst_MtrNm_T_f32 = DefltAsstLookup_MtrNm_T_f32 * ((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32 < LwrBoundFilt_MtrNm_T_f32) ||
(LowFreqInput_MtrNm_T_f32 > UprBoundFilt_MtrNm_T_f32))=False
&&((AssistFirewall_ActiveRawAcc_Cnt_M_u16)>((AsstFWPstepNstep_Cnt_T_str.Nstep)=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[1])=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 > t_AsstFWPstepNstepThresh_Cnt_u16[0])=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 > t_AsstFWPstepNstepThresh_Cnt_u16[0])=True &&(AssistFirewall_CombAsstSV_MtrNm_M_f32<=-8.8)=True&& (((Abs_f32_m(SumInput_MtrNm_T_f32 - AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=False && (AssistFirewall_CombAsstSV_MtrNm_M_f32<=-8.8)=False && (AsstFWActive_Uls_T_f32>1)=False && (AsstFWActive_Uls_T_f32<=0)=False"

TS3.12"((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HysteresisComp_MtrNm_T_f32)<=(-k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))= False &&((HighFreqAssist_MtrNm_T_f32)<=(-k_AsstFWInpLimitHFA_MtrNm_f32))=True &&((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((BaseAssistCmd_MtrNm_T_f32)<=(-k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32)>=(UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32)<=(-UprBoundFilt_MtrNm_T_f32))=True && DefltAsst_MtrNm_T_f32 = DefltAsstLookup_MtrNm_T_f32 * ((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32 < LwrBoundFilt_MtrNm_T_f32) ||
(LowFreqInput_MtrNm_T_f32 > UprBoundFilt_MtrNm_T_f32))=False
&&((AssistFirewall_ActiveRawAcc_Cnt_M_u16)<((AsstFWPstepNstep_Cnt_T_str.Threshold)-(AsstFWPstepNstep_Cnt_T_str.Pstep)))=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[1])=True && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 > t_AsstFWPstepNstepThresh_Cnt_u16[0])=True &&(AssistFirewall_CombAsstSV_MtrNm_M_f32<=-8.8)=True&& (((Abs_f32_m(SumInput_MtrNm_T_f32 - AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=False && (AssistFirewall_CombAsstSV_MtrNm_M_f32<=-8.8)=False && (AsstFWActive_Uls_T_f32>1)=True "

TS3.13"((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HysteresisComp_MtrNm_T_f32)<=(-k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))= False &&((HighFreqAssist_MtrNm_T_f32)<=(-k_AsstFWInpLimitHFA_MtrNm_f32))=False &&((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=True && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32)>=(UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32)<=(-UprBoundFilt_MtrNm_T_f32))=True && DefltAsst_MtrNm_T_f32 = DefltAsstLookup_MtrNm_T_f32 * ((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=True && ((LowFreqInput_MtrNm_T_f32 < LwrBoundFilt_MtrNm_T_f32) ||
(LowFreqInput_MtrNm_T_f32 > UprBoundFilt_MtrNm_T_f32))=False

&&((AssistFirewall_ActiveRawAcc_Cnt_M_u16)<((AsstFWPstepNstep_Cnt_T_str.Threshold)-(AsstFWPstepNstep_Cnt_T_str.Pstep)))=True && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[1])=True && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 > t_AsstFWPstepNstepThresh_Cnt_u16[0])=True &&(AssistFirewall_CombAsstSV_MtrNm_M_f32<=-8.8)=True&& (((Abs_f32_m(SumInput_MtrNm_T_f32 - AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=False && (AssistFirewall_CombAsstSV_MtrNm_M_f32<=-8.8)=False && (AsstFWActive_Uls_T_f32>1)=False && (AsstFWActive_Uls_T_f32<=0)=False "

TS3.14"((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HysteresisComp_MtrNm_T_f32)<=(-k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))= False &&((HighFreqAssist_MtrNm_T_f32)<=(-k_AsstFWInpLimitHFA_MtrNm_f32))=False &&((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((BaseAssistCmd_MtrNm_T_f32)<=(-k_AsstFWInpLimitBaseAsst_MtrNm_f32))=True && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32)>=(UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32)<=(-UprBoundFilt_MtrNm_T_f32))=True && DefltAsst_MtrNm_T_f32 = DefltAsstLookup_MtrNm_T_f32 * ((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32 < LwrBoundFilt_MtrNm_T_f32) ||

TS3.15"((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HysteresisComp_MtrNm_T_f32)<=(-k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))= False &&((HighFreqAssist_MtrNm_T_f32)<=(-k_AsstFWInpLimitHFA_MtrNm_f32))=False &&((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((BaseAssistCmd_MtrNm_T_f32)<=(-k_AsstFWInpLimitBaseAsst_MtrNm_f32))=True && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32)>=(UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32)<=(-UprBoundFilt_MtrNm_T_f32))=True && DefltAsst_MtrNm_T_f32 = DefltAsstLookup_MtrNm_T_f32 * ((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32 < LwrBoundFilt_MtrNm_T_f32) ||
(LowFreqInput_MtrNm_T_f32 > UprBoundFilt_MtrNm_T_f32))=True &&((AssistFirewall_ActiveRawAcc_Cnt_M_u16)<((AsstFWPstepNstep_Cnt_T_str.Threshold)-(AsstFWPstepNstep_Cnt_T_str.Pstep)))=True && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[1])=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 > t_AsstFWPstepNstepThresh_Cnt_u16[0])=True &&(AssistFirewall_CombAsstSV_MtrNm_M_f32<=-8.8)=True&& (((Abs_f32_m(SumInput_MtrNm_T_f32 - AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=False && (AssistFirewall_CombAsstSV_MtrNm_M_f32<=-8.8)=True && (AsstFWActive_Uls_T_f32>1)=False && (AsstFWActive_Uls_T_f32<=0)=True "

TS3.16"((HysteresisComp_MtrNm_T_f32)>=(k_AsstFWInpLimitHysComp_MtrNm_f32))=False && ((HysteresisComp_MtrNm_T_f32)<=(-k_AsstFWInpLimitHysComp_MtrNm_f32))=True && ((HighFreqAssist_MtrNm_T_f32)>=(k_AsstFWInpLimitHFA_MtrNm_f32))= true &&((BaseAssistCmd_MtrNm_T_f32)>=(k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((BaseAssistCmd_MtrNm_T_f32)<=(-k_AsstFWInpLimitBaseAsst_MtrNm_f32))=False && ((DefeatAsstTblSvc_Cnt_T_lgc != D_FALSE_CNT_LGC) && (MECCounter_Cnt_T_enum != ProductionMode)) =False && ((LowFreqInput_MtrNm_T_f32)>=(UprBoundFilt_MtrNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32)<=(-UprBoundFilt_MtrNm_T_f32))=True && DefltAsst_MtrNm_T_f32 = DefltAsstLookup_MtrNm_T_f32 * ((float32)Sign_f32_m(HwTorque_HwNm_T_f32))=False && ((LowFreqInput_MtrNm_T_f32 < LwrBoundFilt_MtrNm_T_f32) ||
(LowFreqInput_MtrNm_T_f32 > UprBoundFilt_MtrNm_T_f32))=True &&((AssistFirewall_ActiveRawAcc_Cnt_M_u16)<((AsstFWPstepNstep_Cnt_T_str.Threshold)-(AsstFWPstepNstep_Cnt_T_str.Pstep)))=True && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[1])=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 > t_AsstFWPstepNstepThresh_Cnt_u16[0])=True &&(AssistFirewall_CombAsstSV_MtrNm_M_f32<=-8.8)=True&& (((Abs_f32_m(SumInput_MtrNm_T_f32 - AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=False && (AssistFirewall_CombAsstSV_MtrNm_M_f32<=-8.8)=True && (AsstFWActive_Uls_T_f32>1)=True"

(LowFreqInput_MtrNm_T_f32 > UprBoundFilt_MtrNm_T_f32))=True &&((AssistFirewall_ActiveRawAcc_Cnt_M_u16)<((AsstFWPstepNstep_Cnt_T_str.Threshold)-(AsstFWPstepNstep_Cnt_T_str.Pstep)))=True && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 >= t_AsstFWPstepNstepThresh_Cnt_u16[1])=False && (AssistFirewall_ActiveRawAcc_Cnt_M_u16 > t_AsstFWPstepNstepThresh_Cnt_u16[0])=True &&(AssistFirewall_CombAsstSV_MtrNm_M_f32<=-8.8)=True&& (((Abs_f32_m(SumInput_MtrNm_T_f32 - AssistFirewall_CombAsstSV_MtrNm_M_f32) > k_RestoreThresh_MtrNm_f32) && (AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc == TRUE)) || (TRUE == AssistFirewall_PNCountStatus_Cnt_M_lgc))=True && (AssistFirewall_CombAsstSV_MtrNm_M_f32>8.8)=False && (AssistFirewall_CombAsstSV_MtrNm_M_f32<=-8.8)=True && (AsstFWActive_Uls_T_f32>1)=False && (AsstFWActive_Uls_T_f32<=0)=True "

Test Step 3.1 (Repeat Count = 1)

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0900000036
AssistFirewall_ActiveRawAcc_Cnt_M_u16	109
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.89999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0700000003
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00999999978
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4
k_AsstFWInpLimitHFA_MtrNm_f32	2.5
k_AsstFWInpLimitHysComp_MtrNm_f32	3.78999996
k_AsstFWNstep_Cnt_u16	3928
k_AsstFWPstep_Cnt_u16	1107
k_RestoreThresh_MtrNm_f32	1.89999998
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-10240

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	26
t_AsstFWDefltAssistX_HwNm_u8p8[1]	51
t_AsstFWDefltAssistX_HwNm_u8p8[2]	77
t_AsstFWDefltAssistX_HwNm_u8p8[3]	102
t_AsstFWDefltAssistX_HwNm_u8p8[4]	128
t_AsstFWDefltAssistX_HwNm_u8p8[5]	154
t_AsstFWDefltAssistX_HwNm_u8p8[6]	179
t_AsstFWDefltAssistX_HwNm_u8p8[7]	205
t_AsstFWDefltAssistX_HwNm_u8p8[8]	230
t_AsstFWDefltAssistX_HwNm_u8p8[9]	256
t_AsstFWDefltAssistX_HwNm_u8p8[10]	282
t_AsstFWDefltAssistX_HwNm_u8p8[11]	307
t_AsstFWDefltAssistX_HwNm_u8p8[12]	333
t_AsstFWDefltAssistX_HwNm_u8p8[13]	358
t_AsstFWDefltAssistX_HwNm_u8p8[14]	384
t_AsstFWDefltAssistX_HwNm_u8p8[15]	410
t_AsstFWDefltAssistX_HwNm_u8p8[16]	435
t_AsstFWDefltAssistX_HwNm_u8p8[17]	461
t_AsstFWDefltAssistX_HwNm_u8p8[18]	486
t_AsstFWDefltAssistX_HwNm_u8p8[19]	512
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-204
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	0
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720
t_AsstFWPstepNstepThresh_Cnt_u16[0]	0
t_AsstFWPstepNstepThresh_Cnt_u16[1]	0
t_AsstFWVehSpd_Kph_u9p7[0]	1408
t_AsstFWVehSpd_Kph_u9p7[1]	1536
t_AsstFWVehSpd_Kph_u9p7[2]	1664
t_AsstFWVehSpd_Kph_u9p7[3]	1792
t_AsstFWVehSpd_Kph_u9p7[4]	1920
t_AsstFWVehSpd_Kph_u9p7[5]	2048
t_AsstFWVehSpd_Kph_u9p7[6]	2176
t_AsstFWVehSpd_Kph_u9p7[7]	2304
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-8.80000019

TEST DETAILS REPORT

Name	Input Value
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	9
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	90
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.82099986	2.8210001 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0	0 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.9920001	1.99199998 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.2329998	5.2329998 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.11900008	1.11899996 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 3.2 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0399999991
AssistFirewall_ActiveRawAcc_Cnt_M_u16	6500
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.14999998
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0299999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.39999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0199999996
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00499999989
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3
k_AsstFWInpLimitHFA_MtrNm_f32	1.5
k_AsstFWInpLimitHysComp_MtrNm_f32	1.10000002
k_AsstFWNstep_Cnt_u16	4548
k_AsstFWPstep_Cnt_u16	492
k_RestoreThresh_MtrNm_f32	1.39999998
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	0

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	102
t_AsstFWDefltAssistX_HwNm_u8p8[1]	128
t_AsstFWDefltAssistX_HwNm_u8p8[2]	154
t_AsstFWDefltAssistX_HwNm_u8p8[3]	179
t_AsstFWDefltAssistX_HwNm_u8p8[4]	205
t_AsstFWDefltAssistX_HwNm_u8p8[5]	230
t_AsstFWDefltAssistX_HwNm_u8p8[6]	256
t_AsstFWDefltAssistX_HwNm_u8p8[7]	282
t_AsstFWDefltAssistX_HwNm_u8p8[8]	307
t_AsstFWDefltAssistX_HwNm_u8p8[9]	333
t_AsstFWDefltAssistX_HwNm_u8p8[10]	358
t_AsstFWDefltAssistX_HwNm_u8p8[11]	384
t_AsstFWDefltAssistX_HwNm_u8p8[12]	410
t_AsstFWDefltAssistX_HwNm_u8p8[13]	435
t_AsstFWDefltAssistX_HwNm_u8p8[14]	461
t_AsstFWDefltAssistX_HwNm_u8p8[15]	486
t_AsstFWDefltAssistX_HwNm_u8p8[16]	512
t_AsstFWDefltAssistX_HwNm_u8p8[17]	538
t_AsstFWDefltAssistX_HwNm_u8p8[18]	563
t_AsstFWDefltAssistX_HwNm_u8p8[19]	589
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	20480
t_AsstFWPstepNstepThresh_Cnt_u16[0]	125
t_AsstFWPstepNstepThresh_Cnt_u16[1]	219
t_AsstFWVehSpd_Kph_u9p7[0]	10240
t_AsstFWVehSpd_Kph_u9p7[1]	10368
t_AsstFWVehSpd_Kph_u9p7[2]	10496
t_AsstFWVehSpd_Kph_u9p7[3]	10624
t_AsstFWVehSpd_Kph_u9p7[4]	10752
t_AsstFWVehSpd_Kph_u9p7[5]	10880
t_AsstFWVehSpd_Kph_u9p7[6]	11008
t_AsstFWVehSpd_Kph_u9p7[7]	11136

Name	Input Value
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	4
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	4
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	40
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.76000023	5.76000023 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	219	219 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.01800013	5.01800013 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	8.03999996	8.03999996 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.97000003	3.97000003 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 3.3 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	8
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_ActiveRawAcc_Cnt_M_u16	1000
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.16999996
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	7
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.60000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0399999991
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00700000022
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	1
k_AsstFWInpLimitHFA_MtrNm_f32	1.89999998
k_AsstFWInpLimitHysComp_MtrNm_f32	2.5
k_AsstFWNstep_Cnt_u16	4300
k_AsstFWPstep_Cnt_u16	738
k_RestoreThresh_MtrNm_f32	1.60000002
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	18432
t_AsstFWDefltAssistX_HwNm_u8p8[0]	154
t_AsstFWDefltAssistX_HwNm_u8p8[1]	179
t_AsstFWDefltAssistX_HwNm_u8p8[2]	205
t_AsstFWDefltAssistX_HwNm_u8p8[3]	230
t_AsstFWDefltAssistX_HwNm_u8p8[4]	256
t_AsstFWDefltAssistX_HwNm_u8p8[5]	282
t_AsstFWDefltAssistX_HwNm_u8p8[6]	307
t_AsstFWDefltAssistX_HwNm_u8p8[7]	333
t_AsstFWDefltAssistX_HwNm_u8p8[8]	358
t_AsstFWDefltAssistX_HwNm_u8p8[9]	384
t_AsstFWDefltAssistX_HwNm_u8p8[10]	410
t_AsstFWDefltAssistX_HwNm_u8p8[11]	435
t_AsstFWDefltAssistX_HwNm_u8p8[12]	461
t_AsstFWDefltAssistX_HwNm_u8p8[13]	486
t_AsstFWDefltAssistX_HwNm_u8p8[14]	512
t_AsstFWDefltAssistX_HwNm_u8p8[15]	538
t_AsstFWDefltAssistX_HwNm_u8p8[16]	563
t_AsstFWDefltAssistX_HwNm_u8p8[17]	589
t_AsstFWDefltAssistX_HwNm_u8p8[18]	614
t_AsstFWDefltAssistX_HwNm_u8p8[19]	640
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720
t_AsstFWPstepNstepThresh_Cnt_u16[0]	127
t_AsstFWPstepNstepThresh_Cnt_u16[1]	227
t_AsstFWVehSpd_Kph_u9p7[0]	16128
t_AsstFWVehSpd_Kph_u9p7[1]	16256
t_AsstFWVehSpd_Kph_u9p7[2]	16384
t_AsstFWVehSpd_Kph_u9p7[3]	16512
t_AsstFWVehSpd_Kph_u9p7[4]	16640
t_AsstFWVehSpd_Kph_u9p7[5]	16768
t_AsstFWVehSpd_Kph_u9p7[6]	16896

Name	Input Value
t_AsstFWVehSpd_Kph_u9p7[7]	17024
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-8.80000019
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	6
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	6
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	60
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7.51999998	7.51999998 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	227	227 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.73000002	6.73000002 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.51200008	2.51200008 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.95800018	5.95800018 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 3.4 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0199999996
AssistFirewall_ActiveRawAcc_Cnt_M_u16	200
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.13
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00999999978
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.20000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00899999961
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00300000003
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.20000005
k_AsstFWInpLimitHFA_MtrNm_f32	1.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	3
k_AsstFWNstep_Cnt_u16	4796
k_AsstFWPstep_Cnt_u16	246
k_RestoreThresh_MtrNm_f32	1.20000005
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-14336

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	51
t_AsstFWDefltAssistX_HwNm_u8p8[1]	77
t_AsstFWDefltAssistX_HwNm_u8p8[2]	102
t_AsstFWDefltAssistX_HwNm_u8p8[3]	128
t_AsstFWDefltAssistX_HwNm_u8p8[4]	154
t_AsstFWDefltAssistX_HwNm_u8p8[5]	179
t_AsstFWDefltAssistX_HwNm_u8p8[6]	205
t_AsstFWDefltAssistX_HwNm_u8p8[7]	230
t_AsstFWDefltAssistX_HwNm_u8p8[8]	256
t_AsstFWDefltAssistX_HwNm_u8p8[9]	282
t_AsstFWDefltAssistX_HwNm_u8p8[10]	307
t_AsstFWDefltAssistX_HwNm_u8p8[11]	333
t_AsstFWDefltAssistX_HwNm_u8p8[12]	358
t_AsstFWDefltAssistX_HwNm_u8p8[13]	384
t_AsstFWDefltAssistX_HwNm_u8p8[14]	410
t_AsstFWDefltAssistX_HwNm_u8p8[15]	435
t_AsstFWDefltAssistX_HwNm_u8p8[16]	461
t_AsstFWDefltAssistX_HwNm_u8p8[17]	486
t_AsstFWDefltAssistX_HwNm_u8p8[18]	512
t_AsstFWDefltAssistX_HwNm_u8p8[19]	538
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	0
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720
t_AsstFWPstepNstepThresh_Cnt_u16[0]	123
t_AsstFWPstepNstepThresh_Cnt_u16[1]	211
t_AsstFWVehSpd_Kph_u9p7[0]	4352
t_AsstFWVehSpd_Kph_u9p7[1]	4480
t_AsstFWVehSpd_Kph_u9p7[2]	4608
t_AsstFWVehSpd_Kph_u9p7[3]	4736
t_AsstFWVehSpd_Kph_u9p7[4]	4864
t_AsstFWVehSpd_Kph_u9p7[5]	4992

TEST DETAILS REPORT

Name	Input Value
t_AsstFWVehSpd_Kph_u9p7[6]	5120
t_AsstFWVehSpd_Kph_u9p7[7]	5248
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	8.80000019
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	2.20000005
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	2
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	20
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.92000008	3.92000008 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	211	211 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.02399993	3.02399993 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6.01800013	6.01800013 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1.98199999	1.98199999 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 3.5 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.30000019
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.400000006
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11199999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.119999997
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.219999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.80000019
k_AsstFWInpLimitHFA_MtrNm_f32	6.40999985
k_AsstFWInpLimitHysComp_MtrNm_f32	6.71000004
k_AsstFWNstep_Cnt_u16	4052
k_AsstFWPstep_Cnt_u16	2460
k_RestoreThresh_MtrNm_f32	4.42999983
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	333
t_AsstFWDefltAssistX_HwNm_u8p8[1]	358
t_AsstFWDefltAssistX_HwNm_u8p8[2]	384
t_AsstFWDefltAssistX_HwNm_u8p8[3]	410
t_AsstFWDefltAssistX_HwNm_u8p8[4]	435
t_AsstFWDefltAssistX_HwNm_u8p8[5]	461
t_AsstFWDefltAssistX_HwNm_u8p8[6]	486
t_AsstFWDefltAssistX_HwNm_u8p8[7]	512
t_AsstFWDefltAssistX_HwNm_u8p8[8]	538
t_AsstFWDefltAssistX_HwNm_u8p8[9]	563
t_AsstFWDefltAssistX_HwNm_u8p8[10]	589
t_AsstFWDefltAssistX_HwNm_u8p8[11]	614
t_AsstFWDefltAssistX_HwNm_u8p8[12]	640
t_AsstFWDefltAssistX_HwNm_u8p8[13]	666
t_AsstFWDefltAssistX_HwNm_u8p8[14]	691
t_AsstFWDefltAssistX_HwNm_u8p8[15]	717
t_AsstFWDefltAssistX_HwNm_u8p8[16]	742
t_AsstFWDefltAssistX_HwNm_u8p8[17]	768
t_AsstFWDefltAssistX_HwNm_u8p8[18]	794
t_AsstFWDefltAssistX_HwNm_u8p8[19]	819
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-204
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	0
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720
t_AsstFWPstepNstepThresh_Cnt_u16[0]	134
t_AsstFWPstepNstepThresh_Cnt_u16[1]	255
t_AsstFWVehSpd_Kph_u9p7[0]	36736
t_AsstFWVehSpd_Kph_u9p7[1]	36864
t_AsstFWVehSpd_Kph_u9p7[2]	36992
t_AsstFWVehSpd_Kph_u9p7[3]	37120
t_AsstFWVehSpd_Kph_u9p7[4]	37248

TEST DETAILS REPORT

Name	Input Value
t_AsstFWVehSpd_Kph_u9p7[5]	37376
t_AsstFWVehSpd_Kph_u9p7[6]	37504
t_AsstFWVehSpd_Kph_u9p7[7]	37632
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.19999981
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	1
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.5999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.4000001
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.5999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.30000019	-5.30000019 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487	8487 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-16	-16 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-6.06399965	-6.06399965 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019	-5.30000019 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999	5.0999999 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-16	-16 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x00	0x00	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x00	0x00	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 3.6 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.20000005
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0799999982
AssistFirewall_ActiveRawAcc_Cnt_M_u16	106
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.19000006
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.10000002
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0700000003
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.0999999
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0599999987
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	8
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00899999961
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3
k_AsstFWInpLimitHFA_MtrNm_f32	1.29999995
k_AsstFWInpLimitHysComp_MtrNm_f32	3.29999995
k_AsstFWNstep_Cnt_u16	4052
k_AsstFWPstep_Cnt_u16	984
k_RestoreThresh_MtrNm_f32	1.79999995
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	205
t_AsstFWDefltAssistX_HwNm_u8p8[1]	230
t_AsstFWDefltAssistX_HwNm_u8p8[2]	256
t_AsstFWDefltAssistX_HwNm_u8p8[3]	282
t_AsstFWDefltAssistX_HwNm_u8p8[4]	307
t_AsstFWDefltAssistX_HwNm_u8p8[5]	333
t_AsstFWDefltAssistX_HwNm_u8p8[6]	358
t_AsstFWDefltAssistX_HwNm_u8p8[7]	384
t_AsstFWDefltAssistX_HwNm_u8p8[8]	410
t_AsstFWDefltAssistX_HwNm_u8p8[9]	435
t_AsstFWDefltAssistX_HwNm_u8p8[10]	461
t_AsstFWDefltAssistX_HwNm_u8p8[11]	486
t_AsstFWDefltAssistX_HwNm_u8p8[12]	512
t_AsstFWDefltAssistX_HwNm_u8p8[13]	538
t_AsstFWDefltAssistX_HwNm_u8p8[14]	563
t_AsstFWDefltAssistX_HwNm_u8p8[15]	589
t_AsstFWDefltAssistX_HwNm_u8p8[16]	614
t_AsstFWDefltAssistX_HwNm_u8p8[17]	640
t_AsstFWDefltAssistX_HwNm_u8p8[18]	666
t_AsstFWDefltAssistX_HwNm_u8p8[19]	691
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-204
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	0
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720
t_AsstFWPstepNstepThresh_Cnt_u16[0]	129
t_AsstFWPstepNstepThresh_Cnt_u16[1]	235
t_AsstFWVehSpd_Kph_u9p7[0]	22016
t_AsstFWVehSpd_Kph_u9p7[1]	22144
t_AsstFWVehSpd_Kph_u9p7[2]	22272
t_AsstFWVehSpd_Kph_u9p7[3]	22400
t_AsstFWVehSpd_Kph_u9p7[4]	22528
t_AsstFWVehSpd_Kph_u9p7[5]	22656

TEST DETAILS REPORT

Name	Input Value
t_AsstFWVehSpd_Kph_u9p7[6]	22784
t_AsstFWVehSpd_Kph_u9p7[7]	22912
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	0
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	8
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	80
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.02400017	2.02399993 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	235	235 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.46399999	1.46399999 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	4.33400011	4.33400011 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.9460001	7.9460001 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 3.7 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00600000005
AssistFirewall_ActiveRawAcc_Cnt_M_u16	115
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.29999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0599999987
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.01999998
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0900000036
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0299999993
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.4000001
k_AsstFWInpLimitHFA_MtrNm_f32	2.20000005
k_AsstFWInpLimitHysComp_MtrNm_f32	4.76999998
k_AsstFWNstep_Cnt_u16	3680
k_AsstFWPstep_Cnt_u16	1353
k_RestoreThresh_MtrNm_f32	2.0999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	282
t_AsstFWDefltAssistX_HwNm_u8p8[1]	307
t_AsstFWDefltAssistX_HwNm_u8p8[2]	333
t_AsstFWDefltAssistX_HwNm_u8p8[3]	358
t_AsstFWDefltAssistX_HwNm_u8p8[4]	384
t_AsstFWDefltAssistX_HwNm_u8p8[5]	410
t_AsstFWDefltAssistX_HwNm_u8p8[6]	435
t_AsstFWDefltAssistX_HwNm_u8p8[7]	461
t_AsstFWDefltAssistX_HwNm_u8p8[8]	486
t_AsstFWDefltAssistX_HwNm_u8p8[9]	512
t_AsstFWDefltAssistX_HwNm_u8p8[10]	538
t_AsstFWDefltAssistX_HwNm_u8p8[11]	563
t_AsstFWDefltAssistX_HwNm_u8p8[12]	589
t_AsstFWDefltAssistX_HwNm_u8p8[13]	614
t_AsstFWDefltAssistX_HwNm_u8p8[14]	640
t_AsstFWDefltAssistX_HwNm_u8p8[15]	666
t_AsstFWDefltAssistX_HwNm_u8p8[16]	691
t_AsstFWDefltAssistX_HwNm_u8p8[17]	717
t_AsstFWDefltAssistX_HwNm_u8p8[18]	742
t_AsstFWDefltAssistX_HwNm_u8p8[19]	768
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	20480
t_AsstFWPstepNstepThresh_Cnt_u16[0]	132
t_AsstFWPstepNstepThresh_Cnt_u16[1]	247
t_AsstFWVehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1]	30976
t_AsstFWVehSpd_Kph_u9p7[2]	31104
t_AsstFWVehSpd_Kph_u9p7[3]	31232
t_AsstFWVehSpd_Kph_u9p7[4]	31360

TEST DETAILS REPORT

Name	Input Value

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	18432

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	8192
t_AsstFWDefltAssistX_HwNm_u8p8[0]	282
t_AsstFWDefltAssistX_HwNm_u8p8[1]	307
t_AsstFWDefltAssistX_HwNm_u8p8[2]	333
t_AsstFWDefltAssistX_HwNm_u8p8[3]	358
t_AsstFWDefltAssistX_HwNm_u8p8[4]	384
t_AsstFWDefltAssistX_HwNm_u8p8[5]	410
t_AsstFWDefltAssistX_HwNm_u8p8[6]	435
t_AsstFWDefltAssistX_HwNm_u8p8[7]	461
t_AsstFWDefltAssistX_HwNm_u8p8[8]	486
t_AsstFWDefltAssistX_HwNm_u8p8[9]	512
t_AsstFWDefltAssistX_HwNm_u8p8[10]	538
t_AsstFWDefltAssistX_HwNm_u8p8[11]	563
t_AsstFWDefltAssistX_HwNm_u8p8[12]	589
t_AsstFWDefltAssistX_HwNm_u8p8[13]	614
t_AsstFWDefltAssistX_HwNm_u8p8[14]	640
t_AsstFWDefltAssistX_HwNm_u8p8[15]	666
t_AsstFWDefltAssistX_HwNm_u8p8[16]	691
t_AsstFWDefltAssistX_HwNm_u8p8[17]	717
t_AsstFWDefltAssistX_HwNm_u8p8[18]	742
t_AsstFWDefltAssistX_HwNm_u8p8[19]	768
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	30720
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720
t_AsstFWPstepNstepThresh_Cnt_u16[0]	170
t_AsstFWPstepNstepThresh_Cnt_u16[1]	399
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456

TEST DETAILS REPORT

Name	Input Value
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
t_AsstFWVehSpd_Kph_u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	4.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-9
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1.10000002
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	77
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1.98000002	1.98000002 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	246	246 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	4	4 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.15799999	1.15799999 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-6.19999981	-6.19999981 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	7.90100002	7.90100002 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	4	4 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x00	0x00	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x00	0x00	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 3.9 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	7
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0500000007
AssistFirewall_ActiveRawAcc_Cnt_M_u16	800
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	1.15999997
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0399999991
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.5
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.0299999993
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00600000005
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2
k_AsstFWInpLimitHFA_MtrNm_f32	1.70000005
k_AsstFWInpLimitHysComp_MtrNm_f32	2.0999999
k_AsstFWNstep_Cnt_u16	4424
k_AsstFWPstep_Cnt_u16	615
k_RestoreThresh_MtrNm_f32	1.5
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	-2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-14336

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	14336
t_AsstFWDefltAssistX_HwNm_u8p8[0]	128
t_AsstFWDefltAssistX_HwNm_u8p8[1]	154
t_AsstFWDefltAssistX_HwNm_u8p8[2]	179
t_AsstFWDefltAssistX_HwNm_u8p8[3]	205
t_AsstFWDefltAssistX_HwNm_u8p8[4]	230
t_AsstFWDefltAssistX_HwNm_u8p8[5]	256
t_AsstFWDefltAssistX_HwNm_u8p8[6]	282
t_AsstFWDefltAssistX_HwNm_u8p8[7]	307
t_AsstFWDefltAssistX_HwNm_u8p8[8]	333
t_AsstFWDefltAssistX_HwNm_u8p8[9]	358
t_AsstFWDefltAssistX_HwNm_u8p8[10]	384
t_AsstFWDefltAssistX_HwNm_u8p8[11]	410
t_AsstFWDefltAssistX_HwNm_u8p8[12]	435
t_AsstFWDefltAssistX_HwNm_u8p8[13]	461
t_AsstFWDefltAssistX_HwNm_u8p8[14]	486
t_AsstFWDefltAssistX_HwNm_u8p8[15]	512
t_AsstFWDefltAssistX_HwNm_u8p8[16]	538
t_AsstFWDefltAssistX_HwNm_u8p8[17]	563
t_AsstFWDefltAssistX_HwNm_u8p8[18]	589
t_AsstFWDefltAssistX_HwNm_u8p8[19]	614
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	28672
t_AsstFWPstepNstepThresh_Cnt_u16[0]	126
t_AsstFWPstepNstepThresh_Cnt_u16[1]	223
t_AsstFWVehSpd_Kph_u9p7[0]	13184
t_AsstFWVehSpd_Kph_u9p7[1]	13312
t_AsstFWVehSpd_Kph_u9p7[2]	13440

TEST DETAILS REPORT

Name	Input Value
t_AsstFWVehSpd_Kph_u9p7[3]	13568
t_AsstFWVehSpd_Kph_u9p7[4]	13696
t_AsstFWVehSpd_Kph_u9p7[5]	13824
t_AsstFWVehSpd_Kph_u9p7[6]	13952
t_AsstFWVehSpd_Kph_u9p7[7]	14080
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	5
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	1
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	50
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	6.6500001	6.6500001 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	223	223 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019	8.80000019 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	5.83199978	5.83199978 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	1.39700007	1.39699996 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	4.96400023	4.96400023 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.80000019	8.80000019 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 3.10 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.79999995
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.100000001
AssistFirewall_ActiveRawAcc_Cnt_M_u16	344
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	6.30000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0500000007
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.79999995
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.5
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.129999995
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.19999981
k_AsstFWInpLimitHFA_MtrNm_f32	1.70000005
k_AsstFWInpLimitHysComp_MtrNm_f32	4.5
k_AsstFWNstep_Cnt_u16	2564
k_AsstFWPstep_Cnt_u16	2214
k_RestoreThresh_MtrNm_f32	3.30999994
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-10240

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-30720
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	8192

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	10240
t_AsstFWDefltAssistX_HwNm_u8p8[0]	230
t_AsstFWDefltAssistX_HwNm_u8p8[1]	256
t_AsstFWDefltAssistX_HwNm_u8p8[2]	282
t_AsstFWDefltAssistX_HwNm_u8p8[3]	307
t_AsstFWDefltAssistX_HwNm_u8p8[4]	333
t_AsstFWDefltAssistX_HwNm_u8p8[5]	358
t_AsstFWDefltAssistX_HwNm_u8p8[6]	384
t_AsstFWDefltAssistX_HwNm_u8p8[7]	410
t_AsstFWDefltAssistX_HwNm_u8p8[8]	435
t_AsstFWDefltAssistX_HwNm_u8p8[9]	461
t_AsstFWDefltAssistX_HwNm_u8p8[10]	486
t_AsstFWDefltAssistX_HwNm_u8p8[11]	512
t_AsstFWDefltAssistX_HwNm_u8p8[12]	538
t_AsstFWDefltAssistX_HwNm_u8p8[13]	563
t_AsstFWDefltAssistX_HwNm_u8p8[14]	589
t_AsstFWDefltAssistX_HwNm_u8p8[15]	614
t_AsstFWDefltAssistX_HwNm_u8p8[16]	640
t_AsstFWDefltAssistX_HwNm_u8p8[17]	666
t_AsstFWDefltAssistX_HwNm_u8p8[18]	691
t_AsstFWDefltAssistX_HwNm_u8p8[19]	717
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-204
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	0
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720
t_AsstFWPstepNstepThresh_Cnt_u16[0]	5000
t_AsstFWPstepNstepThresh_Cnt_u16[1]	5000
t_AsstFWVehSpd_Kph_u9p7[0]	30848
t_AsstFWVehSpd_Kph_u9p7[1]	30976

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	-4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	28672
t_AsstFWDefltAssistX_HwNm_u8p8[0]	128
t_AsstFWDefltAssistX_HwNm_u8p8[1]	154
t_AsstFWDefltAssistX_HwNm_u8p8[2]	179
t_AsstFWDefltAssistX_HwNm_u8p8[3]	205
t_AsstFWDefltAssistX_HwNm_u8p8[4]	230
t_AsstFWDefltAssistX_HwNm_u8p8[5]	256
t_AsstFWDefltAssistX_HwNm_u8p8[6]	282
t_AsstFWDefltAssistX_HwNm_u8p8[7]	307
t_AsstFWDefltAssistX_HwNm_u8p8[8]	333
t_AsstFWDefltAssistX_HwNm_u8p8[9]	358
t_AsstFWDefltAssistX_HwNm_u8p8[10]	384
t_AsstFWDefltAssistX_HwNm_u8p8[11]	410
t_AsstFWDefltAssistX_HwNm_u8p8[12]	435
t_AsstFWDefltAssistX_HwNm_u8p8[13]	461
t_AsstFWDefltAssistX_HwNm_u8p8[14]	486
t_AsstFWDefltAssistX_HwNm_u8p8[15]	512
t_AsstFWDefltAssistX_HwNm_u8p8[16]	538
t_AsstFWDefltAssistX_HwNm_u8p8[17]	563
t_AsstFWDefltAssistX_HwNm_u8p8[18]	589
t_AsstFWDefltAssistX_HwNm_u8p8[19]	614
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	20480
t_AsstFWPstepNstepThresh_Cnt_u16[0]	202
t_AsstFWPstepNstepThresh_Cnt_u16[1]	527
t_AsstFWVehSpd_Kph_u9p7[0]	19072

Name	Input Value
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
t_AsstFWVehSpd_Kph_u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-3
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	2
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	123
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.99000001	0.99000001 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	0	0 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0	0	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.19999981	8.19999981 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	4.30499983	4.30499983 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-1	-1 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	0	0	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	3.15699983	3.15700006 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.99000001	0.99000001 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	8.19999981	8.19999981 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x00	0x00	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x00	0x00	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 3.12 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00999999978
AssistFirewall_ActiveRawAcc_Cnt_M_u16	112
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.20000005
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	2
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00899999961
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.10000002
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00800000038
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	1
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00200000009
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	2.0999999
k_AsstFWInpLimitHFA_MtrNm_f32	2.5999999
k_AsstFWInpLimitHysComp_MtrNm_f32	4.28000021
k_AsstFWNstep_Cnt_u16	3804
k_AsstFWPstep_Cnt_u16	1230

TEST DETAILS REPORT

Name	Input Value
k_RestoreThresh_MtrNm_f32	2
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-10240

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	6144
t_AsstFWDefltAssistX_HwNm_u8p8[0]	256
t_AsstFWDefltAssistX_HwNm_u8p8[1]	282
t_AsstFWDefltAssistX_HwNm_u8p8[2]	307
t_AsstFWDefltAssistX_HwNm_u8p8[3]	333
t_AsstFWDefltAssistX_HwNm_u8p8[4]	358
t_AsstFWDefltAssistX_HwNm_u8p8[5]	384
t_AsstFWDefltAssistX_HwNm_u8p8[6]	410
t_AsstFWDefltAssistX_HwNm_u8p8[7]	435
t_AsstFWDefltAssistX_HwNm_u8p8[8]	461
t_AsstFWDefltAssistX_HwNm_u8p8[9]	486
t_AsstFWDefltAssistX_HwNm_u8p8[10]	512
t_AsstFWDefltAssistX_HwNm_u8p8[11]	538
t_AsstFWDefltAssistX_HwNm_u8p8[12]	563
t_AsstFWDefltAssistX_HwNm_u8p8[13]	589
t_AsstFWDefltAssistX_HwNm_u8p8[14]	614
t_AsstFWDefltAssistX_HwNm_u8p8[15]	640
t_AsstFWDefltAssistX_HwNm_u8p8[16]	666
t_AsstFWDefltAssistX_HwNm_u8p8[17]	691
t_AsstFWDefltAssistX_HwNm_u8p8[18]	717
t_AsstFWDefltAssistX_HwNm_u8p8[19]	742
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	24576
t_AsstFWPstepNstepThresh_Cnt_u16[0]	131
t_AsstFWPstepNstepThresh_Cnt_u16[1]	243

TEST DETAILS REPORT

Name	Input Value
t_AsstFWVehSpd_Kph_u9p7[0]	27904
t_AsstFWVehSpd_Kph_u9p7[1]	28032
t_AsstFWVehSpd_Kph_u9p7[2]	28160
t_AsstFWVehSpd_Kph_u9p7[3]	28288
t_AsstFWVehSpd_Kph_u9p7[4]	28416
t_AsstFWVehSpd_Kph_u9p7[5]	28544
t_AsstFWVehSpd_Kph_u9p7[6]	28672
t_AsstFWVehSpd_Kph_u9p7[7]	28800
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	1
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	1
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	10
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	2.97000003	2.97000003 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	243	243 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	1	1 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	1.97660005	1.97660005 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.0079999	5.0079999 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	0.987999976	0.987999976 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	1	1 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 3.13 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	1
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00800000038
AssistFirewall_ActiveRawAcc_Cnt_M_u16	121
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.5
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.0999999
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00899999961
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.03999996
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	3
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00600000005
AssistFirewall_PNCountStatus_Cnt_M_lgc	0
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0500000007
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3
k_AsstFWInpLimitHFA_MtrNm_f32	4.5
k_AsstFWInpLimitHysComp_MtrNm_f32	5.75
k_AsstFWNstep_Cnt_u16	3432

TEST DETAILS REPORT

Name	Input Value
k_AsstFWPstep_Cnt_u16	1599
k_RestoreThresh_MtrNm_f32	2.29999995
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	-6144

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	12288
t_AsstFWDefltAssistX_HwNm_u8p8[0]	333
t_AsstFWDefltAssistX_HwNm_u8p8[1]	358
t_AsstFWDefltAssistX_HwNm_u8p8[2]	384
t_AsstFWDefltAssistX_HwNm_u8p8[3]	410
t_AsstFWDefltAssistX_HwNm_u8p8[4]	435
t_AsstFWDefltAssistX_HwNm_u8p8[5]	461
t_AsstFWDefltAssistX_HwNm_u8p8[6]	486
t_AsstFWDefltAssistX_HwNm_u8p8[7]	512
t_AsstFWDefltAssistX_HwNm_u8p8[8]	538
t_AsstFWDefltAssistX_HwNm_u8p8[9]	563
t_AsstFWDefltAssistX_HwNm_u8p8[10]	589
t_AsstFWDefltAssistX_HwNm_u8p8[11]	614
t_AsstFWDefltAssistX_HwNm_u8p8[12]	640
t_AsstFWDefltAssistX_HwNm_u8p8[13]	666
t_AsstFWDefltAssistX_HwNm_u8p8[14]	691
t_AsstFWDefltAssistX_HwNm_u8p8[15]	717
t_AsstFWDefltAssistX_HwNm_u8p8[16]	742
t_AsstFWDefltAssistX_HwNm_u8p8[17]	768
t_AsstFWDefltAssistX_HwNm_u8p8[18]	794
t_AsstFWDefltAssistX_HwNm_u8p8[19]	819
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720
t_AsstFWPstepNstepThresh_Cnt_u16[0]	134

TEST DETAILS REPORT

Name	Input Value
t_AsstFWPstepNstepThresh_Cnt_u16[1]	255
t_AsstFWVehSpd_Kph_u9p7[0]	36736
t_AsstFWVehSpd_Kph_u9p7[1]	36864
t_AsstFWVehSpd_Kph_u9p7[2]	36992
t_AsstFWVehSpd_Kph_u9p7[3]	37120
t_AsstFWVehSpd_Kph_u9p7[4]	37248
t_AsstFWVehSpd_Kph_u9p7[5]	37376
t_AsstFWVehSpd_Kph_u9p7[6]	37504
t_AsstFWVehSpd_Kph_u9p7[7]	37632
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	8
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	0
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	5.0999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	44
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	0.991999984	0.991999984 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	255	255 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	5	5 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	6.14589977	6.14589977 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	2.95799994	2.95799994 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.04500008	5.04500008 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0.991999984	0.991999984 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	5	5 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 3.14 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.30000019
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.400000006
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11199999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.119999997
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.219999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.80000019
k_AsstFWInpLimitHFA_MtrNm_f32	6.40999985
k_AsstFWInpLimitHysComp_MtrNm_f32	6.71000004

TEST DETAILS REPORT

Name	Input Value
k_AsstFWNstep_Cnt_u16	4052
k_AsstFWPstep_Cnt_u16	2460
k_RestoreThresh_MtrNm_f32	4.42999983
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-18432
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	947
t_AsstFWDefltAssistX_HwNm_u8p8[1]	947
t_AsstFWDefltAssistX_HwNm_u8p8[2]	998
t_AsstFWDefltAssistX_HwNm_u8p8[3]	998
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1408
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1408
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-204
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	0
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720

TEST DETAILS REPORT

Name	Input Value
t_AsstFWPstepNstepThresh_Cnt_u16[0]	234
t_AsstFWPstepNstepThresh_Cnt_u16[1]	655
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
t_AsstFWVehSpd_Kph_u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.19999981
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	1
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.5999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.4000001
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.5999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-3.18000007	-3.18000007 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	655	655 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019	-8.80000019 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-6.06399965	-6.06400013 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-4.90400028	-4.90399981 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.79002142	2.79002142 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-8.80000019	-8.80000019 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 3.15 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-5.30000019
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.400000006
AssistFirewall_ActiveRawAcc_Cnt_M_u16	8487
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1
AssistFirewall_CombAsstSV_MtrNm_M_f32	8.80000019
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-5.19999981
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0799999982
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.11199999
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-5.30000019
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.119999997
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	5.0999999
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.219999999
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	4.80000019
k_AsstFWInpLimitHFA_MtrNm_f32	6.40999985

t2_AsstFWUprBoundX_HwNm_s4p1151][1] -8192

Name	Input Value
k_AsstFWInpLimitHysComp_MtrNm_f32	6.71000004
k_AsstFWNstep_Cnt_u16	4052
k_AsstFWPstep_Cnt_u16	2460
k_RestoreThresh_MtrNm_f32	4.42999983
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	=

t2_AsstFWUprBoundX_HwNm_s4p1151][0]
t2_AsstFWUprBoundX_HwNm_s4p1142][0]

t2_AsstFWUprBoundX_HwNm_s4p1142][7]

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	22528

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	4096
t_AsstFWDefltAssistX_HwNm_u8p8[0]	947
t_AsstFWDefltAssistX_HwNm_u8p8[1]	973
t_AsstFWDefltAssistX_HwNm_u8p8[2]	998
t_AsstFWDefltAssistX_HwNm_u8p8[3]	1024
t_AsstFWDefltAssistX_HwNm_u8p8[4]	1050
t_AsstFWDefltAssistX_HwNm_u8p8[5]	1075
t_AsstFWDefltAssistX_HwNm_u8p8[6]	1101
t_AsstFWDefltAssistX_HwNm_u8p8[7]	1126
t_AsstFWDefltAssistX_HwNm_u8p8[8]	1152
t_AsstFWDefltAssistX_HwNm_u8p8[9]	1178
t_AsstFWDefltAssistX_HwNm_u8p8[10]	1203
t_AsstFWDefltAssistX_HwNm_u8p8[11]	1229
t_AsstFWDefltAssistX_HwNm_u8p8[12]	1254
t_AsstFWDefltAssistX_HwNm_u8p8[13]	1280
t_AsstFWDefltAssistX_HwNm_u8p8[14]	1306
t_AsstFWDefltAssistX_HwNm_u8p8[15]	1331
t_AsstFWDefltAssistX_HwNm_u8p8[16]	1357
t_AsstFWDefltAssistX_HwNm_u8p8[17]	1382
t_AsstFWDefltAssistX_HwNm_u8p8[18]	1408
t_AsstFWDefltAssistX_HwNm_u8p8[19]	1434
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	-204
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	0
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	2048
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	4096
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	10240
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	12288
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	14336
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	16384
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	18432
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	20480
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	22528
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	24576
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	26624
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	28672

TEST DETAILS REPORT

Name	Input Value
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	30720
t_AsstFWPstepNstepThresh_Cnt_u16[0]	234
t_AsstFWPstepNstepThresh_Cnt_u16[1]	655
t_AsstFWVehSpd_Kph_u9p7[0]	19072
t_AsstFWVehSpd_Kph_u9p7[1]	19200
t_AsstFWVehSpd_Kph_u9p7[2]	19328
t_AsstFWVehSpd_Kph_u9p7[3]	19456
t_AsstFWVehSpd_Kph_u9p7[4]	19584
t_AsstFWVehSpd_Kph_u9p7[5]	19712
t_AsstFWVehSpd_Kph_u9p7[6]	19840
t_AsstFWVehSpd_Kph_u9p7[7]	19968
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	-5.19999981
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	1
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	-5.5999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-5.4000001
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-5.5999999
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	176
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	-3.18000007	-3.18000007 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	655	655 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-8.80000019	-8.80000019 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	-6.06399965	-6.06400013 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	-4.90400028	-4.90399981 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.79002142	2.79002142 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	0	0 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-8.80000019	-8.80000019 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

Test Step 3.16 (Repeat Count = 1) ✔

Name	Input Value
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	4
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.0199999996
AssistFirewall_ActiveRawAcc_Cnt_M_u16	130
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	0
AssistFirewall_CombAsstSV_MtrNm_M_f32	-1.79999995
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.0299999993
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.07000005
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	6
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00899999961
AssistFirewall_PNCountStatus_Cnt_M_lgc	1
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.0799999982
Rte_Inst_Ap_AssistFirewall	tgt_Rte_Inst_Ap_AssistFirewall
k_AsstFWInpLimitBaseAsst_MtrNm_f32	3.9000001

TEST DETAILS REPORT

Name	Input Value
k_AsstFWInpLimitHFA_MtrNm_f32	1.89999998
k_AsstFWInpLimitHysComp_MtrNm_f32	1.39999998
k_AsstFWNstep_Cnt_u16	3060
k_AsstFWPstep_Cnt_u16	1968
k_RestoreThresh_MtrNm_f32	2.5999999
t2_AsstFWUprBoundX_HwNm_s4p11[0][0]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][1]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][2]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][3]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][4]	0
t2_AsstFWUprBoundX_HwNm_s4p11[0][5]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[0][6]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[0][7]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[0][8]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[0][9]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[0][10]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[1][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[1][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[1][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[1][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[1][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[1][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[1][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[2][0]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][1]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][2]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][3]	0
t2_AsstFWUprBoundX_HwNm_s4p11[2][4]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[2][5]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[2][6]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[2][7]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[2][8]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[2][9]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[2][10]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[3][0]	-10240
t2_AsstFWUprBoundX_HwNm_s4p11[3][1]	-8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][2]	-6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][3]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][4]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][5]	0
t2_AsstFWUprBoundX_HwNm_s4p11[3][6]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[3][7]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[3][8]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[3][9]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[3][10]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[4][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[4][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[4][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[4][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[4][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[4][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[4][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[4][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[4][10]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[5][0]	-4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][1]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][2]	0
t2_AsstFWUprBoundX_HwNm_s4p11[5][3]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[5][4]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[5][5]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[5][6]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[5][7]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[5][8]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[5][9]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[5][10]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][0]	0
t2_AsstFWUprBoundX_HwNm_s4p11[6][1]	2048

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundX_HwNm_s4p11[6][2]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[6][3]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[6][4]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[6][5]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[6][6]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[6][7]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[6][8]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[6][9]	18432
t2_AsstFWUprBoundX_HwNm_s4p11[6][10]	20480
t2_AsstFWUprBoundX_HwNm_s4p11[7][0]	-2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][1]	0
t2_AsstFWUprBoundX_HwNm_s4p11[7][2]	2048
t2_AsstFWUprBoundX_HwNm_s4p11[7][3]	4096
t2_AsstFWUprBoundX_HwNm_s4p11[7][4]	6144
t2_AsstFWUprBoundX_HwNm_s4p11[7][5]	8192
t2_AsstFWUprBoundX_HwNm_s4p11[7][6]	10240
t2_AsstFWUprBoundX_HwNm_s4p11[7][7]	12288
t2_AsstFWUprBoundX_HwNm_s4p11[7][8]	14336
t2_AsstFWUprBoundX_HwNm_s4p11[7][9]	16384
t2_AsstFWUprBoundX_HwNm_s4p11[7][10]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[0][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[0][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[0][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[0][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[0][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[0][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[0][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[0][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[0][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[0][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[1][0]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][1]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][2]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][3]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][4]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[1][5]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[1][6]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[1][7]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[1][8]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[1][9]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[1][10]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][0]	-28672
t2_AsstFWUprBoundY_MtrNm_s4p11[2][1]	-26624
t2_AsstFWUprBoundY_MtrNm_s4p11[2][2]	-24576
t2_AsstFWUprBoundY_MtrNm_s4p11[2][3]	-22528
t2_AsstFWUprBoundY_MtrNm_s4p11[2][4]	-20480
t2_AsstFWUprBoundY_MtrNm_s4p11[2][5]	-18432
t2_AsstFWUprBoundY_MtrNm_s4p11[2][6]	-16384
t2_AsstFWUprBoundY_MtrNm_s4p11[2][7]	-14336
t2_AsstFWUprBoundY_MtrNm_s4p11[2][8]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[2][9]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[2][10]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][0]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[3][1]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[3][2]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[3][3]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[3][4]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[3][5]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[3][6]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[3][7]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[3][8]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[3][9]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[3][10]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[4][0]	-12288
t2_AsstFWUprBoundY_MtrNm_s4p11[4][1]	-10240
t2_AsstFWUprBoundY_MtrNm_s4p11[4][2]	-8192
t2_AsstFWUprBoundY_MtrNm_s4p11[4][3]	-6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][4]	-4096
t2_AsstFWUprBoundY_MtrNm_s4p11[4][5]	-2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][6]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[4][7]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[4][8]	4096

TEST DETAILS REPORT

Name	Input Value
t2_AsstFWUprBoundY_MtrNm_s4p11[4][9]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[4][10]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][0]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[5][1]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[5][2]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[5][3]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[5][4]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[5][5]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[5][6]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[5][7]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[5][8]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[5][9]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[5][10]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][0]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[6][1]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[6][2]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[6][3]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[6][4]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[6][5]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[6][6]	20480
t2_AsstFWUprBoundY_MtrNm_s4p11[6][7]	22528
t2_AsstFWUprBoundY_MtrNm_s4p11[6][8]	24576
t2_AsstFWUprBoundY_MtrNm_s4p11[6][9]	26624
t2_AsstFWUprBoundY_MtrNm_s4p11[6][10]	28672
t2_AsstFWUprBoundY_MtrNm_s4p11[7][0]	0
t2_AsstFWUprBoundY_MtrNm_s4p11[7][1]	2048
t2_AsstFWUprBoundY_MtrNm_s4p11[7][2]	4096
t2_AsstFWUprBoundY_MtrNm_s4p11[7][3]	6144
t2_AsstFWUprBoundY_MtrNm_s4p11[7][4]	8192
t2_AsstFWUprBoundY_MtrNm_s4p11[7][5]	10240
t2_AsstFWUprBoundY_MtrNm_s4p11[7][6]	12288
t2_AsstFWUprBoundY_MtrNm_s4p11[7][7]	14336
t2_AsstFWUprBoundY_MtrNm_s4p11[7][8]	16384
t2_AsstFWUprBoundY_MtrNm_s4p11[7][9]	18432
t2_AsstFWUprBoundY_MtrNm_s4p11[7][10]	20480
t_AsstFWDefltAssistX_HwNm_u8p8[0]	410
t_AsstFWDefltAssistX_HwNm_u8p8[1]	435
t_AsstFWDefltAssistX_HwNm_u8p8[2]	461
t_AsstFWDefltAssistX_HwNm_u8p8[3]	486
t_AsstFWDefltAssistX_HwNm_u8p8[4]	512
t_AsstFWDefltAssistX_HwNm_u8p8[5]	538
t_AsstFWDefltAssistX_HwNm_u8p8[6]	563
t_AsstFWDefltAssistX_HwNm_u8p8[7]	589
t_AsstFWDefltAssistX_HwNm_u8p8[8]	614
t_AsstFWDefltAssistX_HwNm_u8p8[9]	640
t_AsstFWDefltAssistX_HwNm_u8p8[10]	666
t_AsstFWDefltAssistX_HwNm_u8p8[11]	691
t_AsstFWDefltAssistX_HwNm_u8p8[12]	717
t_AsstFWDefltAssistX_HwNm_u8p8[13]	742
t_AsstFWDefltAssistX_HwNm_u8p8[14]	768
t_AsstFWDefltAssistX_HwNm_u8p8[15]	794
t_AsstFWDefltAssistX_HwNm_u8p8[16]	819
t_AsstFWDefltAssistX_HwNm_u8p8[17]	845
t_AsstFWDefltAssistX_HwNm_u8p8[18]	870
t_AsstFWDefltAssistX_HwNm_u8p8[19]	896
t_AsstFWDefltAssistY_MtrNm_s4p11[0]	5120
t_AsstFWDefltAssistY_MtrNm_s4p11[1]	5324
t_AsstFWDefltAssistY_MtrNm_s4p11[2]	5529
t_AsstFWDefltAssistY_MtrNm_s4p11[3]	5734
t_AsstFWDefltAssistY_MtrNm_s4p11[4]	5939
t_AsstFWDefltAssistY_MtrNm_s4p11[5]	6144
t_AsstFWDefltAssistY_MtrNm_s4p11[6]	6348
t_AsstFWDefltAssistY_MtrNm_s4p11[7]	6553
t_AsstFWDefltAssistY_MtrNm_s4p11[8]	6758
t_AsstFWDefltAssistY_MtrNm_s4p11[9]	6963
t_AsstFWDefltAssistY_MtrNm_s4p11[10]	7168
t_AsstFWDefltAssistY_MtrNm_s4p11[11]	7372
t_AsstFWDefltAssistY_MtrNm_s4p11[12]	7577
t_AsstFWDefltAssistY_MtrNm_s4p11[13]	7782
t_AsstFWDefltAssistY_MtrNm_s4p11[14]	7987
t_AsstFWDefltAssistY_MtrNm_s4p11[15]	8192
t_AsstFWDefltAssistY_MtrNm_s4p11[16]	8396
t_AsstFWDefltAssistY_MtrNm_s4p11[17]	8601

TEST DETAILS REPORT

Name	Input Value
t_AsstFWDefltAssistY_MtrNm_s4p11[18]	8806
t_AsstFWDefltAssistY_MtrNm_s4p11[19]	9011
t_AsstFWPstepNstepThresh_Cnt_u16[0]	137
t_AsstFWPstepNstepThresh_Cnt_u16[1]	267
t_AsstFWVehSpd_Kph_u9p7[0]	45568
t_AsstFWVehSpd_Kph_u9p7[1]	45696
t_AsstFWVehSpd_Kph_u9p7[2]	45824
t_AsstFWVehSpd_Kph_u9p7[3]	45952
t_AsstFWVehSpd_Kph_u9p7[4]	46080
t_AsstFWVehSpd_Kph_u9p7[5]	46208
t_AsstFWVehSpd_Kph_u9p7[6]	46336
t_AsstFWVehSpd_Kph_u9p7[7]	46464
tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32.value	3.0999999
tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc.value	0
tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32.value	6.0999999
tgt_AssistFirewall_Per1_HwTorque_HwNm_f32.value	-2
tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32.value	-8.80000019
tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum.value	0
tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32.value	77.1999969
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_AsstFirewallActive_Uls_f32	tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32	tgt_AssistFirewall_Per1_BaseAssistCmd_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_CombinedAssist_MtrNm_f32	tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_l	tgt_AssistFirewall_Per1_Defeat_AsstTbl_Service_Cnt_lgc
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HighFreqAssist_MtrNm_f32	tgt_AssistFirewall_Per1_HighFreqAssist_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HwTorque_HwNm_f32	tgt_AssistFirewall_Per1_HwTorque_HwNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_HysteresisComp_MtrNm_f32	tgt_AssistFirewall_Per1_HysteresisComp_MtrNm_f32
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_MEC_Counter_Cnt_enum	tgt_AssistFirewall_Per1_MEC_Counter_Cnt_enum
tgt_Rte_Inst_Ap_AssistFirewall.AssistFirewall_Per1_VehicleSpeed_Kph_f32	tgt_AssistFirewall_Per1_VehicleSpeed_Kph_f32

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.SV_Uls_f32	3.92000008	3.92000008 ± 4.88E-04	✔
AssistFirewall_ActiveRawAcc_Cnt_M_u16	267	267 ± 1	✔
AssistFirewall_AsstReducedPerfSV_Cnt_M_lgc	1	1	✔
AssistFirewall_CombAsstSV_MtrNm_M_f32	-2.89990234	-2.89990234 ± 4.88E-04	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.SV_Uls_f32	3.01799989	3.01799989 ± 4.88E-04	✔
AssistFirewall_LwrBoundKSV_M_str.SV_Uls_f32	5.8829999	5.8829999 ± 4.88E-04	✔
AssistFirewall_PNCountStatus_Cnt_M_lgc	1	1	✔
AssistFirewall_UprBoundKSV_M_str.SV_Uls_f32	2.07999992	2.07999992 ± 4.88E-04	✔
tgt_AssistFirewall_Per1_AsstFirewallActive_Uls_f32.value	1	1 ± 3.05E-05	✔
tgt_AssistFirewall_Per1_CombinedAssist_MtrNm_f32.value	-2.89990234	-2.89990234 ± 9.77E-04	✔
NTC_Cnt_T_enum	0xC6	0xC6	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔
NTC_Cnt_T_enum	0xC9	0xC9	✔
Param_Cnt_T_u08	0x01	0x01	✔
Status_Cnt_T_enum	0x01	0x01	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP0_CheckpointReached	1	✔
BilinearXMYM_s16_s16XMs16YM_Cnt	2	BilinearXMYM_s16_s16XMs16YM_Cnt	2	✔
IntplVarXY_s16_u16Xs16Y_Cnt	1	IntplVarXY_s16_u16Xs16Y_Cnt	1	✔
Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	Rte_Call_Ap_AssistFirewall_NxtrDiagMgr_SetNTCStatus	2	✔
Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	Rte_Call_AssistFirewall_Per1_CP1_CheckpointReached	1	✔

TEST DETAILS REPORT

AssistFirewall_Init1

2015-03-23, 11:35:13+0530

Project	AssistFirewall
Module	AssistFireWall
Test Object	AssistFirewall_Init1

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

Statistics

Total Testcases	1
Successful	1
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\AssistFirewall
Configuration File	D:\Synergy_Work_Area\AssistFirewall\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	$(PROJECTROOT)\src\Ap_AssistFirewall.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -DBC_ASSISTFIREWALL_FAULTINJECTIONPOINT=STD_OFF -I$(PROJECTROOT)\utp\contract \Ap_AssistFirewall -I$(PROJECTROOT)\utp\contract -I$(PROJECTROOT)\NxtrLib\include -I$(PROJECTROOT)\StdDef\include -I$ (Compiler Install Path)\include
File	$(PROJECTROOT)\NxtrLib\src\interpolation.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -DBC_ASSISTFIREWALL_FAULTINJECTIONPOINT=STD_OFF -I$(PROJECTROOT)\utp\contract \Ap_AssistFirewall -I$(PROJECTROOT)\utp\contract -I$(PROJECTROOT)\NxtrLib\include -I$(PROJECTROOT)\StdDef\include -I$ (Compiler Install Path)\include

Comments/Description/Specification

Name	Text
Module 'AssistFireWall'	**********Unit Test Information********** Name of Tester:Ankita Bhardwaj Code File(s) Under Test:Ap_AssistFirewall.c Code File(s) Version:14 Module Design Document:Assist_Firewall_MDD.docx Module Design Document Version:14 Data Dictionary Version:16 Unit Test Plan Version:11 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.31 Total FLASH Used (Bytes):1568 Total RAM Used (Bytes):79 Total CALS Used (Bytes):480 Special Test Requirements: Test Date:03-23-2015 Comments:"NOTE:1) Inline functions defined in GlobalMacro.h are not Unit Tested. 2)""CBD_Sandbox_dbg.map""map file is embedded for reference. 3) In ""AssistFirewall_Per1"" function, ""Defeat_AsstTbl_Service_Cnt_lgc"" always kept FALSE to make ""if((DefeatAsstTblSvc_Cnt_T_lgc <> D_FALSE_CNT_LGC) And (MECCounter_Cnt_T_enum <> ProductionMode))"" condition FALSE except Boundray Test for variables used in Condition and Path coverage. " **********
Test Object 'AssistFirewall_Init1'	

Attributes

Name	Value
Compiler Install Path	$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd

Attributes

Name	Value
Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	$(ProgramFiles)\pls\UDE 3.2
Time Unit	Cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\AssistFirewall\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

Test Case 1: Boundary Test

Specification

```
Performance Metrics (With "None" Instrumentation
and WithPS Environment)
CPU Cycles:

TC1.1 1813.00 Cycles
TC1.2 1820.00 Cycles
TC1.3 1820.00 Cycles
TC1.4 1820.00 Cycles
TC1.5 1820.00 Cycles
TC1.6 1820.00 Cycles
TC1.7 1820.00 Cycles
TC1.8 1820.00 Cycles
```

Description

Vector Description

TS1.1k_AsstFWFiltKn_Hz_f32 = min
TS1.2k_AsstFWFiltKn_Hz_f32 = max
TS1.3k_AsstFWFiltKn_Hz_f32 = mid
TS1.4k_AsstFWFWActiveLPF_Hz_f32 = min
TS1.5k_AsstFWFWActiveLPF_Hz_f32 = max
TS1.6k_AsstFWFWActiveLPF_Hz_f32= mid
TS1.7All min
TS1.8All max

Test Step 1.1 (Repeat Count = 1)

Name	Input Value
k_AsstFWFWActiveLPF_Hz_f32	40.0999985
k_AsstFWFiltKn_Hz_f32	0.100000001

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.395837128	0.395837128 ± 1.53E-05	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	✔
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00062871	1.00062859 ± 6.10E-05	✔
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	✔
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	✔

Test Step 1.2 (Repeat Count = 1)

Name	Input Value
k_AsstFWFWActiveLPF_Hz_f32	50.2999992
k_AsstFWFiltKn_Hz_f32	100

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.46851933	0.46851933 ± 1.53E-05	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	✔
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	2.09537983	2.09537959 ± 6.10E-05	✔
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	✔
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	✔

Test Step 1.3 (Repeat Count = 1)

Name	Input Value
k_AsstFWFWActiveLPF_Hz_f32	60.4000015
k_AsstFWFiltKn_Hz_f32	50.2999992

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.531869829	0.531869769 ± 1.53E-05	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.46851933	0.46851933 ± 1.53E-05	✔
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.41246235	1.41246235 ± 6.10E-05	✔
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.46851933	0.46851933 ± 1.53E-05	✔
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.46851933	0.46851933 ± 1.53E-05	✔

Test Step 1.4 (Repeat Count = 1)

Name	Input Value
k_AsstFWFWActiveLPF_Hz_f32	0.100000001
k_AsstFWFiltKn_Hz_f32	10.1999998

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.12030232	0.120302327 ± 1.53E-05	✔
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.06748891	1.06748891 ± 6.10E-05	✔
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.12030232	0.120302327 ± 1.53E-05	✔
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.12030232	0.120302327 ± 1.53E-05	✔

Test Step 1.5 (Repeat Count = 1) ✔

Name	Input Value
k_AsstFWFWActiveLPF_Hz_f32	100
k_AsstFWFiltKn_Hz_f32	20.2999992

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.22515893	0.225158915 ± 1.53E-05	✔
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.14153636	1.14153647 ± 6.10E-05	✔
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.22515893	0.225158915 ± 1.53E-05	✔
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.22515893	0.225158915 ± 1.53E-05	✔

Test Step 1.6 (Repeat Count = 1) ✔

Name	Input Value
k_AsstFWFWActiveLPF_Hz_f32	50.2999992
k_AsstFWFiltKn_Hz_f32	30.1000004

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.46851933	0.46851933 ± 1.53E-05	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.31493926	0.31493926 ± 1.53E-05	✔
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.22104383	1.22104394 ± 6.10E-05	✔
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.31493926	0.31493926 ± 1.53E-05	✔
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.31493926	0.31493926 ± 1.53E-05	✔

Test Step 1.7 (Repeat Count = 1) ✔

Name	Input Value
k_AsstFWFWActiveLPF_Hz_f32	0.100000001
k_AsstFWFiltKn_Hz_f32	0.100000001

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	✔
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	1.00062871	1.00062859 ± 6.10E-05	✔
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	✔
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.00125586987	0.00125584798 ± 1.53E-05	✔

Test Step 1.8 (Repeat Count = 1) ✔

Name	Input Value
k_AsstFWFWActiveLPF_Hz_f32	100
k_AsstFWFiltKn_Hz_f32	100

Name	Actual Value	Expected Value	Result
AssistFirewall_ActiveKSV_M_str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	✔
AssistFirewall_HiFreqKSV_M_str.LPF_Str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	✔
AssistFirewall_HiFreqKSV_M_str.CF_Uls_f32	2.09537983	2.09537959 ± 6.10E-05	✔
AssistFirewall_LwrBoundKSV_M_str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	✔
AssistFirewall_UprBoundKSV_M_str.K_Uls_f32	0.715390444	0.715390444 ± 1.53E-05	✔