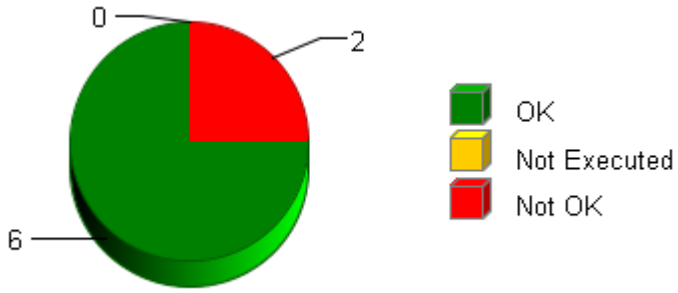
Summary

Total Test Objects:	8
Successful:	6
Failed:	2
Not Executed:	0
Date:	2014-10-14
Time:	23:47:43+0530

Overall Test Object Results (including Coverage)



Selected Project Items

Test Collection "CBD_UnitTest"

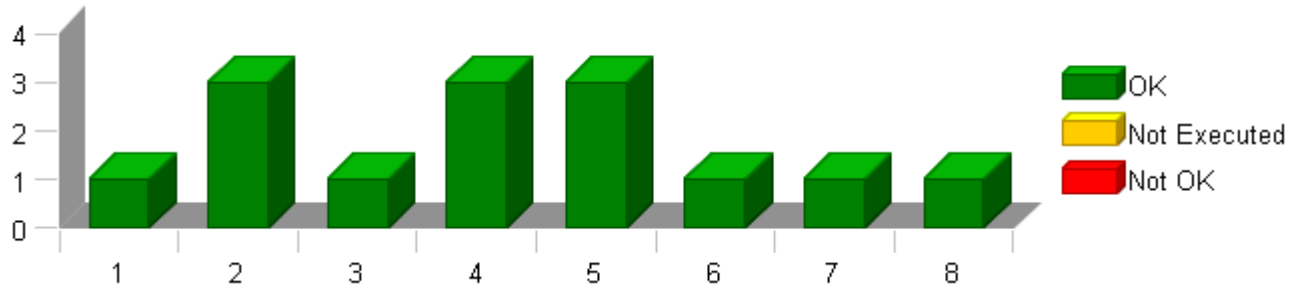
Used Test Environments

TI TMS 570 PLS UDE (Default)

Batch Operation Settings

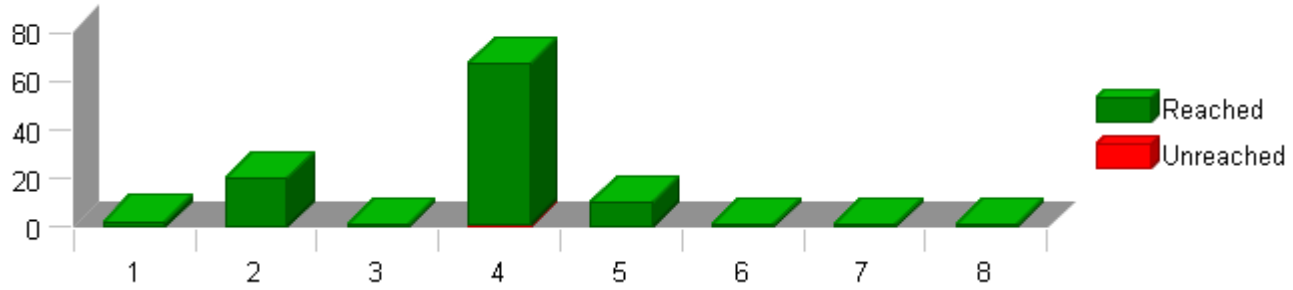
Check Interface:	No
Generate Driver:	Yes
Execute Test:	Yes
Create New Test Run:	No
Instrumentation:	Test Object Only
Coverage:	Statement Coverage, Branch Coverage, Modified Condition / Decision Coverage, Multiple Condition Coverage

Test Case Results for Each Test Object (without Coverage)



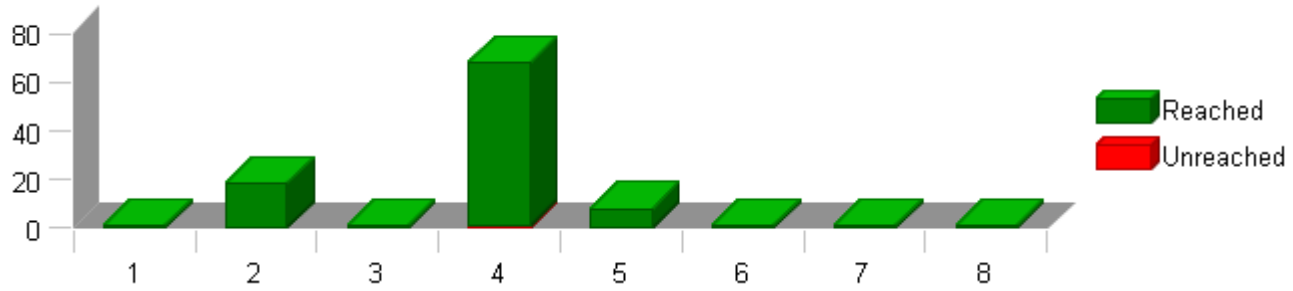
The table above shows each test object on the x axis and the number of test cases of the respective test object on the y axis. Each bar is divided into passed, not executed and failed test cases. The test case results do not take into account any coverage result (i.e. if all test cases of a test object are passed in this table but the coverage is failed, the overall test object result will be failed).

Statement (C0) Coverage: Total Statements for Each Test Object



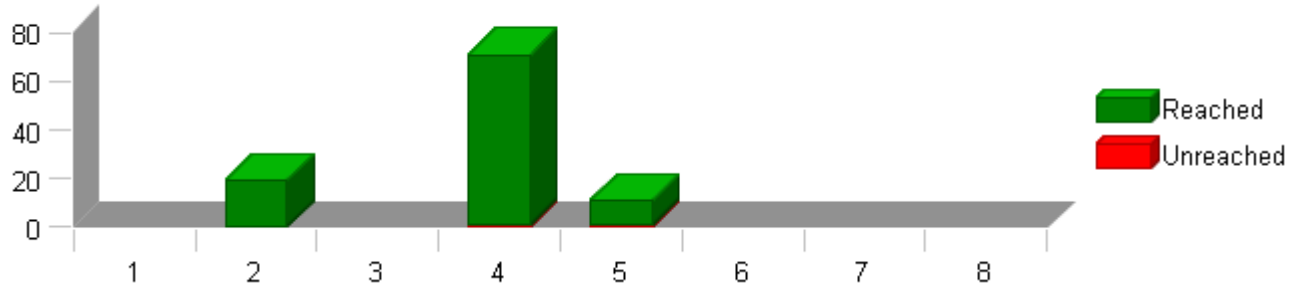
The table above shows each test object on the x axis and the number of statements of the respective test object on the y axis. Each bar is divided into reached statements (i.e. statements that have been executed during the test) and unreached statements.

Branch (C1) Coverage: Total Branches for Each Test Object



The table above shows each test object on the x axis and the number of branches of the respective test object on the y axis. Each bar is divided into reached branches (i.e. branches that have been executed during the test) and unreached branches.

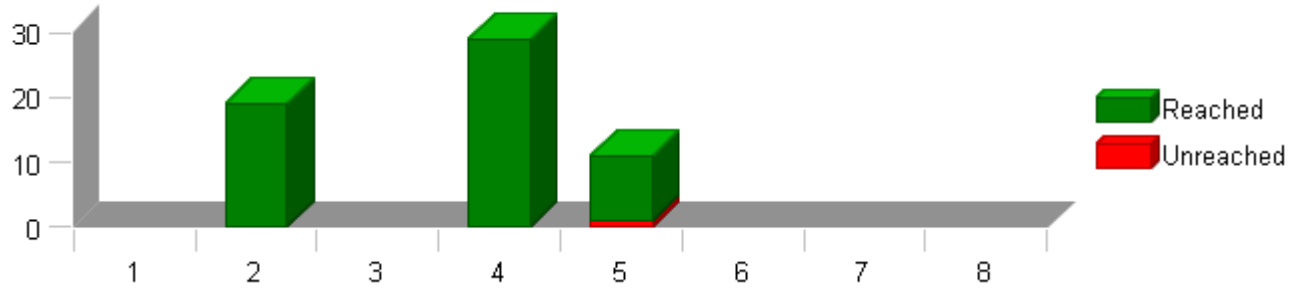
MC/DC Coverage: Total Condition Combinations for Each Test Object



The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MC/DC coverage, each decision requires all contained atomic conditions to evaluate to both true and false independently of all other conditions. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.

MCC Coverage: Total Condition Combinations for Each Test Object



The table above shows test objects on the x axis and the number of condition combinations of all decisions of the respective test object on the y axis. The number of condition combinations is based on the number of boolean conditions within each decision of the test object. To achieve full MCC coverage, each decision requires all contained atomic conditions to evaluate to all possible combinations of true and false values. The cumulated number of rows within such tables of condition combinations is what is displayed in this table.

Each bar is divided into reached condition combinations (i.e. combinations of boolean condition values that have been executed during the test) and unreached condition combinations.

Test Object List

The following table lists all test objects with their test case and coverage results. The cumulated results for modules, folders and test collections are also displayed, the indentation within the name column indicates the parent relationship of the elements.

Please note that only test objects are numbered within the first column. This number is referenced on the x axis within the overview charts for test case and coverage results available on previous pages (if included into the report).

No.	Name	C0	C1	MC/DC	MCC	Test Cases	Result
	DigColPsInt	99.02 %	98.98 %	98.01 %	98.3 %	14 of 14 passed	✗
	CBD_UnitTest	99.02 %	98.98 %	98.01 %	98.3 %	14 of 14 passed	✗
	DigColPsInt	99.02 %	98.98 %	98.01 %	98.3 %	14 of 14 passed	✗
1	DigColPsInt_GetCustData	100 %	100 %	-	-	1 of 1 passed	✓
2	DigColPsInt_GetData	100 %	100 %	100 %	100 %	3 of 3 passed	✓
3	DigColPsInt_Init	100 %	100 %	-	-	1 of 1 passed	✓
4	DigColPsInt_InterruptNotification	98.5 %	98.52 %	98.59 %	100 %	3 of 3 passed	✗
5	DigColPsInt_StartRequest	100 %	100 %	90.9 %	90.9 %	3 of 3 passed	✗
6	SetupRead	100 %	100 %	-	-	1 of 1 passed	✓
7	SetupWriteData	100 %	100 %	-	-	1 of 1 passed	✓
8	SetupWriteRegister	100 %	100 %	-	-	1 of 1 passed	✓

TEST DETAILS REPORT

DigColPsInt_GetData

2014-10-14, 23:35:27+0530

Project	DigColPsInt
Module	DigColPsInt
Test Object	DigColPsInt_GetData

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %
MCC Coverage	100 %
MC/DC Coverage	100 %

Statistics

Total Testcases	3
Successful	3
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\C1xx_DigColPs
Configuration File	D:\Synergy_Work_Area\C1xx_DigColPs\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	$(PROJECTROOT)\DigColPs\src\Sa_DigColPsInt.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -DSTATIC= -D__inline= -I$(PROJECTROOT)\DigColPs\utp\contract -I$(PROJECTROOT)\DigColPs\utp\contract\Sa_DigColPs -I$(PROJECTROOT)\DigColPs\include -I$(PROJECTROOT)\NxtrLib\include -I$(PROJECTROOT)\StdDef\include -I$(PROJECTROOT)\StdDef\include\TMS570_HerculesRegs -I$(Compiler Install Path)\include

Comments/Description/Specification	
Name	**Text**

Module 'DigColPsInt'	**********Unit Test Descrption********** Name of Tester:Priti Mangalekar Code File(s) Under Test:Sa_DigColPsInt.c Code File(s) Version:7 Module Design Document:DigColPsInt_MDD.docx Module Design Document Version:8 Data Dictionary Version:9 Unit Test Plan Version:2 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.30 Total FLASH Used (Bytes):N/A Total RAM Used (Bytes):N/A Total CALS Used (Bytes):N/A Special Test Requirements: Test Date:10/13/2014 Comments: NOTE 1: In """"DigColPsInt_StartRequest"""" function, path """"(Type_Cnt_T_u08 > D_NONE_CNT_U08) = TRUE && (Type_Cnt_T_u08 <= D_STATUSREG_CNT_U08) = FALSE"""" cannot be covered because range of """"Type_Cnt_T_u08"""" is '0-5' and value of """"D_STATUSREG_CNT_U08"""" is '34'. NOTE2: In function ""DigColPsInt_GetData"",""DigColPsInt_StartRequest"" and ""DigColPsInt_InterruptNotification"" values for """"I2c_Send(Length_Cnt_T_u32)"""", """"I2c_SetRecv(Length_Cnt_T_u32)"""", """"I2c_SetStatus(Status_Cnt_T_u16)"""", """"I2c_SetupMasterReceive(DataLength_Cnt_T_u16)"""" and I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) are ignored in few vectors as they are taking garbage value when they are not updated with expected value in particular vector. NOTE3: The return value of """"DigColPsInt_GetData"""" function is going out of range, anomaly """"6156"""" is raised for the same. NOTE4:Range of DigColPsInt_CurrentStepNo_Cnt_M_enum is considered as 0 to 36, as enum DigColPsInt_CurrentStepNo_Cnt_M_enum is of type CommStepType which is of 37 elements. NOTE5:In function ""DigColPsInt_InterruptNotification"", path ""Case I2C_RECV_OVERRUN: True"" cannot be covered because range of ""Flags_Cnt_T_b16"" is 0 to 64 given in MDD. NOTE6:In function ""DigColPsInt_InterruptNotification"", output variable ""DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08"" is going out of range." **********

Attributes

Name	Value
Compiler Install Path	$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	$(Compiler Install Path)\include
Time Unit	Cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\C1xx_DigColPs\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

Test Case 1: Metrics Test

Description Test Vector Description:

TS1.1"Shortest Execution Path:
(DigColPsInt_SensInitialized_Cnt_M_lgc == FALSE)=True
(ElapsedTime_mS_T_u16 >= (uint16)D_SENSINITDELAY_MS_U08)=False
(DigColPsInt_NackOccured_Cnt_M_lgc == TRUE)=False
(DigColPsInt_RecvOverrunError_Cnt_M_lgc == TRUE)=False
(DigColPsInt_BusBusySeqError_Cnt_M_lgc == TRUE)=False
(DigColPsInt_CmdFailOccurred_Cnt_M_lgc == TRUE)=False
((DigColPsInt_TransactionCnt_Cnt_M_u08 == DigColPsInt_PrevTransactionCnt_Cnt_M_u08) && (DigColPsInt_RecvdDataType_Cnt_M_u08 != D_NONE_CNT_U08))=False"
TS1.2"Longest Execution Path:
(DigColPsInt_SensInitialized_Cnt_M_lgc == FALSE)=False
(DigColPsInt_CurrentStepNo_Cnt_M_enum < INIT_COMPLETE)=True
(ElapsedTime_mS_T_u16 > (uint16)(k_I2CHWInitTransactionTime_Sec_f32*D_SECTOMILLSEC_CNT_F32))=True
(DigColPsInt_NackOccured_Cnt_M_lgc == TRUE)=True
(DigColPsInt_RecvOverrunError_Cnt_M_lgc == TRUE)=True
(DigColPsInt_BusBusySeqError_Cnt_M_lgc == TRUE)=True
(DigColPsInt_CmdFailOccurred_Cnt_M_lgc == TRUE)=True
((DigColPsInt_TransactionCnt_Cnt_M_u08 == DigColPsInt_PrevTransactionCnt_Cnt_M_u08) && (DigColPsInt_RecvdDataType_Cnt_M_u08 != D_NONE_CNT_U08))=True"

Test Step 1.1 (Repeat Count = 1)

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	0
DigColPsInt_Buffer_Cnt_M_u08[1]	0
DigColPsInt_Buffer_Cnt_M_u08[2]	0
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	0
DigColPsInt_CurrentSlave_Cnt_M_u08	0
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_NOT_INITIALIZED
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	0
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	0
DigColPsInt_TransactionCnt_Cnt_M_u08	0
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	0
k_I2CHWInitTransactionTime_Sec_f32	0
target_DtrmnElapsedTime_mS_u16_ElapsedTime	0
target_GetSystemTime_mS_u32_CurrentTime	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0

TEST DETAILS REPORT

DigColPsInt_GetData

2014-10-14, 23:35:27+0530

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	0
target_i2cREG1_temp.IMR	0
target_i2cREG1_temp.STR	0
target_i2cREG1_temp.CLKL	0
target_i2cREG1_temp.CLKH	0
target_i2cREG1_temp.CNT	0
target_i2cREG1_temp.DRR	0
target_i2cREG1_temp.SAR	0
target_i2cREG1_temp.DXR	0
target_i2cREG1_temp.MDR	0
target_i2cREG1_temp.IVR	0
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	0
target_i2cREG1_temp.PID11	0
target_i2cREG1_temp.PID12	0
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	0
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	0	0	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	0	0	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	0	0	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	0	0	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_NOT_INITIALIZED	INIT_NOT_INITIALIZED	✔
DigColPsInt_GetData()	0	0	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	0	0	✔
I2c_Send(Length_Cnt_T_u32)	0	0	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	0	0	✔
target_ColSnsrDataPtr_Cnt_T_u16	0	0	✔
target_DataTypePtr_Cnt_T_u08	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	0	0	✔

Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_SpurSnsrDataPtr_Cnt_T_u16	0	0	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔

Test Step 1.2 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	255
DigColPsInt_Buffer_Cnt_M_u08[1]	255
DigColPsInt_Buffer_Cnt_M_u08[2]	255
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	65535
DigColPsInt_CurrentSlave_Cnt_M_u08	127
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADDATREG_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	4294967295
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	255
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1

Name	Input Value
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	65535
DigColPsInt_TransactionCnt_Cnt_M_u08	255
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	127
k_I2CHWInitTransactionTime_Sec_f32	10
target_DtrmnElapsedTime_mS_u16_ElapsedTime	65535
target_GetSystemTime_mS_u32_CurrentTime	4294967295
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	32767
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	1023
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	4095
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	1023
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	32767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	1023
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	4095
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	1023
target_i2cREG1_temp.IMR	255
target_i2cREG1_temp.STR	32767
target_i2cREG1_temp.CLKL	65535
target_i2cREG1_temp.CLKH	65535
target_i2cREG1_temp.CNT	65535
target_i2cREG1_temp.DRR	255
target_i2cREG1_temp.SAR	1023
target_i2cREG1_temp.DXR	255

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Input Value
target_i2cREG1_temp.MDR	65535
target_i2cREG1_temp.IVR	4095
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	255
target_i2cREG1_temp.PID11	65535
target_i2cREG1_temp.PID12	255
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	3
target_i2cREG1_temp.DIN	3
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	3
target_i2cREG1_temp.ODR	3
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	255	255	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	255	255	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	255	255	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADDATREG_READ	INIT_SENSOR2_EXTREADDATREG_READ	✔
DigColPsInt_GetData()	190	190	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	255	255	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
I2c_Send(Length_Cnt_T_u32)	0	0	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	0	0	✔
target_ColSnsrDataPtr_Cnt_T_u16	65535	65535	✔
target_DataTypePtr_Cnt_T_u08	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023	1023	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	255	255	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	32767	32767	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	65535	65535	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	255	255	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	1023	1023	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	255	255	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	65535	65535	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	4095	4095	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	255	255	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	65535	65535	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	255	255	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	1023	1023	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	255	255	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	32767	32767	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	65535	65535	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	255	255	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	1023	1023	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	255	255	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	65535	65535	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	4095	4095	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	255	255	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	65535	65535	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	255	255	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_SpurSnsrDataPtr_Cnt_T_u16	65535	65535	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔

Test Case 2: Boundary Test ✔

Description Test Vector Description:

TS2.1DigColPsInt_NackOccured_Cnt_M_lgc=min
TS2.2DigColPsInt_NackOccured_Cnt_M_lgc=max
TS2.3DigColPsInt_BusBusySeqError_Cnt_M_lgc=min
TS2.4DigColPsInt_BusBusySeqError_Cnt_M_lgc=max
TS2.5DigColPsInt_TransactionCnt_Cnt_M_u08=min
TS2.6DigColPsInt_TransactionCnt_Cnt_M_u08=max
TS2.7DigColPsInt_TransactionCnt_Cnt_M_u08=mid
TS2.8DigColPsInt_PrevTransactionCnt_Cnt_M_u08=min
TS2.9DigColPsInt_PrevTransactionCnt_Cnt_M_u08=max
TS2.10DigColPsInt_PrevTransactionCnt_Cnt_M_u08=mid
TS2.11DigColPsInt_ColSnsrData_Cnt_M_u16=min
TS2.12DigColPsInt_ColSnsrData_Cnt_M_u16=max
TS2.13DigColPsInt_ColSnsrData_Cnt_M_u16=mid
TS2.14DigColPsInt_SpurSnsrData_Cnt_M_u16=min
TS2.15DigColPsInt_SpurSnsrData_Cnt_M_u16=max
TS2.16DigColPsInt_SpurSnsrData_Cnt_M_u16=mid
TS2.17DigColPsInt_RecvdDataType_Cnt_M_u08=min
TS2.18DigColPsInt_RecvdDataType_Cnt_M_u08=max
TS2.19DigColPsInt_RecvdDataType_Cnt_M_u08=mid
TS2.20DigColPsInt_SensInitialized_Cnt_M_lgc=min
TS2.21DigColPsInt_SensInitialized_Cnt_M_lgc=max
TS2.22DigColPsInt_CurrentStepNo_Cnt_M_enum=min
TS2.23DigColPsInt_CurrentStepNo_Cnt_M_enum=max
TS2.24DigColPsInt_CurrentStepNo_Cnt_M_enum=pos
TS2.25k_I2CHWInitTransactionTime_Sec_f32=min
TS2.26k_I2CHWInitTransactionTime_Sec_f32=max
TS2.27k_I2CHWInitTransactionTime_Sec_f32=pos
TS2.28DigColPsInt_RecvOverrunError_Cnt_M_lgc=min
TS2.29DigColPsInt_RecvOverrunError_Cnt_M_lgc=max
TS2.30DigColPsInt_CmdFailOccurred_Cnt_M_lgc=min
TS2.31DigColPsInt_CmdFailOccurred_Cnt_M_lgc=max
TS2.32DtrmnElapsedTime_mS_u16=min
TS2.33DtrmnElapsedTime_mS_u16=max
TS2.34DtrmnElapsedTime_mS_u16=pos
TS2.35k_ColSensorI2CAddress_Cnt_u08=min
TS2.36k_ColSensorI2CAddress_Cnt_u08=max
TS2.37k_ColSensorI2CAddress_Cnt_u08=pos
TS2.38GetSystemTime_mS_u32=min
TS2.39GetSystemTime_mS_u32=max
TS2.40GetSystemTime_mS_u32=pos
TS2.41All Min
TS2.42All Max

Test Step 2.1 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	5600
DigColPsInt_CurrentSlave_Cnt_M_u08	14
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	5486797
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	19

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Input Value
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	9687
DigColPsInt_TransactionCnt_Cnt_M_u08	12
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	119
k_I2CHWInitTransactionTime_Sec_f32	1.10000002
target_DtrmnElapsedTime_mS_u16_ElapsedTime	1247
target_GetSystemTime_mS_u32_CurrentTime	1475789
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Input Value
target_i2cREG1_temp.DXR	78
target_i2cREG1_temp.MDR	495
target_i2cREG1_temp.IVR	66
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	78
target_i2cREG1_temp.PID11	56
target_i2cREG1_temp.PID12	78
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	119	119	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	✔
DigColPsInt_GetData()	40	40	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	12	12	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	5600	5600	✔
target_DataTypePtr_Cnt_T_u08	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	✔

TEST DETAILS REPORT

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_SpurSnsrDataPtr_Cnt_T_u16	9687	9687	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	✔

Test Step 2.2 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	40
DigColPsInt_Buffer_Cnt_M_u08[1]	50
DigColPsInt_Buffer_Cnt_M_u08[2]	60
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	7985
DigColPsInt_CurrentSlave_Cnt_M_u08	21
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	6489549
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	31
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	11230
DigColPsInt_TransactionCnt_Cnt_M_u08	29
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	126
k_I2CHWInitTransactionTime_Sec_f32	1.5
target_DtrmnElapsedTime_mS_u16_ElapsedTime	7841
target_GetSystemTime_mS_u32_CurrentTime	2478541
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2

TEST DETAILS REPORT

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Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.MDR	566
target_i2cREG1_temp.IVR	554
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	44
target_i2cREG1_temp.PID11	4466
target_i2cREG1_temp.PID12	44
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	0
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	40	40	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	50	50	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	60	60	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	21	21	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_READ	INIT_SENSOR1_READEXTERR_READ	✔
DigColPsInt_GetData()	134	134	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	29	29	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	7985	7985	✔
target_DataTypePtr_Cnt_T_u08	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	✔

TEST DETAILS REPORT

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_SpurSnsrDataPtr_Cnt_T_u16	11230	11230	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔

Test Step 2.3 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	70
DigColPsInt_Buffer_Cnt_M_u08[1]	80
DigColPsInt_Buffer_Cnt_M_u08[2]	90
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	10370
DigColPsInt_CurrentSlave_Cnt_M_u08	28
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	7492301
DigColPsInt_NackOccured_Cnt_M_lgc	0

Name	Input Value
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	43
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	12773
DigColPsInt_TransactionCnt_Cnt_M_u08	33
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	17
k_I2CHWInitTransactionTime_Sec_f32	1.89999998
target_DtrmnElapsedTime_mS_u16_ElapsedTime	14435
target_GetSystemTime_mS_u32_CurrentTime	3481293
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	65
target_i2cREG1_temp.IMR	89
target_i2cREG1_temp.STR	67
target_i2cREG1_temp.CLKL	7
target_i2cREG1_temp.CLKH	577
target_i2cREG1_temp.CNT	88
target_i2cREG1_temp.DRR	23

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Name	Input Value
target_i2cREG1_temp.SAR	65
target_i2cREG1_temp.DXR	89
target_i2cREG1_temp.MDR	7
target_i2cREG1_temp.IVR	44
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	89
target_i2cREG1_temp.PID11	577
target_i2cREG1_temp.PID12	89
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	2
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	70	70	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	80	80	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	90	90	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	28	28	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ	INIT_SENSOR1_CHECKSTAT_READ	✔
DigColPsInt_GetData()	168	168	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	33	33	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	10370	10370	✔
target_DataTypePtr_Cnt_T_u08	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_SpurSnsrDataPtr_Cnt_T_u16	12773	12773	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔

Test Step 2.4 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	3
DigColPsInt_Buffer_Cnt_M_u08[1]	6
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	12755
DigColPsInt_CurrentSlave_Cnt_M_u08	35
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	8495053
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	55
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	14316
DigColPsInt_TransactionCnt_Cnt_M_u08	46
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	24
k_I2CHWInitTransactionTime_Sec_f32	2.29999995
target_DtrmnElapsedTime_mS_u16_ElapsedTime	21029
target_GetSystemTime_mS_u32_CurrentTime	4484045
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1

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Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1
target_i2cREG1_temp.OAR	10
target_i2cREG1_temp.IMR	10
target_i2cREG1_temp.STR	1223
target_i2cREG1_temp.CLKL	7846
target_i2cREG1_temp.CLKH	8974
target_i2cREG1_temp.CNT	98
target_i2cREG1_temp.DRR	12
target_i2cREG1_temp.SAR	10
target_i2cREG1_temp.DXR	10
target_i2cREG1_temp.MDR	7846
target_i2cREG1_temp.IVR	55
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	10
target_i2cREG1_temp.PID11	8974
target_i2cREG1_temp.PID12	10
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	1
target_i2cREG1_temp.PSL	1

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	6	6	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	9	9	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	24	24	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	✔
DigColPsInt_GetData()	6	6	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	46	46	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	12755	12755	✔
target_DataTypePtr_Cnt_T_u08	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_SpurSnsrDataPtr_Cnt_T_u16	14316	14316	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	✔

Test Step 2.5 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	11
DigColPsInt_Buffer_Cnt_M_u08[1]	22
DigColPsInt_Buffer_Cnt_M_u08[2]	33
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	15140
DigColPsInt_CurrentSlave_Cnt_M_u08	42
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READEXTERR_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	9497805

Name	Input Value
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	67
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	15859
DigColPsInt_TransactionCnt_Cnt_M_u08	0
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	31
k_I2CHWInitTransactionTime_Sec_f32	2.70000005
target_DtrmnElapsedTime_mS_u16_ElapsedTime	27623
target_GetSystemTime_mS_u32_CurrentTime	5486797
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2
target_i2cREG1_temp.OAR	34
target_i2cREG1_temp.IMR	24
target_i2cREG1_temp.STR	455
target_i2cREG1_temp.CLKL	847
target_i2cREG1_temp.CLKH	987
target_i2cREG1_temp.CNT	487

TEST DETAILS REPORT

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Name	Input Value
target_i2cREG1_temp.DRR	34
target_i2cREG1_temp.SAR	34
target_i2cREG1_temp.DXR	24
target_i2cREG1_temp.MDR	847
target_i2cREG1_temp.IVR	56
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	24
target_i2cREG1_temp.PID11	987
target_i2cREG1_temp.PID12	24
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	3
target_i2cREG1_temp.DIN	3
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	2
target_i2cREG1_temp.CLR	3
target_i2cREG1_temp.ODR	3
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	2

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	11	11	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	22	22	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	33	33	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	42	42	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READEXTERR_READ	INIT_SENSOR2_READEXTERR_READ	✔
DigColPsInt_GetData()	168	168	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	15140	15140	✔
target_DataTypePtr_Cnt_T_u08	4	4	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987	987	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_SpurSnsrDataPtr_Cnt_T_u16	15859	15859	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔

Test Step 2.6 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	44
DigColPsInt_Buffer_Cnt_M_u08[1]	55
DigColPsInt_Buffer_Cnt_M_u08[2]	66
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	17525
DigColPsInt_CurrentSlave_Cnt_M_u08	49
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	10500557
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	79
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	17402
DigColPsInt_TransactionCnt_Cnt_M_u08	255
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	38
k_I2CHWInitTransactionTime_Sec_f32	3.0999999
target_DtrmnElapsedTime_mS_u16_ElapsedTime	34217
target_GetSystemTime_mS_u32_CurrentTime	6489549
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1

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Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	55	55	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	66	66	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	38	38	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	✔
DigColPsInt_GetData()	6	6	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	255	255	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	17525	17525	✔
target_DataTypePtr_Cnt_T_u08	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔

Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_SpurSnsrDataPtr_Cnt_T_u16	17402	17402	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	✔

Test Step 2.7 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	66
DigColPsInt_Buffer_Cnt_M_u08[1]	77
DigColPsInt_Buffer_Cnt_M_u08[2]	88
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	19910
DigColPsInt_CurrentSlave_Cnt_M_u08	56
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0

Name	Input Value
DigColPsInt_InitialTime_mS_M_u32	11503309
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	91
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	18945
DigColPsInt_TransactionCnt_Cnt_M_u08	120
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	45
k_I2CHWInitTransactionTime_Sec_f32	3.5
target_DtrmnElapsedTime_mS_u16_ElapsedTime	40811
target_GetSystemTime_mS_u32_CurrentTime	7492301
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	78
target_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56

TEST DETAILS REPORT

DigColPsInt_GetData

2014-10-14, 23:35:27+0530

Name	Input Value
target_i2cREG1_temp.CNT	897
target_i2cREG1_temp.DRR	98
target_i2cREG1_temp.SAR	66
target_i2cREG1_temp.DXR	78
target_i2cREG1_temp.MDR	495
target_i2cREG1_temp.IVR	66
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	78
target_i2cREG1_temp.PID11	56
target_i2cREG1_temp.PID12	78
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	66	66	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	77	77	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	88	88	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	56	56	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ	INIT_SENSOR1_READERROR_READ	✔
DigColPsInt_GetData()	168	168	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	120	120	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	19910	19910	✔
target_DataTypePtr_Cnt_T_u08	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_SpurSnsrDataPtr_Cnt_T_u16	18945	18945	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔

Test Step 2.8 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	40
DigColPsInt_Buffer_Cnt_M_u08[1]	50
DigColPsInt_Buffer_Cnt_M_u08[2]	60
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	22295
DigColPsInt_CurrentSlave_Cnt_M_u08	63
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	12506061
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	0
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	20488
DigColPsInt_TransactionCnt_Cnt_M_u08	51
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	52
k_I2CHWInitTransactionTime_Sec_f32	3.9000001
target_DtrmnElapsedTime_mS_u16_ElapsedTime	47405
target_GetSystemTime_mS_u32_CurrentTime	8495053
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1

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DigColPsInt_GetData

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Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.MDR	566
target_i2cREG1_temp.IVR	554
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	44
target_i2cREG1_temp.PID11	4466
target_i2cREG1_temp.PID12	44
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	0
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	50	50	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	60	60	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	52	52	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	✔
DigColPsInt_GetData()	6	6	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	51	51	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	22295	22295	✔
target_DataTypePtr_Cnt_T_u08	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	✔

Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_SpurSnsrDataPtr_Cnt_T_u16	20488	20488	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	✔

Test Step 2.9 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	70
DigColPsInt_Buffer_Cnt_M_u08[1]	80
DigColPsInt_Buffer_Cnt_M_u08[2]	90
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	24680
DigColPsInt_CurrentSlave_Cnt_M_u08	70
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_SETREG

Name	Input Value
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	13508813
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	255
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	22031
DigColPsInt_TransactionCnt_Cnt_M_u08	65
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	59
k_I2CHWInitTransactionTime_Sec_f32	4.30000019
target_DtrmnElapsedTime_mS_u16_ElapsedTime	53999
target_GetSystemTime_mS_u32_CurrentTime	9497805
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	65
target_i2cREG1_temp.IMR	89
target_i2cREG1_temp.STR	67
target_i2cREG1_temp.CLKL	7

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DigColPsInt_GetData

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Name	Input Value
target_i2cREG1_temp.CLKH	577
target_i2cREG1_temp.CNT	88
target_i2cREG1_temp.DRR	23
target_i2cREG1_temp.SAR	65
target_i2cREG1_temp.DXR	89
target_i2cREG1_temp.MDR	7
target_i2cREG1_temp.IVR	44
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	89
target_i2cREG1_temp.PID11	577
target_i2cREG1_temp.PID12	89
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	2
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	70	70	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	80	80	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	90	90	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	70	70	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_SETREG	INIT_SENSOR1_READEXTERR_SETREG	✔
DigColPsInt_GetData()	168	168	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	65	65	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	24680	24680	✔
target_DataTypePtr_Cnt_T_u08	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_SpurSnsrDataPtr_Cnt_T_u16	22031	22031	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔

Test Step 2.10 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	3
DigColPsInt_Buffer_Cnt_M_u08[1]	6
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	27065
DigColPsInt_CurrentSlave_Cnt_M_u08	77
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_SETREG
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	14511565
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	130
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	23574
DigColPsInt_TransactionCnt_Cnt_M_u08	79
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	66
k_I2CHWInitTransactionTime_Sec_f32	4.69999981
target_DtrmnElapsedTime_mS_u16_ElapsedTime	741
target_GetSystemTime_mS_u32_CurrentTime	10500557
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2
target_i2cREG1_temp.OAR	54
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	8
target_i2cREG1_temp.CLKL	554
target_i2cREG1_temp.CLKH	344
target_i2cREG1_temp.CNT	123
target_i2cREG1_temp.DRR	45
target_i2cREG1_temp.SAR	54
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	554
target_i2cREG1_temp.IVR	788
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	344
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	3
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	3
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	1
target_i2cREG1_temp.PSL	2

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	3	3	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	6	6	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	9	9	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	77	77	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_SETREG	INIT_SENSOR2_READERROR_SETREG	✔
DigColPsInt_GetData()	6	6	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	79	79	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	27065	27065	✔
target_DataTypePtr_Cnt_T_u08	4	4	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8	8	✔

Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_SpurSnsrDataPtr_Cnt_T_u16	23574	23574	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔

Test Step 2.11 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	11
DigColPsInt_Buffer_Cnt_M_u08[1]	22
DigColPsInt_Buffer_Cnt_M_u08[2]	33
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	0
DigColPsInt_CurrentSlave_Cnt_M_u08	84
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	15514317
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	93
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1

Name	Input Value
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	25117
DigColPsInt_TransactionCnt_Cnt_M_u08	93
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	73
k_I2CHWInitTransactionTime_Sec_f32	5.0999999
target_DtrmnElapsedTime_mS_u16_ElapsedTime	1248
target_GetSystemTime_mS_u32_CurrentTime	11503309
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	3
target_i2cREG1_temp.IMR	100
target_i2cREG1_temp.STR	7788
target_i2cREG1_temp.CLKL	2767
target_i2cREG1_temp.CLKH	556
target_i2cREG1_temp.CNT	564
target_i2cREG1_temp.DRR	88
target_i2cREG1_temp.SAR	3
target_i2cREG1_temp.DXR	100

TEST DETAILS REPORT

DigColPsInt_GetData

2014-10-14, 23:35:27+0530

Name	Input Value
target_i2cREG1_temp.MDR	2767
target_i2cREG1_temp.IVR	9
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	100
target_i2cREG1_temp.PID11	556
target_i2cREG1_temp.PID12	100
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	3
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	3
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	22	22	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	33	33	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	73	73	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	✔
DigColPsInt_GetData()	40	40	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	93	93	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	0	0	✔
target_DataTypePtr_Cnt_T_u08	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	100	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_SpurSnsrDataPtr_Cnt_T_u16	25117	25117	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	✔

Test Step 2.12 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	44
DigColPsInt_Buffer_Cnt_M_u08[1]	55
DigColPsInt_Buffer_Cnt_M_u08[2]	66
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	65535
DigColPsInt_CurrentSlave_Cnt_M_u08	91
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READEXTERR_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	16517069
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	113
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	26660
DigColPsInt_TransactionCnt_Cnt_M_u08	107
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	80
k_I2CHWInitTransactionTime_Sec_f32	5.5
target_DtrmnElapsedTime_mS_u16_ElapsedTime	1755
target_GetSystemTime_mS_u32_CurrentTime	12506061
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	678
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	6788
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	7878
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	678
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	778
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	6788
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	678
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	6788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	7878
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	678
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	778
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	6788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1
target_i2cREG1_temp.OAR	678
target_i2cREG1_temp.IMR	45
target_i2cREG1_temp.STR	66
target_i2cREG1_temp.CLKL	56
target_i2cREG1_temp.CLKH	6788
target_i2cREG1_temp.CNT	7878
target_i2cREG1_temp.DRR	12
target_i2cREG1_temp.SAR	678
target_i2cREG1_temp.DXR	45
target_i2cREG1_temp.MDR	56
target_i2cREG1_temp.IVR	778
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	45
target_i2cREG1_temp.PID11	6788
target_i2cREG1_temp.PID12	45
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	1

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	44	44	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	55	55	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	66	66	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	91	91	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READEXTERR_READ	INIT_SENSOR2_READEXTERR_READ	✔
DigColPsInt_GetData()	6	6	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	107	107	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	65535	65535	✔
target_DataTypePtr_Cnt_T_u08	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	678	678	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	45	45	✔

Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	7878	7878	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	678	678	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	45	45	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	778	778	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	45	45	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	6788	6788	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	45	45	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	678	678	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	45	45	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	7878	7878	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	678	678	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	45	45	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	778	778	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	45	45	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	6788	6788	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	45	45	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_SpurSnsrDataPtr_Cnt_T_u16	26660	26660	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔

Test Step 2.13 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	20000
DigColPsInt_CurrentSlave_Cnt_M_u08	98
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_SETREG
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	17519821
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	131

Name	Input Value
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	28203
DigColPsInt_TransactionCnt_Cnt_M_u08	121
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	87
k_I2CHWInitTransactionTime_Sec_f32	5.9000001
target_DtrmnElapsedTime_mS_u16_ElapsedTime	2262
target_GetSystemTime_mS_u32_CurrentTime	13508813
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	78
target_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56
target_i2cREG1_temp.CNT	897
target_i2cREG1_temp.DRR	98
target_i2cREG1_temp.SAR	66

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Input Value
target_i2cREG1_temp.DXR	78
target_i2cREG1_temp.MDR	495
target_i2cREG1_temp.IVR	66
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	78
target_i2cREG1_temp.PID11	56
target_i2cREG1_temp.PID12	78
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	87	87	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	✔
DigColPsInt_GetData()	40	40	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	121	121	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	20000	20000	✔
target_DataTypePtr_Cnt_T_u08	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_SpurSnsrDataPtr_Cnt_T_u16	28203	28203	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	✔

Test Step 2.14 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	40
DigColPsInt_Buffer_Cnt_M_u08[1]	50
DigColPsInt_Buffer_Cnt_M_u08[2]	60
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	33568
DigColPsInt_CurrentSlave_Cnt_M_u08	105
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADADDRREG_SENDCMD
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	18522573
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	149
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	0
DigColPsInt_TransactionCnt_Cnt_M_u08	135
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	94
k_I2CHWInitTransactionTime_Sec_f32	6.30000019
target_DtrmnElapsedTime_mS_u16_ElapsedTime	2769
target_GetSystemTime_mS_u32_CurrentTime	14511565
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.MDR	566
target_i2cREG1_temp.IVR	554
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	44
target_i2cREG1_temp.PID11	4466
target_i2cREG1_temp.PID12	44
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	0
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	40	40	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	50	50	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	60	60	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	105	105	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADADDRREG_SEN	INIT_SENSOR2_EXTREADADDRREG_SEN	✔
DigColPsInt_GetData()	6	6	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	135	135	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	33568	33568	✔
target_DataTypePtr_Cnt_T_u08	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	✔

Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_SpurSnsrDataPtr_Cnt_T_u16	0	0	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔

Test Step 2.15 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	70
DigColPsInt_Buffer_Cnt_M_u08[1]	80
DigColPsInt_Buffer_Cnt_M_u08[2]	90
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	45897
DigColPsInt_CurrentSlave_Cnt_M_u08	112
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	19525325
DigColPsInt_NackOccured_Cnt_M_lgc	0

Name	Input Value
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	167
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	65535
DigColPsInt_TransactionCnt_Cnt_M_u08	149
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	101
k_I2CHWInitTransactionTime_Sec_f32	6.69999981
target_DtrmnElapsedTime_mS_u16_ElapsedTime	3276
target_GetSystemTime_mS_u32_CurrentTime	15514317
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	65
target_i2cREG1_temp.IMR	89
target_i2cREG1_temp.STR	67
target_i2cREG1_temp.CLKL	7
target_i2cREG1_temp.CLKH	577
target_i2cREG1_temp.CNT	88
target_i2cREG1_temp.DRR	23

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Input Value
target_i2cREG1_temp.SAR	65
target_i2cREG1_temp.DXR	89
target_i2cREG1_temp.MDR	7
target_i2cREG1_temp.IVR	44
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	89
target_i2cREG1_temp.PID11	577
target_i2cREG1_temp.PID12	89
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	2
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	80	80	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	90	90	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	101	101	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	✔
DigColPsInt_GetData()	40	40	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	149	149	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	45897	45897	✔
target_DataTypePtr_Cnt_T_u08	4	4	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_SpurSnsrDataPtr_Cnt_T_u16	65535	65535	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	✔

Test Step 2.16 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	44
DigColPsInt_Buffer_Cnt_M_u08[1]	55
DigColPsInt_Buffer_Cnt_M_u08[2]	66
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	58226
DigColPsInt_CurrentSlave_Cnt_M_u08	119
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADADDRREG_SENDCMD
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	20528077
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	185
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	35000
DigColPsInt_TransactionCnt_Cnt_M_u08	163
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	108
k_I2CHWInitTransactionTime_Sec_f32	7.0999999
target_DtrmnElapsedTime_mS_u16_ElapsedTime	3783
target_GetSystemTime_mS_u32_CurrentTime	16517069
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	44	44	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	55	55	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	66	66	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	119	119	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADADDRREG_SEN	INIT_SENSOR1_EXTREADADDRREG_SEN	✔
DigColPsInt_GetData()	6	6	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	163	163	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	58226	58226	✔
target_DataTypePtr_Cnt_T_u08	1	1	✔

Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_SpurSnsrDataPtr_Cnt_T_u16	35000	35000	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔

Test Step 2.17 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	66
DigColPsInt_Buffer_Cnt_M_u08[1]	77
DigColPsInt_Buffer_Cnt_M_u08[2]	88
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	62548
DigColPsInt_CurrentSlave_Cnt_M_u08	126
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_DUMMY_SEND
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	21530829

Name	Input Value
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	203
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	37896
DigColPsInt_TransactionCnt_Cnt_M_u08	177
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	115
k_I2CHWInitTransactionTime_Sec_f32	7.5
target_DtrmnElapsedTime_mS_u16_ElapsedTime	4290
target_GetSystemTime_mS_u32_CurrentTime	17519821
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	78
target_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56
target_i2cREG1_temp.CNT	897

TEST DETAILS REPORT

DigColPsInt_GetData

2014-10-14, 23:35:27+0530

Name	Input Value
target_i2cREG1_temp.DRR	98
target_i2cREG1_temp.SAR	66
target_i2cREG1_temp.DXR	78
target_i2cREG1_temp.MDR	495
target_i2cREG1_temp.IVR	66
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	78
target_i2cREG1_temp.PID11	56
target_i2cREG1_temp.PID12	78
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	77	77	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	88	88	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	115	115	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	✔
DigColPsInt_GetData()	40	40	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	177	177	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	62548	62548	✔
target_DataTypePtr_Cnt_T_u08	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_SpurSnsrDataPtr_Cnt_T_u16	37896	37896	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	✔

Test Step 2.18 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	66
DigColPsInt_Buffer_Cnt_M_u08[1]	77
DigColPsInt_Buffer_Cnt_M_u08[2]	88
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	64896
DigColPsInt_CurrentSlave_Cnt_M_u08	17
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_SENDCMD
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	22533581
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	221
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	45863
DigColPsInt_TransactionCnt_Cnt_M_u08	191
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	122
k_I2CHWInitTransactionTime_Sec_f32	7.9000001
target_DtrmnElapsedTime_mS_u16_ElapsedTime	4797
target_GetSystemTime_mS_u32_CurrentTime	18522573
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	78
target_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56
target_i2cREG1_temp.CNT	897
target_i2cREG1_temp.DRR	98
target_i2cREG1_temp.SAR	66
target_i2cREG1_temp.DXR	78
target_i2cREG1_temp.MDR	495
target_i2cREG1_temp.IVR	66
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	78
target_i2cREG1_temp.PID11	56
target_i2cREG1_temp.PID12	78
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	77	77	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	88	88	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	122	122	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	✔
DigColPsInt_GetData()	6	6	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	191	191	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Actual Value	Expected Value	Result
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	64896	64896	✔
target_DataTypePtr_Cnt_T_u08	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_SpurSnsrDataPtr_Cnt_T_u16	45863	45863	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	✔

Test Step 2.19 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	40
DigColPsInt_Buffer_Cnt_M_u08[1]	50
DigColPsInt_Buffer_Cnt_M_u08[2]	60

Name	Input Value
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	65325
DigColPsInt_CurrentSlave_Cnt_M_u08	24
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_SENDCMD
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	23536333
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	239
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	55797
DigColPsInt_TransactionCnt_Cnt_M_u08	205
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	1
k_I2CHWInitTransactionTime_Sec_f32	8.30000019
target_DtrmnElapsedTime_mS_u16_ElapsedTime	5304
target_GetSystemTime_mS_u32_CurrentTime	19525325
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Input Value
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.MDR	566
target_i2cREG1_temp.IVR	554
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	44
target_i2cREG1_temp.PID11	4466
target_i2cREG1_temp.PID12	44
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	0
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	40	40	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	50	50	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	60	60	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	24	24	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_SENDCMD	INIT_SENSOR1_SENDCMD	✔
DigColPsInt_GetData()	40	40	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	205	205	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	65325	65325	✔
target_DataTypePtr_Cnt_T_u08	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_SpurSnsrDataPtr_Cnt_T_u16	55797	55797	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔

Test Step 2.20 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	70
DigColPsInt_Buffer_Cnt_M_u08[1]	80
DigColPsInt_Buffer_Cnt_M_u08[2]	90
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	5600
DigColPsInt_CurrentSlave_Cnt_M_u08	31
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	24539085
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	19
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	9687
DigColPsInt_TransactionCnt_Cnt_M_u08	12
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	115
k_I2CHWInitTransactionTime_Sec_f32	8.69999981
target_DtrmnElapsedTime_mS_u16_ElapsedTime	5811
target_GetSystemTime_mS_u32_CurrentTime	20528077
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	65
target_i2cREG1_temp.IMR	89
target_i2cREG1_temp.STR	67
target_i2cREG1_temp.CLKL	7
target_i2cREG1_temp.CLKH	577
target_i2cREG1_temp.CNT	88
target_i2cREG1_temp.DRR	23
target_i2cREG1_temp.SAR	65
target_i2cREG1_temp.DXR	89
target_i2cREG1_temp.MDR	7
target_i2cREG1_temp.IVR	44
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	89
target_i2cREG1_temp.PID11	577
target_i2cREG1_temp.PID12	89
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	2
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	80	80	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	90	90	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	115	115	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	✔
DigColPsInt_GetData()	0	0	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	12	12	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Actual Value	Expected Value	Result
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	5600	5600	✔
target_DataTypePtr_Cnt_T_u08	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_SpurSnsrDataPtr_Cnt_T_u16	9687	9687	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	✔

Test Step 2.21 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	3
DigColPsInt_Buffer_Cnt_M_u08[1]	6

Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	7985
DigColPsInt_CurrentSlave_Cnt_M_u08	38
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	25541837
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	31
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	11230
DigColPsInt_TransactionCnt_Cnt_M_u08	29
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	122
k_I2CHWInitTransactionTime_Sec_f32	9.10000038
target_DtrmnElapsedTime_mS_u16_ElapsedTime	6318
target_GetSystemTime_mS_u32_CurrentTime	21530829
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Input Value
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1
target_i2cREG1_temp.OAR	10
target_i2cREG1_temp.IMR	10
target_i2cREG1_temp.STR	1223
target_i2cREG1_temp.CLKL	7846
target_i2cREG1_temp.CLKH	8974
target_i2cREG1_temp.CNT	98
target_i2cREG1_temp.DRR	12
target_i2cREG1_temp.SAR	10
target_i2cREG1_temp.DXR	10
target_i2cREG1_temp.MDR	7846
target_i2cREG1_temp.IVR	55
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	10
target_i2cREG1_temp.PID11	8974
target_i2cREG1_temp.PID12	10
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	1
target_i2cREG1_temp.PSL	1

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	3	3	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	6	6	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	9	9	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	38	38	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_READ	INIT_SENSOR1_READEXTERR_READ	✔
DigColPsInt_GetData()	46	46	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	29	29	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	7985	7985	✔
target_DataTypePtr_Cnt_T_u08	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98	98	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_SpurSnsrDataPtr_Cnt_T_u16	11230	11230	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔

Test Step 2.22 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	11
DigColPsInt_Buffer_Cnt_M_u08[1]	22
DigColPsInt_Buffer_Cnt_M_u08[2]	33
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	10370
DigColPsInt_CurrentSlave_Cnt_M_u08	45
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_NOT_INITIALIZED
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	26544589
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	43
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	12773
DigColPsInt_TransactionCnt_Cnt_M_u08	33
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	1
k_I2CHWInitTransactionTime_Sec_f32	9.5
target_DtrmnElapsedTime_mS_u16_ElapsedTime	6825
target_GetSystemTime_mS_u32_CurrentTime	22533581
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2
target_i2cREG1_temp.OAR	34
target_i2cREG1_temp.IMR	24
target_i2cREG1_temp.STR	455
target_i2cREG1_temp.CLKL	847
target_i2cREG1_temp.CLKH	987
target_i2cREG1_temp.CNT	487
target_i2cREG1_temp.DRR	34
target_i2cREG1_temp.SAR	34
target_i2cREG1_temp.DXR	24
target_i2cREG1_temp.MDR	847
target_i2cREG1_temp.IVR	56
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	24
target_i2cREG1_temp.PID11	987
target_i2cREG1_temp.PID12	24
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	3
target_i2cREG1_temp.DIN	3
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	2
target_i2cREG1_temp.CLR	3
target_i2cREG1_temp.ODR	3
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	2

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	11	11	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	22	22	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	33	33	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	45	45	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_NOT_INITIALIZED	INIT_NOT_INITIALIZED	✔
DigColPsInt_GetData()	0	0	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	33	33	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Actual Value	Expected Value	Result
DigColPsInt_SensInitialized_Cnt_M_Igc	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	10370	10370	✔
target_DataTypePtr_Cnt_T_u08	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_SpurSnsrDataPtr_Cnt_T_u16	12773	12773	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔

Test Step 2.23 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	44
DigColPsInt_Buffer_Cnt_M_u08[1]	55
DigColPsInt_Buffer_Cnt_M_u08[2]	66
DigColPsInt_BusBusySeqError_Cnt_M_Igc	1
DigColPsInt_CmdFailOccurred_Cnt_M_Igc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	12755
DigColPsInt_CurrentSlave_Cnt_M_u08	52

Name	Input Value
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	27547341
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	55
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	14316
DigColPsInt_TransactionCnt_Cnt_M_u08	46
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	14
k_I2CHWInitTransactionTime_Sec_f32	9.89999962
target_DtrmnElapsedTime_mS_u16_ElapsedTime	7332
target_GetSystemTime_mS_u32_CurrentTime	23536333
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Input Value
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	55	55	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	66	66	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	14	14	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	✔
DigColPsInt_GetData()	38	38	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	46	46	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	12755	12755	✔
target_DataTypePtr_Cnt_T_u08	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_SpurSnsrDataPtr_Cnt_T_u16	14316	14316	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	✔

Test Step 2.24 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	20000
DigColPsInt_CurrentSlave_Cnt_M_u08	59
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	28550093
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	131
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	28203
DigColPsInt_TransactionCnt_Cnt_M_u08	121
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	21
k_I2CHWInitTransactionTime_Sec_f32	1.20000005
target_DtrmnElapsedTime_mS_u16_ElapsedTime	7839
target_GetSystemTime_mS_u32_CurrentTime	24539085
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	78
target_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56
target_i2cREG1_temp.CNT	897
target_i2cREG1_temp.DRR	98
target_i2cREG1_temp.SAR	66
target_i2cREG1_temp.DXR	78
target_i2cREG1_temp.MDR	495
target_i2cREG1_temp.IVR	66
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	78
target_i2cREG1_temp.PID11	56
target_i2cREG1_temp.PID12	78
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	59	59	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_READ	INIT_SENSOR2_CHECKSTAT_READ	✔
DigColPsInt_GetData()	136	136	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	121	121	✔

Name	Actual Value	Expected Value	Result
DigColPsInt_RecvOverrunError_Cnt_M_Igc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_Igc	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	20000	20000	✔
target_DataTypePtr_Cnt_T_u08	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_SpurSnsrDataPtr_Cnt_T_u16	28203	28203	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔

Test Step 2.25 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	40
DigColPsInt_Buffer_Cnt_M_u08[1]	50
DigColPsInt_Buffer_Cnt_M_u08[2]	60
DigColPsInt_BusBusySeqError_Cnt_M_Igc	0
DigColPsInt_CmdFailOccurred_Cnt_M_Igc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	14752

Name	Input Value
DigColPsInt_CurrentSlave_Cnt_M_u08	66
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_DUMMY_SEND
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	29552845
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	11
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	21478
DigColPsInt_TransactionCnt_Cnt_M_u08	14
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	28
k_I2CHWInitTransactionTime_Sec_f32	0
target_DtrmnElapsedTime_mS_u16_ElapsedTime	8346
target_GetSystemTime_mS_u32_CurrentTime	25541837
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44

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Name	Input Value
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.MDR	566
target_i2cREG1_temp.IVR	554
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	44
target_i2cREG1_temp.PID11	4466
target_i2cREG1_temp.PID12	44
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	0
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	40	40	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	50	50	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	60	60	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	66	66	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_DUMMY_SEND	INIT_SENSOR1_DUMMY_SEND	✔
DigColPsInt_GetData()	170	170	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	14	14	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	14752	14752	✔
target_DataTypePtr_Cnt_T_u08	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	✔

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_SpurSnsrDataPtr_Cnt_T_u16	21478	21478	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔

Test Step 2.26 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	70
DigColPsInt_Buffer_Cnt_M_u08[1]	80
DigColPsInt_Buffer_Cnt_M_u08[2]	90
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	17542
DigColPsInt_CurrentSlave_Cnt_M_u08	73
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_SENDCMD
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	30555597
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	17
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	22177
DigColPsInt_TransactionCnt_Cnt_M_u08	18
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	35
k_I2CHWInitTransactionTime_Sec_f32	10
target_DtrmnElapsedTime_mS_u16_ElapsedTime	8853
target_GetSystemTime_mS_u32_CurrentTime	26544589
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0

TEST DETAILS REPORT

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Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	65
target_i2cREG1_temp.IMR	89
target_i2cREG1_temp.STR	67
target_i2cREG1_temp.CLKL	7
target_i2cREG1_temp.CLKH	577
target_i2cREG1_temp.CNT	88
target_i2cREG1_temp.DRR	23
target_i2cREG1_temp.SAR	65
target_i2cREG1_temp.DXR	89
target_i2cREG1_temp.MDR	7
target_i2cREG1_temp.IVR	44
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	89
target_i2cREG1_temp.PID11	577
target_i2cREG1_temp.PID12	89
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	2
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	70	70	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	80	80	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	90	90	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	73	73	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_SEN	INIT_SENSOR2_EXTREADCTRLREG_SEN	✔
DigColPsInt_GetData()	12	12	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	18	18	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	17542	17542	✔
target_DataTypePtr_Cnt_T_u08	4	4	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	✔

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_SpurSnsrDataPtr_Cnt_T_u16	22177	22177	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔

Test Step 2.27 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	44
DigColPsInt_Buffer_Cnt_M_u08[1]	55
DigColPsInt_Buffer_Cnt_M_u08[2]	66
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	20332
DigColPsInt_CurrentSlave_Cnt_M_u08	80
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_SETREG
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	31558349
DigColPsInt_NackOccured_Cnt_M_lgc	1

Name	Input Value
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	23
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	22876
DigColPsInt_TransactionCnt_Cnt_M_u08	22
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	42
k_I2CHWInitTransactionTime_Sec_f32	2.5
target_DtrmnElapsedTime_mS_u16_ElapsedTime	9360
target_GetSystemTime_mS_u32_CurrentTime	27547341
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2
target_i2cREG1_temp.OAR	54
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	8
target_i2cREG1_temp.CLKL	554
target_i2cREG1_temp.CLKH	344
target_i2cREG1_temp.CNT	123
target_i2cREG1_temp.DRR	45

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Input Value
target_i2cREG1_temp.SAR	54
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	554
target_i2cREG1_temp.IVR	788
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	344
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	3
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	3
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	1
target_i2cREG1_temp.PSL	2

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	44	44	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	55	55	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	66	66	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	80	80	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_SET	INIT_SENSOR1_EXTREADCTRLREG_SET	✔
DigColPsInt_GetData()	162	162	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	22	22	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	20332	20332	✔
target_DataTypePtr_Cnt_T_u08	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_SpurSnsrDataPtr_Cnt_T_u16	22876	22876	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔

Test Step 2.28 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	66
DigColPsInt_Buffer_Cnt_M_u08[1]	77
DigColPsInt_Buffer_Cnt_M_u08[2]	88
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	23122
DigColPsInt_CurrentSlave_Cnt_M_u08	87
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	32561101
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	29
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	23575
DigColPsInt_TransactionCnt_Cnt_M_u08	26
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	49
k_I2CHWInitTransactionTime_Sec_f32	0.699999988
target_DtrmnElapsedTime_mS_u16_ElapsedTime	9867
target_GetSystemTime_mS_u32_CurrentTime	28550093
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	3
target_i2cREG1_temp.IMR	100
target_i2cREG1_temp.STR	7788
target_i2cREG1_temp.CLKL	2767
target_i2cREG1_temp.CLKH	556
target_i2cREG1_temp.CNT	564
target_i2cREG1_temp.DRR	88
target_i2cREG1_temp.SAR	3
target_i2cREG1_temp.DXR	100
target_i2cREG1_temp.MDR	2767
target_i2cREG1_temp.IVR	9
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	100
target_i2cREG1_temp.PID11	556
target_i2cREG1_temp.PID12	100
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	3
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	3
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	66	66	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	77	77	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	88	88	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	87	87	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_REA	INIT_SENSOR2_EXTREADCTRLREG_REA	✔
DigColPsInt_GetData()	130	130	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	26	26	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	23122	23122	✔
target_DataTypePtr_Cnt_T_u08	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	564	✔

Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_SpurSnsrDataPtr_Cnt_T_u16	23575	23575	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔

Test Step 2.29 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	25912
DigColPsInt_CurrentSlave_Cnt_M_u08	94
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADDATREG_SETREG
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	33563853
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	35
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	24274

Name	Input Value
DigColPsInt_TransactionCnt_Cnt_M_u08	30
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	56
k_I2CHWInitTransactionTime_Sec_f32	1.10000002
target_DtrmnElapsedTime_mS_u16_ElapsedTime	10374
target_GetSystemTime_mS_u32_CurrentTime	29552845
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	678
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	6788
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	7878
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	678
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	778
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	6788
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	678
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	6788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	7878
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	678
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	778
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	6788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1
target_i2cREG1_temp.OAR	678
target_i2cREG1_temp.IMR	45
target_i2cREG1_temp.STR	66
target_i2cREG1_temp.CLKL	56
target_i2cREG1_temp.CLKH	6788
target_i2cREG1_temp.CNT	7878
target_i2cREG1_temp.DRR	12
target_i2cREG1_temp.SAR	678
target_i2cREG1_temp.DXR	45
target_i2cREG1_temp.MDR	56
target_i2cREG1_temp.IVR	778
target_i2cREG1_temp.EMDR	1

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Name	Input Value
target_i2cREG1_temp.PSC	45
target_i2cREG1_temp.PID11	6788
target_i2cREG1_temp.PID12	45
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	1

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	56	56	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	✔
DigColPsInt_GetData()	44	44	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	30	30	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	25912	25912	✔
target_DataTypePtr_Cnt_T_u08	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	678	678	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	45	45	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	7878	7878	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	678	678	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	45	45	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	778	778	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	45	45	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	6788	6788	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	45	45	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	678	678	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	45	45	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	7878	7878	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	678	678	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	45	45	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	778	778	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	45	45	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	6788	6788	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	45	45	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_SpurSnsrDataPtr_Cnt_T_u16	24274	24274	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	✔

Test Step 2.30 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	40
DigColPsInt_Buffer_Cnt_M_u08[1]	50
DigColPsInt_Buffer_Cnt_M_u08[2]	60
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	28702
DigColPsInt_CurrentSlave_Cnt_M_u08	101
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	34566605
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	41
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	24973
DigColPsInt_TransactionCnt_Cnt_M_u08	34
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	63
k_I2CHWInitTransactionTime_Sec_f32	1.5
target_DtrmnElapsedTime_mS_u16_ElapsedTime	10881
target_GetSystemTime_mS_u32_CurrentTime	30555597
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0

TEST DETAILS REPORT

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Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	78
target_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56
target_i2cREG1_temp.CNT	897
target_i2cREG1_temp.DRR	98
target_i2cREG1_temp.SAR	66
target_i2cREG1_temp.DXR	78
target_i2cREG1_temp.MDR	495
target_i2cREG1_temp.IVR	66
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	78
target_i2cREG1_temp.PID11	56
target_i2cREG1_temp.PID12	78
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	40	40	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	50	50	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	60	60	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	101	101	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG	READ_SENSOR1_SETREG	✔
DigColPsInt_GetData()	2	2	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	34	34	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	28702	28702	✔
target_DataTypePtr_Cnt_T_u08	4	4	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_SpurSnsrDataPtr_Cnt_T_u16	24973	24973	✔

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Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.31 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	70
DigColPsInt_Buffer_Cnt_M_u08[1]	80
DigColPsInt_Buffer_Cnt_M_u08[2]	90
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	31492
DigColPsInt_CurrentSlave_Cnt_M_u08	108
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_GETDATA
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	35569357
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	47
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0

Name	Input Value
DigColPsInt_SpurSnsrData_Cnt_M_u16	25672
DigColPsInt_TransactionCnt_Cnt_M_u08	38
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	70
k_I2CHWInitTransactionTime_Sec_f32	1.89999998
target_DtrmnElapsedTime_mS_u16_ElapsedTime	11388
target_GetSystemTime_mS_u32_CurrentTime	31558349
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.MDR	566
target_i2cREG1_temp.IVR	554

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Input Value
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	44
target_i2cREG1_temp.PID11	4466
target_i2cREG1_temp.PID12	44
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	0
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	80	80	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	90	90	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	70	70	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	✔
DigColPsInt_GetData()	44	44	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	38	38	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	31492	31492	✔
target_DataTypePtr_Cnt_T_u08	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_SpurSnsrDataPtr_Cnt_T_u16	25672	25672	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	✔

Test Step 2.32 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	3
DigColPsInt_Buffer_Cnt_M_u08[1]	6
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	34282
DigColPsInt_CurrentSlave_Cnt_M_u08	115
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	36572109
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	53
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	26371
DigColPsInt_TransactionCnt_Cnt_M_u08	42
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	77
k_I2CHWInitTransactionTime_Sec_f32	2.29999995
target_DtrmnElapsedTime_mS_u16_ElapsedTime	0
target_GetSystemTime_mS_u32_CurrentTime	32561101
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2

TEST DETAILS REPORT

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Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	65
target_i2cREG1_temp.IMR	89
target_i2cREG1_temp.STR	67
target_i2cREG1_temp.CLKL	7
target_i2cREG1_temp.CLKH	577
target_i2cREG1_temp.CNT	88
target_i2cREG1_temp.DRR	23
target_i2cREG1_temp.SAR	65
target_i2cREG1_temp.DXR	89
target_i2cREG1_temp.MDR	7
target_i2cREG1_temp.IVR	44
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	89
target_i2cREG1_temp.PID11	577
target_i2cREG1_temp.PID12	89
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	2
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	3	3	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	6	6	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	9	9	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	115	115	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	✔
DigColPsInt_GetData()	34	34	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	42	42	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	34282	34282	✔
target_DataTypePtr_Cnt_T_u08	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔

TEST DETAILS REPORT

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_SpurSnsrDataPtr_Cnt_T_u16	26371	26371	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔

Test Step 2.33 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	11
DigColPsInt_Buffer_Cnt_M_u08[1]	22
DigColPsInt_Buffer_Cnt_M_u08[2]	33
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	37072
DigColPsInt_CurrentSlave_Cnt_M_u08	122
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	37574861
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	59
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2

TEST DETAILS REPORT

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Name	Input Value
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	22	22	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	33	33	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	84	84	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	✔
DigColPsInt_GetData()	6	6	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	46	46	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	37072	37072	✔
target_DataTypePtr_Cnt_T_u08	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_SpurSnsrDataPtr_Cnt_T_u16	27070	27070	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	✔

Test Step 2.34 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	39862
DigColPsInt_CurrentSlave_Cnt_M_u08	1
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	38577613
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	65
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	27769
DigColPsInt_TransactionCnt_Cnt_M_u08	50
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	91
k_I2CHWInitTransactionTime_Sec_f32	3.0999999
target_DtrmnElapsedTime_mS_u16_ElapsedTime	14789
target_GetSystemTime_mS_u32_CurrentTime	34566605
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	78
target_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56
target_i2cREG1_temp.CNT	897
target_i2cREG1_temp.DRR	98
target_i2cREG1_temp.SAR	66
target_i2cREG1_temp.DXR	78
target_i2cREG1_temp.MDR	495
target_i2cREG1_temp.IVR	66
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	78
target_i2cREG1_temp.PID11	56
target_i2cREG1_temp.PID12	78
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	1	1	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_READ	INIT_SENSOR2_READERROR_READ	✔
DigColPsInt_GetData()	168	168	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	50	50	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	39862	39862	✔
target_DataTypePtr_Cnt_T_u08	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	✔

Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_SpurSnsrDataPtr_Cnt_T_u16	27769	27769	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔

Test Step 2.35 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	40
DigColPsInt_Buffer_Cnt_M_u08[1]	50
DigColPsInt_Buffer_Cnt_M_u08[2]	60
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	34282
DigColPsInt_CurrentSlave_Cnt_M_u08	115
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	39580365
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	53
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0

Name	Input Value
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	26371
DigColPsInt_TransactionCnt_Cnt_M_u08	42
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	0
k_I2CHWInitTransactionTime_Sec_f32	2.29999995
target_DtrmnElapsedTime_mS_u16_ElapsedTime	18975
target_GetSystemTime_mS_u32_CurrentTime	35569357
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	65
target_i2cREG1_temp.IMR	89
target_i2cREG1_temp.STR	67
target_i2cREG1_temp.CLKL	7
target_i2cREG1_temp.CLKH	577
target_i2cREG1_temp.CNT	88
target_i2cREG1_temp.DRR	23
target_i2cREG1_temp.SAR	65
target_i2cREG1_temp.DXR	89

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Input Value
target_i2cREG1_temp.MDR	7
target_i2cREG1_temp.IVR	44
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	89
target_i2cREG1_temp.PID11	577
target_i2cREG1_temp.PID12	89
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	2
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	40	40	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	50	50	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	60	60	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	115	115	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	✔
DigColPsInt_GetData()	162	162	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	42	42	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	34282	34282	✔
target_DataTypePtr_Cnt_T_u08	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_SpurSnsrDataPtr_Cnt_T_u16	26371	26371	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔

Test Step 2.36 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	70
DigColPsInt_Buffer_Cnt_M_u08[1]	80
DigColPsInt_Buffer_Cnt_M_u08[2]	90
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	37072
DigColPsInt_CurrentSlave_Cnt_M_u08	122
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	40583117
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	59
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	27070
DigColPsInt_TransactionCnt_Cnt_M_u08	46
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	127
k_I2CHWInitTransactionTime_Sec_f32	2.70000005
target_DtrmnElapsedTime_mS_u16_ElapsedTime	21458
target_GetSystemTime_mS_u32_CurrentTime	36572109
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Input Value
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	80	80	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	90	90	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	✔
DigColPsInt_GetData()	6	6	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	46	46	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	37072	37072	✔
target_DataTypePtr_Cnt_T_u08	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔

Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_SpurSnsrDataPtr_Cnt_T_u16	27070	27070	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	✔

Test Step 2.37 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	44
DigColPsInt_Buffer_Cnt_M_u08[1]	55
DigColPsInt_Buffer_Cnt_M_u08[2]	66
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	39862
DigColPsInt_CurrentSlave_Cnt_M_u08	1
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	41585869
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	65

Name	Input Value
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	27769
DigColPsInt_TransactionCnt_Cnt_M_u08	50
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	91
k_I2CHWInitTransactionTime_Sec_f32	3.0999999
target_DtrmnElapsedTime_mS_u16_ElapsedTime	14789
target_GetSystemTime_mS_u32_CurrentTime	37574861
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	78
target_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56
target_i2cREG1_temp.CNT	897
target_i2cREG1_temp.DRR	98
target_i2cREG1_temp.SAR	66

TEST DETAILS REPORT

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Name	Input Value
target_i2cREG1_temp.DXR	78
target_i2cREG1_temp.MDR	495
target_i2cREG1_temp.IVR	66
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	78
target_i2cREG1_temp.PID11	56
target_i2cREG1_temp.PID12	78
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	44	44	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	55	55	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	66	66	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	1	1	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_READ	INIT_SENSOR2_READERROR_READ	✔
DigColPsInt_GetData()	168	168	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	50	50	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	39862	39862	✔
target_DataTypePtr_Cnt_T_u08	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_SpurSnsrDataPtr_Cnt_T_u16	27769	27769	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔

Test Step 2.38 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	3
DigColPsInt_Buffer_Cnt_M_u08[1]	6
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	34282
DigColPsInt_CurrentSlave_Cnt_M_u08	115
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	42588621
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	53
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	26371
DigColPsInt_TransactionCnt_Cnt_M_u08	42
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	77
k_I2CHWInitTransactionTime_Sec_f32	2.29999995
target_DtrmnElapsedTime_mS_u16_ElapsedTime	9360
target_GetSystemTime_mS_u32_CurrentTime	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2

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Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	65
target_i2cREG1_temp.IMR	89
target_i2cREG1_temp.STR	67
target_i2cREG1_temp.CLKL	7
target_i2cREG1_temp.CLKH	577
target_i2cREG1_temp.CNT	88
target_i2cREG1_temp.DRR	23
target_i2cREG1_temp.SAR	65
target_i2cREG1_temp.DXR	89
target_i2cREG1_temp.MDR	7
target_i2cREG1_temp.IVR	44
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	89
target_i2cREG1_temp.PID11	577
target_i2cREG1_temp.PID12	89
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	2
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	6	6	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	9	9	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	77	77	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	✔
DigColPsInt_GetData()	34	34	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	42	42	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	34282	34282	✔
target_DataTypePtr_Cnt_T_u08	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_SpurSnsrDataPtr_Cnt_T_u16	26371	26371	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	✔

Test Step 2.39 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	11
DigColPsInt_Buffer_Cnt_M_u08[1]	22
DigColPsInt_Buffer_Cnt_M_u08[2]	33
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	37072
DigColPsInt_CurrentSlave_Cnt_M_u08	122
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	43591373
DigColPsInt_NackOccured_Cnt_M_lgc	1

Name	Input Value
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	59
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	27070
DigColPsInt_TransactionCnt_Cnt_M_u08	46
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	84
k_I2CHWInitTransactionTime_Sec_f32	2.70000005
target_DtrmnElapsedTime_mS_u16_ElapsedTime	9867
target_GetSystemTime_mS_u32_CurrentTime	4294967295
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Input Value
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	22	22	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	33	33	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	84	84	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	✔
DigColPsInt_GetData()	6	6	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	46	46	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	37072	37072	✔
target_DataTypePtr_Cnt_T_u08	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_SpurSnsrDataPtr_Cnt_T_u16	27070	27070	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	✔

Test Step 2.40 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	39862
DigColPsInt_CurrentSlave_Cnt_M_u08	1
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	44594125
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	65
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	27769
DigColPsInt_TransactionCnt_Cnt_M_u08	50
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	91
k_I2CHWInitTransactionTime_Sec_f32	3.0999999
target_DtrmnElapsedTime_mS_u16_ElapsedTime	10374
target_GetSystemTime_mS_u32_CurrentTime	1478524
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0

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DigColPsInt_GetData

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Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	78
target_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56
target_i2cREG1_temp.CNT	897
target_i2cREG1_temp.DRR	98
target_i2cREG1_temp.SAR	66
target_i2cREG1_temp.DXR	78
target_i2cREG1_temp.MDR	495
target_i2cREG1_temp.IVR	66
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	78
target_i2cREG1_temp.PID11	56
target_i2cREG1_temp.PID12	78
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	91	91	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	✔
DigColPsInt_GetData()	40	40	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	50	50	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Actual Value	Expected Value	Result
target_ColSnsrDataPtr_Cnt_T_u16	39862	39862	✔
target_DataTypePtr_Cnt_T_u08	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_SpurSnsrDataPtr_Cnt_T_u16	27769	27769	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	✔

Test Step 2.41 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	0
DigColPsInt_Buffer_Cnt_M_u08[1]	0
DigColPsInt_Buffer_Cnt_M_u08[2]	0
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0

Name	Input Value
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	0
DigColPsInt_CurrentSlave_Cnt_M_u08	0
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_NOT_INITIALIZED
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	0
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	0
DigColPsInt_TransactionCnt_Cnt_M_u08	0
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	0
k_I2CHWInitTransactionTime_Sec_f32	0
target_DtrmnElapsedTime_mS_u16_ElapsedTime	0
target_GetSystemTime_mS_u32_CurrentTime	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Input Value
target_i2cREG1_temp.OAR	0
target_i2cREG1_temp.IMR	0
target_i2cREG1_temp.STR	0
target_i2cREG1_temp.CLKL	0
target_i2cREG1_temp.CLKH	0
target_i2cREG1_temp.CNT	0
target_i2cREG1_temp.DRR	0
target_i2cREG1_temp.SAR	0
target_i2cREG1_temp.DXR	0
target_i2cREG1_temp.MDR	0
target_i2cREG1_temp.IVR	0
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	0
target_i2cREG1_temp.PID11	0
target_i2cREG1_temp.PID12	0
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	0
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	0	0	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	0	0	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	0	0	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	0	0	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_NOT_INITIALIZED	INIT_NOT_INITIALIZED	✔
DigColPsInt_GetData()	0	0	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	0	0	✔
target_ColSnsrDataPtr_Cnt_T_u16	0	0	✔
target_DataTypePtr_Cnt_T_u08	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	0	0	✔

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_SpurSnsrDataPtr_Cnt_T_u16	0	0	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔

Test Step 2.42 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	255
DigColPsInt_Buffer_Cnt_M_u08[1]	255
DigColPsInt_Buffer_Cnt_M_u08[2]	255
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	65535
DigColPsInt_CurrentSlave_Cnt_M_u08	127
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	4294967295
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	255
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	65535
DigColPsInt_TransactionCnt_Cnt_M_u08	255
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	127
k_I2CHWInitTransactionTime_Sec_f32	10
target_DtrmnElapsedTime_mS_u16_ElapsedTime	65535
target_GetSystemTime_mS_u32_CurrentTime	4294967295
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	32767
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	1023
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	4095
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	1023
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	32767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	1023
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	4095
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	1023
target_i2cREG1_temp.IMR	255
target_i2cREG1_temp.STR	32767
target_i2cREG1_temp.CLKL	65535
target_i2cREG1_temp.CLKH	65535
target_i2cREG1_temp.CNT	65535
target_i2cREG1_temp.DRR	255
target_i2cREG1_temp.SAR	1023
target_i2cREG1_temp.DXR	255
target_i2cREG1_temp.MDR	65535
target_i2cREG1_temp.IVR	4095
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	255
target_i2cREG1_temp.PID11	65535
target_i2cREG1_temp.PID12	255
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	3
target_i2cREG1_temp.DIN	3
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	3
target_i2cREG1_temp.ODR	3
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	255	255	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	255	255	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	255	255	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE	READ_COMPLETE	✔
DigColPsInt_GetData()	62	62	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	255	255	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	65535	65535	✔

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Actual Value	Expected Value	Result
target_DataTypePtr_Cnt_T_u08	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023	1023	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	255	255	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	32767	32767	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	65535	65535	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	255	255	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	1023	1023	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	255	255	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	65535	65535	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	4095	4095	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	255	255	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	65535	65535	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	255	255	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	1023	1023	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	255	255	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	32767	32767	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	65535	65535	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	255	255	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	1023	1023	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	255	255	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	65535	65535	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	4095	4095	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	255	255	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	65535	65535	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	255	255	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_SpurSnsrDataPtr_Cnt_T_u16	65535	65535	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
none	0	*** No Call Expected ***	0	✔

Test Case 3: Path Test

Description Test Vector Description:

TS3.1"(DigColPsInt_SensInitialized_Cnt_M_lgc == FALSE)=True
(ElapsedTime_mS_T_u16 >= (uint16)D_SENSINITDELAY_MS_U08)=True
(DigColPsInt_NackOccured_Cnt_M_lgc == TRUE)=False
(DigColPsInt_RecvOverrunError_Cnt_M_lgc == TRUE)=True
(DigColPsInt_BusBusySeqError_Cnt_M_lgc == TRUE)=False
(DigColPsInt_CmdFailOccurred_Cnt_M_lgc == TRUE)=True
((DigColPsInt_TransactionCnt_Cnt_M_u08 == DigColPsInt_PrevTransactionCnt_Cnt_M_u08) && (DigColPsInt_RecvdDataType_Cnt_M_u08 != D_NONE_CNT_U08))=False"
TS3.2"(DigColPsInt_SensInitialized_Cnt_M_lgc == FALSE)=False
(DigColPsInt_CurrentStepNo_Cnt_M_enum < INIT_COMPLETE)=True
(ElapsedTime_mS_T_u16 > (uint16)(k_I2CHWInitTransactionTime_Sec_f32*D_SECTOMILLSEC_CNT_F32))=True
(DigColPsInt_NackOccured_Cnt_M_lgc == TRUE)=True
(DigColPsInt_RecvOverrunError_Cnt_M_lgc == TRUE)=False
(DigColPsInt_BusBusySeqError_Cnt_M_lgc == TRUE)=True
(DigColPsInt_CmdFailOccurred_Cnt_M_lgc == TRUE)=False"
TS3.3"(DigColPsInt_SensInitialized_Cnt_M_lgc == FALSE)=False
(DigColPsInt_CurrentStepNo_Cnt_M_enum < INIT_COMPLETE)=True
(ElapsedTime_mS_T_u16 > (uint16)(k_I2CHWInitTransactionTime_Sec_f32*D_SECTOMILLSEC_CNT_F32))=False"
TS3.4((DigColPsInt_TransactionCnt_Cnt_M_u08 == DigColPsInt_PrevTransactionCnt_Cnt_M_u08) =True &&
(DigColPsInt_RecvdDataType_Cnt_M_u08 != D_NONE_CNT_U08) =False)
TS3.5"(DigColPsInt_SensInitialized_Cnt_M_lgc == FALSE)=False
(DigColPsInt_CurrentStepNo_Cnt_M_enum < INIT_COMPLETE)=False"
TS3.6"(DigColPsInt_SensInitialized_Cnt_M_lgc == FALSE)=True
(ElapsedTime_mS_T_u16 >= (uint16)D_SENSINITDELAY_MS_U08)=False"
TS3.7((DigColPsInt_TransactionCnt_Cnt_M_u08 == DigColPsInt_PrevTransactionCnt_Cnt_M_u08) &&
(DigColPsInt_RecvdDataType_Cnt_M_u08 != D_NONE_CNT_U08))=True

Test Step 3.1 (Repeat Count = 1)

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	5600
DigColPsInt_CurrentSlave_Cnt_M_u08	14
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	5486797
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	19
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	9687
DigColPsInt_TransactionCnt_Cnt_M_u08	12
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	119
k_I2CHWInitTransactionTime_Sec_f32	1.10000002
target_DtrmnElapsedTime_mS_u16_ElapsedTime	1247
target_GetSystemTime_mS_u32_CurrentTime	1475789
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	78
target_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56
target_i2cREG1_temp.CNT	897
target_i2cREG1_temp.DRR	98
target_i2cREG1_temp.SAR	66
target_i2cREG1_temp.DXR	78
target_i2cREG1_temp.MDR	495
target_i2cREG1_temp.IVR	66
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	78
target_i2cREG1_temp.PID11	56
target_i2cREG1_temp.PID12	78
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	119	119	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	✔
DigColPsInt_GetData()	40	40	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	12	12	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Actual Value	Expected Value	Result
target_ColSnsrDataPtr_Cnt_T_u16	5600	5600	✔
target_DataTypePtr_Cnt_T_u08	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_SpurSnsrDataPtr_Cnt_T_u16	9687	9687	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	✔

Test Step 3.2 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	40
DigColPsInt_Buffer_Cnt_M_u08[1]	50
DigColPsInt_Buffer_Cnt_M_u08[2]	60
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1

Name	Input Value
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	7985
DigColPsInt_CurrentSlave_Cnt_M_u08	21
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	6489549
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	31
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	11230
DigColPsInt_TransactionCnt_Cnt_M_u08	29
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	126
k_I2CHWInitTransactionTime_Sec_f32	1.5
target_DtrmnElapsedTime_mS_u16_ElapsedTime	7841
target_GetSystemTime_mS_u32_CurrentTime	2478541
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Input Value
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.MDR	566
target_i2cREG1_temp.IVR	554
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	44
target_i2cREG1_temp.PID11	4466
target_i2cREG1_temp.PID12	44
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	0
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	40	40	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	50	50	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	60	60	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	21	21	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_READ	INIT_SENSOR1_READEXTERR_READ	✔
DigColPsInt_GetData()	134	134	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	29	29	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	7985	7985	✔
target_DataTypePtr_Cnt_T_u08	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_SpurSnsrDataPtr_Cnt_T_u16	11230	11230	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔

Test Step 3.3 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	3
DigColPsInt_Buffer_Cnt_M_u08[1]	6
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	27065
DigColPsInt_CurrentSlave_Cnt_M_u08	77
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_SETREG
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	14511565
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	130
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	23574
DigColPsInt_TransactionCnt_Cnt_M_u08	79
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	66
k_I2CHWInitTransactionTime_Sec_f32	4.69999981
target_DtrmnElapsedTime_mS_u16_ElapsedTime	741
target_GetSystemTime_mS_u32_CurrentTime	10500557
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2
target_i2cREG1_temp.OAR	54
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	8
target_i2cREG1_temp.CLKL	554
target_i2cREG1_temp.CLKH	344
target_i2cREG1_temp.CNT	123
target_i2cREG1_temp.DRR	45
target_i2cREG1_temp.SAR	54
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	554
target_i2cREG1_temp.IVR	788
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	344
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	3
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	3
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	1
target_i2cREG1_temp.PSL	2

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	3	3	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	6	6	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	9	9	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	77	77	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_SETREG	INIT_SENSOR2_READERROR_SETREG	✔
DigColPsInt_GetData()	6	6	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	79	79	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	27065	27065	✔

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Actual Value	Expected Value	Result
target_DataTypePtr_Cnt_T_u08	4	4	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_SpurSnsrDataPtr_Cnt_T_u16	23574	23574	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔

Test Step 3.4 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	11
DigColPsInt_Buffer_Cnt_M_u08[1]	22
DigColPsInt_Buffer_Cnt_M_u08[2]	33
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	0
DigColPsInt_CurrentSlave_Cnt_M_u08	84
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1

Name	Input Value
DigColPsInt_InitialTime_mS_M_u32	15514317
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	93
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	25117
DigColPsInt_TransactionCnt_Cnt_M_u08	93
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	73
k_I2CHWInitTransactionTime_Sec_f32	5.0999999
target_DtrmnElapsedTime_mS_u16_ElapsedTime	1248
target_GetSystemTime_mS_u32_CurrentTime	11503309
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	3
target_i2cREG1_temp.IMR	100
target_i2cREG1_temp.STR	7788
target_i2cREG1_temp.CLKL	2767
target_i2cREG1_temp.CLKH	556

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Name	Input Value
target_i2cREG1_temp.CNT	564
target_i2cREG1_temp.DRR	88
target_i2cREG1_temp.SAR	3
target_i2cREG1_temp.DXR	100
target_i2cREG1_temp.MDR	2767
target_i2cREG1_temp.IVR	9
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	100
target_i2cREG1_temp.PID11	556
target_i2cREG1_temp.PID12	100
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	3
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	3
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	22	22	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	33	33	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	73	73	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	✔
DigColPsInt_GetData()	40	40	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	93	93	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	0	0	✔
target_DataTypePtr_Cnt_T_u08	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_SpurSnsrDataPtr_Cnt_T_u16	25117	25117	✔

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Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	✔

Test Step 3.5 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	40
DigColPsInt_Buffer_Cnt_M_u08[1]	50
DigColPsInt_Buffer_Cnt_M_u08[2]	60
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	28702
DigColPsInt_CurrentSlave_Cnt_M_u08	101
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	34566605
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	41
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	24973
DigColPsInt_TransactionCnt_Cnt_M_u08	34
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	63
k_I2CHWInitTransactionTime_Sec_f32	1.5
target_DtrmnElapsedTime_mS_u16_ElapsedTime	10881
target_GetSystemTime_mS_u32_CurrentTime	30555597
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	78
target_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56
target_i2cREG1_temp.CNT	897
target_i2cREG1_temp.DRR	98
target_i2cREG1_temp.SAR	66
target_i2cREG1_temp.DXR	78
target_i2cREG1_temp.MDR	495
target_i2cREG1_temp.IVR	66
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	78
target_i2cREG1_temp.PID11	56
target_i2cREG1_temp.PID12	78
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	40	40	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	50	50	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	60	60	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	101	101	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG	READ_SENSOR1_SETREG	✔
DigColPsInt_GetData()	2	2	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	34	34	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Actual Value	Expected Value	Result
target_ColSnsrDataPtr_Cnt_T_u16	28702	28702	✔
target_DataTypePtr_Cnt_T_u08	4	4	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_SpurSnsrDataPtr_Cnt_T_u16	24973	24973	✔

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Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 3.6 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	0
DigColPsInt_Buffer_Cnt_M_u08[1]	0
DigColPsInt_Buffer_Cnt_M_u08[2]	0
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	0
DigColPsInt_CurrentSlave_Cnt_M_u08	0
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_NOT_INITIALIZED

Name	Input Value
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_InitialTime_mS_M_u32	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	0
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	0
DigColPsInt_TransactionCnt_Cnt_M_u08	0
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	0
k_I2CHWInitTransactionTime_Sec_f32	0
target_DtrmnElapsedTime_mS_u16_ElapsedTime	0
target_GetSystemTime_mS_u32_CurrentTime	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	0
target_i2cREG1_temp.IMR	0
target_i2cREG1_temp.STR	0
target_i2cREG1_temp.CLKL	0

TEST DETAILS REPORT

DigColPsInt_GetData

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Name	Input Value
target_i2cREG1_temp.CLKH	0
target_i2cREG1_temp.CNT	0
target_i2cREG1_temp.DRR	0
target_i2cREG1_temp.SAR	0
target_i2cREG1_temp.DXR	0
target_i2cREG1_temp.MDR	0
target_i2cREG1_temp.IVR	0
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	0
target_i2cREG1_temp.PID11	0
target_i2cREG1_temp.PID12	0
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	0
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	0	0	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	0	0	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	0	0	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	0	0	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_NOT_INITIALIZED	INIT_NOT_INITIALIZED	✔
DigColPsInt_GetData()	0	0	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	0	0	✔
target_ColSnsrDataPtr_Cnt_T_u16	0	0	✔
target_DataTypePtr_Cnt_T_u08	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_SpurSnsrDataPtr_Cnt_T_u16	0	0	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
DtrmnElapsedTime_mS_u16	1	DtrmnElapsedTime_mS_u16	1	✔

Test Step 3.7 (Repeat Count = 1) ✔

Name	Input Value
ColSnsrDataPtr_Cnt_T_u16	target_ColSnsrDataPtr_Cnt_T_u16
DataTypePtr_Cnt_T_u08	target_DataTypePtr_Cnt_T_u08
DigColPsInt_Buffer_Cnt_M_u08[0]	255
DigColPsInt_Buffer_Cnt_M_u08[1]	255
DigColPsInt_Buffer_Cnt_M_u08[2]	255
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	65535
DigColPsInt_CurrentSlave_Cnt_M_u08	127
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_InitialTime_mS_M_u32	4294967295
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	255
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	65535
DigColPsInt_TransactionCnt_Cnt_M_u08	255
DtrmnElapsedTime_mS_u16(ElapsedTime)	target_DtrmnElapsedTime_mS_u16_ElapsedTime
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
SpurSnsrDataPtr_Cnt_T_u16	target_SpurSnsrDataPtr_Cnt_T_u16
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	127
k_I2CHWInitTransactionTime_Sec_f32	10
target_DtrmnElapsedTime_mS_u16_ElapsedTime	65535
target_GetSystemTime_mS_u32_CurrentTime	4294967295
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	32767
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	1023
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	4095
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	1023
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	32767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	1023
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	4095
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	1023
target_i2cREG1_temp.IMR	255
target_i2cREG1_temp.STR	32767
target_i2cREG1_temp.CLKL	65535
target_i2cREG1_temp.CLKH	65535
target_i2cREG1_temp.CNT	65535
target_i2cREG1_temp.DRR	255
target_i2cREG1_temp.SAR	1023
target_i2cREG1_temp.DXR	255
target_i2cREG1_temp.MDR	65535
target_i2cREG1_temp.IVR	4095
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	255
target_i2cREG1_temp.PID11	65535
target_i2cREG1_temp.PID12	255
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	3
target_i2cREG1_temp.DIN	3
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	3
target_i2cREG1_temp.ODR	3
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	255	255	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	255	255	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	255	255	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE	READ_COMPLETE	✔
DigColPsInt_GetData()	62	62	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_PrevTransactionCnt_Cnt_M_u08	255	255	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_SensInitialized_Cnt_M_lgc	1	1	✔
target_ColSnsrDataPtr_Cnt_T_u16	65535	65535	✔
target_DataTypePtr_Cnt_T_u08	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023	1023	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	255	255	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	32767	32767	✔

TEST DETAILS REPORT

DigColPsInt_GetData

2014-10-14, 23:35:27+0530

Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	65535	65535	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	255	255	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	1023	1023	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	255	255	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	65535	65535	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	4095	4095	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	255	255	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	65535	65535	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	255	255	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	1023	1023	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	255	255	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	32767	32767	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	65535	65535	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	255	255	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	1023	1023	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	255	255	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	65535	65535	✔
[redacted]	[redacted]	[redacted]	target_I2c_Send_I2cI

TEST DETAILS REPORT

DigColPsInt_StartRequest

2014-10-14, 23:44:33+0530

Project	DigColPsInt
Module	DigColPsInt
Test Object	DigColPsInt_StartRequest

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %
MCC Coverage	90.9 %
MC/DC Coverage	90.9 %

Statistics

Total Testcases	3
Successful	3
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\C1xx_DigColPs
Configuration File	D:\Synergy_Work_Area\C1xx_DigColPs\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	$(PROJECTROOT)\DigColPs\src\Sa_DigColPsInt.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -DSTATIC= -D__inline= -I$(PROJECTROOT)\DigColPs\utp\contract -I$(PROJECTROOT)\DigColPs\utp\contract\Sa_DigColPs -I$(PROJECTROOT)\DigColPs\include -I$(PROJECTROOT)\NxtrLib\include -I$(PROJECTROOT)\StdDef\include -I$(PROJECTROOT)\StdDef\include\TMS570_HerculesRegs -I$(Compiler Install Path)\include

Comments/Description/Specification	
Name	**Text**

Module 'DigColPsInt'	**********Unit Test Descrption********** Name of Tester:Priti Mangalekar Code File(s) Under Test:Sa_DigColPsInt.c Code File(s) Version:7 Module Design Document:DigColPsInt_MDD.docx Module Design Document Version:8 Data Dictionary Version:9 Unit Test Plan Version:2 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.30 Total FLASH Used (Bytes):N/A Total RAM Used (Bytes):N/A Total CALS Used (Bytes):N/A Special Test Requirements: Test Date:10/13/2014 Comments: NOTE 1: In """"DigColPsInt_StartRequest"""" function, path """"(Type_Cnt_T_u08 > D_NONE_CNT_U08) = TRUE && (Type_Cnt_T_u08 <= D_STATUSREG_CNT_U08) = FALSE"""" cannot be covered because range of """"Type_Cnt_T_u08"""" is '0-5' and value of """"D_STATUSREG_CNT_U08"""" is '34'. NOTE2: In function ""DigColPsInt_GetData"",""DigColPsInt_StartRequest"" and ""DigColPsInt_InterruptNotification"" values for """"I2c_Send(Length_Cnt_T_u32)"""", """"I2c_SetRecv(Length_Cnt_T_u32)"""", """"I2c_SetStatus(Status_Cnt_T_u16)"""", """"I2c_SetupMasterReceive(DataLength_Cnt_T_u16)"""" and I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) are ignored in few vectors as they are taking garbage value when they are not updated with expected value in particular vector. NOTE3: The return value of """"DigColPsInt_GetData"""" function is going out of range, anomaly """"6156"""" is raised for the same. NOTE4:Range of DigColPsInt_CurrentStepNo_Cnt_M_enum is considered as 0 to 36, as enum DigColPsInt_CurrentStepNo_Cnt_M_enum is of type CommStepType which is of 37 elements. NOTE5:In function ""DigColPsInt_InterruptNotification"", path ""Case I2C_RECV_OVERRUN: True"" cannot be covered because range of ""Flags_Cnt_T_b16"" is 0 to 64 given in MDD. NOTE6:In function ""DigColPsInt_InterruptNotification"", output variable ""DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08"" is going out of range." **********

Attributes

Name	Value
Compiler Install Path	$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	$(Compiler Install Path)\include
Time Unit	Cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\C1xx_DigColPs\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

Test Case 1: Metrics Test ✔

Description Test Vector Description:

TS1.1"Shortest Execution Path:
((DigColPsInt_SensInitialized_Cnt_M_lgc == TRUE) && (DigColPsInt_CurrentStepNo_Cnt_M_enum >= INIT_COMPLETE))=False"
TS1.2"Longest Execution Path:
((DigColPsInt_SensInitialized_Cnt_M_lgc == TRUE) && (DigColPsInt_CurrentStepNo_Cnt_M_enum >= INIT_COMPLETE))=True
((Status_Cnt_T_u16 & I2C_BUSBUSY) == 0U)=True
((Type_Cnt_T_u08 == D_ANGLEDATA_CNT_U08) && (DigColPsInt_PrevReqDataType_Cnt_M_u08 == D_ANGLEDATA_CNT_U08))=False
((Type_Cnt_T_u08 > D_NONE_CNT_U08) && (Type_Cnt_T_u08 <= D_STATUSREG_CNT_U08))=False"

Test Step 1.1 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	44
DigColPsInt_Buffer_Cnt_M_u08[1]	55
DigColPsInt_Buffer_Cnt_M_u08[2]	66
DigColPsInt_CurrentSlave_Cnt_M_u08	55
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_READ
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
I2c_GetStatus()	655
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	3
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	55
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	55
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	556
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	87
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	67
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	55
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	5
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	1

TEST DETAILS REPORT

DigColPsInt_StartRequest

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Name	Input Value
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3

TEST DETAILS REPORT

DigColPsInt_StartRequest

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Name	Input Value
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	44	44	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	55	55	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	66	66	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	55	55	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_READ	INIT_SENSOR2_CHECKSTAT_READ	✔
DigColPsInt_PrevReqDataType_Cnt_M_u08	0	0	✔
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1	1	✔
I2c_Send(Length_Cnt_T_u32)	0	0	✔
I2c_SetRecv(Length_Cnt_T_u32)	0	0	✔
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	0	0	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔

TEST DETAILS REPORT

DigColPsInt_StartRequest

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Name	Actual Value	Expected Value	Result
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 1.2 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_CurrentSlave_Cnt_M_u08	40
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
I2c_GetStatus()	123
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	0
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	10
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	78
target_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56
target_i2cREG1_temp.CNT	897
target_i2cREG1_temp.DRR	98
target_i2cREG1_temp.SAR	66
target_i2cREG1_temp.DXR	78
target_i2cREG1_temp.MDR	495
target_i2cREG1_temp.IVR	66
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	78
target_i2cREG1_temp.PID11	56
target_i2cREG1_temp.PID12	78
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0

Name	Input Value
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	56
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1

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Name	Input Value
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	10	10	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE	INIT_COMPLETE	✔
DigColPsInt_PrevReqDataType_Cnt_M_u08	0	0	✔
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	✔
I2c_Send(Length_Cnt_T_u32)	0	0	✔
I2c_SetRecv(Length_Cnt_T_u32)	0	0	✔
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	0	0	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	78	78	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔

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Name	Actual Value	Expected Value	Result
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78	78	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78	78	✔

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Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	✔

Test Case 2: Boundary Test

Description Test Vector Description:

TS2.1Type_Cnt_T_u08=min
TS2.2Type_Cnt_T_u08=max
TS2.3Type_Cnt_T_u08=mid
TS2.4k_ColSensorI2CAddress_Cnt_u08=min
TS2.5k_ColSensorI2CAddress_Cnt_u08=max
TS2.6k_ColSensorI2CAddress_Cnt_u08=mid
TS2.7DigColPsInt_PrevReqDataType_Cnt_M_u08=min
TS2.8DigColPsInt_PrevReqDataType_Cnt_M_u08=max
TS2.9DigColPsInt_PrevReqDataType_Cnt_M_u08=mid
TS2.10I2c_GetStatus = min
TS2.11I2c_GetStatus = max
TS2.12I2c_GetStatus = mid
TS2.13DigColPsInt_CurrentStepNo_Cnt_M_enum=min
TS2.14DigColPsInt_CurrentStepNo_Cnt_M_enum=max
TS2.15DigColPsInt_CurrentStepNo_Cnt_M_enum=mid
TS2.16DigColPsInt_SensInitialized_Cnt_M_lgc=min
TS2.17DigColPsInt_SensInitialized_Cnt_M_lgc=max
TS2.18all min
TS2.19all max

Test Step 2.1 (Repeat Count = 1)

Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_CurrentSlave_Cnt_M_u08	40
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
I2c_GetStatus()	123
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	0
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	10
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	78
target_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56
target_i2cREG1_temp.CNT	897
target_i2cREG1_temp.DRR	98
target_i2cREG1_temp.SAR	66
target_i2cREG1_temp.DXR	78
target_i2cREG1_temp.MDR	495
target_i2cREG1_temp.IVR	66
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	78
target_i2cREG1_temp.PID11	56
target_i2cREG1_temp.PID12	78
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	495

Name	Input Value
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	56
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66

Name	Input Value
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	10	10	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE	INIT_COMPLETE	✔
DigColPsInt_PrevReqDataType_Cnt_M_u08	0	0	✔
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	✔
I2c_Send(Length_Cnt_T_u32)	0	0	✔
I2c_SetRecv(Length_Cnt_T_u32)	0	0	✔
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	0	0	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	78	78	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	✔

TEST DETAILS REPORT

DigColPsInt_StartRequest

2014-10-14, 23:44:33+0530

Name	Actual Value	Expected Value	Result
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78	78	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78	78	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔

Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	✔

Test Step 2.2 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	40
DigColPsInt_Buffer_Cnt_M_u08[1]	50
DigColPsInt_Buffer_Cnt_M_u08[2]	60
DigColPsInt_CurrentSlave_Cnt_M_u08	55
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
I2c_GetStatus()	554
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	5
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	20
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.MDR	566
target_i2cREG1_temp.IVR	554
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	44

Name	Input Value
target_i2cREG1_temp.PID11	4466
target_i2cREG1_temp.PID12	44
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	0
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	567
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	44
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	4444
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	566
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	129
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	6
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	567
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	44
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	566
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	554
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	44
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	4466
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	44
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554

Name	Input Value
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	34	34	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	50	50	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	60	60	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	20	20	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG	READ_SENSOR1_SETREG	✔
DigColPsInt_PrevReqDataType_Cnt_M_u08	5	5	✔
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔

TEST DETAILS REPORT

DigColPsInt_StartRequest

2014-10-14, 23:44:33+0530

Name	Actual Value	Expected Value	Result
I2c_SetRecv(Length_Cnt_T_u32)	0	0	✔
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	0	0	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔

TEST DETAILS REPORT

DigColPsInt_StartRequest

2014-10-14, 23:44:33+0530

Name	Actual Value	Expected Value	Result
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

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Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 2.3 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	70
DigColPsInt_Buffer_Cnt_M_u08[1]	80
DigColPsInt_Buffer_Cnt_M_u08[2]	90
DigColPsInt_CurrentSlave_Cnt_M_u08	60
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE

Name	Input Value
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
I2c_GetStatus()	766
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	3
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	30
target_i2cREG1_temp.OAR	65
target_i2cREG1_temp.IMR	89
target_i2cREG1_temp.STR	67
target_i2cREG1_temp.CLKL	7
target_i2cREG1_temp.CLKH	577
target_i2cREG1_temp.CNT	88
target_i2cREG1_temp.DRR	23
target_i2cREG1_temp.SAR	65
target_i2cREG1_temp.DXR	89
target_i2cREG1_temp.MDR	7
target_i2cREG1_temp.IVR	44
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	89
target_i2cREG1_temp.PID11	577
target_i2cREG1_temp.PID12	89
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	2
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	65
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	89
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	67
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	7
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	577
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	88
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	23
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	65
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	89
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	7
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	44
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	89
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	577
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	89
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44

Name	Input Value
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89

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Name	Input Value
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	80	80	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	90	90	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	30	30	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG	READ_SENSOR1_SETREG	✔
DigColPsInt_PrevReqDataType_Cnt_M_u08	3	3	✔
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetRecv(Length_Cnt_T_u32)	0	0	✔
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	0	0	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	67	67	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔

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Name	Actual Value	Expected Value	Result
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67	67	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67	67	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔

Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔

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Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 2.4 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	3
DigColPsInt_Buffer_Cnt_M_u08[1]	6
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_CurrentSlave_Cnt_M_u08	69
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	4
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
I2c_GetStatus()	788
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	1
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	0
target_i2cREG1_temp.OAR	10
target_i2cREG1_temp.IMR	10
target_i2cREG1_temp.STR	1223
target_i2cREG1_temp.CLKL	7846
target_i2cREG1_temp.CLKH	8974
target_i2cREG1_temp.CNT	98
target_i2cREG1_temp.DRR	12
target_i2cREG1_temp.SAR	10
target_i2cREG1_temp.DXR	10
target_i2cREG1_temp.MDR	7846
target_i2cREG1_temp.IVR	55
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	10
target_i2cREG1_temp.PID11	8974
target_i2cREG1_temp.PID12	10
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	1
target_i2cREG1_temp.PSL	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	10
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	10
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	1223
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	8974
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	98
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	12
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	10
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	10
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	7846
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	55

Name	Input Value
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	10
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	8974
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	10
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	10
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10

Name	Input Value
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	8974
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	10
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	32	32	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	6	6	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	9	9	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	0	0	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG	READ_SENSOR1_SETREG	✔
DigColPsInt_PrevReqDataType_Cnt_M_u08	1	1	✔
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetRecv(Length_Cnt_T_u32)	0	0	✔
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	0	0	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔

TEST DETAILS REPORT

DigColPsInt_StartRequest

2014-10-14, 23:44:33+0530

Name	Actual Value	Expected Value	Result
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	✔

Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	✔

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Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 2.5 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	11
DigColPsInt_Buffer_Cnt_M_u08[1]	22
DigColPsInt_Buffer_Cnt_M_u08[2]	33
DigColPsInt_CurrentSlave_Cnt_M_u08	33
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
I2c_GetStatus()	887
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	2
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	127
target_i2cREG1_temp.OAR	34
target_i2cREG1_temp.IMR	24
target_i2cREG1_temp.STR	455
target_i2cREG1_temp.CLKL	847
target_i2cREG1_temp.CLKH	987
target_i2cREG1_temp.CNT	487
target_i2cREG1_temp.DRR	34
target_i2cREG1_temp.SAR	34
target_i2cREG1_temp.DXR	24
target_i2cREG1_temp.MDR	847
target_i2cREG1_temp.IVR	56

Name	Input Value
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	24
target_i2cREG1_temp.PID11	987
target_i2cREG1_temp.PID12	24
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	3
target_i2cREG1_temp.DIN	3
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	2
target_i2cREG1_temp.CLR	3
target_i2cREG1_temp.ODR	3
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	34
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	24
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	455
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	847
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	987
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	487
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	34
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	34
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	24
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	847
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	56
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	24
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	987
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	24
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	34
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	24
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	455
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	847
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	987
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	487
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	34
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	34
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	24

TEST DETAILS REPORT

DigColPsInt_StartRequest

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Name	Input Value
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	847
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	56
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	24
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	987
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	24
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	34
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	24
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	455
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	847
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	987
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	487
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	34
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	34
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	24
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	847
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	56
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	24
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	987
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	24
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	30	30	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	22	22	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	33	33	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG	READ_SENSOR1_SETREG	✔
DigColPsInt_PrevReqDataType_Cnt_M_u08	2	2	✔

TEST DETAILS REPORT

DigColPsInt_StartRequest

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Name	Actual Value	Expected Value	Result
DigColPsInt_SkipRegisterWrite_Cnt_M_Igc	0	0	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetRecv(Length_Cnt_T_u32)	0	0	✔
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	0	0	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	455	455	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455	455	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	455	455	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	✔

TEST DETAILS REPORT

DigColPsInt_StartRequest

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Name	Actual Value	Expected Value	Result
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	455	455	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455	455	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	✔

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Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 2.6 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	44
DigColPsInt_Buffer_Cnt_M_u08[1]	55
DigColPsInt_Buffer_Cnt_M_u08[2]	66

Name	Input Value
DigColPsInt_CurrentSlave_Cnt_M_u08	55
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
I2c_GetStatus()	655
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	3
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	55
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	55
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	556
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	87
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	67
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	55
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	5
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66

Name	Input Value
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67

Name	Input Value
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	55	55	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	66	66	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	55	55	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG	READ_SENSOR1_SETREG	✔
DigColPsInt_PrevReqDataType_Cnt_M_u08	3	3	✔
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetRecv(Length_Cnt_T_u32)	0	0	✔
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	0	0	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔

TEST DETAILS REPORT

DigColPsInt_StartRequest

2014-10-14, 23:44:33+0530

Name	Actual Value	Expected Value	Result
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	

Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

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Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 2.7 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	66
DigColPsInt_Buffer_Cnt_M_u08[1]	77
DigColPsInt_Buffer_Cnt_M_u08[2]	88
DigColPsInt_CurrentSlave_Cnt_M_u08	11
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
I2c_GetStatus()	123
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	1
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	40
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	78
target_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56
target_i2cREG1_temp.CNT	897
target_i2cREG1_temp.DRR	98
target_i2cREG1_temp.SAR	66
target_i2cREG1_temp.DXR	78
target_i2cREG1_temp.MDR	495
target_i2cREG1_temp.IVR	66
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	78
target_i2cREG1_temp.PID11	56
target_i2cREG1_temp.PID12	78
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	78

Name	Input Value
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	56
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98

TEST DETAILS REPORT

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Name	Input Value
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	32	32	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	77	77	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	88	88	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	40	40	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG	READ_SENSOR1_SETREG	✔
DigColPsInt_PrevReqDataType_Cnt_M_u08	1	1	✔
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetRecv(Length_Cnt_T_u32)	0	0	✔
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	0	0	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	78	78	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	✔

TEST DETAILS REPORT

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Name	Actual Value	Expected Value	Result
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78	78	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78	78	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔

Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 2.8 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	40
DigColPsInt_Buffer_Cnt_M_u08[1]	50
DigColPsInt_Buffer_Cnt_M_u08[2]	60
DigColPsInt_CurrentSlave_Cnt_M_u08	12
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
I2c_GetStatus()	766
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	1
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	55
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44

Name	Input Value
target_i2cREG1_temp.MDR	566
target_i2cREG1_temp.IVR	554
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	44
target_i2cREG1_temp.PID11	4466
target_i2cREG1_temp.PID12	44
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	0
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	567
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	44
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	4444
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	566
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	129
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	6
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	567
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	44
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	566
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	554
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	44
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	4466
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	44
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6

Name	Input Value
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	32	32	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	50	50	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	60	60	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	55	55	✔

TEST DETAILS REPORT

DigColPsInt_StartRequest

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Name	Actual Value	Expected Value	Result
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG	READ_SENSOR1_SETREG	✔
DigColPsInt_PrevReqDataType_Cnt_M_u08	1	1	✔
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetRecv(Length_Cnt_T_u32)	0	0	✔
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	0	0	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	

Name	Actual Value	Expected Value	Result
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 2.9 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	70

Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[1]	80
DigColPsInt_Buffer_Cnt_M_u08[2]	90
DigColPsInt_CurrentSlave_Cnt_M_u08	45
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
I2c_GetStatus()	886
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	1
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	60
target_i2cREG1_temp.OAR	65
target_i2cREG1_temp.IMR	89
target_i2cREG1_temp.STR	67
target_i2cREG1_temp.CLKL	7
target_i2cREG1_temp.CLKH	577
target_i2cREG1_temp.CNT	88
target_i2cREG1_temp.DRR	23
target_i2cREG1_temp.SAR	65
target_i2cREG1_temp.DXR	89
target_i2cREG1_temp.MDR	7
target_i2cREG1_temp.IVR	44
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	89
target_i2cREG1_temp.PID11	577
target_i2cREG1_temp.PID12	89
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	2
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	65
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	89
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	67
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	7
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	577
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	88
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	23
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	65
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	89
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	7
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	44
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	89
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	577
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	89
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23

Name	Input Value
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577

Name	Input Value
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	32	32	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	80	80	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	90	90	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	60	60	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG	READ_SENSOR1_SETREG	✔
DigColPsInt_PrevReqDataType_Cnt_M_u08	1	1	✔
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetRecv(Length_Cnt_T_u32)	0	0	✔
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	0	0	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	67	67	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔

TEST DETAILS REPORT

DigColPsInt_StartRequest

2014-10-14, 23:44:33+0530

Name	Actual Value	Expected Value	Result
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67	67	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67	67	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	✔

Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 2.10 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	3
DigColPsInt_Buffer_Cnt_M_u08[1]	6
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_CurrentSlave_Cnt_M_u08	77
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
I2c_GetStatus()	0
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	1
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	69
target_i2cREG1_temp.OAR	54
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	8
target_i2cREG1_temp.CLKL	554
target_i2cREG1_temp.CLKH	344
target_i2cREG1_temp.CNT	123
target_i2cREG1_temp.DRR	45
target_i2cREG1_temp.SAR	54
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	554
target_i2cREG1_temp.IVR	788
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	344
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	3
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	3
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	1
target_i2cREG1_temp.PSL	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	54
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	8
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	554
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	344
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	123
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	45

Name	Input Value
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	54
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	554
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	788
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	344
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344

TEST DETAILS REPORT

DigColPsInt_StartRequest

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Name	Input Value
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	3	3	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	6	6	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	9	9	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	69	69	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_GETDATA	READ_SENSOR1_GETDATA	✔
DigColPsInt_PrevReqDataType_Cnt_M_u08	1	1	✔
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1	1	✔
I2c_SetRecv(Length_Cnt_T_u32)	2	2	✔
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	8	8	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	✔

TEST DETAILS REPORT

DigColPsInt_StartRequest

2014-10-14, 23:44:33+0530

Name	Actual Value	Expected Value	Result
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8	8	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8	8	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8	8	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔

Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8	8	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	✔
SetupRead	1	SetupRead	1	✔
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	✔
I2c_SetRecv	1	I2c_SetRecv	1	✔

Test Step 2.11 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	11
DigColPsInt_Buffer_Cnt_M_u08[1]	22
DigColPsInt_Buffer_Cnt_M_u08[2]	33
DigColPsInt_CurrentSlave_Cnt_M_u08	65
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
I2c_GetStatus()	65535
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	2
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	33
target_i2cREG1_temp.OAR	3
target_i2cREG1_temp.IMR	100
target_i2cREG1_temp.STR	7788
target_i2cREG1_temp.CLKL	2767
target_i2cREG1_temp.CLKH	556
target_i2cREG1_temp.CNT	564
target_i2cREG1_temp.DRR	88
target_i2cREG1_temp.SAR	3
target_i2cREG1_temp.DXR	100

Name	Input Value
target_i2cREG1_temp.MDR	2767
target_i2cREG1_temp.IVR	9
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	100
target_i2cREG1_temp.PID11	556
target_i2cREG1_temp.PID12	100
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	3
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	3
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	100
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	7788
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	556
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	564
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	88
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	100
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	2767
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	9
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	100
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	556
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	100
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88

TEST DETAILS REPORT

DigColPsInt_StartRequest

2014-10-14, 23:44:33+0530

Name	Input Value
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	11	11	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	22	22	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	33	33	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	65	65	✔

TEST DETAILS REPORT

DigColPsInt_StartRequest

2014-10-14, 23:44:33+0530

Name	Actual Value	Expected Value	Result
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE	INIT_COMPLETE	✔
DigColPsInt_PrevReqDataType_Cnt_M_u08	2	2	✔
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔

Name	Actual Value	Expected Value	Result
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	✔

Test Step 2.12 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	44
DigColPsInt_Buffer_Cnt_M_u08[1]	55
DigColPsInt_Buffer_Cnt_M_u08[2]	66
DigColPsInt_CurrentSlave_Cnt_M_u08	78
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_SETREG
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1

Name	Input Value
I2c_GetStatus()	4000
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	3
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	55
target_i2cREG1_temp.OAR	678
target_i2cREG1_temp.IMR	45
target_i2cREG1_temp.STR	66
target_i2cREG1_temp.CLKL	56
target_i2cREG1_temp.CLKH	6788
target_i2cREG1_temp.CNT	7878
target_i2cREG1_temp.DRR	12
target_i2cREG1_temp.SAR	678
target_i2cREG1_temp.DXR	45
target_i2cREG1_temp.MDR	56
target_i2cREG1_temp.IVR	778
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	45
target_i2cREG1_temp.PID11	6788
target_i2cREG1_temp.PID12	45
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	678
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	45
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	56
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	6788
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	7878
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	12
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	678
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	45
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	56
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	778
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	45
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	6788
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	45
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	678
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	45
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	56
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	6788
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	7878
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	678
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	45
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	56
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	778
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	45
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	6788

Name	Input Value
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	45
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	678
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	45
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	56
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	6788
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	7878
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	678
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	45
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	56
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	778
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	45
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	6788
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	45
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	678
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	45
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	56
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	6788
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	7878
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	678
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	45
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	56
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	778
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	45
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	6788
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	45
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	678
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	45
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	56
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	6788
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	7878
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	678
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	45
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	56
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	778
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1

TEST DETAILS REPORT

DigColPsInt_StartRequest

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Name	Input Value
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	45
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	6788
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	45
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	44	44	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	55	55	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	66	66	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	78	78	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_SETREG	INIT_SENSOR1_READEXTERR_SETREG	✔
DigColPsInt_PrevReqDataType_Cnt_M_u08	3	3	✔
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	678	678	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	45	45	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	56	56	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	7878	7878	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	678	678	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	45	45	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	56	56	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	778	778	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	45	45	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	6788	6788	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	45	45	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	678	678	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	45	45	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	56	56	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	7878	7878	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	678	678	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	45	45	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	56	56	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	778	778	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	45	45	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	6788	6788	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	45	45	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	678	678	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	45	45	✔

TEST DETAILS REPORT

DigColPsInt_StartRequest

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Name	Actual Value	Expected Value	Result
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	56	56	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	7878	7878	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	678	678	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	45	45	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	56	56	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	778	778	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	45	45	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	6788	6788	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	45	45	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	678	678	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	45	45	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	56	56	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	7878	7878	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	678	678	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	45	45	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	56	56	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	778	778	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	45	45	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	6788	6788	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	45	45	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	678	678	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	45	45	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	56	56	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	7878	7878	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	678	678	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	45	45	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	56	56	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	778	778	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	45	45	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	6788	6788	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	45	45	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	✔

Name	Input Value
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0

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Name	Input Value
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	40	40	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_NOT_INITIALIZED	INIT_NOT_INITIALIZED	✔
DigColPsInt_PrevReqDataType_Cnt_M_u08	1	1	✔
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	78	78	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	✔

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Name	Actual Value	Expected Value	Result
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78	78	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78	78	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	✔

Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.14 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	40
DigColPsInt_Buffer_Cnt_M_u08[1]	50
DigColPsInt_Buffer_Cnt_M_u08[2]	60
DigColPsInt_CurrentSlave_Cnt_M_u08	55
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
I2c_GetStatus()	554
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	4
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	20
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.MDR	566
target_i2cREG1_temp.IVR	554
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	44
target_i2cREG1_temp.PID11	4466
target_i2cREG1_temp.PID12	44
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	0
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	567
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	44
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	4444
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	566

Name	Input Value
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	129
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	6
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	567
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	44
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	566
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	554
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	44
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	4466
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	44
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44

TEST DETAILS REPORT

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Name	Input Value
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	38	38	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	50	50	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	60	60	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	20	20	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG	READ_SENSOR1_SETREG	✔
DigColPsInt_PrevReqDataType_Cnt_M_u08	4	4	✔
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔

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Name	Actual Value	Expected Value	Result
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔

Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

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Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 2.15 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	70
DigColPsInt_Buffer_Cnt_M_u08[1]	80
DigColPsInt_Buffer_Cnt_M_u08[2]	90
DigColPsInt_CurrentSlave_Cnt_M_u08	60
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
I2c_GetStatus()	766
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	3
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	30
target_i2cREG1_temp.OAR	65
target_i2cREG1_temp.IMR	89
target_i2cREG1_temp.STR	67
target_i2cREG1_temp.CLKL	7
target_i2cREG1_temp.CLKH	577
target_i2cREG1_temp.CNT	88
target_i2cREG1_temp.DRR	23

Name	Input Value
target_i2cREG1_temp.SAR	65
target_i2cREG1_temp.DXR	89
target_i2cREG1_temp.MDR	7
target_i2cREG1_temp.IVR	44
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	89
target_i2cREG1_temp.PID11	577
target_i2cREG1_temp.PID12	89
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	2
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	65
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	89
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	67
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	7
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	577
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	88
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	23
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	65
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	89
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	7
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	44
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	89
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	577
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	89
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577

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Name	Input Value
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	80	80	✔

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DigColPsInt_StartRequest

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Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[2]	90	90	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	30	30	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG	READ_SENSOR1_SETREG	✔
DigColPsInt_PrevReqDataType_Cnt_M_u08	3	3	✔
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	67	67	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67	67	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔

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DigColPsInt_StartRequest

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Name	Actual Value	Expected Value	Result
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67	67	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 2.16 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	44

Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[1]	55
DigColPsInt_Buffer_Cnt_M_u08[2]	66
DigColPsInt_CurrentSlave_Cnt_M_u08	55
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_READ
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
I2c_GetStatus()	655
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	3
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	55
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	55
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	556
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	87
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	67
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	55
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	5
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67

Name	Input Value
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204

TEST DETAILS REPORT

DigColPsInt_StartRequest

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Name	Input Value
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	44	44	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	55	55	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	66	66	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	55	55	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_READ	INIT_SENSOR2_CHECKSTAT_READ	✔
DigColPsInt_PrevReqDataType_Cnt_M_u08	0	0	✔
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔

TEST DETAILS REPORT

DigColPsInt_StartRequest

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Name	Actual Value	Expected Value	Result
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔

Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.17 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	66
DigColPsInt_Buffer_Cnt_M_u08[1]	77
DigColPsInt_Buffer_Cnt_M_u08[2]	88
DigColPsInt_CurrentSlave_Cnt_M_u08	11
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADADDRREG_SENDCMD
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
I2c_GetStatus()	123
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	1
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	40
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	78
target_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56
target_i2cREG1_temp.CNT	897
target_i2cREG1_temp.DRR	98
target_i2cREG1_temp.SAR	66
target_i2cREG1_temp.DXR	78
target_i2cREG1_temp.MDR	495
target_i2cREG1_temp.IVR	66
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	78
target_i2cREG1_temp.PID11	56
target_i2cREG1_temp.PID12	78
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	56

Name	Input Value
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0

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Name	Input Value
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	66	66	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	77	77	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	88	88	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	11	11	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR2 EXTREADADDRREG SEN	INIT SENSOR2 EXTREADADDRREG SEN	✔
DigColPsInt_PrevReqDataType_Cnt_M_u08	0	0	✔
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	78	78	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	✔

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Name	Actual Value	Expected Value	Result
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78	78	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78	78	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	✔

Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.18 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	0
DigColPsInt_Buffer_Cnt_M_u08[1]	0
DigColPsInt_Buffer_Cnt_M_u08[2]	0
DigColPsInt_CurrentSlave_Cnt_M_u08	0
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_NOT_INITIALIZED
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
I2c_GetStatus()	0
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	0
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	0
target_i2cREG1_temp.OAR	0
target_i2cREG1_temp.IMR	0
target_i2cREG1_temp.STR	0
target_i2cREG1_temp.CLKL	0
target_i2cREG1_temp.CLKH	0
target_i2cREG1_temp.CNT	0
target_i2cREG1_temp.DRR	0
target_i2cREG1_temp.SAR	0
target_i2cREG1_temp.DXR	0
target_i2cREG1_temp.MDR	0
target_i2cREG1_temp.IVR	0
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	0
target_i2cREG1_temp.PID11	0
target_i2cREG1_temp.PID12	0
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0

Name	Input Value
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	0
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0

Name	Input Value
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	0	0	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	0	0	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	0	0	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_NOT_INITIALIZED	INIT_NOT_INITIALIZED	✔
DigColPsInt_PrevReqDataType_Cnt_M_u08	0	0	✔
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	0	0	✔

TEST DETAILS REPORT

DigColPsInt_StartRequest

2014-10-14, 23:44:33+0530

Name	Actual Value	Expected Value	Result
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	0	0	✔

Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.19 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	255
DigColPsInt_Buffer_Cnt_M_u08[1]	255
DigColPsInt_Buffer_Cnt_M_u08[2]	255
DigColPsInt_CurrentSlave_Cnt_M_u08	127
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
I2c_GetStatus()	65535
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	5
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	127
target_i2cREG1_temp.OAR	1023
target_i2cREG1_temp.IMR	255
target_i2cREG1_temp.STR	32767

Name	Input Value
target_i2cREG1_temp.CLKL	65535
target_i2cREG1_temp.CLKH	65535
target_i2cREG1_temp.CNT	65535
target_i2cREG1_temp.DRR	255
target_i2cREG1_temp.SAR	1023
target_i2cREG1_temp.DXR	255
target_i2cREG1_temp.MDR	65535
target_i2cREG1_temp.IVR	4095
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	255
target_i2cREG1_temp.PID11	65535
target_i2cREG1_temp.PID12	255
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	3
target_i2cREG1_temp.DIN	3
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	3
target_i2cREG1_temp.ODR	3
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	1023
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	255
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	32767
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	65535
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	65535
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	65535
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	255
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	1023
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	255
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	65535
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	4095
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	255
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	65535
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	255
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	255
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	32767
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	65535
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	65535
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	255
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	1023
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	255
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	65535
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	4095
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	255
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	65535
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	255
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	1023

Name	Input Value
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	255
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	32767
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	65535
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	65535
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	65535
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	255
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	1023
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	255
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	65535
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	4095
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	255
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	65535
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	255
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	1023
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	255
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	32767
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	65535
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	65535
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	65535
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	255
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	1023
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	255
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	65535
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	4095
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	255
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	65535
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	255
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	1023
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	255
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	32767
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	65535
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	65535
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	65535
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	255
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	1023
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	255
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	65535
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	4095
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	255
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	65535
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	255
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3

TEST DETAILS REPORT

DigColPsInt_StartRequest

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Name	Input Value		
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3		
Name	**Actual Value**	**Expected Value**	**Result**
DigColPsInt_Buffer_Cnt_M_u08[0]	255	255	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	255	255	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	255	255	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE	READ_COMPLETE	✔
DigColPsInt_PrevReqDataType_Cnt_M_u08	5	5	✔
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	1023	1023	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	255	255	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	32767	32767	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	65535	65535	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	255	255	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	1023	1023	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	255	255	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	65535	65535	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	4095	4095	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	255	255	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	65535	65535	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	255	255	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023	1023	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	255	255	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	32767	32767	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	65535	65535	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	255	255	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	1023	1023	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	255	255	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	65535	65535	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	4095	4095	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	255	255	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	65535	65535	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	255	255	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	1023	1023	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	255	255	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	32767	32767	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	65535	65535	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	255	255	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	1023	1023	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	255	255	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	65535	65535	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	4095	4095	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	255	255	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	65535	65535	✔

TEST DETAILS REPORT

DigColPsInt_StartRequest

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Name	Actual Value	Expected Value	Result
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	255	255	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	1023	1023	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	255	255	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	32767	32767	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	65535	65535	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	255	255	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	1023	1023	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	255	255	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	65535	65535	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	4095	4095	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	255	255	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	65535	65535	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	255	255	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	1023	1023	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	255	255	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	32767	32767	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	65535	65535	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	255	255	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	1023	1023	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	255	255	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	65535	65535	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	4095	4095	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	255	255	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	65535	65535	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	255	255	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
I2c_GetStatus	1	I2c_GetStatus	1	✔

Test Case 3: Path Test

Description Test Vector Description:

TS3.1"((DigColPsInt_SensInitialized_Cnt_M_lgc == TRUE) && (DigColPsInt_CurrentStepNo_Cnt_M_enum >= INIT_COMPLETE))=True
((Status_Cnt_T_u16 & I2C_BUSBUSY) == 0U)=True
((Type_Cnt_T_u08 == D_ANGLEDATA_CNT_U08) && (DigColPsInt_PrevReqDataType_Cnt_M_u08 == D_ANGLEDATA_CNT_U08))=False
((Type_Cnt_T_u08 > D_NONE_CNT_U08) && (Type_Cnt_T_u08 <= D_STATUSREG_CNT_U08))=False"
TS3.2"((DigColPsInt_SensInitialized_Cnt_M_lgc == TRUE) && (DigColPsInt_CurrentStepNo_Cnt_M_enum >= INIT_COMPLETE))=True
((Status_Cnt_T_u16 & I2C_BUSBUSY) == 0U)=True
((Type_Cnt_T_u08 == D_ANGLEDATA_CNT_U08) && (DigColPsInt_PrevReqDataType_Cnt_M_u08 == D_ANGLEDATA_CNT_U08))=False
((Type_Cnt_T_u08 > D_NONE_CNT_U08) && (Type_Cnt_T_u08 <= D_STATUSREG_CNT_U08))=True"
TS3.3"((DigColPsInt_SensInitialized_Cnt_M_lgc == TRUE) && (DigColPsInt_CurrentStepNo_Cnt_M_enum >= INIT_COMPLETE))=True
((Status_Cnt_T_u16 & I2C_BUSBUSY) == 0U)=True
((Type_Cnt_T_u08 == D_ANGLEDATA_CNT_U08) && (DigColPsInt_PrevReqDataType_Cnt_M_u08 == D_ANGLEDATA_CNT_U08))=True"
TS3.4"((DigColPsInt_SensInitialized_Cnt_M_lgc == TRUE) && (DigColPsInt_CurrentStepNo_Cnt_M_enum >= INIT_COMPLETE))=True
((Status_Cnt_T_u16 & I2C_BUSBUSY) == 0U)=False"
TS3.5((DigColPsInt_SensInitialized_Cnt_M_lgc == TRUE) && (DigColPsInt_CurrentStepNo_Cnt_M_enum >= INIT_COMPLETE))=False

Test Step 3.1 (Repeat Count = 1)

Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_CurrentSlave_Cnt_M_u08	40
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
I2c_GetStatus()	123
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	0
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	10
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	78
target_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56
target_i2cREG1_temp.CNT	897
target_i2cREG1_temp.DRR	98
target_i2cREG1_temp.SAR	66
target_i2cREG1_temp.DXR	78
target_i2cREG1_temp.MDR	495
target_i2cREG1_temp.IVR	66
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	78
target_i2cREG1_temp.PID11	56
target_i2cREG1_temp.PID12	78
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	56

Name	Input Value
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	78
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0

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Name	Input Value
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	10	10	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE	INIT_COMPLETE	✔
DigColPsInt_PrevReqDataType_Cnt_M_u08	0	0	✔
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	78	78	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	✔

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Name	Actual Value	Expected Value	Result
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78	78	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78	78	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	✔

Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	✔

Test Step 3.2 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	40
DigColPsInt_Buffer_Cnt_M_u08[1]	50
DigColPsInt_Buffer_Cnt_M_u08[2]	60
DigColPsInt_CurrentSlave_Cnt_M_u08	55
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
I2c_GetStatus()	554
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	5
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	20
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.MDR	566
target_i2cREG1_temp.IVR	554
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	44
target_i2cREG1_temp.PID11	4466
target_i2cREG1_temp.PID12	44
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1

Name	Input Value
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	0
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	567
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	44
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	4444
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	566
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	129
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	6
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	567
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	44
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	566
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	554
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	44
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	4466
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	44
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0

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Name	Input Value
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	34	34	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	50	50	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	60	60	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	20	20	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG	READ_SENSOR1_SETREG	✔
DigColPsInt_PrevReqDataType_Cnt_M_u08	5	5	✔
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	✔

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Name	Actual Value	Expected Value	Result
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔

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Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

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Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 3.3 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	3
DigColPsInt_Buffer_Cnt_M_u08[1]	6
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_CurrentSlave_Cnt_M_u08	77
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
I2c_GetStatus()	0
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	1

Name	Input Value
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	69
target_i2cREG1_temp.OAR	54
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	8
target_i2cREG1_temp.CLKL	554
target_i2cREG1_temp.CLKH	344
target_i2cREG1_temp.CNT	123
target_i2cREG1_temp.DRR	45
target_i2cREG1_temp.SAR	54
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	554
target_i2cREG1_temp.IVR	788
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	344
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	3
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	3
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	1
target_i2cREG1_temp.PSL	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	54
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	8
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	554
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	344
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	123
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	45
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	54
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	554
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	788
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	344
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3

Name	Input Value
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2

TEST DETAILS REPORT

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Name	Input Value
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	3	3	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	6	6	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	9	9	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	69	69	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_GETDATA	READ_SENSOR1_GETDATA	✔
DigColPsInt_PrevReqDataType_Cnt_M_u08	1	1	✔
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1	1	✔
I2c_SetRecv(Length_Cnt_T_u32)	2	2	✔
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	8	8	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8	8	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8	8	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45	45	✔

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Name	Actual Value	Expected Value	Result
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8	8	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8	8	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
I2c_GetStatus	1	I2c_GetStatus	1	✔
SetupRead	1	SetupRead	1	✔
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	✔
I2c_SetRecv	1	I2c_SetRecv	1	✔

Test Step 3.4 (Repeat Count = 1)	✔
Name	**Input Value**
DigColPsInt_Buffer_Cnt_M_u08[0]	11
DigColPsInt_Buffer_Cnt_M_u08[1]	22
DigColPsInt_Buffer_Cnt_M_u08[2]	33
DigColPsInt_CurrentSlave_Cnt_M_u08	65
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_SensInitialized_Cnt_M_lgc	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
I2c_GetStatus()	65535
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	2
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	33
target_i2cREG1_temp.OAR	3
target_i2cREG1_temp.IMR	100
target_i2cREG1_temp.STR	7788
target_i2cREG1_temp.CLKL	2767
target_i2cREG1_temp.CLKH	556
target_i2cREG1_temp.CNT	564
target_i2cREG1_temp.DRR	88
target_i2cREG1_temp.SAR	3
target_i2cREG1_temp.DXR	100
target_i2cREG1_temp.MDR	2767
target_i2cREG1_temp.IVR	9
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	100
target_i2cREG1_temp.PID11	556
target_i2cREG1_temp.PID12	100
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	3
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	3
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	100
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	7788
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	556
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	564
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	88
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	100
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	2767
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	9
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	100
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	556
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	100
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	3

Name	Input Value
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0

TEST DETAILS REPORT

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Name	Input Value
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	11	11	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	22	22	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	33	33	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	65	65	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE	INIT_COMPLETE	✔
DigColPsInt_PrevReqDataType_Cnt_M_u08	2	2	✔
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	88	✔

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Name	Actual Value	Expected Value	Result
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔

Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
I2c_GetStatus	1	I2c_GetStatus	1	✔

Test Step 3.5 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	44
DigColPsInt_Buffer_Cnt_M_u08[1]	55
DigColPsInt_Buffer_Cnt_M_u08[2]	66
DigColPsInt_CurrentSlave_Cnt_M_u08	55
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_READ
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt_SensInitialized_Cnt_M_lgc	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
I2c_GetStatus()	655
I2c_GetStatus(I2cRegPtr_Cnt_T_str)	tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	tgt_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
Type_Cnt_T_u08	3
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	55
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	55

Name	Input Value
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	556
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	87
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	67
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	55
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	5
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	1
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	2
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3

TEST DETAILS REPORT

DigColPsInt_StartRequest

2014-10-14, 23:44:33+0530

Name	Input Value
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	44	44	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	55	55	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	66	66	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	55	55	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_READ	INIT_SENSOR2_CHECKSTAT_READ	✔
DigColPsInt_PrevReqDataType_Cnt_M_u08	0	0	✔
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔

TEST DETAILS REPORT

DigColPsInt_StartRequest

2014-10-14, 23:44:33+0530

Name	Actual Value	Expected Value	Result
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_GetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔

TEST DETAILS REPORT

DigColPsInt_StartRequest

2014-10-14, 23:44:33+0530

Name	Actual Value	Expected Value	Result
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
tgt_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

	DigColPsInt
	DigColPsInt
	DigColPsInt_GetCustData

100 %
100 %

	1
	1
	0
	0

	D:\Synergy_Work_Area\C1xx_DigColPs
	D:\Synergy_Work_Area\C1xx_DigColPs\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
	TI TMS 570 PLS UDE (Default)
	Unit Test
	$(PROJECTROOT)\DigColPs\src\Sa_DigColPsInt.c
	-D_DATA_ACCESS= -Dconst= -DSTATIC= -D__inline= -I$(PROJECTROOT)\DigColPs\utp\contract -I$(PROJECTROOT)\DigColPs\utp\contract\Sa_DigColPs -I$(PROJECTROOT)\DigColPs\include -I$(PROJECTROOT)\NxtrLib\include -I$(PROJECTROOT)\StdDef\include -I$(PROJECTROOT)\StdDef\include\TMS570_HerculesRegs -I$(Compiler Install Path)\include

Module 'DigColPsInt'	**********Unit Test Descrption********** Name of Tester:Priti Mangalekar Code File(s) Under Test:Sa_DigColPsInt.c Code File(s) Version:7 Module Design Document:DigColPsInt_MDD.docx Module Design Document Version:8 Data Dictionary Version:9 Unit Test Plan Version:2 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.30 Total FLASH Used (Bytes):N/A Total RAM Used (Bytes):N/A Total CALS Used (Bytes):N/A Special Test Requirements: Test Date:10/13/2014 Comments: NOTE 1: In """"DigColPsInt_StartRequest"""" function, path """"(Type_Cnt_T_u08 > D_NONE_CNT_U08) = TRUE && (Type_Cnt_T_u08 <= D_STATUSREG_CNT_U08) = FALSE"""" cannot be covered because range of """"Type_Cnt_T_u08"""" is '0-5' and value of """"D_STATUSREG_CNT_U08"""" is '34'. NOTE2: In function ""DigColPsInt_GetData"",""DigColPsInt_StartRequest"" and ""DigColPsInt_InterruptNotification"" values for """"I2c_Send(Length_Cnt_T_u32)"""", """"I2c_SetRecv(Length_Cnt_T_u32)"""", """"I2c_SetStatus(Status_Cnt_T_u16)"""", """"I2c_SetupMasterReceive(DataLength_Cnt_T_u16)"""" and I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) are ignored in few vectors as they are taking garbage value when they are not updated with expected value in particular vector. NOTE3: The return value of """"DigColPsInt_GetData"""" function is going out of range, anomaly """"6156"""" is raised for the same. NOTE4:Range of DigColPsInt_CurrentStepNo_Cnt_M_enum is considered as 0 to 36, as enum DigColPsInt_CurrentStepNo_Cnt_M_enum is of type CommStepType which is of 37 elements. NOTE5:In function ""DigColPsInt_InterruptNotification"", path ""Case I2C_RECV_OVERRUN: True"" cannot be covered because range of ""Flags_Cnt_T_b16"" is 0 to 64 given in MDD. NOTE6:In function ""DigColPsInt_InterruptNotification"", output variable ""DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08"" is going out of range." **********

Compiler Install Path	$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	$(Compiler Install Path)\include
Time Unit	Cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\C1xx_DigColPs\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

Test Vector Description:

TS1.1DigColPsInt_I2CHwCustData_Uls_M_u16=>Min
TS1.2DigColPsInt_I2CHwCustData_Uls_M_u16=>Max
TS1.3DigColPsInt_I2CHwCustData_Uls_M_u16=Pos

DigColPsInt_I2CHwCustData_Uls_M_u16	0		
DigColPsInt_GetCustData()	0	0	✔

DigColPsInt_I2CHwCustData_Uls_M_u16	511		
DigColPsInt_GetCustData()	511	511	✔

DigColPsInt_I2CHwCustData_Uls_M_u16	124		
DigColPsInt_GetCustData()	124	124	✔

TEST DETAILS REPORT

DigColPsInt_Init

2014-10-14, 23:36:07+0530

Project	DigColPsInt
Module	DigColPsInt
Test Object	DigColPsInt_Init

Instrumentation: Test Object Only

Statement (C0) Coverage	100 %
Branch (C1) Coverage	100 %

Statistics

Total Testcases	1
Successful	1
Failed	0
Not Executed	0

Module Properties

Project Root Directory	D:\Synergy_Work_Area\C1xx_DigColPs
Configuration File	D:\Synergy_Work_Area\C1xx_DigColPs\UnitTestEnv\config\TMS570_GCC_UDE_CCS4_Config.xml
Target Environment	TI TMS 570 PLS UDE (Default)
Kind of Test	Unit Test
Linker Options	
Source File(s)	
File	$(PROJECTROOT)\DigColPs\src\Sa_DigColPsInt.c
Compiler Options	-D_DATA_ACCESS= -Dconst= -DSTATIC= -D__inline= -I$(PROJECTROOT)\DigColPs\utp\contract -I$(PROJECTROOT)\DigColPs\utp\contract\Sa_DigColPs -I$(PROJECTROOT)\DigColPs\include -I$(PROJECTROOT)\NxtrLib\include -I$(PROJECTROOT)\StdDef\include -I$(PROJECTROOT)\StdDef\include\TMS570_HerculesRegs -I$(Compiler Install Path)\include

Comments/Description/Specification	
Name	**Text**

Module 'DigColPsInt'	**********Unit Test Descrption********** Name of Tester:Priti Mangalekar Code File(s) Under Test:Sa_DigColPsInt.c Code File(s) Version:7 Module Design Document:DigColPsInt_MDD.docx Module Design Document Version:8 Data Dictionary Version:9 Unit Test Plan Version:2 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.30 Total FLASH Used (Bytes):N/A Total RAM Used (Bytes):N/A Total CALS Used (Bytes):N/A Special Test Requirements: Test Date:10/13/2014 Comments: NOTE 1: In """"DigColPsInt_StartRequest"""" function, path """"(Type_Cnt_T_u08 > D_NONE_CNT_U08) = TRUE && (Type_Cnt_T_u08 <= D_STATUSREG_CNT_U08) = FALSE"""" cannot be covered because range of """"Type_Cnt_T_u08"""" is '0-5' and value of """"D_STATUSREG_CNT_U08"""" is '34'. NOTE2: In function ""DigColPsInt_GetData"",""DigColPsInt_StartRequest"" and ""DigColPsInt_InterruptNotification"" values for """"I2c_Send(Length_Cnt_T_u32)"""", """"I2c_SetRecv(Length_Cnt_T_u32)"""", """"I2c_SetStatus(Status_Cnt_T_u16)"""", """"I2c_SetupMasterReceive(DataLength_Cnt_T_u16)"""" and I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) are ignored in few vectors as they are taking garbage value when they are not updated with expected value in particular vector. NOTE3: The return value of """"DigColPsInt_GetData"""" function is going out of range, anomaly """"6156"""" is raised for the same. NOTE4:Range of DigColPsInt_CurrentStepNo_Cnt_M_enum is considered as 0 to 36, as enum DigColPsInt_CurrentStepNo_Cnt_M_enum is of type CommStepType which is of 37 elements. NOTE5:In function ""DigColPsInt_InterruptNotification"", path ""Case I2C_RECV_OVERRUN: True"" cannot be covered because range of ""Flags_Cnt_T_b16"" is 0 to 64 given in MDD. NOTE6:In function ""DigColPsInt_InterruptNotification"", output variable ""DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08"" is going out of range." **********

Attributes

Name	Value
Compiler Install Path	$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	$(Compiler Install Path)\include
Time Unit	Cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\C1xx_DigColPs\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

Test Case 1: Boundary Test ✔

Description Test Vector Description:

TS1.1GetSystemTime_mS_u32=min
TS1.2GetSystemTime_mS_u32=max
TS1.3GetSystemTime_mS_u32=mid
TS1.4All min
TS1.5All max

Test Step 1.1 (Repeat Count = 1) ✔

Name	Input Value
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Enable(I2cRegPtr_Cnt_T_str)	target_I2c_Enable_I2cRegPtr_Cnt_T_str
I2c_EnableNotification(I2cRegPtr_Cnt_T_str)	target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str
I2c_Init(I2cRegPtr_Cnt_T_str)	target_I2c_Init_I2cRegPtr_Cnt_T_str
I2c_SetCount(I2cRegPtr_Cnt_T_str)	target_I2c_SetCount_I2cRegPtr_Cnt_T_str
i2cREG1_temp	target_i2cREG1_temp
target_GetSystemTime_mS_u32_CurrentTime	0
target_i2cREG1_temp.OAR	23
target_i2cREG1_temp.IMR	10
target_i2cREG1_temp.STR	1000
target_i2cREG1_temp.CLKL	666
target_i2cREG1_temp.CLKH	7587
target_i2cREG1_temp.CNT	356
target_i2cREG1_temp.DRR	98
target_i2cREG1_temp.SAR	876
target_i2cREG1_temp.DXR	98
target_i2cREG1_temp.MDR	764
target_i2cREG1_temp.IVR	736
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	33
target_i2cREG1_temp.PID11	7
target_i2cREG1_temp.PID12	12
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	1

Name	Actual Value	Expected Value	Result
DigColPsInt_I2CHwCustData_Uls_M_u16	511	511	✔
DigColPsInt_InitialTime_mS_M_u32	0	0	✔
I2c_EnableNotification(Flags_Cnt_T_b32)	63	63	✔
I2c_SetCount(Count_Cnt_T_u16)	2	2	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR	23	23	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR	1000	1000	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL	666	666	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKH	7587	7587	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT	356	356	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.SAR	876	876	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR	98	98	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.MDR	764	764	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IVR	736	736	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PSC	33	33	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID11	7	7	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID12	12	12	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PD	0	0	✔
			✔

TEST DETAILS REPORT

DigColPsInt_Init

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Name	Actual Value	Expected Value	Result
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PSL	1	1	
target_I2c_Enable_I2cRegPtr_Cnt_T_str.OAR	23	23	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.STR	1000	1000	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLKL	666	666	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLKH	7587	7587	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CNT	356	356	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.SAR	876	876	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DXR	98	98	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.MDR	764	764	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.IVR	736	736	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PSC	33	33	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PID11	7	7	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PID12	12	12	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.OAR	23	23	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.STR	1000	1000	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.CLKL	666	666	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.CLKH	7587	7587	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.CNT	356	356	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.SAR	876	876	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.DXR	98	98	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.MDR	764	764	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.IVR	736	736	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.PSC	33	33	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.PID11	7	7	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.PID12	12	12	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.OAR	23	23	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.STR	1000	1000	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLKL	666	666	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLKH	7587	7587	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CNT	356	356	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.SAR	876	876	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DXR	98	98	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.MDR	764	764	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.IVR	736	736	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PSC	33	33	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PID11	7	7	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PID12	12	12	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLR	0	0	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PSL	1	1	✔

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Actual Function	Count	Expected Function	Count	Result
I2c_Init	1	I2c_Init	1	✔
I2c_SetCount	1	I2c_SetCount	1	✔
I2c_EnableNotification	1	I2c_EnableNotification	1	✔
I2c_Enable	1	I2c_Enable	1	✔
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	✔

Test Step 1.2 (Repeat Count = 1) ✔

Name	Input Value
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Enable(I2cRegPtr_Cnt_T_str)	target_I2c_Enable_I2cRegPtr_Cnt_T_str
I2c_EnableNotification(I2cRegPtr_Cnt_T_str)	target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str
I2c_Init(I2cRegPtr_Cnt_T_str)	target_I2c_Init_I2cRegPtr_Cnt_T_str
I2c_SetCount(I2cRegPtr_Cnt_T_str)	target_I2c_SetCount_I2cRegPtr_Cnt_T_str
i2cREG1_temp	target_i2cREG1_temp
target_GetSystemTime_mS_u32_CurrentTime	4294967295
target_i2cREG1_temp.OAR	456
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	56
target_i2cREG1_temp.CLKL	4555
target_i2cREG1_temp.CLKH	987
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	54
target_i2cREG1_temp.SAR	1000
target_i2cREG1_temp.DXR	45
target_i2cREG1_temp.MDR	98
target_i2cREG1_temp.IVR	332
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	4
target_i2cREG1_temp.PID11	7788
target_i2cREG1_temp.PID12	34
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	3
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	1
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_I2CHwCustData_Uls_M_u16	511	511	✔
DigColPsInt_InitialTime_mS_M_u32	4294967295	4294967295	✔
I2c_EnableNotification(Flags_Cnt_T_b32)	63	63	✔
I2c_SetCount(Count_Cnt_T_u16)	2	2	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR	456	456	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR	56	56	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL	4555	4555	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR	54	54	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.SAR	1000	1000	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR	45	45	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.MDR	98	98	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IVR	332	332	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PSC	4	4	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID11	7788	7788	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID12	34	34	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DIN	2	2	✔

TEST DETAILS REPORT

DigColPsInt_Init

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Name	Actual Value	Expected Value	Result
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.OAR	456	456	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.STR	56	56	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLKL	4555	4555	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DRR	54	54	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.SAR	1000	1000	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DXR	45	45	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.MDR	98	98	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.IVR	332	332	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PSC	4	4	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PID11	7788	7788	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PID12	34	34	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.OAR	456	456	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.STR	56	56	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.CLKL	4555	4555	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.DRR	54	54	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.SAR	1000	1000	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.DXR	45	45	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.MDR	98	98	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.IVR	332	332	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.PSC	4	4	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.PID11	7788	7788	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.PID12	34	34	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.OAR	456	456	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.STR	56	56	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLKL	4555	4555	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DRR	54	54	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.SAR	1000	1000	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DXR	45	45	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.MDR	98	98	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.IVR	332	332	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PSC	4	4	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PID11	7788	7788	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PID12	34	34	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.FUN	0	0	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PSL	0	0	✔

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Actual Function	Count	Expected Function	Count	Result
I2c_Init	1	I2c_Init	1	✔
I2c_SetCount	1	I2c_SetCount	1	✔
I2c_EnableNotification	1	I2c_EnableNotification	1	✔
I2c_Enable	1	I2c_Enable	1	✔
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	✔

Test Step 1.3 (Repeat Count = 1) ✔

Name	Input Value
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Enable(I2cRegPtr_Cnt_T_str)	target_I2c_Enable_I2cRegPtr_Cnt_T_str
I2c_EnableNotification(I2cRegPtr_Cnt_T_str)	target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str
I2c_Init(I2cRegPtr_Cnt_T_str)	target_I2c_Init_I2cRegPtr_Cnt_T_str
I2c_SetCount(I2cRegPtr_Cnt_T_str)	target_I2c_SetCount_I2cRegPtr_Cnt_T_str
i2cREG1_temp	target_i2cREG1_temp
target_GetSystemTime_mS_u32_CurrentTime	1457865
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	125
target_i2cREG1_temp.STR	44
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	3298
target_i2cREG1_temp.CNT	455
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	123
target_i2cREG1_temp.DXR	7
target_i2cREG1_temp.MDR	2
target_i2cREG1_temp.IVR	66
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	75
target_i2cREG1_temp.PID11	5444
target_i2cREG1_temp.PID12	76
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	3
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	3
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_I2CHwCustData_Uls_M_u16	511	511	✔
DigColPsInt_InitialTime_mS_M_u32	1457865	1457865	✔
I2c_EnableNotification(Flags_Cnt_T_b32)	63	63	✔
I2c_SetCount(Count_Cnt_T_u16)	2	2	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR	125	125	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR	44	44	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKH	3298	3298	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT	455	455	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.SAR	123	123	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR	7	7	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.MDR	2	2	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PSC	75	75	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID11	5444	5444	✔

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DigColPsInt_Init

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Name	Actual Value	Expected Value	Result
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID12	76	76	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.IMR	125	125	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.STR	44	44	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLKH	3298	3298	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CNT	455	455	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.SAR	123	123	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DXR	7	7	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.MDR	2	2	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PSC	75	75	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PID11	5444	5444	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PID12	76	76	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.IMR	125	125	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.STR	44	44	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.CLKH	3298	3298	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.CNT	455	455	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.SAR	123	123	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.DXR	7	7	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.MDR	2	2	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.PSC	75	75	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.PID11	5444	5444	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.PID12	76	76	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.IMR	125	125	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.STR	44	44	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLKH	3298	3298	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CNT	455	455	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.SAR	123	123	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DXR	7	7	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.MDR	2	2	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PSC	75	75	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PID11	5444	5444	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PID12	76	76	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

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Actual Function	Count	Expected Function	Count	Result
I2c_Init	1	I2c_Init	1	✔
I2c_SetCount	1	I2c_SetCount	1	✔
I2c_EnableNotification	1	I2c_EnableNotification	1	✔
I2c_Enable	1	I2c_Enable	1	✔
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	✔

Test Step 1.4 (Repeat Count = 1) ✔

Name	Input Value
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Enable(I2cRegPtr_Cnt_T_str)	target_I2c_Enable_I2cRegPtr_Cnt_T_str
I2c_EnableNotification(I2cRegPtr_Cnt_T_str)	target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str
I2c_Init(I2cRegPtr_Cnt_T_str)	target_I2c_Init_I2cRegPtr_Cnt_T_str
I2c_SetCount(I2cRegPtr_Cnt_T_str)	target_I2c_SetCount_I2cRegPtr_Cnt_T_str
i2cREG1_temp	target_i2cREG1_temp
target_GetSystemTime_mS_u32_CurrentTime	0
target_i2cREG1_temp.OAR	0
target_i2cREG1_temp.IMR	0
target_i2cREG1_temp.STR	0
target_i2cREG1_temp.CLKL	0
target_i2cREG1_temp.CLKH	0
target_i2cREG1_temp.CNT	0
target_i2cREG1_temp.DRR	0
target_i2cREG1_temp.SAR	0
target_i2cREG1_temp.DXR	0
target_i2cREG1_temp.MDR	0
target_i2cREG1_temp.IVR	0
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	0
target_i2cREG1_temp.PID11	0
target_i2cREG1_temp.PID12	0
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	0
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_I2CHwCustData_Uls_M_u16	511	511	✔
DigColPsInt_InitialTime_mS_M_u32	0	0	✔
I2c_EnableNotification(Flags_Cnt_T_b32)	63	63	✔
I2c_SetCount(Count_Cnt_T_u16)	2	2	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR	0	0	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR	0	0	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR	0	0	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL	0	0	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKH	0	0	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT	0	0	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR	0	0	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.SAR	0	0	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR	0	0	✔

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Name	Actual Value	Expected Value	Result
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.MDR	0	0	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IVR	0	0	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PSC	0	0	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID11	0	0	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID12	0	0	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.OAR	0	0	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.IMR	0	0	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.STR	0	0	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLKL	0	0	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLKH	0	0	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CNT	0	0	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DRR	0	0	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.SAR	0	0	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DXR	0	0	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.MDR	0	0	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.IVR	0	0	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PSC	0	0	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PID11	0	0	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PID12	0	0	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.OAR	0	0	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.IMR	0	0	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.STR	0	0	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.CLKL	0	0	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.CLKH	0	0	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.CNT	0	0	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.DRR	0	0	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.SAR	0	0	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.DXR	0	0	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.MDR	0	0	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.IVR	0	0	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.PSC	0	0	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.PID11	0	0	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.PID12	0	0	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.OAR	0	0	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.IMR	0	0	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.STR	0	0	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLKL	0	0	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLKH	0	0	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CNT	0	0	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DRR	0	0	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.SAR	0	0	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DXR	0	0	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.MDR	0	0	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.IVR	0	0	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PSC	0	0	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PID11	0	0	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PID12	0	0	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PSL	0	0	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
I2c_Init	1	I2c_Init	1	✔
I2c_SetCount	1	I2c_SetCount	1	✔
I2c_EnableNotification	1	I2c_EnableNotification	1	✔
I2c_Enable	1	I2c_Enable	1	✔
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	✔

Test Step 1.5 (Repeat Count = 1) ✔

Name	Input Value
GetSystemTime_mS_u32(CurrentTime)	target_GetSystemTime_mS_u32_CurrentTime
I2c_Enable(I2cRegPtr_Cnt_T_str)	target_I2c_Enable_I2cRegPtr_Cnt_T_str
I2c_EnableNotification(I2cRegPtr_Cnt_T_str)	target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str
I2c_Init(I2cRegPtr_Cnt_T_str)	target_I2c_Init_I2cRegPtr_Cnt_T_str
I2c_SetCount(I2cRegPtr_Cnt_T_str)	target_I2c_SetCount_I2cRegPtr_Cnt_T_str
i2cREG1_temp	target_i2cREG1_temp
target_GetSystemTime_mS_u32_CurrentTime	4294967295
target_i2cREG1_temp.OAR	1023
target_i2cREG1_temp.IMR	255
target_i2cREG1_temp.STR	32767
target_i2cREG1_temp.CLKL	65535
target_i2cREG1_temp.CLKH	65535
target_i2cREG1_temp.CNT	65535
target_i2cREG1_temp.DRR	255
target_i2cREG1_temp.SAR	1023
target_i2cREG1_temp.DXR	255
target_i2cREG1_temp.MDR	65535
target_i2cREG1_temp.IVR	4095
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	255
target_i2cREG1_temp.PID11	65535
target_i2cREG1_temp.PID12	255
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	3
target_i2cREG1_temp.DIN	3
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	3
target_i2cREG1_temp.ODR	3
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_I2CHwCustData_Uls_M_u16	511	511	✔
DigColPsInt_InitialTime_mS_M_u32	4294967295	4294967295	✔
I2c_EnableNotification(Flags_Cnt_T_b32)	63	63	✔
I2c_SetCount(Count_Cnt_T_u16)	2	2	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.OAR	1023	1023	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IMR	255	255	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.STR	32767	32767	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	✔

TEST DETAILS REPORT

DigColPsInt_Init

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Name	Actual Value	Expected Value	Result
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CNT	65535	65535	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DRR	255	255	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.SAR	1023	1023	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DXR	255	255	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.MDR	65535	65535	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.IVR	4095	4095	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PSC	255	255	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID11	65535	65535	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PID12	255	255	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_EnableNotification_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.OAR	1023	1023	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.IMR	255	255	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.STR	32767	32767	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CNT	65535	65535	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DRR	255	255	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.SAR	1023	1023	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DXR	255	255	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.MDR	65535	65535	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.IVR	4095	4095	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PSC	255	255	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PID11	65535	65535	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PID12	255	255	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Enable_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.OAR	1023	1023	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.IMR	255	255	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.STR	32767	32767	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.CNT	65535	65535	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.DRR	255	255	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.SAR	1023	1023	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.DXR	255	255	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.MDR	65535	65535	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.IVR	4095	4095	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.PSC	255	255	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.PID11	65535	65535	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.PID12	255	255	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Init_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.OAR	1023	1023	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.IMR	255	255	✔

TEST DETAILS REPORT

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Name	Actual Value	Expected Value	Result
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.STR	32767	32767	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CNT	65535	65535	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DRR	255	255	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.SAR	1023	1023	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DXR	255	255	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.MDR	65535	65535	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.IVR	4095	4095	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PSC	255	255	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PID11	65535	65535	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PID12	255	255	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetCount_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T			✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
I2c_Init	1	I2c_Init	1	✔
I2c_SetCount	1	I2c_SetCount	1	✔
I2c_EnableNotification	1	I2c_EnableNotification	1	✔
I2c_Enable	1	I2c_Enable	1	✔
GetSystemTime_mS_u32	1	GetSystemTime_mS_u32	1	✔

TEST DETAILS REPORT

SetupRead

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Project	
Module	
Test Object	

Instrumentation: Test Object Only

Statement (C0) Coverage	
Branch (C1) Coverage	

Statistics

Total Testcases	
Successful	
Failed	
Not Executed	

Module Properties

Project Root Directory	
Configuration File	
Target Environment	
Kind of Test	
Linker Options	
Source File(s)	
File	
Compiler Options	

Comments/Description/Specification	
Name	**Text**

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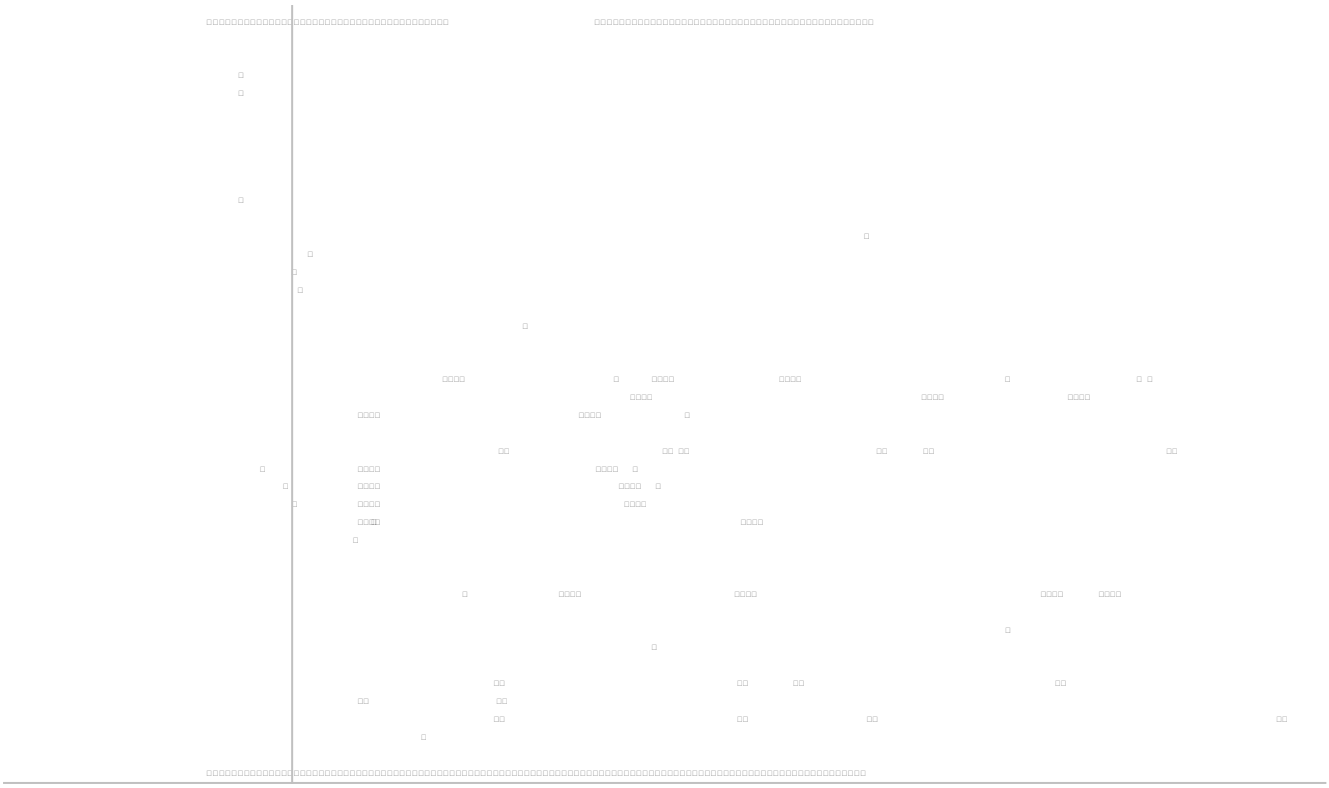

Attributes

Name	Value
Compiler Install Path	$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	$(Compiler Install Path)\include
Time Unit	Cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\C1xx_DigColPs\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

TEST DETAILS REPORT

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Test Case 1: Boundary Test

Description

Test Step 1.1 (Repeat Count = 1)

Name	Input Value

Name	Actual Value	Expected Value	Result
			✔
			✔
			✔
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Name	Actual Value	Expected Value	Result
			✔
			✔
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T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
				✔
				✔

TEST DETAILS REPORT

SetupRead

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Test Step 1.2 (Repeat Count = 1)

Name	Input Value

Name	Actual Value	Expected Value	Result

TEST DETAILS REPORT

SetupRead

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Name	Actual Value	Expected Value	Result
			✔
			✔
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			✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
				✔
				✔

Test Step 1.3 (Repeat Count = 1) ✔

Name	Input Value

Name	Actual Value	Expected Value	Result
			✔
			✔
			✔
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			✔
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Name	Actual Value	Expected Value	Result
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			✔
			✔
	□	□	✔
	□	□	✔
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	□	□	✔
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	□	□	✔
	□	□	✔
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T ✔

Actual Function	Count	Expected Function	Count	Result
				✔
				✔

Test Step 1.4 (Repeat Count = 1) ✔

Name	Input Value
□	
	□
	□

TEST DETAILS REPORT

SetupRead

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Name	Input Value

Name	Actual Value	Expected Value	Result
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			✔
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T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
				✔
				✔

Test Step 1.5 (Repeat Count = 1) ✔

Name	Input Value

Name	Actual Value	Expected Value	Result
			✔
			✔
			✔
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			✔
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TEST DETAILS REPORT

SetupRead

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Name	Actual Value	Expected Value	Result
			✔
			✔
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			✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
				✔
				✔

Test Step 1.6 (Repeat Count = 1)		✔
Name	**Input Value**	

Name	Actual Value	Expected Value	Result
			✔
			✔
			✔
			✔

TEST DETAILS REPORT

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Name	Actual Value	Expected Value	Result
□			✓
			✓
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T ✓

Actual Function	Count	Expected Function	Count	Result
				✓
				✓

Test Step 1.7 (Repeat Count = 1) ✓

Name	Input Value
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TEST DETAILS REPORT

SetupRead

2014-10-14, 23:45:17+0530

Name	Input Value

Name	Actual Value	Expected Value	Result

TEST DETAILS REPORT

SetupRead

2014-10-14, 23:45:17+0530

Name	Actual Value	Expected Value	Result
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			✔
			✔
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Actual Function	Count	Expected Function	Count	Result
				✔
				✔

Test Step 1.8 (Repeat Count = 1) ✔

Name	Input Value

Name	Actual Value	Expected Value	Result
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TEST DETAILS REPORT

SetupRead

2014-10-14, 23:45:17+0530

Name	Actual Value	Expected Value	Result
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T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
				✔
				✔

Module 'DigColPsInt'	**********Unit Test Descrption********** Name of Tester:Priti Mangalekar Code File(s) Under Test:Sa_DigColPsInt.c Code File(s) Version:7 Module Design Document:DigColPsInt_MDD.docx Module Design Document Version:8 Data Dictionary Version:9 Unit Test Plan Version:2 Optimization Level:Level 2 Compiler (CodeGen) Version:TMS470_4.9.5 Model Type:Excel Macro Model Version:Nexteer EPS Unit Test Tool 2.7d/EPS Library 1.30 Total FLASH Used (Bytes):N/A Total RAM Used (Bytes):N/A Total CALS Used (Bytes):N/A Special Test Requirements: Test Date:10/13/2014 Comments: NOTE 1: In """"DigColPsInt_StartRequest"""" function, path """"(Type_Cnt_T_u08 > D_NONE_CNT_U08) = TRUE && (Type_Cnt_T_u08 <= D_STATUSREG_CNT_U08) = FALSE"""" cannot be covered because range of """"Type_Cnt_T_u08"""" is '0-5' and value of """"D_STATUSREG_CNT_U08"""" is '34'. NOTE2: In function ""DigColPsInt_GetData"","DigColPsInt_StartRequest"" and ""DigColPsInt_InterruptNotification"" values for """"I2c_Send(Length_Cnt_T_u32)"""", """"I2c_SetRecv(Length_Cnt_T_u32)"""", """"I2c_SetStatus(Status_Cnt_T_u16)"""", """"I2c_SetupMasterReceive(DataLength_Cnt_T_u16)"""" and I2c_SetupMasterTransmit(DataLength_Cnt_T_u16) are ignored in few vectors as they are taking garbage value when they are not updated with expected value in particular vector. NOTE3: The return value of """"DigColPsInt_GetData"""" function is going out of range, anomaly """"6156"""" is raised for the same. NOTE4:Range of DigColPsInt_CurrentStepNo_Cnt_M_enum is considered as 0 to 36, as enum DigColPsInt_CurrentStepNo_Cnt_M_enum is of type CommStepType which is of 37 elements. NOTE5:In function ""DigColPsInt_InterruptNotification"", path ""Case I2C_RECV_OVERRUN: True"" cannot be covered because range of ""Flags_Cnt_T_b16"" is 0 to 64 given in MDD. NOTE6:In function ""DigColPsInt_InterruptNotification"", output variable ""DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08"" is going out of range." **********

Attributes

Name	Value
Compiler Install Path	$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	$(Compiler Install Path)\include
Time Unit	Cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\C1xx_DigColPs\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

Test Case 1: Metrics Test ✔

Description Test Vector Description:

TS1.1"Shortest Execution Path
switch ((i2cIntFlags)Flags_Cnt_T_b16)=>Default"
TS1.2"Longest Execution Path
switch case INIT_SENSOR2_EXTREADCTRLREG_READ:True
((DigColPsInt_Buffer_Cnt_M_u08[1] & 0x01U) == 0x01U)=True
((DigColPsInt_ColCustDatFound_Cnt_M_lgc == TRUE) && (DigColPsInt_SpurCustDatFound_Cnt_M_lgc == TRUE))=False
(DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 > D_MAXATTEMPTSFORCUSTDATREAD_CNT_U08)=False"

Test Step 1.1 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2
DigColPsInt_Buffer_Cnt_M_u08[0]	22
DigColPsInt_Buffer_Cnt_M_u08[1]	44
DigColPsInt_Buffer_Cnt_M_u08[2]	55
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	495
DigColPsInt_CurrentSlave_Cnt_M_u08	100
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	7
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	5
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	897
DigColPsInt_TransactionCnt_Cnt_M_u08	20
Flags_Cnt_T_b16	64
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	14
k_SpurSensorI2CAddress_Cnt_u08	20
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	0

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0

Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	78
target_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56
target_i2cREG1_temp.CNT	897
target_i2cREG1_temp.DRR	98
target_i2cREG1_temp.SAR	66
target_i2cREG1_temp.DXR	78
target_i2cREG1_temp.MDR	495
target_i2cREG1_temp.IVR	66
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	78
target_i2cREG1_temp.PID11	56
target_i2cREG1_temp.PID12	78
target_i2cREG1_temp.DMAC	0

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Input Value
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2	2	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	22	22	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	44	44	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	55	55	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	495	495	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	100	100	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ	INIT_SENSOR1_READERROR_READ	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	7	7	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	5	5	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	1	1	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	897	897	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	20	20	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 1.2 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	0
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	2767
DigColPsInt_CurrentSlave_Cnt_M_u08	45
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	76
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	77
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	564
DigColPsInt_TransactionCnt_Cnt_M_u08	130
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32

Name	Input Value
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	7
k_SpurSensorI2CAddress_Cnt_u08	123
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100

Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9

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Name	Input Value
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	3
target_i2cREG1_temp.IMR	100
target_i2cREG1_temp.STR	7788
target_i2cREG1_temp.CLKL	2767
target_i2cREG1_temp.CLKH	556
target_i2cREG1_temp.CNT	564
target_i2cREG1_temp.DRR	88
target_i2cREG1_temp.SAR	3
target_i2cREG1_temp.DXR	100
target_i2cREG1_temp.MDR	2767
target_i2cREG1_temp.IVR	9
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	100
target_i2cREG1_temp.PID11	556
target_i2cREG1_temp.PID12	100
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	3
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	3
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2767	2767	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	7	7	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_SET	INIT_SENSOR1_EXTREADCTRLREG_SET	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	76	76	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	77	77	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	2	2	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	564	564	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	130	130	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔

TEST DETAILS REPORT

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Case 2: Boundary Test

Description Test Vector Description:

TS2.1Flags_Cnt_T_b16 = min
TS2.2Flags_Cnt_T_b16 = max
TS2.3Flags_Cnt_T_b16 = mid
TS2.4DigColPsInt_CurrentStepNo_Cnt_M_enum = min
TS2.5DigColPsInt_CurrentStepNo_Cnt_M_enum = max
TS2.6DigColPsInt_CurrentStepNo_Cnt_M_enum = mid
TS2.7k_SpurSensorI2CAddress_Cnt_u08 = min
TS2.8k_SpurSensorI2CAddress_Cnt_u08 = max
TS2.9k_SpurSensorI2CAddress_Cnt_u08 = mid
TS2.10DigColPsInt_Buffer_Cnt_M_u08[3] = min
TS2.11DigColPsInt_Buffer_Cnt_M_u08[3] = max
TS2.12DigColPsInt_Buffer_Cnt_M_u08[3] = mid
TS2.13DigColPsInt_InitFailedOnce_Cnt_M_lgc = min
TS2.14DigColPsInt_InitFailedOnce_Cnt_M_lgc = max
TS2.15DigColPsInt_SkipRegisterWrite_Cnt_M_lgc = min
TS2.16DigColPsInt_SkipRegisterWrite_Cnt_M_lgc = max
TS2.17DigColPsInt_PrevReqDataType_Cnt_M_u08 = min
TS2.18DigColPsInt_PrevReqDataType_Cnt_M_u08 = max
TS2.19DigColPsInt_PrevReqDataType_Cnt_M_u08 = mid
TS2.20DigColPsInt_TransactionCnt_Cnt_M_u08 = min
TS2.21DigColPsInt_TransactionCnt_Cnt_M_u08 = max
TS2.22DigColPsInt_TransactionCnt_Cnt_M_u08 = mid
TS2.23k_ColSensorI2CAddress_Cnt_u08 = min
TS2.24k_ColSensorI2CAddress_Cnt_u08 = max
TS2.25k_ColSensorI2CAddress_Cnt_u08 = mid
TS2.26DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 = min
TS2.27DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 = max
TS2.28DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 = mid
TS2.29DigColPsInt_ColCustDatFound_Cnt_M_lgc = min
TS2.30DigColPsInt_ColCustDatFound_Cnt_M_lgc = max
TS2.31DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 = min
TS2.32DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 = max
TS2.33DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16 = mid
TS2.34DigColPsInt_SpurCustDatFound_Cnt_M_lgc = min
TS2.35DigColPsInt_SpurCustDatFound_Cnt_M_lgc = max
TS2.36All min
TS2.37All max

Test Step 2.1 (Repeat Count = 1)

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	1
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12

Name	Input Value
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	9
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2

Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1

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Name	Input Value
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE	INIT_COMPLETE	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	✔
I2c_SetStatus(Status_Cnt_T_u16)	7	7	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	✔

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
I2c_SetStatus	1	I2c_SetStatus	1	✔

Test Step 2.2 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2
DigColPsInt_Buffer_Cnt_M_u08[0]	22
DigColPsInt_Buffer_Cnt_M_u08[1]	44
DigColPsInt_Buffer_Cnt_M_u08[2]	55
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1

Name	Input Value
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	495
DigColPsInt_CurrentSlave_Cnt_M_u08	100
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	7
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	5
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	897
DigColPsInt_TransactionCnt_Cnt_M_u08	20
Flags_Cnt_T_b16	64
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	14
k_SpurSensorI2CAddress_Cnt_u08	20
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66

Name	Input Value
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	78
target_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56
target_i2cREG1_temp.CNT	897
target_i2cREG1_temp.DRR	98
target_i2cREG1_temp.SAR	66
target_i2cREG1_temp.DXR	78
target_i2cREG1_temp.MDR	495
target_i2cREG1_temp.IVR	66
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	78
target_i2cREG1_temp.PID11	56
target_i2cREG1_temp.PID12	78
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2	2	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	22	22	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	44	44	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	55	55	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	495	495	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
DigColPsInt_CurrentSlave_Cnt_M_u08	100	100	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ	INIT_SENSOR1_READERROR_READ	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	7	7	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
[illegible]	lt 0	tRecv_I2cRegPtr_ 78	tRecv_ tRecvuptNotificat=

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.3 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	15
DigColPsInt_Buffer_Cnt_M_u08[2]	16
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	566
DigColPsInt_CurrentSlave_Cnt_M_u08	110
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	7
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	8
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	129
DigColPsInt_TransactionCnt_Cnt_M_u08	30
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	19
k_SpurSensorI2CAddress_Cnt_u08	30
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129

Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566

Name	Input Value
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.MDR	566
target_i2cREG1_temp.IVR	554
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	44
target_i2cREG1_temp.PID11	4466
target_i2cREG1_temp.PID12	44
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	0
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3	3	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	15	15	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	16	16	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	566	566	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	110	110	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_SETREG	INIT_SENSOR1_READEXTERR_SETREG	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	7	7	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	8	8	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	2	2	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	129	129	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	30	30	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.4 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	4
DigColPsInt_Buffer_Cnt_M_u08[0]	28
DigColPsInt_Buffer_Cnt_M_u08[1]	56
DigColPsInt_Buffer_Cnt_M_u08[2]	100
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	7
DigColPsInt_CurrentSlave_Cnt_M_u08	120
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_NOT_INITIALIZED
DigColPsInt_I2CHwCustData_Uls_M_u16	10
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	11
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	4
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1

Name	Input Value
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	88
DigColPsInt_TransactionCnt_Cnt_M_u08	40
Flags_Cnt_T_b16	2
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	24
k_SpurSensorI2CAddress_Cnt_u08	40
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65

Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2

Name	Input Value
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	65
target_i2cREG1_temp.IMR	89
target_i2cREG1_temp.STR	67
target_i2cREG1_temp.CLKL	7
target_i2cREG1_temp.CLKH	577
target_i2cREG1_temp.CNT	88
target_i2cREG1_temp.DRR	23
target_i2cREG1_temp.SAR	65
target_i2cREG1_temp.DXR	89
target_i2cREG1_temp.MDR	7
target_i2cREG1_temp.IVR	44
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	89
target_i2cREG1_temp.PID11	577
target_i2cREG1_temp.PID12	89
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	2
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	4	4	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	56	56	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	100	100	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	7	7	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	40	40	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_SETREG	INIT_SENSOR2_READERROR_SETREG	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	10	10	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	11	11	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	88	88	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	40	40	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44	44	

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔

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Actual Function	Count	Expected Function	Count	Result
I2c_GenStopCond	1	I2c_GenStopCond	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 2.5 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	5
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	554
DigColPsInt_CurrentSlave_Cnt_M_u08	5
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE
DigColPsInt_I2CHwCustData_Uls_M_u16	13
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	14
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	123
DigColPsInt_TransactionCnt_Cnt_M_u08	50
Flags_Cnt_T_b16	1
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	29
k_SpurSensorI2CAddress_Cnt_u08	50
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344

Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2
target_i2cREG1_temp.OAR	54
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	8
target_i2cREG1_temp.CLKL	554
target_i2cREG1_temp.CLKH	344
target_i2cREG1_temp.CNT	123
target_i2cREG1_temp.DRR	45
target_i2cREG1_temp.SAR	54
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	554
target_i2cREG1_temp.IVR	788
target_i2cREG1_temp.EMDR	3

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Name	Input Value
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	344
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	3
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	3
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	1
target_i2cREG1_temp.PSL	2

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	5	5	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	123	123	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	554	554	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	5	5	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE	READ_COMPLETE	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	13	13	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	14	14	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	123	123	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	50	50	✔
I2c_SetStatus(Status_Cnt_T_u16)	7	7	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344	344	✔

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
I2c_SetStatus	1	I2c_SetStatus	1	✔

Test Step 2.6 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	6
DigColPsInt_Buffer_Cnt_M_u08[0]	100
DigColPsInt_Buffer_Cnt_M_u08[1]	200
DigColPsInt_Buffer_Cnt_M_u08[2]	250
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	7846
DigColPsInt_CurrentSlave_Cnt_M_u08	10
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READEXTERR_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	16
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	17
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	98
DigColPsInt_TransactionCnt_Cnt_M_u08	60
Flags_Cnt_T_b16	1
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str

Name	Input Value
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	34
k_SpurSensorI2CAddress_Cnt_u08	60
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10

Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98

Name	Input Value
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1
target_i2cREG1_temp.OAR	10
target_i2cREG1_temp.IMR	10
target_i2cREG1_temp.STR	1223
target_i2cREG1_temp.CLKL	7846
target_i2cREG1_temp.CLKH	8974
target_i2cREG1_temp.CNT	98
target_i2cREG1_temp.DRR	12
target_i2cREG1_temp.SAR	10
target_i2cREG1_temp.DXR	10
target_i2cREG1_temp.MDR	7846
target_i2cREG1_temp.IVR	55
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	10
target_i2cREG1_temp.PID11	8974
target_i2cREG1_temp.PID12	10
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	1
target_i2cREG1_temp.PSL	1

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	6	6	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	100	100	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	200	200	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	250	250	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	7846	7846	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	10	10	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE	INIT_COMPLETE	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	16	16	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	17	17	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	5	5	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	98	98	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	60	60	✔
I2c_SetStatus(Status_Cnt_T_u16)	7	7	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10	10	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
I2c_SetStatus	1	I2c_SetStatus	1	✔

Test Step 2.7 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	7
DigColPsInt_Buffer_Cnt_M_u08[0]	1
DigColPsInt_Buffer_Cnt_M_u08[1]	5
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	847
DigColPsInt_CurrentSlave_Cnt_M_u08	15
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_DUMMY_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	19
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	20
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	487
DigColPsInt_TransactionCnt_Cnt_M_u08	70
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	39
k_SpurSensorI2CAddress_Cnt_u08	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3

Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2
target_i2cREG1_temp.OAR	34
target_i2cREG1_temp.IMR	24
target_i2cREG1_temp.STR	455
target_i2cREG1_temp.CLKL	847
target_i2cREG1_temp.CLKH	987
target_i2cREG1_temp.CNT	487
target_i2cREG1_temp.DRR	34
target_i2cREG1_temp.SAR	34
target_i2cREG1_temp.DXR	24
target_i2cREG1_temp.MDR	847
target_i2cREG1_temp.IVR	56
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	24
target_i2cREG1_temp.PID11	987
target_i2cREG1_temp.PID12	24
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	3
target_i2cREG1_temp.DIN	3
target_i2cREG1_temp.DOUT	2

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Name	Input Value
target_i2cREG1_temp.SET	2
target_i2cREG1_temp.CLR	3
target_i2cREG1_temp.ODR	3
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	2

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	7	7	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	3	3	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	7	7	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	847	847	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	0	0	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADADDRREG_SEN	INIT_SENSOR2_EXTREADADDRREG_SEN	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	19	19	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	20	20	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	1	1	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	487	487	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	70	70	✔
I2c_Send(Length_Cnt_T_u32)	3	3	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	✔

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
SetupWriteData	1	SetupWriteData	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 2.8 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8
DigColPsInt_Buffer_Cnt_M_u08[0]	28
DigColPsInt_Buffer_Cnt_M_u08[1]	56
DigColPsInt_Buffer_Cnt_M_u08[2]	100
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	20
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	22
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	23
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	80
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32

Name	Input Value
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	44
k_SpurSensorI2CAddress_Cnt_u08	127
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66

Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5

Name	Input Value
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8	8	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	56	56	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	100	100	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_SET	INIT_SENSOR2_EXTREADCTRLREG_SET	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	22	22	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	23	23	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	2	2	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	80	80	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔

TEST DETAILS REPORT

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 2.9 (Repeat Count = 1)

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	9
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	495
DigColPsInt_CurrentSlave_Cnt_M_u08	25
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	25
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	26
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	897
DigColPsInt_TransactionCnt_Cnt_M_u08	90
Flags_Cnt_T_b16	2
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	49
k_SpurSensorI2CAddress_Cnt_u08	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78

Name	Input Value
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	78
target_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56
target_i2cREG1_temp.CNT	897
target_i2cREG1_temp.DRR	98
target_i2cREG1_temp.SAR	66
target_i2cREG1_temp.DXR	78
target_i2cREG1_temp.MDR	495
target_i2cREG1_temp.IVR	66
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	78
target_i2cREG1_temp.PID11	56
target_i2cREG1_temp.PID12	78
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	0

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	9	9	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	495	495	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	100	100	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_SETREG	INIT_SENSOR2_READERROR_SETREG	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	25	25	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	26	26	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	897	897	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	90	90	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	78	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	98	

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
I2c_GenStopCond	1	I2c_GenStopCond	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 2.10 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	10
DigColPsInt_Buffer_Cnt_M_u08[0]	0
DigColPsInt_Buffer_Cnt_M_u08[1]	0
DigColPsInt_Buffer_Cnt_M_u08[2]	0
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	566
DigColPsInt_CurrentSlave_Cnt_M_u08	30
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	28
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	29
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	4
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	129
DigColPsInt_TransactionCnt_Cnt_M_u08	100
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10

Name	Input Value
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	54
k_SpurSensorI2CAddress_Cnt_u08	120
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2

Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1

Name	Input Value
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.MDR	566
target_i2cREG1_temp.IVR	554
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	44
target_i2cREG1_temp.PID11	4466
target_i2cREG1_temp.PID12	44
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	0
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	0	0	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	0	0	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	566	566	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	120	120	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_SETREG	INIT_SENSOR2_READERROR_SETREG	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	28	28	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	29	29	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	129	129	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	100	100	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 2.11 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2

Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[0]	255
DigColPsInt_Buffer_Cnt_M_u08[1]	255
DigColPsInt_Buffer_Cnt_M_u08[2]	255
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	7
DigColPsInt_CurrentSlave_Cnt_M_u08	35
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	31
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	32
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	88
DigColPsInt_TransactionCnt_Cnt_M_u08	110
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	59
k_SpurSensorI2CAddress_Cnt_u08	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23

Name	Input Value
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	65
target_i2cREG1_temp.IMR	89
target_i2cREG1_temp.STR	67
target_i2cREG1_temp.CLKL	7
target_i2cREG1_temp.CLKH	577
target_i2cREG1_temp.CNT	88
target_i2cREG1_temp.DRR	23
target_i2cREG1_temp.SAR	65
target_i2cREG1_temp.DXR	89
target_i2cREG1_temp.MDR	7
target_i2cREG1_temp.IVR	44
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	89
target_i2cREG1_temp.PID11	577
target_i2cREG1_temp.PID12	89
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	2
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2	2	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	38	38	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	255	255	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	255	255	✔

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Name	Actual Value	Expected Value	Result
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	7	7	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	35	35	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_SETREG	INIT_SENSOR1_READEXTERR_SETREG	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	31	31	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	32	32	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	5	5	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	88	88	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	110	110	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88	88	✔

TEST DETAILS REPORT

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89	89	

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔

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Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 2.12 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	4
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	554
DigColPsInt_CurrentSlave_Cnt_M_u08	40
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	34
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	35
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	123
DigColPsInt_TransactionCnt_Cnt_M_u08	120
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	64
k_SpurSensorI2CAddress_Cnt_u08	10

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2

Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3

TEST DETAILS REPORT

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Name	Input Value
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2
target_i2cREG1_temp.OAR	54
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	8
target_i2cREG1_temp.CLKL	554
target_i2cREG1_temp.CLKH	344
target_i2cREG1_temp.CNT	123
target_i2cREG1_temp.DRR	45
target_i2cREG1_temp.SAR	54
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	554
target_i2cREG1_temp.IVR	788
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	344
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	3
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	3
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	1
target_i2cREG1_temp.PSL	2

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	4	4	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	38	38	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	554	554	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	40	40	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READEXTERR_SETREG	INIT_SENSOR2_READEXTERR_SETREG	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	34	34	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	35	35	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	1	1	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	123	123	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	120	120	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	✔

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 2.13 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	6
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0

Name	Input Value
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	2767
DigColPsInt_CurrentSlave_Cnt_M_u08	45
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	37
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	38
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	564
DigColPsInt_TransactionCnt_Cnt_M_u08	130
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	69
k_SpurSensorI2CAddress_Cnt_u08	123
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0

Name	Input Value
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	3
target_i2cREG1_temp.IMR	100
target_i2cREG1_temp.STR	7788
target_i2cREG1_temp.CLKL	2767
target_i2cREG1_temp.CLKH	556
target_i2cREG1_temp.CNT	564
target_i2cREG1_temp.DRR	88
target_i2cREG1_temp.SAR	3
target_i2cREG1_temp.DXR	100
target_i2cREG1_temp.MDR	2767
target_i2cREG1_temp.IVR	9
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	100
target_i2cREG1_temp.PID11	556
target_i2cREG1_temp.PID12	100
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	3
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	3
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	6	6	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2767	2767	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	45	45	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Actual Value	Expected Value	Result
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	37	37	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	38	38	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	2	2	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	564	564	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	130	130	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9	9	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100	100	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 2.14 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8
DigColPsInt_Buffer_Cnt_M_u08[0]	100
DigColPsInt_Buffer_Cnt_M_u08[1]	200
DigColPsInt_Buffer_Cnt_M_u08[2]	250
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	7846
DigColPsInt_CurrentSlave_Cnt_M_u08	10
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	40
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	41
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	98
DigColPsInt_TransactionCnt_Cnt_M_u08	12
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	74
k_SpurSensorI2CAddress_Cnt_u08	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	1223

Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1
target_i2cREG1_temp.OAR	10

Name	Input Value
target_i2cREG1_temp.IMR	10
target_i2cREG1_temp.STR	1223
target_i2cREG1_temp.CLKL	7846
target_i2cREG1_temp.CLKH	8974
target_i2cREG1_temp.CNT	98
target_i2cREG1_temp.DRR	12
target_i2cREG1_temp.SAR	10
target_i2cREG1_temp.DXR	10
target_i2cREG1_temp.MDR	7846
target_i2cREG1_temp.IVR	55
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	10
target_i2cREG1_temp.PID11	8974
target_i2cREG1_temp.PID12	10
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	1
target_i2cREG1_temp.PSL	1

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8	8	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	3	3	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	7	7	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	7846	7846	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	74	74	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADADDRREG_SEN	INIT_SENSOR1_EXTREADADDRREG_SEN	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	40	40	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	41	41	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	98	98	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	12	12	✔
I2c_Send(Length_Cnt_T_u32)	3	3	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	10	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1	1	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
SetupWriteData	1	SetupWriteData	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 2.15 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	10
DigColPsInt_Buffer_Cnt_M_u08[0]	1
DigColPsInt_Buffer_Cnt_M_u08[1]	5
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	847
DigColPsInt_CurrentSlave_Cnt_M_u08	20
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_GETDATA
DigColPsInt_I2CHwCustData_Uls_M_u16	43

Name	Input Value
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	44
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	4
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	487
DigColPsInt_TransactionCnt_Cnt_M_u08	13
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	79
k_SpurSensorI2CAddress_Cnt_u08	110
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0

Name	Input Value
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2
target_i2cREG1_temp.OAR	34
target_i2cREG1_temp.IMR	24
target_i2cREG1_temp.STR	455
target_i2cREG1_temp.CLKL	847
target_i2cREG1_temp.CLKH	987
target_i2cREG1_temp.CNT	487
target_i2cREG1_temp.DRR	34
target_i2cREG1_temp.SAR	34
target_i2cREG1_temp.DXR	24
target_i2cREG1_temp.MDR	847
target_i2cREG1_temp.IVR	56
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	24
target_i2cREG1_temp.PID11	987
target_i2cREG1_temp.PID12	24
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	3
target_i2cREG1_temp.DIN	3
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	2
target_i2cREG1_temp.CLR	3
target_i2cREG1_temp.ODR	3
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	2

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	38	38	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	5	5	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	9	9	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	261	261	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	110	110	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_SETREG	READ_SENSOR2_SETREG	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	43	43	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	44	44	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Actual Value	Expected Value	Result
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	487	487	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	13	13	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987	987	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	✔

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Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 2.16 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	30
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_GETDATA
DigColPsInt_I2CHwCustData_Uls_M_u16	46
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	47
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	14
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	84
k_SpurSensorI2CAddress_Cnt_u08	120
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55

Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87

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Name	Input Value
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2580	2580	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	120	120	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_GETDATA	READ_SENSOR2_GETDATA	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	46	46	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	47	47	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	5	5	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	14	14	✔
I2c_SetRecv(Length_Cnt_T_u32)	2	2	✔
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	✔
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	✔
I2c_SetRecv	1	I2c_SetRecv	1	✔

Test Step 2.17 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3
DigColPsInt_Buffer_Cnt_M_u08[0]	22
DigColPsInt_Buffer_Cnt_M_u08[1]	44
DigColPsInt_Buffer_Cnt_M_u08[2]	55
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	495
DigColPsInt_CurrentSlave_Cnt_M_u08	40
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_GETDATA
DigColPsInt_I2CHwCustData_Uls_M_u16	49
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	50
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0

Name	Input Value
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	897
DigColPsInt_TransactionCnt_Cnt_M_u08	6
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	89
k_SpurSensorI2CAddress_Cnt_u08	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0

TEST DETAILS REPORT

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Name	Input Value
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	78
target_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56
target_i2cREG1_temp.CNT	897
target_i2cREG1_temp.DRR	98
target_i2cREG1_temp.SAR	66
target_i2cREG1_temp.DXR	78
target_i2cREG1_temp.MDR	495
target_i2cREG1_temp.IVR	66
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	78
target_i2cREG1_temp.PID11	56
target_i2cREG1_temp.PID12	78
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3	3	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	0	0	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	44	44	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	55	55	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	5676	5676	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	5	5	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_SETREG	READ_SENSOR2_SETREG	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	49	49	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	50	50	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	1	1	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	897	897	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	6	6	✔

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Name	Actual Value	Expected Value	Result
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔

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Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 2.18 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	5
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	15
DigColPsInt_Buffer_Cnt_M_u08[2]	16
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	566
DigColPsInt_CurrentSlave_Cnt_M_u08	50
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_GETDATA
DigColPsInt_I2CHwCustData_Uls_M_u16	52
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	53
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	129
DigColPsInt_TransactionCnt_Cnt_M_u08	7
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	94
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44

Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.MDR	566
target_i2cREG1_temp.IVR	554

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Input Value
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	44
target_i2cREG1_temp.PID11	4466
target_i2cREG1_temp.PID12	44
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	0
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	5	5	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	15	15	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	16	16	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	566	566	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	50	50	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE	READ_COMPLETE	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	52	52	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	53	53	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	5	5	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	2575	2575	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	8	8	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	44	

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.19 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	7
DigColPsInt_Buffer_Cnt_M_u08[0]	28
DigColPsInt_Buffer_Cnt_M_u08[1]	56
DigColPsInt_Buffer_Cnt_M_u08[2]	100
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	7
DigColPsInt_CurrentSlave_Cnt_M_u08	60
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_GETDATA
DigColPsInt_I2CHwCustData_Uls_M_u16	55
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	56
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	88
DigColPsInt_TransactionCnt_Cnt_M_u08	8
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str

Name	Input Value
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	99
k_SpurSensorI2CAddress_Cnt_u08	15
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65

Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88

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Name	Input Value
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	65
target_i2cREG1_temp.IMR	89
target_i2cREG1_temp.STR	67
target_i2cREG1_temp.CLKL	7
target_i2cREG1_temp.CLKH	577
target_i2cREG1_temp.CNT	88
target_i2cREG1_temp.DRR	23
target_i2cREG1_temp.SAR	65
target_i2cREG1_temp.DXR	89
target_i2cREG1_temp.MDR	7
target_i2cREG1_temp.IVR	44
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	89
target_i2cREG1_temp.PID11	577
target_i2cREG1_temp.PID12	89
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	2
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	7	7	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	56	56	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	100	100	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	7224	7224	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	15	15	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_SETREG	READ_SENSOR2_SETREG	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	55	55	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	56	56	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	88	88	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	8	8	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23	23	✔

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 2.20 (Repeat Count = 1)	✔
Name	**Input Value**
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	9
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	554
DigColPsInt_CurrentSlave_Cnt_M_u08	70
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_GETDATA
DigColPsInt_I2CHwCustData_Uls_M_u16	58
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	59
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	123
DigColPsInt_TransactionCnt_Cnt_M_u08	0
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	104
k_SpurSensorI2CAddress_Cnt_u08	20
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3

Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2
target_i2cREG1_temp.OAR	54
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	8
target_i2cREG1_temp.CLKL	554
target_i2cREG1_temp.CLKH	344
target_i2cREG1_temp.CNT	123
target_i2cREG1_temp.DRR	45
target_i2cREG1_temp.SAR	54
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	554
target_i2cREG1_temp.IVR	788
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	344
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	3

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Name	Input Value
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	3
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	1
target_i2cREG1_temp.PSL	2

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	9	9	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	123	123	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	554	554	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	70	70	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE	READ_COMPLETE	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	58	58	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	59	59	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	1	1	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	31633	31633	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.21 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	100
DigColPsInt_Buffer_Cnt_M_u08[1]	200
DigColPsInt_Buffer_Cnt_M_u08[2]	250
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2767
DigColPsInt_CurrentSlave_Cnt_M_u08	80
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_GETDATA
DigColPsInt_I2CHwCustData_Uls_M_u16	61
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	62
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	564
DigColPsInt_TransactionCnt_Cnt_M_u08	255
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36

Name	Input Value
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	109
k_SpurSensorI2CAddress_Cnt_u08	25
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100

Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100

Name	Input Value
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	3
target_i2cREG1_temp.IMR	100
target_i2cREG1_temp.STR	7788
target_i2cREG1_temp.CLKL	2767
target_i2cREG1_temp.CLKH	556
target_i2cREG1_temp.CNT	564
target_i2cREG1_temp.DRR	88
target_i2cREG1_temp.SAR	3
target_i2cREG1_temp.DXR	100
target_i2cREG1_temp.MDR	2767
target_i2cREG1_temp.IVR	9
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	100
target_i2cREG1_temp.PID11	556
target_i2cREG1_temp.PID12	100
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	3
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	3
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	100	100	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	200	200	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	250	250	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2767	2767	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	80	80	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE	READ_COMPLETE	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	61	61	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	62	62	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	2	2	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	25800	25800	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88	88	

Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.22 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2
DigColPsInt_Buffer_Cnt_M_u08[0]	1

Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[1]	5
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	56
DigColPsInt_CurrentSlave_Cnt_M_u08	90
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_GETDATA
DigColPsInt_I2CHwCustData_Uls_M_u16	64
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	65
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	7878
DigColPsInt_TransactionCnt_Cnt_M_u08	100
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	114
k_SpurSensorI2CAddress_Cnt_u08	30
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	678
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	45
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	6788
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	7878
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	678
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	45
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	778
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	45
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	6788
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	45
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	678
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	6788
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	7878
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	678
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	56

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	778
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	6788
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	678
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	45
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	6788
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	7878
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	678
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	45
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	778
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	45
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	6788
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	45
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	678
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	45
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	6788
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	7878
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	678
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	45
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	778
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	45
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	6788
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	45
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	678
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	45
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	6788
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	7878
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	678

Name	Input Value
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	45
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	778
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	45
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	6788
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	45
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	678
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	6788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	7878
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	678
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	778
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	6788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1
target_i2cREG1_temp.OAR	678
target_i2cREG1_temp.IMR	45
target_i2cREG1_temp.STR	66
target_i2cREG1_temp.CLKL	56
target_i2cREG1_temp.CLKH	6788
target_i2cREG1_temp.CNT	7878
target_i2cREG1_temp.DRR	12
target_i2cREG1_temp.SAR	678
target_i2cREG1_temp.DXR	45
target_i2cREG1_temp.MDR	56
target_i2cREG1_temp.IVR	778
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	45
target_i2cREG1_temp.PID11	6788
target_i2cREG1_temp.PID12	45
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	1

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2	2	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	1	1	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	5	5	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	9	9	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	56	56	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	90	90	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE	READ_COMPLETE	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	64	64	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	65	65	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	261	261	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	101	101	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	678	678	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	45	45	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	56	56	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	7878	7878	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	678	678	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	45	45	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	56	56	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	778	778	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	45	45	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	6788	6788	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	45	45	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	678	678	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	45	45	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	7878	7878	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	678	678	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	45	45	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	778	778	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	45	45	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	6788	6788	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	45	45	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	678	678	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	45	45	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	56	56	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	7878	7878	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	678	678	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	45	45	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	56	56	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	778	778	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	45	45	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	6788	6788	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	45	45	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	678	678	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	45	45	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	56	56	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	7878	7878	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	678	678	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	45	45	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	56	56	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	778	778	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	45	45	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	6788	6788	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	45	45	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	678	678	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	45	45	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	56	56	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	7878	7878	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	678	678	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	45	45	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	56	56	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	778	778	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	45	45	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	6788	6788	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	45	45	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	678	678	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	45	45	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	7878	7878	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	678	678	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	45	45	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	778	778	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	45	45	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	6788	6788	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	45	45	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.23 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	566
DigColPsInt_CurrentSlave_Cnt_M_u08	30
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READEXTERR_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	67
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	68
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	4
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	129
DigColPsInt_TransactionCnt_Cnt_M_u08	100
Flags_Cnt_T_b16	2
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	0
k_SpurSensorI2CAddress_Cnt_u08	120
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444

Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	567

Name	Input Value
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.MDR	566
target_i2cREG1_temp.IVR	554
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	44
target_i2cREG1_temp.PID11	4466
target_i2cREG1_temp.PID12	44
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	0
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3	3	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	3	3	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	7	7	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	566	566	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	0	0	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADADDRREG_SEN	INIT_SENSOR1_EXTREADADDRREG_SEN	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	67	67	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	68	68	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	129	129	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	100	100	✔
I2c_Send(Length_Cnt_T_u32)	3	3	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
I2c_GenStopCond	1	I2c_GenStopCond	1	✔
SetupWriteData	1	SetupWriteData	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 2.24 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	4
DigColPsInt_Buffer_Cnt_M_u08[0]	100
DigColPsInt_Buffer_Cnt_M_u08[1]	200
DigColPsInt_Buffer_Cnt_M_u08[2]	250
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	7
DigColPsInt_CurrentSlave_Cnt_M_u08	35
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_DUMMY_READ

Name	Input Value
DigColPsInt_I2CHwCustData_Uls_M_u16	70
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	71
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	88
DigColPsInt_TransactionCnt_Cnt_M_u08	110
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	127
k_SpurSensorI2CAddress_Cnt_u08	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2

Name	Input Value
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	65
target_i2cREG1_temp.IMR	89
target_i2cREG1_temp.STR	67
target_i2cREG1_temp.CLKL	7
target_i2cREG1_temp.CLKH	577
target_i2cREG1_temp.CNT	88
target_i2cREG1_temp.DRR	23
target_i2cREG1_temp.SAR	65
target_i2cREG1_temp.DXR	89
target_i2cREG1_temp.MDR	7
target_i2cREG1_temp.IVR	44
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	89
target_i2cREG1_temp.PID11	577
target_i2cREG1_temp.PID12	89
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	2
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	4	4	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	200	200	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	250	250	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	7	7	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_SET	INIT_SENSOR1_EXTREADCTRLREG_SET	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	70	70	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	71	71	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	5	5	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	88	88	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	110	110	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89	89	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔

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Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 2.25 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	5
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	554
DigColPsInt_CurrentSlave_Cnt_M_u08	40
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	73
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	74
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	123
DigColPsInt_TransactionCnt_Cnt_M_u08	120
Flags_Cnt_T_b16	2
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	111
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45

Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2
target_i2cREG1_temp.OAR	54
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	8
target_i2cREG1_temp.CLKL	554
target_i2cREG1_temp.CLKH	344

TEST DETAILS REPORT

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Name	Input Value
target_i2cREG1_temp.CNT	123
target_i2cREG1_temp.DRR	45
target_i2cREG1_temp.SAR	54
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	554
target_i2cREG1_temp.IVR	788
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	344
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	3
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	3
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	1
target_i2cREG1_temp.PSL	2

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	5	5	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	3	3	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	7	7	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	554	554	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	111	111	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADADDRREG_SEN	INIT_SENSOR1_EXTREADADDRREG_SEN	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	73	73	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	74	74	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	1	1	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	123	123	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	120	120	✔
I2c_Send(Length_Cnt_T_u32)	3	3	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	123	✔

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
I2c_GenStopCond	1	I2c_GenStopCond	1	✔
SetupWriteData	1	SetupWriteData	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 2.26 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	0
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	2767
DigColPsInt_CurrentSlave_Cnt_M_u08	45
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	76
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	77
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0

Name	Input Value
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	564
DigColPsInt_TransactionCnt_Cnt_M_u08	130
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	7
k_SpurSensorI2CAddress_Cnt_u08	123
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2

Name	Input Value
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	3
target_i2cREG1_temp.IMR	100
target_i2cREG1_temp.STR	7788
target_i2cREG1_temp.CLKL	2767
target_i2cREG1_temp.CLKH	556
target_i2cREG1_temp.CNT	564
target_i2cREG1_temp.DRR	88
target_i2cREG1_temp.SAR	3
target_i2cREG1_temp.DXR	100
target_i2cREG1_temp.MDR	2767
target_i2cREG1_temp.IVR	9
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	100
target_i2cREG1_temp.PID11	556
target_i2cREG1_temp.PID12	100
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	3
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	3
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2767	2767	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	7	7	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_SET	INIT_SENSOR1_EXTREADCTRLREG_SET	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	76	76	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	77	77	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	2	2	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔

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Name	Actual Value	Expected Value	Result
DigColPsInt_SpurSnsrData_Cnt_M_u16	564	564	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	130	130	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	✔

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

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Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 2.27 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	11
DigColPsInt_Buffer_Cnt_M_u08[0]	100
DigColPsInt_Buffer_Cnt_M_u08[1]	200
DigColPsInt_Buffer_Cnt_M_u08[2]	250
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	7846
DigColPsInt_CurrentSlave_Cnt_M_u08	10
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	79
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	80
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	98
DigColPsInt_TransactionCnt_Cnt_M_u08	12
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	11
k_SpurSensorI2CAddress_Cnt_u08	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	10

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	55

Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1
target_i2cREG1_temp.OAR	10
target_i2cREG1_temp.IMR	10
target_i2cREG1_temp.STR	1223
target_i2cREG1_temp.CLKL	7846
target_i2cREG1_temp.CLKH	8974
target_i2cREG1_temp.CNT	98
target_i2cREG1_temp.DRR	12
target_i2cREG1_temp.SAR	10
target_i2cREG1_temp.DXR	10

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Input Value
target_i2cREG1_temp.MDR	7846
target_i2cREG1_temp.IVR	55
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	10
target_i2cREG1_temp.PID11	8974
target_i2cREG1_temp.PID12	10
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	1
target_i2cREG1_temp.PSL	1

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	12	12	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	14	14	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	200	200	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	250	250	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	7846	7846	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	11	11	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR1 EXTREADDATREG SETR	INIT SENSOR1 EXTREADDATREG SETR	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	79	79	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	80	80	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	98	98	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	12	12	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10	10	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	✔

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Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 2.28 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	5
DigColPsInt_Buffer_Cnt_M_u08[0]	1
DigColPsInt_Buffer_Cnt_M_u08[1]	5
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	847
DigColPsInt_CurrentSlave_Cnt_M_u08	20
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	82
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	83
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	4
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0

Name	Input Value
DigColPsInt_SpurSnsrData_Cnt_M_u16	487
DigColPsInt_TransactionCnt_Cnt_M_u08	13
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	15
k_SpurSensorI2CAddress_Cnt_u08	110
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	24

Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2

Name	Input Value
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2
target_i2cREG1_temp.OAR	34
target_i2cREG1_temp.IMR	24
target_i2cREG1_temp.STR	455
target_i2cREG1_temp.CLKL	847
target_i2cREG1_temp.CLKH	987
target_i2cREG1_temp.CNT	487
target_i2cREG1_temp.DRR	34
target_i2cREG1_temp.SAR	34
target_i2cREG1_temp.DXR	24
target_i2cREG1_temp.MDR	847
target_i2cREG1_temp.IVR	56
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	24
target_i2cREG1_temp.PID11	987
target_i2cREG1_temp.PID12	24
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	3
target_i2cREG1_temp.DIN	3
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	2
target_i2cREG1_temp.CLR	3
target_i2cREG1_temp.ODR	3
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	2

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	6	6	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	5	5	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	9	9	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	847	847	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	15	15	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_SET	INIT_SENSOR1_EXTREADCTRLREG_SET	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	82	82	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	83	83	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	487	487	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	13	13	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	34	34	✔

TEST DETAILS REPORT

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	✔

TEST DETAILS REPORT

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 2.29 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	6
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	30
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	85
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	86
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	14
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	19
k_SpurSensorI2CAddress_Cnt_u08	120
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3

Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Input Value
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	7	7	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	19	19	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_SET	INIT_SENSOR1_EXTREADCTRLREG_SET	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	85	85	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	86	86	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	5	5	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	14	14	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 2.30 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	7
DigColPsInt_Buffer_Cnt_M_u08[0]	22
DigColPsInt_Buffer_Cnt_M_u08[1]	44
DigColPsInt_Buffer_Cnt_M_u08[2]	55
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	495
DigColPsInt_CurrentSlave_Cnt_M_u08	40
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	88
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	89
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	897
DigColPsInt_TransactionCnt_Cnt_M_u08	6
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str

Name	Input Value
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	23
k_SpurSensorI2CAddress_Cnt_u08	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98

Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56

Name	Input Value
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	78
target_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56
target_i2cREG1_temp.CNT	897
target_i2cREG1_temp.DRR	98
target_i2cREG1_temp.SAR	66
target_i2cREG1_temp.DXR	78
target_i2cREG1_temp.MDR	495
target_i2cREG1_temp.IVR	66
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	78
target_i2cREG1_temp.PID11	56
target_i2cREG1_temp.PID12	78
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8	8	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	44	44	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	55	55	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	495	495	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	23	23	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_SET	INIT_SENSOR1_EXTREADCTRLREG_SET	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	88	88	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	89	89	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	1	1	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	897	897	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	6	6	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	897	897	✔

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 2.31 (Repeat Count = 1)	✔
Name	**Input Value**
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	15
DigColPsInt_Buffer_Cnt_M_u08[2]	16
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	566
DigColPsInt_CurrentSlave_Cnt_M_u08	50
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADDATREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	91
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	0
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	129
DigColPsInt_TransactionCnt_Cnt_M_u08	7
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	27
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1

Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.MDR	566
target_i2cREG1_temp.IVR	554
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	44
target_i2cREG1_temp.PID11	4466
target_i2cREG1_temp.PID12	44
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Input Value
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	0
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8	8	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	15	15	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	16	16	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	566	566	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	50	50	✔
DigColPsInt_CurrentStepNo_Cnt_M_enuo			

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.32 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	9
DigColPsInt_Buffer_Cnt_M_u08[0]	28
DigColPsInt_Buffer_Cnt_M_u08[1]	56
DigColPsInt_Buffer_Cnt_M_u08[2]	100
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	7
DigColPsInt_CurrentSlave_Cnt_M_u08	60
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADDATREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	94
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	255
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	88
DigColPsInt_TransactionCnt_Cnt_M_u08	8
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36

Name	Input Value
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	31
k_SpurSensorI2CAddress_Cnt_u08	15
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89

Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89

Name	Input Value
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	65
target_i2cREG1_temp.IMR	89
target_i2cREG1_temp.STR	67
target_i2cREG1_temp.CLKL	7
target_i2cREG1_temp.CLKH	577
target_i2cREG1_temp.CNT	88
target_i2cREG1_temp.DRR	23
target_i2cREG1_temp.SAR	65
target_i2cREG1_temp.DXR	89
target_i2cREG1_temp.MDR	7
target_i2cREG1_temp.IVR	44
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	89
target_i2cREG1_temp.PID11	577
target_i2cREG1_temp.PID12	89
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	2
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	9	9	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	28	28	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	56	56	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	100	100	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	7	7	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	60	60	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE	INIT_COMPLETE	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	255	255	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	255	255	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	88	88	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	8	8	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔

TEST DETAILS REPORT

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 2.33 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	10
DigColPsInt_Buffer_Cnt_M_u08[0]	123

Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	554
DigColPsInt_CurrentSlave_Cnt_M_u08	70
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADDATREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	97
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	147
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	123
DigColPsInt_TransactionCnt_Cnt_M_u08	0
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	35
k_SpurSensorI2CAddress_Cnt_u08	20
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54

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Name	Input Value
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2
target_i2cREG1_temp.OAR	54
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	8
target_i2cREG1_temp.CLKL	554
target_i2cREG1_temp.CLKH	344
target_i2cREG1_temp.CNT	123
target_i2cREG1_temp.DRR	45
target_i2cREG1_temp.SAR	54
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	554
target_i2cREG1_temp.IVR	788
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	344
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	3
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	3
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	1
target_i2cREG1_temp.PSL	2

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	123	123	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Actual Value	Expected Value	Result
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	554	554	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	70	70	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE	INIT_COMPLETE	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	147	147	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	147	147	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	123	123	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45	45	✔

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DigColPsInt_InterruptNotification

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	✔

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556

Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55

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Name	Input Value
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	4	4	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	47	47	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_SET	INIT_SENSOR1_EXTREADCTRLREG_SET	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	106	106	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	180	180	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	5	5	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	14	14	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔

TEST DETAILS REPORT

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 2.35 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2
DigColPsInt_Buffer_Cnt_M_u08[0]	22
DigColPsInt_Buffer_Cnt_M_u08[1]	44
DigColPsInt_Buffer_Cnt_M_u08[2]	55
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	495
DigColPsInt_CurrentSlave_Cnt_M_u08	40
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	109

Name	Input Value
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	191
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	897
DigColPsInt_TransactionCnt_Cnt_M_u08	6
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	51
k_SpurSensorI2CAddress_Cnt_u08	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0

Name	Input Value
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	66
target_i2cREG1_temp.IMR	78
target_i2cREG1_temp.STR	78
target_i2cREG1_temp.CLKL	495
target_i2cREG1_temp.CLKH	56
target_i2cREG1_temp.CNT	897
target_i2cREG1_temp.DRR	98
target_i2cREG1_temp.SAR	66
target_i2cREG1_temp.DXR	78
target_i2cREG1_temp.MDR	495
target_i2cREG1_temp.IVR	66
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	78
target_i2cREG1_temp.PID11	56
target_i2cREG1_temp.PID12	78
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3	3	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	44	44	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	55	55	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	495	495	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	51	51	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_SET	INIT_SENSOR1_EXTREADCTRLREG_SET	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	109	109	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	191	191	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	1	1	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	897	897	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	6	6	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	56	56	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	897	897	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	98	98	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	495	495	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	56	56	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	78	78	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 2.36 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	0
DigColPsInt_Buffer_Cnt_M_u08[0]	0
DigColPsInt_Buffer_Cnt_M_u08[1]	0
DigColPsInt_Buffer_Cnt_M_u08[2]	0
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	0
DigColPsInt_CurrentSlave_Cnt_M_u08	0
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_NOT_INITIALIZED
DigColPsInt_I2CHwCustData_Uls_M_u16	0
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	0
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	0
DigColPsInt_TransactionCnt_Cnt_M_u08	0
Flags_Cnt_T_b16	1
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	0
k_SpurSensorI2CAddress_Cnt_u08	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	0

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	0

Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	0
target_i2cREG1_temp.IMR	0
target_i2cREG1_temp.STR	0
target_i2cREG1_temp.CLKL	0
target_i2cREG1_temp.CLKH	0
target_i2cREG1_temp.CNT	0

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Input Value
target_i2cREG1_temp.DRR	0
target_i2cREG1_temp.SAR	0
target_i2cREG1_temp.DXR	0
target_i2cREG1_temp.MDR	0
target_i2cREG1_temp.IVR	0
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	0
target_i2cREG1_temp.PID11	0
target_i2cREG1_temp.PID12	0
target_i2cREG1_temp.DMAC	0
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	0
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	0
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	0	0	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	0	0	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	0	0	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	0	0	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	0	0	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	0	0	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE	INIT_COMPLETE	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	0	0	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	0	0	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	0	0	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	0	0	✔
I2c_SetStatus(Status_Cnt_T_u16)	7	7	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	0	0	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	0	0	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔

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Actual Function	Count	Expected Function	Count	Result
I2c_SetStatus	1	I2c_SetStatus	1	✔

Test Step 2.37 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	11
DigColPsInt_Buffer_Cnt_M_u08[0]	255
DigColPsInt_Buffer_Cnt_M_u08[1]	255
DigColPsInt_Buffer_Cnt_M_u08[2]	255
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	65535
DigColPsInt_CurrentSlave_Cnt_M_u08	127
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE
DigColPsInt_I2CHwCustData_Uls_M_u16	511
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	255
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1

Name	Input Value
DigColPsInt_SpurSnsrData_Cnt_M_u16	65535
DigColPsInt_TransactionCnt_Cnt_M_u08	255
Flags_Cnt_T_b16	64
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	127
k_SpurSensorI2CAddress_Cnt_u08	127
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	1023
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	255
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	32767
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	65535
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	65535
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	65535
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	255
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	1023
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	255
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	65535
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	4095
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	255
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	65535
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	255
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	32767
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	1023
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	4095
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	1023
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	255

Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	32767
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	65535
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	65535
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	65535
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	255
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	1023
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	255
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	65535
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	4095
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	255
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	65535
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	255
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	1023
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	255
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	32767
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	65535
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	65535
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	65535
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	255
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	1023
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	255
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	65535
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	4095
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	255
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	65535
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	255
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	1023
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	255
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	32767
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	65535
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	65535
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	65535
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	255
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	1023
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	255
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	65535
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	4095
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	255
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	65535
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	255
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3

Name	Input Value
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	1023
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	32767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	1023
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	4095
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	1023
target_i2cREG1_temp.IMR	255
target_i2cREG1_temp.STR	32767
target_i2cREG1_temp.CLKL	65535
target_i2cREG1_temp.CLKH	65535
target_i2cREG1_temp.CNT	65535
target_i2cREG1_temp.DRR	255
target_i2cREG1_temp.SAR	1023
target_i2cREG1_temp.DXR	255
target_i2cREG1_temp.MDR	65535
target_i2cREG1_temp.IVR	4095
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	255
target_i2cREG1_temp.PID11	65535
target_i2cREG1_temp.PID12	255
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	3
target_i2cREG1_temp.DIN	3
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	3
target_i2cREG1_temp.ODR	3
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	11	11	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	255	255	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	255	255	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	255	255	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	65535	65535	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE	READ_COMPLETE	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	511	511	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	255	255	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	5	5	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	65535	65535	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	255	255	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	1023	1023	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	255	255	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	32767	32767	✔

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	65535	65535	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	255	255	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	1023	1023	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	255	255	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	65535	65535	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	4095	4095	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	255	255	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	65535	65535	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	255	255	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023	1023	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	255	255	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	32767	32767	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	65535	65535	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	255	255	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	1023	1023	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	255	255	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	65535	65535	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	4095	4095	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	255	255	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	65535	65535	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	255	255	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	1023	1023	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	255	255	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	32767	32767	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	65535	65535	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	255	255	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	1023	1023	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	255	255	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	65535	65535	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	4095	4095	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	255	255	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	65535	65535	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	255	255	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	1023	1023	✔

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	255	255	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	32767	32767	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	65535	65535	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	255	255	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	1023	1023	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	255	255	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	65535	65535	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	4095	4095	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	255	255	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	65535	65535	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	255	255	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	1023	1023	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	255	255	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	32767	32767	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	65535	65535	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	255	255	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	1023	1023	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	255	255	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	65535	65535	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	4095	4095	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	255	255	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	65535	65535	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	255	255	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	1023	1023	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	255	255	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	32767	32767	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	65535	65535	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	255	255	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	1023	1023	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	255	255	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	65535	65535	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	4095	4095	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	255	255	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	65535	65535	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	255	255	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Case 3: Path Test ✔

Description Test Vector Description:

TS3.1(DigColPsInt_CurrentStepNo_Cnt_M_enum < INIT_SENSOR2_READERROR_SETREG) = TRUE
TS3.2"(DigColPsInt_CurrentStepNo_Cnt_M_enum < INIT_SENSOR2_READERROR_SETREG) = FALSE
(DigColPsInt_CurrentStepNo_Cnt_M_enum < INIT_COMPLETE) = TRUE"
TS3.3"(DigColPsInt_CurrentStepNo_Cnt_M_enum < INIT_SENSOR2_READERROR_SETREG) = FALSE
(DigColPsInt_CurrentStepNo_Cnt_M_enum < INIT_COMPLETE) = FALSE"
TS3.4Case : I2C_AL_INT;(DigColPsInt_CurrentStepNo_Cnt_M_enum < INIT_COMPLETE) = TRUE
TS3.5Case : I2C_AL_INT;(DigColPsInt_CurrentStepNo_Cnt_M_enum < INIT_COMPLETE) = FALSE
TS3.6"Case : INIT_SENSOR1_CHECKSTAT_READ;
((DigColPsInt_Buffer_Cnt_M_u08[0] & 0x40U) != 0U) = TRUE &&
(DigColPsInt_InitFailedOnce_Cnt_M_lgc == FALSE) = TRUE"
TS3.7"Case : INIT_SENSOR1_CHECKSTAT_READ;
((DigColPsInt_Buffer_Cnt_M_u08[0] & 0x40U) != 0U) = TRUE &&
(DigColPsInt_InitFailedOnce_Cnt_M_lgc == FALSE) = FALSE"
TS3.8"Case : INIT_SENSOR1_CHECKSTAT_READ;
((DigColPsInt_Buffer_Cnt_M_u08[0] & 0x40U) != 0U) = FALSE &&
(DigColPsInt_InitFailedOnce_Cnt_M_lgc == FALSE) = TRUE"
TS3.9" Case : INIT_SENSOR2_CHECKSTAT_READ
((DigColPsInt_Buffer_Cnt_M_u08[0] & 0x40U) != 0U) = TRUE&&
(DigColPsInt_InitFailedOnce_Cnt_M_lgc == FALSE) = TRUE"
TS3.10" Case : INIT_SENSOR2_CHECKSTAT_READ
((DigColPsInt_Buffer_Cnt_M_u08[0] & 0x40U) != 0U) = TRUE&&
(DigColPsInt_InitFailedOnce_Cnt_M_lgc == FALSE) = FALSE"
TS3.11" Case : INIT_SENSOR2_CHECKSTAT_READ
((DigColPsInt_Buffer_Cnt_M_u08[0] & 0x40U) != 0U) = FALSE&&
(DigColPsInt_InitFailedOnce_Cnt_M_lgc == FALSE) = TRUE"
TS3.12"Case : READ_SENSOR1_GETDATA;
(DigColPsInt_SkipRegisterWrite_Cnt_M_lgc == TRUE) = TRUE"
TS3.13"Case : READ_SENSOR1_GETDATA;
(DigColPsInt_SkipRegisterWrite_Cnt_M_lgc == TRUE) = FALSE"
TS3.14"case I2C_SCD_INT;
case INIT_SENSOR2_READERROR_READ:"
TS3.15"case I2C_SCD_INT;
case INIT_SENSOR1_READERROR_READ: "
TS3.16"case I2C_SCD_INT;
case INIT_SENSOR1_READEXTERR_READ:"
TS3.17"case I2C_SCD_INT;
case INIT_SENSOR2_READEXTERR_READ: "
TS3.18"case I2C_SCD_INT;
case READ_SENSOR2_GETDATA:"
TS3.19"case I2C_ARDY_INT;
case INIT_SENSOR1_READERROR_SETREG:"
TS3.20"case I2C_ARDY_INT;
case INIT_SENSOR1_READEXTERR_SETREG:"
TS3.21"case I2C_ARDY_INT;
case INIT_SENSOR1_CHECKSTAT_SETREG:"
TS3.22"case I2C_ARDY_INT;
case INIT_SENSOR2_READERROR_SETREG:"
TS3.23"case I2C_ARDY_INT;
case INIT_SENSOR2_READEXTERR_SETREG:"
TS3.24"case I2C_ARDY_INT;
case INIT_SENSOR2_CHECKSTAT_SETREG:"
TS3.25"case I2C_ARDY_INT;
case READ_SENSOR1_SETREG:"
TS3.26"case I2C_ARDY_INT;
case READ_SENSOR2_SETREG:"
TS3.27"case I2C_ARDY_INT;
case INIT_SENSOR1_SENDCMD:"
TS3.28"case I2C_ARDY_INT;
case INIT_SENSOR2_SENDCMD:"
TS3.29case INIT_SENSOR1_EXTREADCTRLREG_SENDCMD:
TS3.30case INIT_SENSOR1_DUMMY_SEND:
TS3.31case INIT_SENSOR2_EXTREADCTRLREG_SENDCMD:
TS3.32case INIT_SENSOR2_DUMMY_SEND:
TS3.33"switch (DigColPsInt_CurrentStepNo_Cnt_M_enum)
default:"
TS3.34"case I2C_NACK_INT:
(DigColPsInt_CurrentStepNo_Cnt_M_enum < INIT_SENSOR2_READERROR_SETREG)=False
(DigColPsInt_CurrentStepNo_Cnt_M_enum < INIT_COMPLETE)=True"
TS3.35"case I2C_NACK_INT:
(DigColPsInt_CurrentStepNo_Cnt_M_enum < INIT_SENSOR2_READERROR_SETREG)=False
(DigColPsInt_CurrentStepNo_Cnt_M_enum < INIT_COMPLETE)=False"
TS3.36case INIT_SENSOR1_READERROR_READ:
TS3.37case INIT_SENSOR2_READEXTERR_READ:
TS3.38case INIT_SENSOR1_EXTREADDATREG_READ:
TS3.39"case INIT_SENSOR2_EXTREADCTRLREG_READ:
(DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08 > D_MAXATTEMPTSFORCUSTDATREAD_CNT_U08)=True"
TS3.40"case INIT_SENSOR1_EXTREADCTRLREG_READ:
if((DigColPsInt_Buffer_Cnt_M_u08[1] & 0x01U) == 0x01U)=true"
TS3.41"case INIT_SENSOR2_CHECKSTAT_READ:
((DigColPsInt_Buffer_Cnt_M_u08[0] & 0x40U) != 0U)=False"
TS3.42"case INIT_SENSOR1_CHECKSTAT_READ:
((DigColPsInt_Buffer_Cnt_M_u08[0] & 0x40U) != 0U)=True"
TS3.43"case INIT_SENSOR2_CHECKSTAT_READ:
(((DigColPsInt_Buffer_Cnt_M_u08[0] & 0x40U) != 0U) && (DigColPsInt_InitFailedOnce_Cnt_M_lgc == FALSE))=true"
TS3.44case INIT_SENSOR1_READERROR_READ:
TS3.45"switch ((i2cIntFlags)Flags_Cnt_T_b16)
default:"
TS3.46case INIT_SENSOR1_DUMMY_READ:
TS3.47case INIT_SENSOR2_READERROR_READ:
TS3.48case INIT_SENSOR2_DUMMY_READ:
TS3.49case READ_SENSOR2_GETDATA:
TS3.50"switch (DigColPsInt_CurrentStepNo_Cnt_M_enum)
default:"
TS3.51case INIT_SENSOR2_EXTREADDATREG_READ:

Test Step 3.1 (Repeat Count = 1)

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	1
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	9
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Input Value
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE	INIT_COMPLETE	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	✔
I2c_SetStatus(Status_Cnt_T_u16)	7	7	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
I2c_SetStatus	1	I2c_SetStatus	1	✔

Test Step 3.2 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	4
DigColPsInt_Buffer_Cnt_M_u08[0]	28
DigColPsInt_Buffer_Cnt_M_u08[1]	56
DigColPsInt_Buffer_Cnt_M_u08[2]	100
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	7
DigColPsInt_CurrentSlave_Cnt_M_u08	120
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_NOT_INITIALIZED
DigColPsInt_I2CHwCustData_Uls_M_u16	10
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	11
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	4
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	88
DigColPsInt_TransactionCnt_Cnt_M_u08	40
Flags_Cnt_T_b16	2
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	24
k_SpurSensorI2CAddress_Cnt_u08	40

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1

Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2

TEST DETAILS REPORT

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Name	Input Value
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	65
target_i2cREG1_temp.IMR	89
target_i2cREG1_temp.STR	67
target_i2cREG1_temp.CLKL	7
target_i2cREG1_temp.CLKH	577
target_i2cREG1_temp.CNT	88
target_i2cREG1_temp.DRR	23
target_i2cREG1_temp.SAR	65
target_i2cREG1_temp.DXR	89
target_i2cREG1_temp.MDR	7
target_i2cREG1_temp.IVR	44
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	89
target_i2cREG1_temp.PID11	577
target_i2cREG1_temp.PID12	89
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	2
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	4	4	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	56	56	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	100	100	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	7	7	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	40	40	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_SETREG	INIT_SENSOR2_READERROR_SETREG	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	10	10	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	11	11	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	88	88	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	40	40	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	✔

TEST DETAILS REPORT

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
I2c_GenStopCond	1	I2c_GenStopCond	1	✔
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 3.3 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	5
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0

Name	Input Value
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	554
DigColPsInt_CurrentSlave_Cnt_M_u08	5
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE
DigColPsInt_I2CHwCustData_Uls_M_u16	13
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	14
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	123
DigColPsInt_TransactionCnt_Cnt_M_u08	50
Flags_Cnt_T_b16	1
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	29
k_SpurSensorI2CAddress_Cnt_u08	50
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788

Name	Input Value
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2
target_i2cREG1_temp.OAR	54
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	8
target_i2cREG1_temp.CLKL	554
target_i2cREG1_temp.CLKH	344
target_i2cREG1_temp.CNT	123
target_i2cREG1_temp.DRR	45
target_i2cREG1_temp.SAR	54
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	554
target_i2cREG1_temp.IVR	788
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	344
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	3
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	3
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	1
target_i2cREG1_temp.PSL	2

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	5	5	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	123	123	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	554	554	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Actual Value	Expected Value	Result
DigColPsInt_CurrentSlave_Cnt_M_u08	5	5	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE	READ_COMPLETE	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	13	13	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	14	14	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	123	123	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	50	50	✔
I2c_SetStatus(Status_Cnt_T_u16)	7	7	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788	788	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	✔

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Actual Function	Count	Expected Function	Count	Result
I2c_SetStatus	1	I2c_SetStatus	1	✔

Test Step 3.4 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8
DigColPsInt_Buffer_Cnt_M_u08[0]	28
DigColPsInt_Buffer_Cnt_M_u08[1]	56
DigColPsInt_Buffer_Cnt_M_u08[2]	100
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	20
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	22
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	23
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	80
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	44
k_SpurSensorI2CAddress_Cnt_u08	127
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204

Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556

TEST DETAILS REPORT

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Name	Input Value
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8	8	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	56	56	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	100	100	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_SET	INIT_SENSOR2_EXTREADCTRLREG_SET	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	22	22	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	23	23	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	2	2	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	80	80	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔

TEST DETAILS REPORT

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 3.5 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	10
DigColPsInt_Buffer_Cnt_M_u08[0]	0
DigColPsInt_Buffer_Cnt_M_u08[1]	0
DigColPsInt_Buffer_Cnt_M_u08[2]	0
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	566
DigColPsInt_CurrentSlave_Cnt_M_u08	30
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	28
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	29
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1

Name	Input Value
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	4
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	129
DigColPsInt_TransactionCnt_Cnt_M_u08	100
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	54
k_SpurSensorI2CAddress_Cnt_u08	120
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0

Name	Input Value
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.MDR	566
target_i2cREG1_temp.IVR	554
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	44
target_i2cREG1_temp.PID11	4466
target_i2cREG1_temp.PID12	44
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	0
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	0	0	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	0	0	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	566	566	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	120	120	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_SETREG	INIT_SENSOR2_READERROR_SETREG	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	28	28	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	29	29	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	129	129	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	100	100	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 3.6 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	6
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	2767
DigColPsInt_CurrentSlave_Cnt_M_u08	45
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	37
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	38
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	564
DigColPsInt_TransactionCnt_Cnt_M_u08	130
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	69
k_SpurSensorI2CAddress_Cnt_u08	123
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2767

Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	3
target_i2cREG1_temp.IMR	100
target_i2cREG1_temp.STR	7788
target_i2cREG1_temp.CLKL	2767
target_i2cREG1_temp.CLKH	556
target_i2cREG1_temp.CNT	564
target_i2cREG1_temp.DRR	88
target_i2cREG1_temp.SAR	3

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Name	Input Value
target_i2cREG1_temp.DXR	100
target_i2cREG1_temp.MDR	2767
target_i2cREG1_temp.IVR	9
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	100
target_i2cREG1_temp.PID11	556
target_i2cREG1_temp.PID12	100
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	3
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	3
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	6	6	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2767	2767	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	45	45	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG	INIT_SENSOR1_READERROR_SETREG	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	37	37	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	38	38	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	2	2	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	564	564	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	130	130	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	100	✔

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88	88	✔

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 3.7 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8
DigColPsInt_Buffer_Cnt_M_u08[0]	100
DigColPsInt_Buffer_Cnt_M_u08[1]	200
DigColPsInt_Buffer_Cnt_M_u08[2]	250
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	7846
DigColPsInt_CurrentSlave_Cnt_M_u08	10
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	40
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	41
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0

Name	Input Value
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	98
DigColPsInt_TransactionCnt_Cnt_M_u08	12
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	74
k_SpurSensorI2CAddress_Cnt_u08	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10

Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1

TEST DETAILS REPORT

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Name	Input Value
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1
target_i2cREG1_temp.OAR	10
target_i2cREG1_temp.IMR	10
target_i2cREG1_temp.STR	1223
target_i2cREG1_temp.CLKL	7846
target_i2cREG1_temp.CLKH	8974
target_i2cREG1_temp.CNT	98
target_i2cREG1_temp.DRR	12
target_i2cREG1_temp.SAR	10
target_i2cREG1_temp.DXR	10
target_i2cREG1_temp.MDR	7846
target_i2cREG1_temp.IVR	55
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	10
target_i2cREG1_temp.PID11	8974
target_i2cREG1_temp.PID12	10
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	1
target_i2cREG1_temp.PSL	1

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8	8	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	3	3	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	7	7	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	7846	7846	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	74	74	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADADDRREG_SEN	INIT_SENSOR1_EXTREADADDRREG_SEN	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	40	40	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	41	41	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	98	98	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	12	12	✔
I2c_Send(Length_Cnt_T_u32)	3	3	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	✔

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	✔

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Actual Function	Count	Expected Function	Count	Result
SetupWriteData	1	SetupWriteData	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 3.8 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	10
DigColPsInt_Buffer_Cnt_M_u08[0]	1
DigColPsInt_Buffer_Cnt_M_u08[1]	5
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	847
DigColPsInt_CurrentSlave_Cnt_M_u08	20
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_GETDATA
DigColPsInt_I2CHwCustData_Uls_M_u16	43
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	44
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	4
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	487
DigColPsInt_TransactionCnt_Cnt_M_u08	13
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	79
k_SpurSensorI2CAddress_Cnt_u08	110
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	24

Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2
target_i2cREG1_temp.OAR	34
target_i2cREG1_temp.IMR	24
target_i2cREG1_temp.STR	455
target_i2cREG1_temp.CLKL	847
target_i2cREG1_temp.CLKH	987
target_i2cREG1_temp.CNT	487
target_i2cREG1_temp.DRR	34
target_i2cREG1_temp.SAR	34
target_i2cREG1_temp.DXR	24
target_i2cREG1_temp.MDR	847
target_i2cREG1_temp.IVR	56
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	24

TEST DETAILS REPORT

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Name	Input Value
target_i2cREG1_temp.PID11	987
target_i2cREG1_temp.PID12	24
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	3
target_i2cREG1_temp.DIN	3
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	2
target_i2cREG1_temp.CLR	3
target_i2cREG1_temp.ODR	3
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	2

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	38	38	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	5	5	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	9	9	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	261	261	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	110	110	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_SETREG	READ_SENSOR2_SETREG	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	43	43	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	44	44	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	487	487	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	13	13	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987	987	✔

TEST DETAILS REPORT

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 3.9 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	30
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_GETDATA
DigColPsInt_I2CHwCustData_Uls_M_u16	46
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	47
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	14
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str

Name	Input Value
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	84
k_SpurSensorI2CAddress_Cnt_u08	120
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87

Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309

Name	Input Value
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2580	2580	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	120	120	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_GETDATA	READ_SENSOR2_GETDATA	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	46	46	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	47	47	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	5	5	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	14	14	✔
I2c_SetRecv(Length_Cnt_T_u32)	2	2	✔
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
SetupRead	1	SetupRead	1	✔
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	✔
I2c_SetRecv	1	I2c_SetRecv	1	✔

Test Step 3.10 (Repeat Count = 1)	✔
Name	**Input Value**
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	566
DigColPsInt_CurrentSlave_Cnt_M_u08	30
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READEXTERR_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	67
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	68
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	4
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	129
DigColPsInt_TransactionCnt_Cnt_M_u08	100
Flags_Cnt_T_b16	2
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	0
k_SpurSensorI2CAddress_Cnt_u08	120
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1

Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.MDR	566
target_i2cREG1_temp.IVR	554
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	44
target_i2cREG1_temp.PID11	4466
target_i2cREG1_temp.PID12	44
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2

TEST DETAILS REPORT

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Name	Input Value
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	0
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3	3	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	3	3	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	7	7	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	566	566	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	0	0	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADADDRREG_SEN	INIT_SENSOR1_EXTREADADDRREG_SEN	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	67	67	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	68	68	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	129	129	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	100	100	✔
I2c_Send(Length_Cnt_T_u32)	3	3	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	✔

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
I2c_GenStopCond	1	I2c_GenStopCond	1	✔
SetupWriteData	1	SetupWriteData	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 3.11 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	0
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	2767
DigColPsInt_CurrentSlave_Cnt_M_u08	45
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	76
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	77
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	564
DigColPsInt_TransactionCnt_Cnt_M_u08	130
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str

Name	Input Value
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	7
k_SpurSensorI2CAddress_Cnt_u08	123
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767

Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3

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Name	Input Value
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	3
target_i2cREG1_temp.IMR	100
target_i2cREG1_temp.STR	7788
target_i2cREG1_temp.CLKL	2767
target_i2cREG1_temp.CLKH	556
target_i2cREG1_temp.CNT	564
target_i2cREG1_temp.DRR	88
target_i2cREG1_temp.SAR	3
target_i2cREG1_temp.DXR	100
target_i2cREG1_temp.MDR	2767
target_i2cREG1_temp.IVR	9
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	100
target_i2cREG1_temp.PID11	556
target_i2cREG1_temp.PID12	100
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	3
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	3
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2767	2767	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	7	7	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_SET	INIT_SENSOR1_EXTREADCTRLREG_SET	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	76	76	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	77	77	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	2	2	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	564	564	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	130	130	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100	100	✔

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88	88	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 3.12 (Repeat Count = 1)	✔
Name	**Input Value**
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	11
DigColPsInt_Buffer_Cnt_M_u08[0]	100
DigColPsInt_Buffer_Cnt_M_u08[1]	200
DigColPsInt_Buffer_Cnt_M_u08[2]	250
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	7846
DigColPsInt_CurrentSlave_Cnt_M_u08	10
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	79
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	80
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	98
DigColPsInt_TransactionCnt_Cnt_M_u08	12
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	11
k_SpurSensorI2CAddress_Cnt_u08	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1

Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1
target_i2cREG1_temp.OAR	10
target_i2cREG1_temp.IMR	10
target_i2cREG1_temp.STR	1223
target_i2cREG1_temp.CLKL	7846
target_i2cREG1_temp.CLKH	8974
target_i2cREG1_temp.CNT	98
target_i2cREG1_temp.DRR	12
target_i2cREG1_temp.SAR	10
target_i2cREG1_temp.DXR	10
target_i2cREG1_temp.MDR	7846
target_i2cREG1_temp.IVR	55
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	10
target_i2cREG1_temp.PID11	8974
target_i2cREG1_temp.PID12	10
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2

TEST DETAILS REPORT

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Name	Input Value
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	1
target_i2cREG1_temp.PSL	1

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	12	12	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	14	14	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	200	200	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	250	250	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	7846	7846	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	11	11	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT SENSOR1 EXTREADDATREG SETR	INIT SENSOR1 EXTREADDATREG SETR	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	79	79	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	80	80	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	98	98	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	12	12	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 3.13 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str

Name	Input Value
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	9
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5

Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66

Name	Input Value
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ	INIT_SENSOR1_READERROR_READ	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔

TEST DETAILS REPORT

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔

TEST DETAILS REPORT

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	✔
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	✔
I2c_SetRecv	1	I2c_SetRecv	1	✔

Test Step 3.14 (Repeat Count = 1)

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	9
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556

Name	Input Value
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_READ	INIT_SENSOR1_READEXTERR_READ	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	✔
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	✔
I2c_SetRecv	1	I2c_SetRecv	1	✔

Test Step 3.15 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp

Name	Input Value
k_ColSensorI2CAddress_Cnt_u08	9
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3

Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2

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Name	Input Value
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ	INIT_SENSOR1_CHECKSTAT_READ	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✔

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	✔
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	✔
I2c_SetRecv	1	I2c_SetRecv	1	✔

Test Step 3.16 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1

Name	Input Value
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	9
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3

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Name	Input Value
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	✔

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Name	Actual Value	Expected Value	Result
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_READ	INIT_SENSOR2_READERROR_READ	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	✔
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	✔
I2c_SetRecv	1	I2c_SetRecv	1	✔

Test Step 3.17 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READEXTERR_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	9
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204

Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Input Value
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READEXTERR_READ	INIT_SENSOR2_READEXTERR_READ	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

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Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	✔
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	✔
I2c_SetRecv	1	I2c_SetRecv	1	✔

Test Step 3.18 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1

Name	Input Value
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	9
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3

Name	Input Value
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_READ	INIT_SENSOR2_CHECKSTAT_READ	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66		

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

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Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	✔
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	✔
I2c_SetRecv	1	I2c_SetRecv	1	✔

Test Step 3.19 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	9
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204

Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3

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Name	Input Value
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_REA	INIT_SENSOR1_EXTREADCTRLREG_REA	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔

TEST DETAILS REPORT

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

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Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	✔
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	✔
I2c_SetRecv	1	I2c_SetRecv	1	✔

Test Step 3.20 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str

Name	Input Value
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	9
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67

Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204

Name	Input Value
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_REA	INIT_SENSOR2_EXTREADCTRLREG_REA	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
SetupRead	1	SetupRead	1	✔
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	✔
I2c_SetRecv	1	I2c_SetRecv	1	✔

Test Step 3.21 (Repeat Count = 1)	✔
Name	**Input Value**
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADDATREG_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	9
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3

Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1

TEST DETAILS REPORT

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Name	Input Value
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADDATREG_READ	INIT_SENSOR1_EXTREADDATREG_READ	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

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Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	✔
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	✔
I2c_SetRecv	1	I2c_SetRecv	1	✔

Test Step 3.22 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADDATREG_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32

Name	Input Value
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	9
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66

Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5

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Name	Input Value
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADDATREG_READ	INIT_SENSOR2_EXTREADDATREG_READ	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
SetupRead	1	SetupRead	1	✔
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	✔
I2c_SetRecv	1	I2c_SetRecv	1	✔

Test Step 3.23 (Repeat Count = 1)

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	9
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Input Value
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_GETDATA	READ_SENSOR1_GETDATA	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

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Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	✔
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	✔
I2c_SetRecv	1	I2c_SetRecv	1	✔

Test Step 3.24 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	9

Name	Input Value
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1

Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3

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Name	Input Value
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_GETDATA	READ_SENSOR2_GETDATA	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	✔
I2c_SetRecv(Length_Cnt_T_u32)	2	2	✔
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	✔
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	✔
I2c_SetRecv	1	I2c_SetRecv	1	✔

Test Step 3.25 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_Igc	0

Name	Input Value
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_SENDCMD
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	9
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5

Name	Input Value
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	32	32	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_SETREG	INIT_SENSOR1_CHECKSTAT_SETREG	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 3.26 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_SENDCMD
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	9
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309

Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66

TEST DETAILS REPORT

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Name	Input Value
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	32	32	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_SETREG	INIT_SENSOR2_CHECKSTAT_SETREG	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	✔

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 3.27 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADADDRREG_SENDCMD
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2

Name	Input Value
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	9
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1

TEST DETAILS REPORT

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Name	Input Value
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	128	128	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	0	0	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_SEN	INIT_SENSOR1_EXTREADCTRLREG_SEN	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Actual Value	Expected Value	Result
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5

Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66

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Name	Input Value
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	128	128	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	0	0	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_SEN	INIT_SENSOR2_EXTREADCTRLREG_SEN	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	✔
I2c_Send(Length_Cnt_T_u32)	3	3	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

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Actual Function	Count	Expected Function	Count	Result
SetupWriteData	1	SetupWriteData	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 3.29 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_SENDCMD
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0

Name	Input Value
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	9
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66

Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3

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Name	Input Value
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	32	32	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_DUMMY_SEND	INIT_SENSOR1_DUMMY_SEND	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	✔

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 3.30 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_DUMMY_SEND
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	9
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3

Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Input Value
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_DUMMY_READ	INIT_SENSOR1_DUMMY_READ	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	✔
I2c_SetRecv(Length_Cnt_T_u32)	2	2	✔
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

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Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	✔
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	✔
I2c_SetRecv	1	I2c_SetRecv	1	✔

Test Step 3.31 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_SENDCMD
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str

Name	Input Value
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	9
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67

Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204

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Name	Input Value
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	0	0	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	32	32	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_DUMMY_SEND	INIT_SENSOR2_DUMMY_SEND	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	✔

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 3.32 (Repeat Count = 1)	✔
Name	**Input Value**
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_DUMMY_SEND
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	9
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3

Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Input Value
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_DUMMY_READ	INIT_SENSOR2_DUMMY_READ	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	✔
I2c_SetRecv(Length_Cnt_T_u32)	2	2	✔
I2c_SetupMasterReceive(DataLength_Cnt_T_u16)	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
SetupRead	1	SetupRead	1	✔
I2c_SetupMasterReceive	1	I2c_SetupMasterReceive	1	✔
I2c_SetRecv	1	I2c_SetRecv	1	✔

Test Step 3.33 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	123
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADDATREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	1
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	0
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	10
Flags_Cnt_T_b16	4
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str

Name	Input Value
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	9
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5

Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Input Value
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	1	1	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADDATREG_READ	INIT_SENSOR1_EXTREADDATREG_READ	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	1	1	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	2	2	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	0	0	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
[redacted]	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
[redacted]	67	67	

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
none	0	*** No Call Expected ***	0	✔

Test Step 3.34 (Repeat Count = 1)

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	566
DigColPsInt_CurrentSlave_Cnt_M_u08	30
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADDATREG_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	67
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	68
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	4
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	129
DigColPsInt_TransactionCnt_Cnt_M_u08	100
Flags_Cnt_T_b16	2
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	0
k_SpurSensorI2CAddress_Cnt_u08	120
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Input Value
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.MDR	566
target_i2cREG1_temp.IVR	554
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	44
target_i2cREG1_temp.PID11	4466
target_i2cREG1_temp.PID12	44
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	0
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3	3	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	123	123	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	566	566	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	30	30	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE	INIT_COMPLETE	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	67	67	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	68	68	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	129	129	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	100	100	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔

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DigColPsInt_InterruptNotification

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
I2c_GenStopCond	1	I2c_GenStopCond	1	✔

Test Step 3.35 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	566
DigColPsInt_CurrentSlave_Cnt_M_u08	30
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR1_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	67
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	68
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	4
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	129
DigColPsInt_TransactionCnt_Cnt_M_u08	100
Flags_Cnt_T_b16	2
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	0
k_SpurSensorI2CAddress_Cnt_u08	120
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3

Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2

Name	Input Value
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.MDR	566
target_i2cREG1_temp.IVR	554
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	44
target_i2cREG1_temp.PID11	4466
target_i2cREG1_temp.PID12	44
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	0
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3	3	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	123	123	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	566	566	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	30	30	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE	READ_COMPLETE	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	67	67	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	68	68	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	129	129	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	100	100	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
I2c_GenStopCond	1	I2c_GenStopCond	1	✔

Test Step 3.36 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	566
DigColPsInt_CurrentSlave_Cnt_M_u08	30
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	67

Name	Input Value
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	68
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	4
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	129
DigColPsInt_TransactionCnt_Cnt_M_u08	100
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	0
k_SpurSensorI2CAddress_Cnt_u08	120
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1

Name	Input Value
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.MDR	566
target_i2cREG1_temp.IVR	554
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	44
target_i2cREG1_temp.PID11	4466
target_i2cREG1_temp.PID12	44
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	0
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3	3	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	30	30	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	7	7	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	70	70	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	566	566	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	30	30	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_SENDCMD	INIT_SENSOR1_SENDCMD	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	67	67	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	68	68	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Actual Value	Expected Value	Result
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	129	129	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	100	100	✔
I2c_Send(Length_Cnt_T_u32)	3	3	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

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Actual Function	Count	Expected Function	Count	Result
SetupWriteData	1	SetupWriteData	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 3.37 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	566
DigColPsInt_CurrentSlave_Cnt_M_u08	30
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READEXTERR_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	67
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	68
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	4
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	129
DigColPsInt_TransactionCnt_Cnt_M_u08	100
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	0
k_SpurSensorI2CAddress_Cnt_u08	120
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567

Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129

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Name	Input Value
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.MDR	566
target_i2cREG1_temp.IVR	554
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	44
target_i2cREG1_temp.PID11	4466
target_i2cREG1_temp.PID12	44
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	0
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3	3	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	30	30	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	7	7	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	70	70	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	566	566	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	30	30	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_SENDCMD	INIT_SENSOR2_SENDCMD	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	67	67	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	68	68	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	129	129	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	100	100	✔
I2c_Send(Length_Cnt_T_u32)	3	3	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	✔

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
SetupWriteData	1	SetupWriteData	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 3.38 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	566
DigColPsInt_CurrentSlave_Cnt_M_u08	30
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADDATREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	67
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	68
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	4
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1

Name	Input Value
DigColPsInt_RecvdDataType_Cnt_M_u08	4
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	129
DigColPsInt_TransactionCnt_Cnt_M_u08	100
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	0
k_SpurSensorI2CAddress_Cnt_u08	120
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Input Value
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.MDR	566
target_i2cREG1_temp.IVR	554
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	44
target_i2cREG1_temp.PID11	4466
target_i2cREG1_temp.PID12	44
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	0
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3	3	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	14	14	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	566	566	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	120	120	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADDATREG_SETR	INIT_SENSOR2_EXTREADDATREG_SETR	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	67	67	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	9	9	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	4	4	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	129	129	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	100	100	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Actual Value	Expected Value	Result
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

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Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 3.39 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	11
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	2767
DigColPsInt_CurrentSlave_Cnt_M_u08	45
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	76
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	77
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	564
DigColPsInt_TransactionCnt_Cnt_M_u08	130
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	7
k_SpurSensorI2CAddress_Cnt_u08	123
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100

Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	3
target_i2cREG1_temp.IMR	100
target_i2cREG1_temp.STR	7788
target_i2cREG1_temp.CLKL	2767
target_i2cREG1_temp.CLKH	556
target_i2cREG1_temp.CNT	564
target_i2cREG1_temp.DRR	88
target_i2cREG1_temp.SAR	3
target_i2cREG1_temp.DXR	100
target_i2cREG1_temp.MDR	2767
target_i2cREG1_temp.IVR	9

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Name	Input Value
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	100
target_i2cREG1_temp.PID11	556
target_i2cREG1_temp.PID12	100
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	3
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	3
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	12	12	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	123	123	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2767	2767	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	45	45	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE	INIT_COMPLETE	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	76	76	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	77	77	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	2	2	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	564	564	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	130	130	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 3.40 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8
DigColPsInt_Buffer_Cnt_M_u08[0]	1
DigColPsInt_Buffer_Cnt_M_u08[1]	1
DigColPsInt_Buffer_Cnt_M_u08[2]	100
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	2309
DigColPsInt_CurrentSlave_Cnt_M_u08	20
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	22
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	23
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	87
DigColPsInt_TransactionCnt_Cnt_M_u08	80
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str

Name	Input Value
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	44
k_SpurSensorI2CAddress_Cnt_u08	127
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87

Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309

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Name	Input Value
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	55
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	556
target_i2cREG1_temp.CLKL	2309
target_i2cREG1_temp.CLKH	1204
target_i2cREG1_temp.CNT	87
target_i2cREG1_temp.DRR	67
target_i2cREG1_temp.SAR	55
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	2309
target_i2cREG1_temp.IVR	5
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	1204
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8	8	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	1	1	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	100	100	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2309	2309	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADCTRLREG_SET	INIT_SENSOR2_EXTREADCTRLREG_SET	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	22	22	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	23	23	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	2	2	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	87	87	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	80	80	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	556	556	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	87	87	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2309	2309	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	5	5	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	1204	1204	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 3.41 (Repeat Count = 1)	✔
Name	**Input Value**
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8
DigColPsInt_Buffer_Cnt_M_u08[0]	28
DigColPsInt_Buffer_Cnt_M_u08[1]	200
DigColPsInt_Buffer_Cnt_M_u08[2]	250
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	7846
DigColPsInt_CurrentSlave_Cnt_M_u08	10
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	40
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	41
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	98
DigColPsInt_TransactionCnt_Cnt_M_u08	12
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	74
k_SpurSensorI2CAddress_Cnt_u08	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1

Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1
target_i2cREG1_temp.OAR	10
target_i2cREG1_temp.IMR	10
target_i2cREG1_temp.STR	1223
target_i2cREG1_temp.CLKL	7846
target_i2cREG1_temp.CLKH	8974
target_i2cREG1_temp.CNT	98
target_i2cREG1_temp.DRR	12
target_i2cREG1_temp.SAR	10
target_i2cREG1_temp.DXR	10
target_i2cREG1_temp.MDR	7846
target_i2cREG1_temp.IVR	55
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	10
target_i2cREG1_temp.PID11	8974
target_i2cREG1_temp.PID12	10
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2

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Name	Input Value
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	1
target_i2cREG1_temp.PSL	1

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8	8	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	3	3	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	7	7	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	7846	7846	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	74	74	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADADDRREG_SEN	INIT_SENSOR1_EXTREADADDRREG_SEN	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	40	40	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	41	41	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	98	98	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	12	12	✔
I2c_Send(Length_Cnt_T_u32)	3	3	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10	10	

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
SetupWriteData	1	SetupWriteData	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 3.42 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	6
DigColPsInt_Buffer_Cnt_M_u08[0]	123
DigColPsInt_Buffer_Cnt_M_u08[1]	145
DigColPsInt_Buffer_Cnt_M_u08[2]	200
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	2767
DigColPsInt_CurrentSlave_Cnt_M_u08	45
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_CHECKSTAT_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	37
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	38
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	2
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	564
DigColPsInt_TransactionCnt_Cnt_M_u08	130
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str

Name	Input Value
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	69
k_SpurSensorI2CAddress_Cnt_u08	123
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9

Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100

Name	Input Value
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	3
target_i2cREG1_temp.IMR	100
target_i2cREG1_temp.STR	7788
target_i2cREG1_temp.CLKL	2767
target_i2cREG1_temp.CLKH	556
target_i2cREG1_temp.CNT	564
target_i2cREG1_temp.DRR	88
target_i2cREG1_temp.SAR	3
target_i2cREG1_temp.DXR	100
target_i2cREG1_temp.MDR	2767
target_i2cREG1_temp.IVR	9
target_i2cREG1_temp.EMDR	0
target_i2cREG1_temp.PSC	100
target_i2cREG1_temp.PID11	556
target_i2cREG1_temp.PID12	100
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	1
target_i2cREG1_temp.DIN	3
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	0
target_i2cREG1_temp.CLR	1
target_i2cREG1_temp.ODR	3
target_i2cREG1_temp.PD	0
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	6	6	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	145	145	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	200	200	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	2767	2767	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	123	123	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_SETREG	INIT_SENSOR2_READERROR_SETREG	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	37	37	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	38	38	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	2	2	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	564	564	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	130	130	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔

TEST DETAILS REPORT

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	3	3	✔

TEST DETAILS REPORT

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	7788	7788	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	2767	2767	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	564	564	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	88	88	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	2767	2767	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	9	9	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	556	556	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	100	100	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 3.43 (Repeat Count = 1)	✔
Name	**Input Value**
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8
DigColPsInt_Buffer_Cnt_M_u08[0]	100
DigColPsInt_Buffer_Cnt_M_u08[1]	200
DigColPsInt_Buffer_Cnt_M_u08[2]	250
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	7846
DigColPsInt_CurrentSlave_Cnt_M_u08	10
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_CHECKSTAT_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	40
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	41
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	3
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	98
DigColPsInt_TransactionCnt_Cnt_M_u08	12
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	74
k_SpurSensorI2CAddress_Cnt_u08	100
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1

Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1
target_i2cREG1_temp.OAR	10
target_i2cREG1_temp.IMR	10
target_i2cREG1_temp.STR	1223
target_i2cREG1_temp.CLKL	7846
target_i2cREG1_temp.CLKH	8974
target_i2cREG1_temp.CNT	98
target_i2cREG1_temp.DRR	12
target_i2cREG1_temp.SAR	10
target_i2cREG1_temp.DXR	10
target_i2cREG1_temp.MDR	7846
target_i2cREG1_temp.IVR	55
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	10
target_i2cREG1_temp.PID11	8974
target_i2cREG1_temp.PID12	10
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Input Value
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	1
target_i2cREG1_temp.PSL	1

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8	8	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	36	36	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	200	200	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	250	250	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	7846	7846	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	10	10	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_SETREG	INIT_SENSOR2_READERROR_SETREG	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	40	40	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	41	41	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	98	98	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	12	12	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	10	10	

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	1223	1223	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7846	7846	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	8974	8974	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	98	98	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7846	7846	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	55	55	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	8974	8974	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	10	10	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 3.44 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2
DigColPsInt_Buffer_Cnt_M_u08[0]	255
DigColPsInt_Buffer_Cnt_M_u08[1]	255
DigColPsInt_Buffer_Cnt_M_u08[2]	255
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	7
DigColPsInt_CurrentSlave_Cnt_M_u08	35
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READERROR_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	31
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	32
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	88
DigColPsInt_TransactionCnt_Cnt_M_u08	110
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str

Name	Input Value
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	59
k_SpurSensorI2CAddress_Cnt_u08	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44

Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89

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Name	Input Value
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	65
target_i2cREG1_temp.IMR	89
target_i2cREG1_temp.STR	67
target_i2cREG1_temp.CLKL	7
target_i2cREG1_temp.CLKH	577
target_i2cREG1_temp.CNT	88
target_i2cREG1_temp.DRR	23
target_i2cREG1_temp.SAR	65
target_i2cREG1_temp.DXR	89
target_i2cREG1_temp.MDR	7
target_i2cREG1_temp.IVR	44
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	89
target_i2cREG1_temp.PID11	577
target_i2cREG1_temp.PID12	89
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	2
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2	2	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	38	38	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	255	255	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	255	255	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	7	7	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	35	35	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_SETREG	INIT_SENSOR1_READEXTERR_SETREG	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	31	31	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	32	32	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	5	5	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	88	88	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	110	110	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7	7	✔

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65	65	✔

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔

T				✔
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 3.45 (Repeat Count = 1)	✔
Name	**Input Value**
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	11
DigColPsInt_Buffer_Cnt_M_u08[0]	255
DigColPsInt_Buffer_Cnt_M_u08[1]	255
DigColPsInt_Buffer_Cnt_M_u08[2]	255
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	65535
DigColPsInt_CurrentSlave_Cnt_M_u08	127
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE
DigColPsInt_I2CHwCustData_Uls_M_u16	511
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	255
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	65535
DigColPsInt_TransactionCnt_Cnt_M_u08	255
Flags_Cnt_T_b16	64
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	127
k_SpurSensorI2CAddress_Cnt_u08	127
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	1023
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	255
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	32767
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	65535
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	65535
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	65535
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	255
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	1023
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	255
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	65535
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	4095
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	255
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	65535
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	255
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	32767
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	1023
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	4095
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	65535
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	255
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	1023
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	255
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	32767
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	65535
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	65535
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	65535
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	255
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	1023
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	255
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	65535
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	4095
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	255
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	65535
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	255
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	1023
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	255
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	32767
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	65535
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	65535
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	65535
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	255
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	1023
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	255
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	65535
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	4095
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	255
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	65535
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	255
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3

Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	1023
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	255
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	32767
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	65535
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	65535
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	65535
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	255
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	1023
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	255
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	65535
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	4095
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	255
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	65535
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	255
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	1023
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	32767
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	1023
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	4095
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	65535
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	255
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	1023
target_i2cREG1_temp.IMR	255
target_i2cREG1_temp.STR	32767
target_i2cREG1_temp.CLKL	65535
target_i2cREG1_temp.CLKH	65535
target_i2cREG1_temp.CNT	65535
target_i2cREG1_temp.DRR	255
target_i2cREG1_temp.SAR	1023
target_i2cREG1_temp.DXR	255
target_i2cREG1_temp.MDR	65535
target_i2cREG1_temp.IVR	4095
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	255
target_i2cREG1_temp.PID11	65535
target_i2cREG1_temp.PID12	255
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	3

TEST DETAILS REPORT

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Name	Input Value
target_i2cREG1_temp.DIN	3
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	3
target_i2cREG1_temp.ODR	3
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	11	11	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	255	255	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	255	255	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	255	255	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	65535	65535	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE	READ_COMPLETE	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	511	511	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	255	255	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	5	5	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	65535	65535	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	255	255	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	1023	1023	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	255	255	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	32767	32767	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	65535	65535	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	255	255	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	1023	1023	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	255	255	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	65535	65535	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	4095	4095	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	255	255	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	65535	65535	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	255	255	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	1023	1023	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	255	255	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	32767	32767	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	65535	65535	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	255	255	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	1023	1023	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	255	255	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	65535	65535	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	4095	4095	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	255	255	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	65535	65535	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	255	255	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	1023	1023	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	255	255	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	32767	32767	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	65535	65535	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	255	255	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	1023	1023	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	255	255	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	65535	65535	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	4095	4095	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	255	255	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	65535	65535	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	255	255	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	1023	1023	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	255	255	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	32767	32767	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	65535	65535	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	255	255	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	1023	1023	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	255	255	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	65535	65535	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	4095	4095	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	255	255	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	65535	65535	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	255	255	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	1023	1023	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	255	255	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	32767	32767	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	65535	65535	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	255	255	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	1023	1023	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	255	255	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	65535	65535	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	4095	4095	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	255	255	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	65535	65535	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	255	255	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	1023	1023	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	255	255	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	32767	32767	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	65535	65535	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	65535	65535	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	65535	65535	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	255	255	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	1023	1023	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	255	255	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	65535	65535	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	4095	4095	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	255	255	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	65535	65535	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	255	255	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 3.46 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	7
DigColPsInt_Buffer_Cnt_M_u08[0]	1
DigColPsInt_Buffer_Cnt_M_u08[1]	5
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	847
DigColPsInt_CurrentSlave_Cnt_M_u08	15
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_DUMMY_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	19
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	20
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	1
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	487
DigColPsInt_TransactionCnt_Cnt_M_u08	70
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36

Name	Input Value
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	39
k_SpurSensorI2CAddress_Cnt_u08	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	24

Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Input Value
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2
target_i2cREG1_temp.OAR	34
target_i2cREG1_temp.IMR	24
target_i2cREG1_temp.STR	455
target_i2cREG1_temp.CLKL	847
target_i2cREG1_temp.CLKH	987
target_i2cREG1_temp.CNT	487
target_i2cREG1_temp.DRR	34
target_i2cREG1_temp.SAR	34
target_i2cREG1_temp.DXR	24
target_i2cREG1_temp.MDR	847
target_i2cREG1_temp.IVR	56
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	24
target_i2cREG1_temp.PID11	987
target_i2cREG1_temp.PID12	24
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	3
target_i2cREG1_temp.DIN	3
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	2
target_i2cREG1_temp.CLR	3
target_i2cREG1_temp.ODR	3
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	2

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	7	7	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	3	3	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	7	7	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	847	847	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	0	0	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADADDRREG_SEN	INIT_SENSOR2_EXTREADADDRREG_SEN	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	19	19	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	20	20	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	1	1	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	487	487	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	70	70	✔
I2c_Send(Length_Cnt_T_u32)	3	3	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	987	987	✔

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	34	34	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	24	24	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	455	455	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	847	847	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	987	987	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	487	487	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	34	34	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	34	34	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	24	24	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	847	847	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	24	24	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	987	987	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	24	24	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	✔

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Actual Function	Count	Expected Function	Count	Result
SetupWriteData	1	SetupWriteData	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 3.47 (Repeat Count = 1)

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	4
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	20
DigColPsInt_Buffer_Cnt_M_u08[2]	30
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	554
DigColPsInt_CurrentSlave_Cnt_M_u08	40
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READERROR_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	34
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	35
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	0
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	123
DigColPsInt_TransactionCnt_Cnt_M_u08	120
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	64
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554

TEST DETAILS REPORT

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Name	Input Value
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2
target_i2cREG1_temp.OAR	54
target_i2cREG1_temp.IMR	66
target_i2cREG1_temp.STR	8
target_i2cREG1_temp.CLKL	554
target_i2cREG1_temp.CLKH	344
target_i2cREG1_temp.CNT	123
target_i2cREG1_temp.DRR	45
target_i2cREG1_temp.SAR	54
target_i2cREG1_temp.DXR	66
target_i2cREG1_temp.MDR	554
target_i2cREG1_temp.IVR	788
target_i2cREG1_temp.EMDR	3
target_i2cREG1_temp.PSC	66
target_i2cREG1_temp.PID11	344
target_i2cREG1_temp.PID12	66
target_i2cREG1_temp.DMAC	3
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	3
target_i2cREG1_temp.DIN	2
target_i2cREG1_temp.DOUT	3
target_i2cREG1_temp.SET	3
target_i2cREG1_temp.CLR	3
target_i2cREG1_temp.ODR	2
target_i2cREG1_temp.PD	1
target_i2cREG1_temp.PSL	2

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	4	4	✔

TEST DETAILS REPORT

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Name	Actual Value	Expected Value	Result
DigColPsInt_Buffer_Cnt_M_u08[0]	38	38	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	20	20	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	30	30	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	554	554	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	40	40	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_READEXTERR_SETREG	INIT_SENSOR2_READEXTERR_SETREG	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	34	34	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	35	35	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	1	1	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	1	1	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	123	123	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	120	120	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	8	8	✔

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	54	54	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	54	54	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	8	8	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	344	344	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	123	123	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	45	45	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	54	54	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	788	788	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	344	344	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	2	2	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 3.48 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	4
DigColPsInt_Buffer_Cnt_M_u08[0]	100
DigColPsInt_Buffer_Cnt_M_u08[1]	200
DigColPsInt_Buffer_Cnt_M_u08[2]	250
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	7
DigColPsInt_CurrentSlave_Cnt_M_u08	35
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_DUMMY_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	70
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	71
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	5
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	88
DigColPsInt_TransactionCnt_Cnt_M_u08	110
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14

Name	Input Value
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	127
k_SpurSensorI2CAddress_Cnt_u08	5
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2

Name	Input Value
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Input Value
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0
target_i2cREG1_temp.OAR	65
target_i2cREG1_temp.IMR	89
target_i2cREG1_temp.STR	67
target_i2cREG1_temp.CLKL	7
target_i2cREG1_temp.CLKH	577
target_i2cREG1_temp.CNT	88
target_i2cREG1_temp.DRR	23
target_i2cREG1_temp.SAR	65
target_i2cREG1_temp.DXR	89
target_i2cREG1_temp.MDR	7
target_i2cREG1_temp.IVR	44
target_i2cREG1_temp.EMDR	2
target_i2cREG1_temp.PSC	89
target_i2cREG1_temp.PID11	577
target_i2cREG1_temp.PID12	89
target_i2cREG1_temp.DMAC	2
target_i2cREG1_temp.FUN	0
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	2
target_i2cREG1_temp.SET	2
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	0

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	4	4	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	12	12	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	200	200	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	250	250	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	0	0	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	7	7	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	127	127	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_EXTREADCTRLREG_SET	INIT_SENSOR1_EXTREADCTRLREG_SET	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	70	70	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	71	71	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	5	5	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	88	88	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	110	110	✔
I2c_Send(Length_Cnt_T_u32)	1	1	✔
I2c_SetupMasterTransmit(DataLength_Cnt_T_u16)	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	✔

TEST DETAILS REPORT

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	0	0	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Actual Value	Expected Value	Result
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	65	65	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	67	67	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	7	7	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	577	577	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	88	88	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	23	23	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	65	65	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	7	7	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	577	577	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	89	89	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	0	0	✔

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Actual Function	Count	Expected Function	Count	Result
SetupWriteRegister	1	SetupWriteRegister	1	✔
I2c_SetupMasterTransmit	1	I2c_SetupMasterTransmit	1	✔
I2c_Send	1	I2c_Send	1	✔

Test Step 3.49 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2
DigColPsInt_Buffer_Cnt_M_u08[0]	1
DigColPsInt_Buffer_Cnt_M_u08[1]	5

Name	Input Value
DigColPsInt_Buffer_Cnt_M_u08[2]	9
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0
DigColPsInt_ColSnsrData_Cnt_M_u16	56
DigColPsInt_CurrentSlave_Cnt_M_u08	90
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_SENSOR2_GETDATA
DigColPsInt_I2CHwCustData_Uls_M_u16	64
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	65
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1
DigColPsInt_RecvdDataType_Cnt_M_u08	1
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	7878
DigColPsInt_TransactionCnt_Cnt_M_u08	100
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	114
k_SpurSensorI2CAddress_Cnt_u08	30
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	678
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	45
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	66
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	6788
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	7878
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	678
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	45
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	56
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	778
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	45
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	6788
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	45
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	678
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	66
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	6788
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	7878
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	678
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	56
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	778

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	6788
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	45
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	678
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	45
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	66
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	6788
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	7878
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	678
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	45
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	56
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	778
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	45
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	6788
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	45
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	678
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	45
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	66
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	6788
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	7878
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	678
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	45
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	56
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	778
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	45
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	6788
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	45
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	678
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	45
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	66
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	6788
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	7878
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	678
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	45

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Name	Input Value
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	56
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	778
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	45
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	6788
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	45
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	678
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	66
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	6788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	7878
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	678
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	56
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	778
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	6788
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	45
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1
target_i2cREG1_temp.OAR	678
target_i2cREG1_temp.IMR	45
target_i2cREG1_temp.STR	66
target_i2cREG1_temp.CLKL	56
target_i2cREG1_temp.CLKH	6788
target_i2cREG1_temp.CNT	7878
target_i2cREG1_temp.DRR	12
target_i2cREG1_temp.SAR	678
target_i2cREG1_temp.DXR	45
target_i2cREG1_temp.MDR	56
target_i2cREG1_temp.IVR	778
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	45
target_i2cREG1_temp.PID11	6788
target_i2cREG1_temp.PID12	45
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	0
target_i2cREG1_temp.DIN	1
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	0
target_i2cREG1_temp.ODR	1
target_i2cREG1_temp.PD	2
target_i2cREG1_temp.PSL	1

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	2	2	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	1	1	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	5	5	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	9	9	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔

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Name	Actual Value	Expected Value	Result
DigColPsInt_ColCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	56	56	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	90	90	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	READ_COMPLETE	READ_COMPLETE	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	64	64	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	65	65	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	3	3	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	261	261	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	101	101	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	678	678	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	45	45	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	66	66	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	56	56	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	7878	7878	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	678	678	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	45	45	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	56	56	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	778	778	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	45	45	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	6788	6788	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	45	45	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	678	678	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	45	45	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	66	66	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	7878	7878	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	678	678	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	45	45	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	56	56	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	778	778	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	45	45	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	6788	6788	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	45	45	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	678	678	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	45	45	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	66	66	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	56	56	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	7878	7878	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	678	678	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	45	45	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	56	56	✔

TEST DETAILS REPORT

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	778	778	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	45	45	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	6788	6788	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	45	45	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	678	678	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	45	45	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	66	66	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	56	56	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	7878	7878	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	678	678	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	45	45	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	56	56	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	778	778	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	45	45	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	6788	6788	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	45	45	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	678	678	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	45	45	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	66	66	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	56	56	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	7878	7878	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	678	678	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	45	45	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	56	56	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	778	778	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	45	45	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	6788	6788	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	45	45	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	678	678	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	45	45	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	66	66	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	6788	6788	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	7878	7878	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	12	12	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	678	678	✔

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	45	45	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	56	56	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	778	778	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	45	45	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	6788	6788	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	45	45	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	1	1	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 3.50 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	15
DigColPsInt_Buffer_Cnt_M_u08[2]	16
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	566
DigColPsInt_CurrentSlave_Cnt_M_u08	110
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_SETREG
DigColPsInt_I2CHwCustData_Uls_M_u16	7
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	8
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	0
DigColPsInt_PrevReqDataType_Cnt_M_u08	3
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	0
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0
DigColPsInt_SpurSnsrData_Cnt_M_u16	129
DigColPsInt_TransactionCnt_Cnt_M_u08	30
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	19
k_SpurSensorI2CAddress_Cnt_u08	30
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129

Name	Input Value
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566

Name	Input Value
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Input Value
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.MDR	566
target_i2cREG1_temp.IVR	554
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	44
target_i2cREG1_temp.PID11	4466
target_i2cREG1_temp.PID12	44
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	0
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	3	3	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	15	15	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	16	16	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	0	0	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	566	566	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	110	110	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR1_READEXTERR_SETREG	INIT_SENSOR1_READEXTERR_SETREG	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	7	7	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	8	8	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	0	0	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	2	2	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	0	0	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	129	129	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	30	30	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Actual Value	Expected Value	Result
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

2014-10-14, 23:42:41+0530

Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

Test Step 3.51 (Repeat Count = 1) ✔

Name	Input Value
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8
DigColPsInt_Buffer_Cnt_M_u08[0]	10
DigColPsInt_Buffer_Cnt_M_u08[1]	15
DigColPsInt_Buffer_Cnt_M_u08[2]	16
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1
DigColPsInt_ColSnsrData_Cnt_M_u16	566
DigColPsInt_CurrentSlave_Cnt_M_u08	50
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_SENSOR2_EXTREADDATREG_READ
DigColPsInt_I2CHwCustData_Uls_M_u16	91
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	0
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0
DigColPsInt_NackOccured_Cnt_M_lgc	1
DigColPsInt_PrevReqDataType_Cnt_M_u08	5
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1

Name	Input Value
DigColPsInt_RecvdDataType_Cnt_M_u08	2
DigColPsInt_SkipRegisterWrite_Cnt_M_lgc	1
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1
DigColPsInt_SpurSnsrData_Cnt_M_u16	129
DigColPsInt_TransactionCnt_Cnt_M_u08	7
Flags_Cnt_T_b16	32
I2c_GenStopCond(I2cRegPtr_Cnt_T_str)	target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str
I2c_Send(I2cRegPtr_Cnt_T_str)	target_I2c_Send_I2cRegPtr_Cnt_T_str
I2c_SetRecv(I2cRegPtr_Cnt_T_str)	target_I2c_SetRecv_I2cRegPtr_Cnt_T_str
I2c_SetStatus(I2cRegPtr_Cnt_T_str)	target_I2c_SetStatus_I2cRegPtr_Cnt_T_str
I2c_SetupMasterReceive(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str
I2c_SetupMasterTransmit(I2cRegPtr_Cnt_T_str)	target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str
T_DataRegisters_Cnt_u08[0]	0
T_DataRegisters_Cnt_u08[1]	32
T_DataRegisters_Cnt_u08[2]	30
T_DataRegisters_Cnt_u08[3]	36
T_DataRegisters_Cnt_u08[4]	38
T_DataRegisters_Cnt_u08[5]	34
T_DataRegisters_Cnt_u08[6]	10
T_DataRegisters_Cnt_u08[7]	12
T_DataRegisters_Cnt_u08[8]	14
i2cREG1_temp	target_i2cREG1_temp
k_ColSensorI2CAddress_Cnt_u08	27
k_SpurSensorI2CAddress_Cnt_u08	10
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3

Name	Input Value
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2

Name	Input Value
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3
target_i2cREG1_temp.OAR	567
target_i2cREG1_temp.IMR	44
target_i2cREG1_temp.STR	4444
target_i2cREG1_temp.CLKL	566
target_i2cREG1_temp.CLKH	4466
target_i2cREG1_temp.CNT	129
target_i2cREG1_temp.DRR	6
target_i2cREG1_temp.SAR	567
target_i2cREG1_temp.DXR	44
target_i2cREG1_temp.MDR	566
target_i2cREG1_temp.IVR	554
target_i2cREG1_temp.EMDR	1
target_i2cREG1_temp.PSC	44
target_i2cREG1_temp.PID11	4466
target_i2cREG1_temp.PID12	44
target_i2cREG1_temp.DMAC	1
target_i2cREG1_temp.FUN	1
target_i2cREG1_temp.DIR	2
target_i2cREG1_temp.DIN	0
target_i2cREG1_temp.DOUT	1
target_i2cREG1_temp.SET	1
target_i2cREG1_temp.CLR	2
target_i2cREG1_temp.ODR	0
target_i2cREG1_temp.PD	3
target_i2cREG1_temp.PSL	3

Name	Actual Value	Expected Value	Result
DigColPsInt_AttempOccurForCustDatRead_Cnt_M_u08	8	8	✔
DigColPsInt_Buffer_Cnt_M_u08[0]	10	10	✔
DigColPsInt_Buffer_Cnt_M_u08[1]	15	15	✔
DigColPsInt_Buffer_Cnt_M_u08[2]	16	16	✔
DigColPsInt_BusBusySeqError_Cnt_M_lgc	1	1	✔
DigColPsInt_CmdFailOccurred_Cnt_M_lgc	1	1	✔
DigColPsInt_ColCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_ColSnsrData_Cnt_M_u16	566	566	✔
DigColPsInt_CurrentSlave_Cnt_M_u08	50	50	✔
DigColPsInt_CurrentStepNo_Cnt_M_enum	INIT_COMPLETE	INIT_COMPLETE	✔
DigColPsInt_I2CHwCustData_Uls_M_u16	0	0	✔
DigColPsInt_I2CHwIncompleteCustData_Uls_M_u16	0	0	✔
DigColPsInt_InitFailedOnce_Cnt_M_lgc	0	0	✔
DigColPsInt_NackOccured_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvOverrunError_Cnt_M_lgc	1	1	✔
DigColPsInt_RecvdDataType_Cnt_M_u08	2	2	✔
DigColPsInt_SpurCustDatFound_Cnt_M_lgc	1	1	✔
DigColPsInt_SpurSnsrData_Cnt_M_u16	129	129	✔
DigColPsInt_TransactionCnt_Cnt_M_u08	7	7	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Actual Value	Expected Value	Result
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_GenStopCond_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_Send_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.ODR	0	0	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Actual Value	Expected Value	Result
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetRecv_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetStatus_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.SET	1	1	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterReceive_I2cRegPtr_Cnt_T_str.PSL	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.OAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IMR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.STR	4444	4444	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKL	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLKH	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CNT	129	129	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DRR	6	6	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SAR	567	567	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DXR	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.MDR	566	566	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.IVR	554	554	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.EMDR	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSC	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID11	4466	4466	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PID12	44	44	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DMAC	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.FUN	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DIN	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.DOUT	1	1	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.SET	1	1	✔

TEST DETAILS REPORT

DigColPsInt_InterruptNotification

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Name	Actual Value	Expected Value	Result
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.CLR	2	2	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.ODR	0	0	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PD	3	3	✔
target_I2c_SetupMasterTransmit_I2cRegPtr_Cnt_T_str.PSL	3	3	✔

T ✔

Actual Function	Count	Expected Function	Count	Result
none	0	*** No Call Expected ***	0	✔

TEST DETAILS REPORT

SetupWriteData

2014-10-14, 23:46:17+0530

Project	
Module	
Test Object	

Instrumentation: Test Object Only

Statement (C0) Coverage	
Branch (C1) Coverage	

Statistics

Total Testcases	
Successful	✔
Failed	
Not Executed	

Module Properties

Project Root Directory	
Configuration File	
Target Environment	
Kind of Test	
Linker Options	
Source File(s)	
File	
Compiler Options	

Comments/Description/Specification	
Name	**Text**

TEST DETAILS REPORT

SetupWriteData

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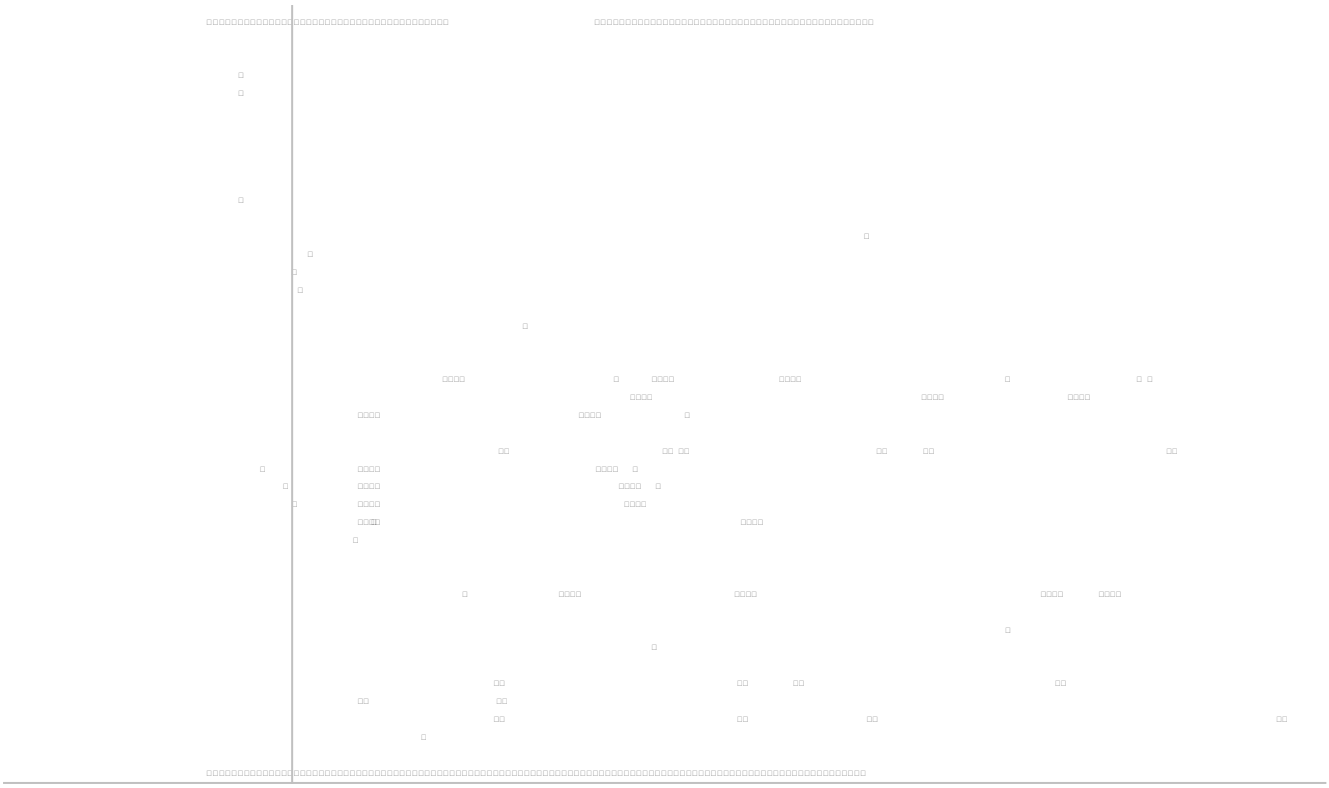

Attributes

Name	Value
Compiler Install Path	$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	$(Compiler Install Path)\include
Time Unit	Cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\C1xx_DigColPs\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

Test Case 1: Boundary Test

Description

Test Step 1.1 (Repeat Count = 1)

Name	Input Value

Name	Actual Value	Expected Value	Result

Name	Actual Value	Expected Value	Result
	□	□	
			✔
			✔
			✔
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	□	□	✔
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			✔
	□	□	✔
	□	□	✔
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	□	□	✔
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			✔
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			✔
			✔

T ✔

Actual Function	Count	Expected Function	Count	Result
				✔
				✔

Test Step 1.2 (Repeat Count = 1) ✔

Name	Input Value
□	
	□
	□

TEST DETAILS REPORT

2014-10-14, 23:46:17+0530

SetupWriteData

Name	Input Value
	□
	□

Name	Actual Value	Expected Value	Result
			✔
			✔
			✔
			✔
□	□	□	✔
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			✔
	□	□	✔
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T ✔

Actual Function	Count	Expected Function	Count	Result
				✔
				✔

TEST DETAILS REPORT

SetupWriteData

2014-10-14, 23:46:17+0530

Test Step 1.3 (Repeat Count = 1)

Name	Input Value

Name	Actual Value	Expected Value	Result

TEST DETAILS REPORT

SetupWriteData

2014-10-14, 23:46:17+0530

Name	Actual Value	Expected Value	Result
	□	□	✓
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	□	□	✓
			✓

T ✓

Actual Function	Count	Expected Function	Count	Result
				✓
				✓

Test Step 1.4 (Repeat Count = 1) ✓

Name	Input Value
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	□

Name	Actual Value	Expected Value	Result
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			✓
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TEST DETAILS REPORT

SetupWriteData

2014-10-14, 23:46:17+0530

Name	Actual Value	Expected Value	Result
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Actual Function	Count	Expected Function	Count	Result
				✓
				✓

Test Step 1.5 (Repeat Count = 1) ✓

Name	Input Value
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	□ □

TEST DETAILS REPORT

SetupWriteData

2014-10-14, 23:46:17+0530

Name	Input Value

Name	Actual Value	Expected Value	Result

TEST DETAILS REPORT

SetupWriteData

2014-10-14, 23:46:17+0530

Name	Actual Value	Expected Value	Result
	□	□	✓
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T ✓

Actual Function	Count	Expected Function	Count	Result
				✓
				✓

Test Step 1.6 (Repeat Count = 1) ✓

Name	Input Value
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Name	Actual Value	Expected Value	Result
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TEST DETAILS REPORT

2014-10-14, 23:46:17+0530

SetupWriteData

Name	Actual Value	Expected Value	Result
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T ✓

Actual Function	Count	Expected Function	Count	Result
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				✓

Test Step 1.7 (Repeat Count = 1) ✓

Name	Input Value

TEST DETAILS REPORT

SetupWriteData

2014-10-14, 23:46:17+0530

Name	Input Value

Name	Actual Value	Expected Value	Result
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Actual Function	Count	Expected Function	Count	Result
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TEST DETAILS REPORT

SetupWriteData

2014-10-14, 23:46:17+0530

Razorcat

Test Step 1.8 (Repeat Count = 1)

Name	Input Value

Name	Actual Value	Expected Value	Result

TEST DETAILS REPORT

SetupWriteData

2014-10-14, 23:46:17+0530

Name	Actual Value	Expected Value	Result
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T

Actual Function	Count	Expected Function	Count	Result
				✔
				✔

Test Step 1.9 (Repeat Count = 1)

Name	Input Value

Name	Actual Value	Expected Value	Result
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TEST DETAILS REPORT

2014-10-14, 23:46:17+0530

SetupWriteData

Name	Actual Value	Expected Value	Result
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T ✔

Actual Function	Count	Expected Function	Count	Result
				✔
				✔

Test Step 1.10 (Repeat Count = 1) ✔

Name	Input Value

TEST DETAILS REPORT

2014-10-14, 23:46:17+0530

SetupWriteData

Name	Input Value
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	□ □

Name	Actual Value	Expected Value	Result
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TEST DETAILS REPORT

SetupWriteData

2014-10-14, 23:46:17+0530

Name	Actual Value	Expected Value	Result
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			✔
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			✔

T ✔

Actual Function	Count	Expected Function	Count	Result
				✔
				✔

Test Step 1.11 (Repeat Count = 1) ✔

Name	Input Value
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Name	Actual Value	Expected Value	Result
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	□	□	✔
			✔

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[redacted]

, 23:46:17+0530

Actual Value	Expected Value	Result
		✔

TEST DETAILS REPORT

SetupWriteData

2014-10-14, 23:46:17+0530

Name	Input Value

Name	Actual Value	Expected Value	Result
			✔
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Actual Function	Count	Expected Function	Count	Result
				✔
				✔

TEST DETAILS REPORT

SetupWriteData

2014-10-14, 23:46:17+0530

Razorcat

Test Step 1.13 (Repeat Count = 1) ✔

Name	Input Value

Name	Actual Value	Expected Value	Result

TEST DETAILS REPORT

SetupWriteData

2014-10-14, 23:46:17+0530

Name	Actual Value	Expected Value	Result
			✓
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T ✓

Actual Function	Count	Expected Function	Count	Result
				✓
				✓

Test Step 1.14 (Repeat Count = 1) ✓

Name	Input Value
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Name	Actual Value	Expected Value	Result
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TEST DETAILS REPORT

SetupWriteData

2014-10-14, 23:46:17+0530

Name	Actual Value	Expected Value	Result
			✓
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T				✓
Actual Function	**Count**	**Expected Function**	**Count**	**Result**
				✓
				✓

TEST DETAILS REPORT

SetupWriteRegister

2014-10-14, 23:47:05+0530

Project	
Module	
Test Object	

Instrumentation: Test Object Only

Statement (C0) Coverage	
Branch (C1) Coverage	

Statistics

Total Testcases	
Successful	✔
Failed	
Not Executed	

Module Properties

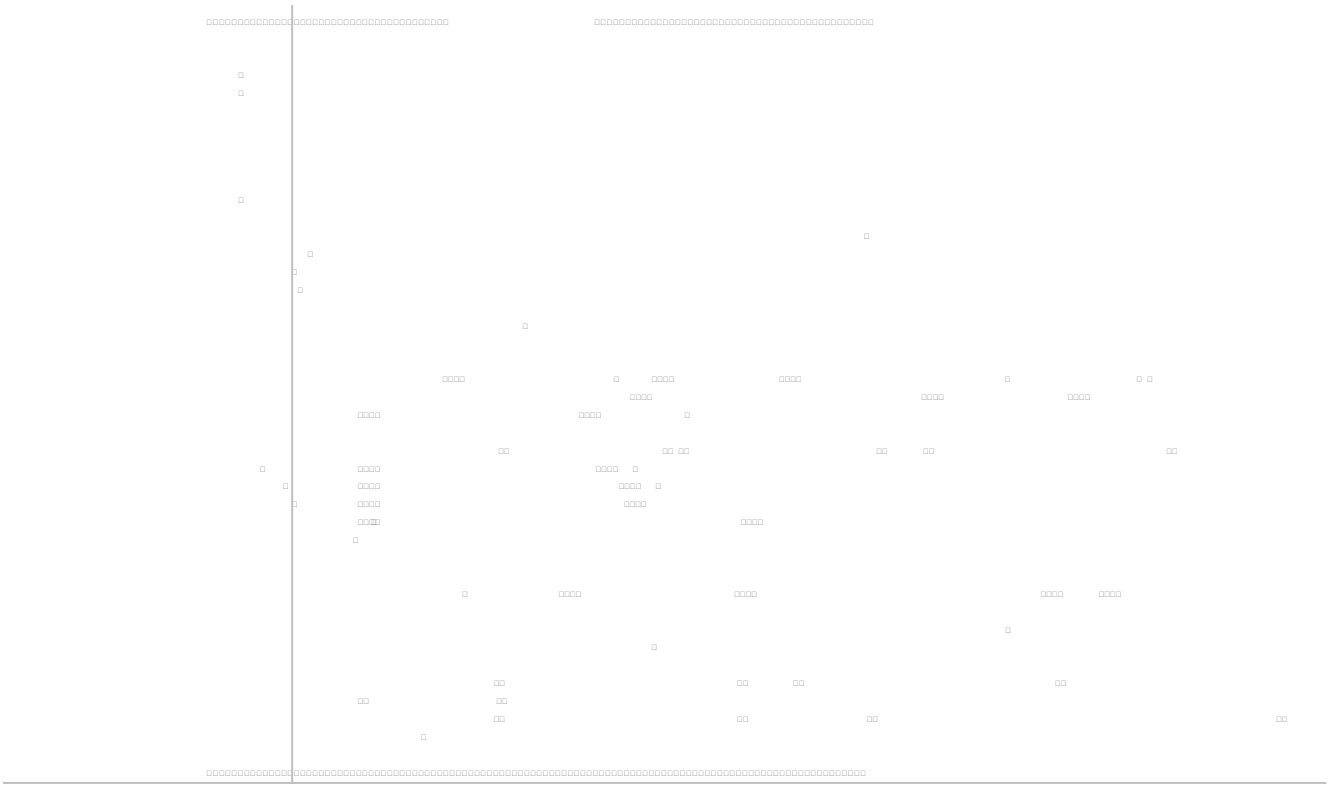
Project Root Directory	
Configuration File	
Target Environment	
Kind of Test	
Linker Options	
Source File(s)	
File	
Compiler Options	

Comments/Description/Specification	
Name	**Text**

TEST DETAILS REPORT

SetupWriteRegister

2014-10-14, 23:47:05+0530



Attributes

Name	Value
Compiler Install Path	$(ProgramFiles)\Texas Instruments\ccsv4\tools\compiler\tms470_4.9.5
Float Precision	9
InitObjDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\obj
InitSrcDir	$(PROJECTROOT)\UnitTestEnv\static_build_files\src
Linker File	$(PROJECTROOT)\UnitTestEnv\static_build_files\sys_link.cmd
Makefile Template	$(PROJECTROOT)\UnitTestEnv\config\Nexteer_ts_make_ude_ti_tms570_ps.tpl
Target Install Path	$(Compiler Install Path)\include
Time Unit	Cycles
Timer Enabled	false
Timer Prescale	0
Timer Resolution	1
UDE Config File	$(PROJECTROOT)\UnitTestEnv\config\TMS570_UDE_12PIN_JTAG.cfg
Workspace File	D:\Synergy_Work_Area\C1xx_DigColPs\UnitTestEnv\config\UDE_TMS570_DEBUG.WSP

TEST DETAILS REPORT

SetupWriteRegister

2014-10-14, 23:47:05+0530

Test Case 1: Boundary Test

Description

Test Step 1.1 (Repeat Count = 1)

Name	Input Value

Name	Actual Value	Expected Value	Result

TEST DETAILS REPORT

SetupWriteRegister

2014-10-14, 23:47:05+0530

Name	Actual Value	Expected Value	Result
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T ✔

Actual Function	Count	Expected Function	Count	Result
				✔
				✔

Test Step 1.2 (Repeat Count = 1) ✔

Name	Input Value

TEST DETAILS REPORT

SetupWriteRegister

2014-10-14, 23:47:05+0530

Name	Input Value

Name	Actual Value	Expected Value	Result
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T ✔

Actual Function	Count	Expected Function	Count	Result
				✔
				✔

Test Step 1.3 (Repeat Count = 1) ✔

Name	Input Value

TEST DETAILS REPORT

SetupWriteRegister

2014-10-14, 23:47:05+0530

Name	Input Value

Name	Actual Value	Expected Value	Result
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TEST DETAILS REPORT

SetupWriteRegister

2014-10-14, 23:47:05+0530

Name	Actual Value	Expected Value	Result
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Actual Function	**Count**	**Expected Function**	**Count**	**Result**
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Test Step 1.4 (Repeat Count = 1) ✔

Name	Input Value

Name	Actual Value	Expected Value	Result
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TEST DETAILS REPORT

SetupWriteRegister

2014-10-14, 23:47:05+0530

Name	Actual Value	Expected Value	Result
			✔

TEST DETAILS REPORT

SetupWriteRegister

2014-10-14, 23:47:05+0530

Name	Input Value
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Name	Actual Value	Expected Value	Result
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TEST DETAILS REPORT

SetupWriteRegister

2014-10-14, 23:47:05+0530

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Actual Function	**Count**	**Expected Function**	**Count**	**Result**
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				✔

Test Step 1.6 (Repeat Count = 1)	✔
Name	**Input Value**

Name	**Actual Value**	**Expected Value**	**Result**
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TEST DETAILS REPORT

SetupWriteRegister

2014-10-14, 23:47:05+0530

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Actual Function	**Count**	**Expected Function**	**Count**	**Result**
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Test Step 1.7 (Repeat Count = 1)		✔
Name	**Input Value**	

Name	Actual Value	Expected Value	Result
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TEST DETAILS REPORT

SetupWriteRegister

2014-10-14, 23:47:05+0530

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Actual Function	Count	Expected Function	Count	Result
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Test Step 1.8 (Repeat Count = 1) ✓

Name	Input Value

TEST DETAILS REPORT

SetupWriteRegister

2014-10-14, 23:47:05+0530

Name	Input Value

Name	Actual Value	Expected Value	Result

TEST DETAILS REPORT

SetupWriteRegister

2014-10-14, 23:47:05+0530

Name	Actual Value	Expected Value	Result
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Actual Function	**Count**	**Expected Function**	**Count**	**Result**
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Test Step 1.9 (Repeat Count = 1) ✔

Name	Input Value

Name	Actual Value	Expected Value	Result
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TEST DETAILS REPORT

SetupWriteRegister

2014-10-14, 23:47:05+0530

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Actual Function	**Count**	**Expected Function**	**Count**	**Result**
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Test Step 1.10 (Repeat Count = 1) ✔

Name	Input Value

TEST DETAILS REPORT

2014-10-14, 23:47:05+0530

SetupWriteRegister

Name	Input Value

Name	Actual Value	Expected Value	Result
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Actual Function	**Count**	**Expected Function**	**Count**	**Result**
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Test Step 1.11 (Repeat Count = 1) ✔

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Name	Actual Value	Expected Value	Result
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TEST DETAILS REPORT

SetupWriteRegister

2014-10-14, 23:47:05+0530

Name	Actual Value	Expected Value	Result
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Actual Function	**Count**	**Expected Function**	**Count**	**Result**
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